CY25701

# Programmable High Frequency Crystal Oscillator with Spread Spectrum (SSXO) and No Spread Spectrum (XO) Option

## Features

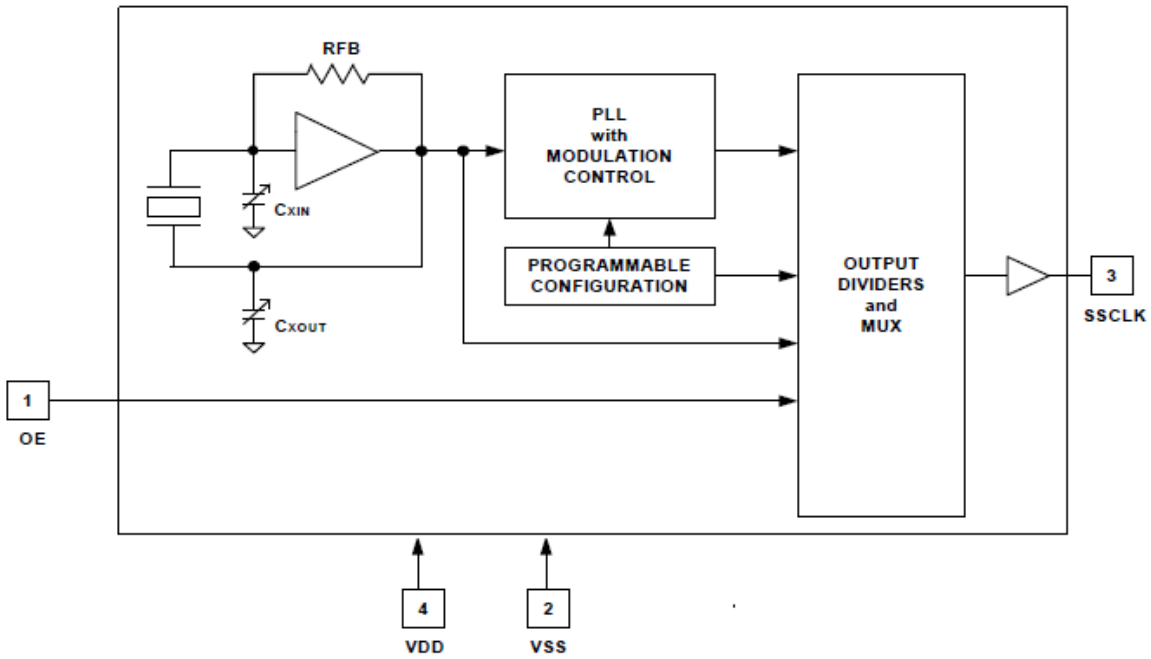
- Crystal Oscillator with Spread Spectrum Clock (SSXO)
- No Spread Spectrum (XO) Option
- Wide operating output clock frequency range of 10 to166 MHz
- Programmable spread spectrum with nominal 31.5 kHz modulation frequency
- Center spread: ±0.25% to ±2.0%
- Down spread: –0.5% to –4.0%
- No spread: ±0.0%
- Integrated phase-locked loop (PLL)
- 85 ps typical cycle-to-cycle jitter with SSCLK = 133 MHz
- 3.3 V operation
- Output enable function
- Package available in 4-pin ceramic LCC SMD
- Pb-free package
- Industrial temperature from –40 °C to 85 °C

## Benefits

- Provides a wide range of spread percentages for maximum electromagnetic interference (EMI) reduction to meet regulatory agency electromagnetic compliance (EMC) requirements. Reduces development and manufacturing costs and time-to-market.
- This versatile programming feature enables the user to switch between SSXO (with Spread) and XO (without Spread) functions with ease.
- Internal PLL to generate up to 166 MHz output.
- Suitable for most PC, consumer, and networking applications
- Application compatibility in standard and low power systems
- In house programming of samples and prototype quantities is available using CY3672-USB programming kit and CY3724 socket adapters. Production quantities are available through Cypress's value added distribution partners or by using third party programmers from BP Microsystems, and HiLo Systems, and others.

For a complete list of related resources, click here.

## Logic Block Diagram



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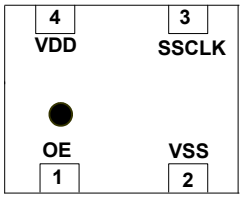
## Pin Configuration

**Figure 1. 4-pin Ceramic SMD pinout**




## Pin Definitions

4-pin Ceramic SMD

| Pin | Name | Description |
|---|---|---|
| 1 | OE | Output Enable pin: Active HIGH. If OE = 1, SSCLK is enabled |
| 2 | VSS | Power supply ground |
| 3 | SSCLK | Spread spectrum clock output (with or without spread) |
| 4 | VDD | 3.3 V power supply |

## Functional Description

The CY25701 is a Spread Spectrum Crystal Oscillator (SSXO) IC used to reduce the EMI found in today's high speed digital electronic systems.

The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the embedded input crystal. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy significantly reduces the cost of complying with regulatory agency (EMC) requirements and improves time-to-market without degrading system performance.

The CY25701 uses a programmable configuration memory array to synthesize output frequency and spread percentage.

The spread percentage is programmed to center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.00%. The range for down spread is from –0.5% to –4.0%. Contact the factory for smaller or larger spread percentage amounts if required. See Table 2 on page 4 for spread selection and no spread values.

The frequency modulated SSCLK output is programmable from 10 to 166 MHz.

The CY25701 is available in a 4-pin ceramic SMD package with an operating temperature range of –40 °C to 85 °C.

## Programming Description

### Factory and Field Programmable CY25701

Factory and field programming is available for samples and manufacturing by Cypress and its distributors. Submit your request to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request is processed, you receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample request and the production orders. Contact your local Cypress FAE or sales representative for details.

Additional information on the CY25701 is available at the Cypress web site www.cypress.com.

### Output Frequency, SSCLK Output (SSCLK, pin 3)

The modulated frequency at the SSCLK output is produced by synthesizing from the embedded crystal oscillator frequency input. The range of synthesized clock is from 10 to 166 MHz.

### Spread Percentage (SSCLK, pin 3)

The SSCLK spread is programmable to various spread percentage values from ±0.25% to ±2.0% for center spread and from –0.5% to –4.0% for down spread. See Table 2 on page 4 for available spread options. Enter ±0.0% (No spread) for XO (crystal oscillator) without spread option.

### Frequency Modulation (SSCLK, pin 3)

The default frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 10 to 166 MHz. Alternate frequency modulations at 30.1 kHz or 32.9 kHz are selectable using CyberClocks™ Online software. Contact the factory for other alternate modulation frequencies if required.

**Table 1. Programming Data Requirement**

| Pin Function | Output Frequency | Spread Percent Code [1] | Frequency Modulation |
|---|---|---|---|
| Pin Name | SSCLK | SSCLK | SSCLK |
| Pin# | 3 | 3 | 3 |
| Units | MHz | % | kHz |
| Program Value | ENTER DATA | ENTER DATA | ENTER DATA 31.5 |

**Table 2. Spread Percent Selection**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Center Spread** | **Code** | **A** | **B** | **C** | **D** | **E** | **F** | **Z** |
| | **Percentage** | ±0.25% | ±0.5% | ±0.75% | ±1.0% | ±1.5% | ±2.0% | ±0.0% |
| **Down Spread** | **Code** | **G** | **H** | **J** | **K** | **L** | **M** | **Z** |
| | **Percentage** | –0.5% | –1.0% | –1.5% | –2.0% | –3.0% | –4.0% | ±0.0% |

## Absolute Maximum Ratings

Supply Voltage ($V_{DD}$) .....–0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to $V_{DD}$ + 0.5 V

Storage Temperature (Non-condensing) ..... –55 °C to +100 °C

Junction Temperature ..... –40 °C to +125 °C

Data Retention at $T_J$ = 125 °C .....> 10 years

Package Power Dissipation ..... 350 mW

## Operating Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3.00 | 3.30 | 3.60 | V |
| $T_A$ | Ambient temperature (commercial) | –20 | – | 70 | °C |
| $T_A$ | Ambient temperature (industrial) | –40 | – | 85 | °C |
| $C_{LOAD}$ | Max. load capacitance at pin 3 | – | – | 15 | pF |
| $F_{SSCLK}$ | SSCLK output frequency, $C_{LOAD}$ = 15 pF | 10 | – | 166 | MHz |
| $F_{MOD}$ | Spread Spectrum Modulation Frequency | 30.0 | 31.5 | 33.0 | kHz |
| $T_{PU}$ | Power up time for VDD to reach minimum specified voltage (power ramp must be monotonic) | 0.05 | – | 500 | ms |

**Note**
1. ±0.0% or Code “Z” for XO (No-Spread) option.

## DC Electrical Characteristics

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | Output high current (pin 3) | $V_{OH} = V_{DD} – 0.5$ V, $V_{DD} = 3.3$ V (source) | 10 | 12 | – | mA |
| $I_{OL}$ | Output low current (pin 3) | $V_{OL} = 0.5$ V, $V_{DD} = 3.3$ V (sink) | 10 | 12 | – | mA |
| $V_{IH}$ | Input high voltage (pin 1) | CMOS levels, 70% of $V_{DD}$ | 0.7 × $V_{DD}$ | – | $V_{DD}$ | V |
| $V_{IL}$ | Input low voltage (pin 1) | CMOS levels, 30% of $V_{DD}$ | – | – | 0.3 × $V_{DD}$ | V |
| $I_{IH}$ | Input high current (pin 1) | $V_{in} = V_{DD}$ | – | – | 10 | µA |
| $I_{IL}$ | Input low current (pin 1) | $V_{in} = V_{SS}$ | – | – | 10 | µA |
| $I_{OZ}$ | Output leakage current (pin 3) | Three-state output, OE = 0 | –10 | – | 10 | µA |
| $C_{IN}$[2] | Input capacitance (pin 1) | Pin 1, or OE | – | 5 | 7 | pF |
| $I_{VDD}$ | Supply current | $V_{DD} = 3.3$ V, SSCLK = 10 to 166 MHz, $C_{LOAD} = 0$, OE = $V_{DD}$ | – | – | 50 | mA |
| Δf/f | Initial accuracy at room temp. | $T_A = 25$ °C, 3.3 V | –25 | – | 25 | ppm |
| | Freq. stability over temp. range | $T_A = –20$ °C to 70 °C, 3.3 V | –25 | – | 25 | ppm |
| | Freq. stability over voltage range | 3.0 to 3.6 V | –12 | – | 12 | ppm |
| | Aging | $T_A = 25$ °C, First year | –5 | – | 5 | ppm |

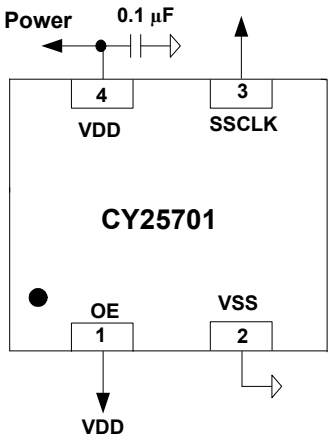
## AC Electrical Characteristics

| Parameter [2] | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC | Output Duty Cycle | SSCLK, Measured at $V_{DD}/2$ | 45 | 50 | 55 | % |
| $t_R$ | Output Rise Time | 20%–80% of $V_{DD}$, $C_L = 15$ pF | – | – | 2.7 | ns |
| $t_F$ | Output Fall Time | 20%–80% of $V_{DD}$, $C_L = 15$ pF | – | – | 2.7 | ns |
| $T_{CCJ1}$[3] | Cycle-to-Cycle Jitter SSCLK (Pin 3) | SSCLK ≥133 MHz, Measured at $V_{DD}/2$ | – | 85 | 200 | ps |
| | | 25 MHz ≤ SSCLK <133 MHz, Measured at $V_{DD}/2$ | – | 215 | 400 | ps |
| | | SSCLK < 25 MHz, Measured at $V_{DD}/2$ | – | – | 1% of 1/SSCK | s |
| $T_{OE1}$ | Output Disable Time (pin1 = OE) | Time from falling edge on OE to stopped outputs (Asynchronous) | – | 150 | 350 | ns |
| $T_{OE2}$ | Output Enable Time (pin1 = OE) | Time from rising edge on OE to outputs at a valid frequency (Asynchronous) | – | 150 | 350 | ns |
| $T_{LOCK}$ | PLL Lock Time | Time for SSCLK to reach valid frequency | – | – | 10 | ms |

**Notes**
2. Guaranteed by characterization, not fully tested.
3. For more information on Jitter Specifications, please see whitepaper - Datasheet Jitter Specifications for Cypress Timing Products available at http://www.cypress.com/?rID=12791.

## Application Circuit

**Figure 2. Application Circuit Diagram**




## Switching Waveforms

**Figure 3. Duty Cycle Waveform**

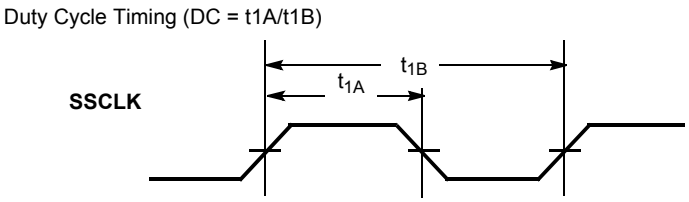
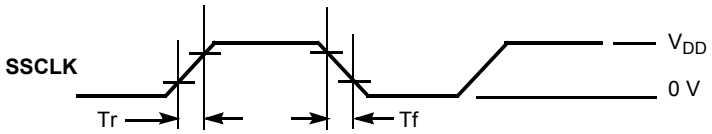
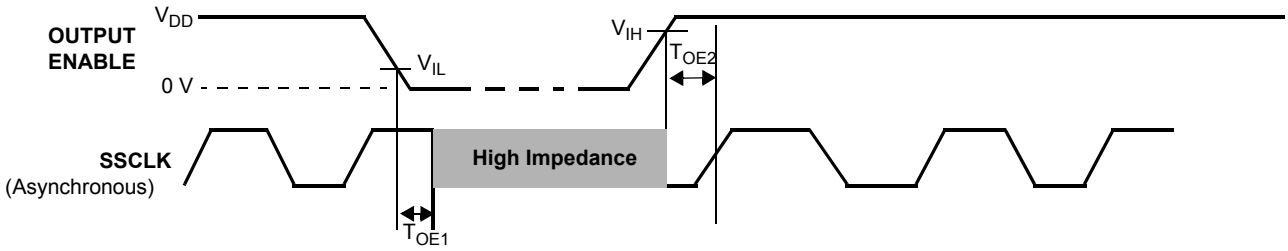



**Figure 4. Output Rise/Fall Time Waveform**

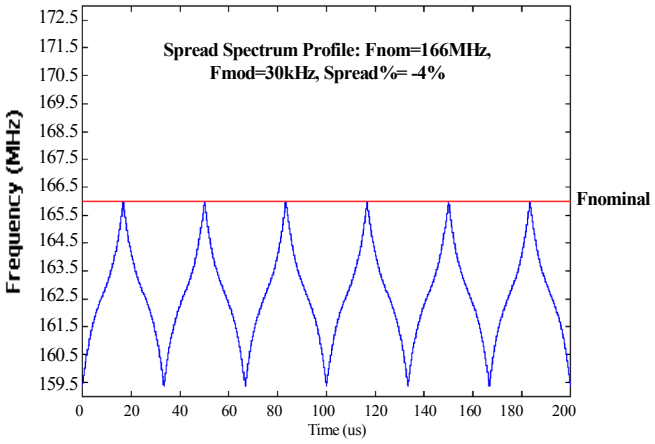


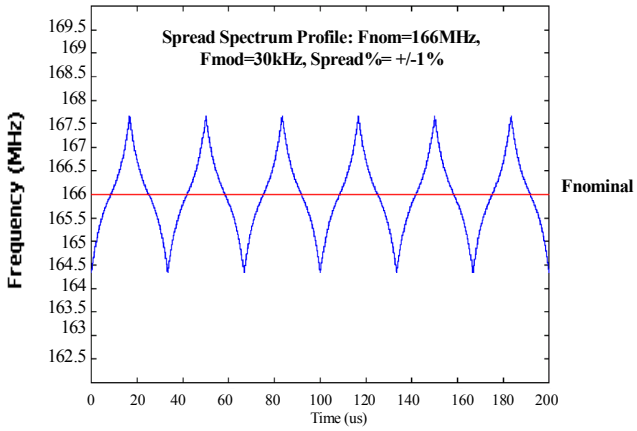

Output Rise time (Tr) = (0.6 × $V_{DD}$)/SR1 (or SR3)
Output Fall time (Tf) = (0.6 × $V_{DD}$)/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

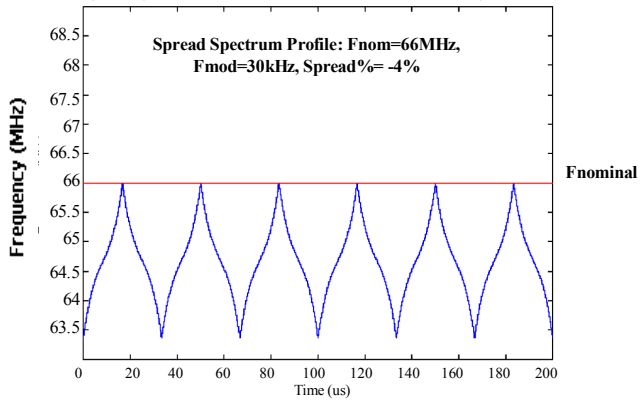
**Figure 5. Output Enable/Disable Timing Waveforms**

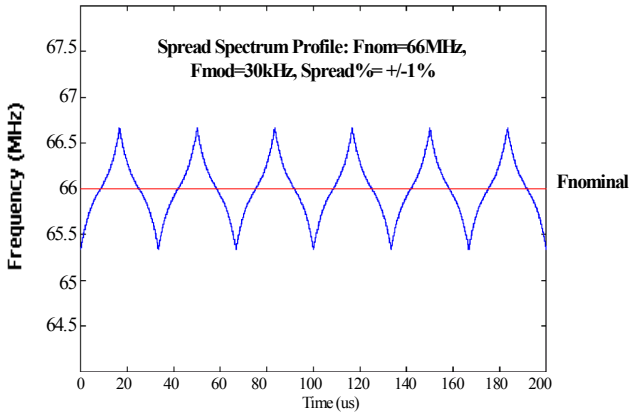


## Informational Graphs[4]




**Note**

4. The “Informational Graphs” are meant to convey typical performance levels. No performance specifications are implied or guaranteed. Refer to the tables on pages three and four for device specifications.

## Ordering Information

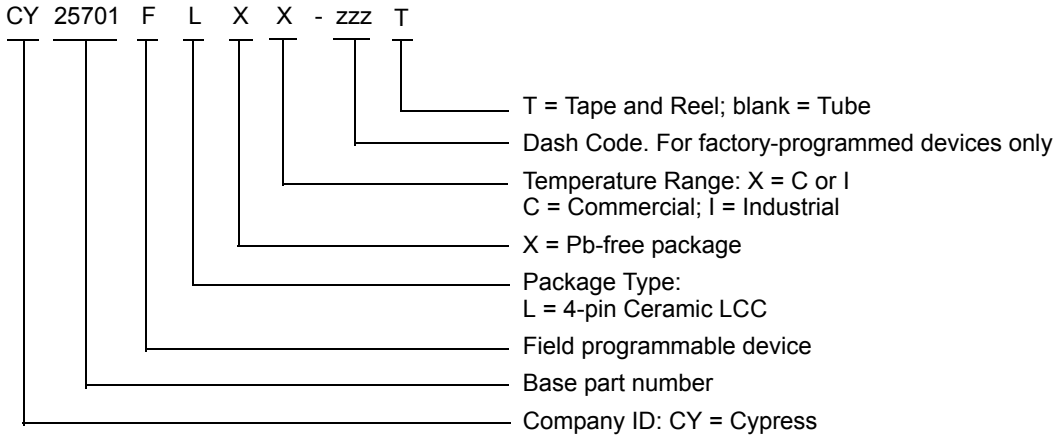
| Part Number | Package Description | Product Flow |
|---|---|---|
| **Pb-free** | | |
| CY25701FLXCT [5, 6] | 4-pin Ceramic LCC SMD – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25701FLXIT [5, 6] | 4-pin Ceramic LCC SMD – Tape and Reel | Industrial, –40 °C to 85 °C |
| **Programmer** | | |
| CY3672-USB | Programming Kit | |
| CY3724 Socket Adapter | Socket adapter board, for programming CY25701 | |

### Possible Configurations

Some product offerings are factory programmed customer specific devices with customized part numbers.The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE of Sales Representative for more information.

| Part Number | Package Description | Product Flow |
|---|---|---|
| **Pb-free** | | |
| CY25701LXCzzzT [6, 7] | 4-pin Ceramic LCC SMD – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25701LXIzzzT [6, 7] | 4-pin Ceramic LCC SMD – Tape and Reel | Industrial, –40 °C to 85 °C |

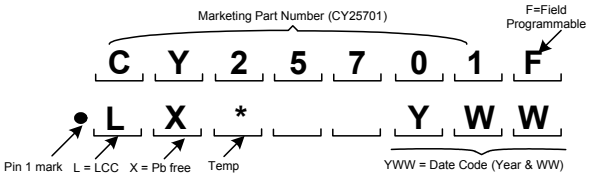
### Ordering Code Definitions



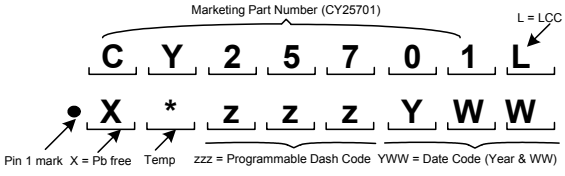

**Notes**
5. "FLX" suffix is used for products programmed in the field by Cypress distributors.
6. Temp can be C (Commercial) or I (Industrial).
7. "ZZZ" denotes the assigned product dash number. This number is assigned by the factory after the output frequency and spread percent programming data is received from the customer.For more details, contact your local Cypress FAE or Sales Representative.

**Figure 6. Actual Marking [8]**

**CY25701FLX***



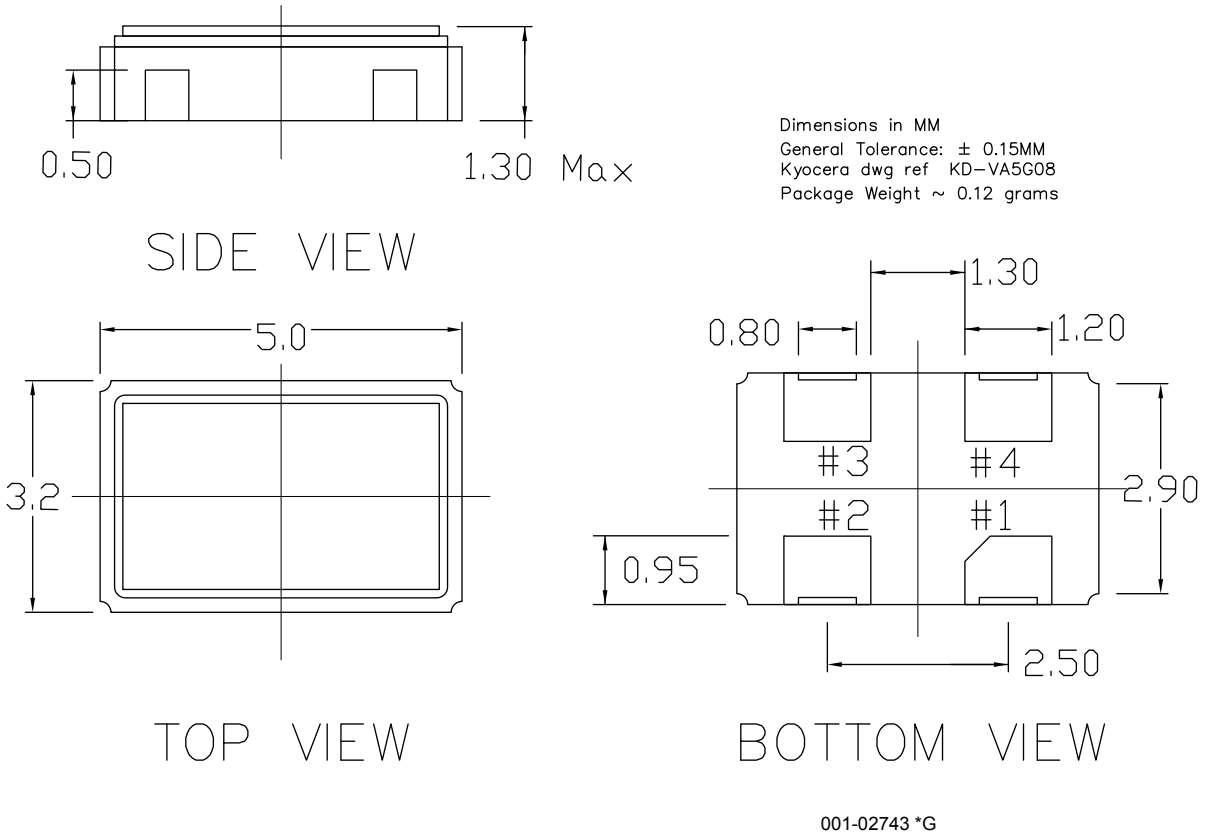

**CY25701LX***




**Note**
8. Temp can be C (Commercial) or I (Industrial).

## Package Drawings and Dimensions

**Figure 7. 4-pin Ceramic LCC (3.2 × 5.0 × 1.3 mm) LZ04A Package Outline, 001-02743**



## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| EMC | Electromagnetic Compliance |
| EMI | Electromagnetic Interference |
| FAE | Field Application Engineer |
| LCC | Leadless Chip Carrier |
| OE | Output Enable |
| PLL | Phase Locked Loop |
| SMD | Surface Mount Device |
| SSC | Spread Spectrum Clock |
| SSXO | Spread Spectrum Crystal Oscillator |
| XO | Crystal Oscillator |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| kHz | kilohertz |
| MHz | megahertz |
| µA | microampere |
| µF | microfarad |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mW | milliwatt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| V | volt |

## Document History Page

| Document Title: CY25701, Programmable High Frequency Crystal Oscillator with Spread Spectrum (SSXO) and No Spread Spectrum (XO) Option<br>Document Number: 001-07313 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 442944 | RGL | See ECN | New data sheet |
| *A | 487736 | KKVTMP | See ECN | Added Industrial temp |
| *B | 1414203 | DPF / VED | See ECN | Replaced the Package Drawing and Dimension figure on page seven and various copy edits;<br>The reference to the software is now CyberClocks™ Online rather than CyberClocks software. |
| *C | 2542310 | AESA | 07/24/08 | Added Note “Not recommended for new designs.”<br>Added part number CY25701KFLXCT, CY25701KFLXIT, CY25701KLXCzzzT, and CY25701KLXIzzzT in Ordering Information.<br>Added note reference 5 to CY25701KFLXCT and CY25701KFLXIT, and note reference 6 to CY25701KLXCzzzT and CY25701KLXIzzzT.<br>Updated to new template. |
| *D | 2624529 | CXQ / PYRS | 12/18/08 | Removed Note “Not recommended for new designs.”<br>Removed part number CY25701KFLXCT, CY25701KFLXIT, CY25701KLXCzzzT, and CY25701KLXIzzzT in Ordering Information. |
| *E | 2897744 | CXQ | 03/23/2010 | Moved ‘ZZZ’ parts to Possible Configurations table<br>Updated Package Drawings and Dimensions. |
| *F | 3381730 | PURU | 09/26/2011 | Updated Benefits (Replaced “CY3672 programming kit” with “CY3672-USB programming kit” and given hyperlink to the same as “http://www.cypress.com/?rID=44009” and also given hyperlink to “CY3724 socket adapters” as “http://www.cypress.com/?rID=37857”.<br>Updated Logic Block Diagram (Replaced the previous Logic Block Diagram with the present Logic Block Diagram).<br>Added Ordering Code Definitions.<br>Updated Package Drawings and Dimensions (Updated the next revision package outline for Figure 7).<br>Added Acronyms and Units of Measure.<br>Updated to new template. |
| *G | 4556401 | TAVA | 10/30/2014 | Updated Package Drawings and Dimensions:<br>spec 001-02743 – Changed revision from *E to *G.<br><br>Updated to new template.<br><br>Completing Sunset Review. |

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