



THIS SPEC IS OBSOLETE

Spec No: 38-07096

Spec Title: CY26112 One-PLL General Purpose Clock Generator

Sunset Owner: IJA

Replaced by: N/A



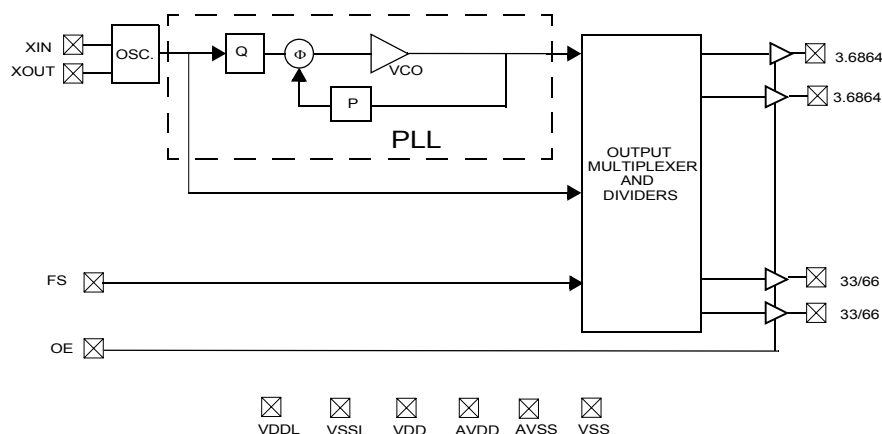
CY26112

One-PLL General Purpose Clock Generator

Features	Benefits
• Integrated phase-locked loop	Internal PLL with up to 333 MHz internal operation
• Low skew, low jitter, high accuracy outputs	Meets critical timing requirements in complex system designs
• Frequency Select Pin	Dynamic frequency selection
• 3.3V Operation with 2.5 V Output Option	Enables application compatibility
• 16-TSSOP	Industry standard package saves on board space

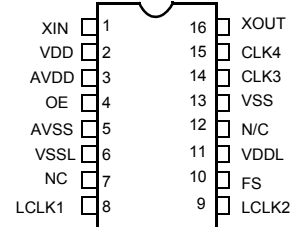
Part Number	Outputs	Input Frequency	Output Frequency Range
CY26112	4	14.7456 MHz	2 x 3.6864 MHz, 2 x 33/66 MHz (selectable)

Logic Block Diagram



Pin Configurations

CY26112
16-pin TSSOP



Output	Pin	Default Frequency	Unit
LCLK1	8	3.6864	MHz
LCLK2	9	3.6864	MHz
CLK3	14	33/66 (selectable)	MHz
CLK4	15	33/66 (selectable)	MHz

Summary

Name	Pin Number	Description
XIN	1	Reference Input
VDD	2	Voltage Supply
AVDD	3	Analog Voltage Supply
OE	4	Output Enable, OE = 0 three-state; OE = 1 active
AVSS	5	Analog Ground
VSSL	6	LCLK Ground
NC	7	No Connect - Reserved
LCLK1	8	3.6864 MHz Clock output 1 at V _{DDL} level
LCLK2	9	3.6864 MHz Clock output 2 at V _{DDL} level
FS	10	Frequency Select Pin $\bar{D}$ FS = 0: 33 MHz, FS = 1: 66 MHz
VDDL	11	LCLK Voltage Supply (2.5V or 3.3V)
NC	12	No Connect - Reserved
VSS	13	Ground
CLK3	14	Clock output 3-33 MHz/66 MHz
CLK4	15	Clock output 4-33 MHz/66 MHz
XOUT ^[1]	16	Reference Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
VDD	Supply Voltage	$\bar{D}0.5$	7.0	V
VDDL	I/O Supply Voltage		7.0	V
T _J	Junction Temperature		125	°C
	Digital Inputs	AV _{SS} $\bar{D}$ 0.3	AV _{DD} + 0.3	V
	Digital Outputs referred to VDD	V _{SS} $\bar{D}$ 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to VDDL	V _{SS} $\bar{D}$ 0.3	V _{DDL} + 0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	3.0	3.3	3.6	V
V _{DDL}	Operating Voltage	2.375	2.5	2.625	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Driven Reference Frequency		14.7456		MHz

Note:

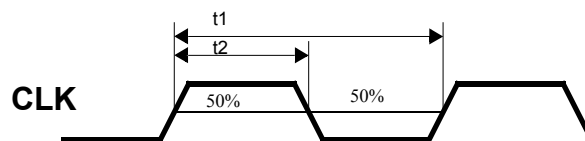
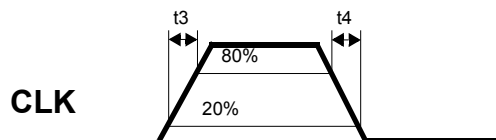
1. Float XOUT if XIN is externally driven.

DC Electrical Characteristics

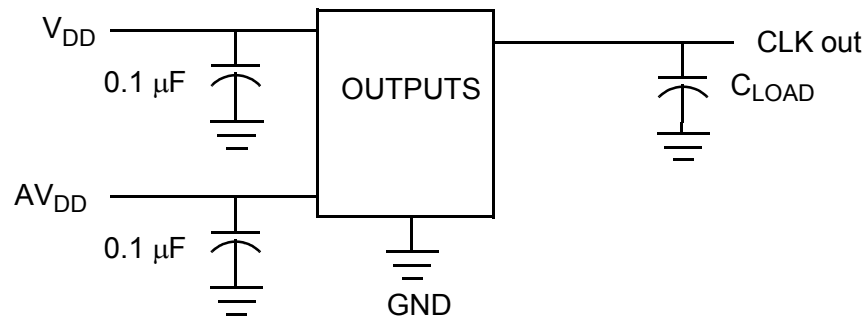
Parameter ^[1]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} \pm 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OH}	Output High Current	$V_{OH} = V_{DDL} \pm 0.5$, $V_{DDL} = 2.5V$	8	16		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5V$	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
C_{IN}	Input Capacitance	OE and FS Pins			7	pF
I_{IZ}	Input Leakage Current	OE and FS Pins		5		μA
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			25	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL} = 3.6V$)			7	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625V$)			5	mA

AC Electrical Characteristics

Parameter ^[1]	Name	Description	Min.	Typ.	Max.	Unit
DC		Duty Cycle is defined in Figure 2; t_1/t_2 @ 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% $\pm$ 80% of $V_{DD}/V_{DDL}=3.3V$	0.8	1.4		V/ns
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% $\pm$ 80% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% $\pm$ 20% of $V_{DD}/V_{DDL}=3.3V$	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% $\pm$ 20% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t_5	Skew	Delay between related outputs at rising edge			250	ps
t_9	Clock Jitter	Peak to Peak period jitter			350	ps
t_{10}	PLL Lock Time				3	ms


Figure 1. Duty Cycle Definition; $DC = t_2/t_2$.

Figure 2. Rise and Fall Time Definitions.
Note:

2. Not 100% tested.

Test Circuit

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26112ZC	Z16	16-Pin TSSOP	Commercial	3.3V



Document Title: CY26112 One-PLL General Purpose Clock Generator
Document Number: 38-07096

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107331	08/28/01	CKN	New Data Sheet
OBS	294816	See ECN	RGL	To Obsolete the DS