

## 100 MHz Differential Buffer for PCI Express and SATA

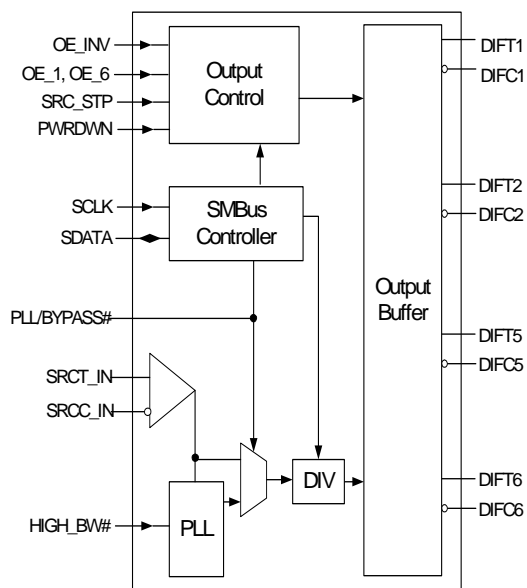
### Features

- CK409 and CK410 companion buffer
- Four differential 0.7V clock output pairs
- OE\_INV input for inverting OE, PWRDWN, and SRC\_STP active levels
- Individual OE controls
- Low CTC jitter (< 50 ps)
- Programmable bandwidth
- SRC\_STP power management control
- SMBus Block/Byte/Word Read and Write support
- 3.3V operation
- PLL Bypass-configurable
- Divide by 2 programmable outputs
- 28-pin SSOP and TSSOP packages

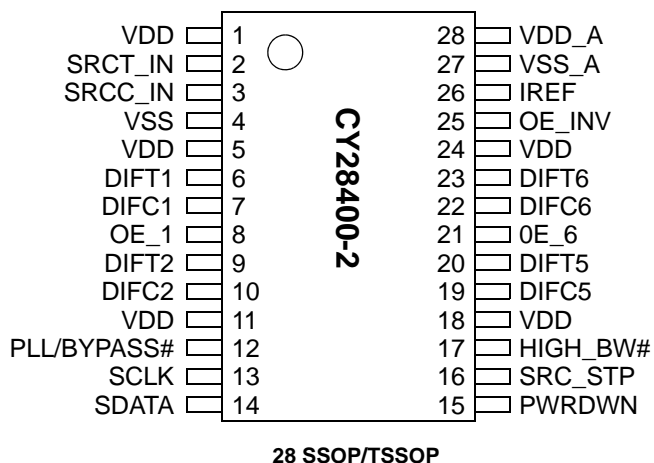
### Functional Description

The CY28400-2 is a differential buffer and serves as a companion device to the CK409 or CK410 clock generator. The device is capable of distributing the Serial Reference Clock (SRC) in PCI Express and SATA implementations.

### Block Diagram



### Pin Configuration



**Pin Description**

Pin	Name	Type	Description
2,3	SRCT_IN, SRCC_IN	I,DIF	<b>0.7V Differential inputs</b>
6,7,9,10;20,19; 23,22	DIF[T/C][2:1] & [6:5]	O,DIF	<b>0.7V Differential Clock Outputs</b>
8,21	OE_1, OE_6	I,SE	<b>3.3V LVTTTL input for enabling differential outputs</b> Active HIGH if OE_INV = 0 Active LOW if OE_INV = 1
17	HIGH_BW#	I,SE	<b>3.3V LVTTTL input for selecting PLL bandwidth</b> 0 = High BW, 1 = Low BW
15	PWRDWN	I,SE	<b>3.3V LVTTTL input for Power Down</b> Active LOW if OE_INV = 0 Active HIGH if OE_INV = 1
16	SRC_STP	I,SE	<b>3.3V LVTTTL input for SRC_STP.</b> Disables stoppable outputs. Active LOW if OE_INV = 0 Active HIGH if OE_INV = 1
13	SCLK	I,SE	<b>SMBus Slave Clock Input</b>
14	SDATA	I/O,OC	<b>Open collector SMBus data</b>
26	IREF	I	<b>A precision resistor is attached to this pin to set the differential output current</b>
12	PLL/BYPASS#	I	<b>3.3V LVTTTL input for selecting fan-out or PLL operation</b>
28	VDD_A	PWR	<b>3.3V Power Supply for PLL</b>
27	VSS_A	GND	<b>Ground for PLL</b>
4	VSS	GND	<b>Ground for outputs</b>
1,5,11,18,24	VDD	PWR	<b>3.3V power supply for outputs</b>
25	OE_INV	I, SE	<b>Input strap for setting polarity of OE_[7:0], SRC_STP, and PWRDWN</b>

**Serial Data Interface**

To enhance the flexibility and function of the clock buffer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

**Data Protocol**

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11011100 (DCh).

**Table 1. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

**Table 2. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits

**Table 2. Block Read and Block Write Protocol** (continued)

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 from master – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 from master – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge from host
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge from host
....	Acknowledge from slave	48:55	Data byte 1 from slave – 8 bits
....	Stop	56	Acknowledge from host
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Acknowledge from host
		....	Stop

**Table 3. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '100xxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '100xxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Acknowledge from master
		39	Stop

**Byte 0: Control Register 0**

Bit	@pup	Name	Description
7	0	PWRDWN Drive Mode	Power Down drive mode 0 = Driven when stopped, 1 = Tri-state
6	0	SRC_STP Drive Mode	SRC Stop drive mode 0 = Driven when stopped, 1 = Tri-state



Byte 0: Control Register 0 (continued)

Bit	@pup	Name	Description
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	1	HIGH_BW#	HIGH_BW# 0 = High Bandwidth, 1 = Low bandwidth
1	1	PLL/BYPASS#	PLL/BYPASS# 0 = Fanout buffer, 1 = PLL mode
0	1	SRC_DIV2#	SRC_DIV2# configures output frequency at half the input frequency 0 = Divided by 2 mode (output = input/2), 1 = Normal (output = input)

Byte 1: Control Register 1

Bit	@pup	Name	Description
7	1	Reserved	Reserved
6	1	OE_6	DIF[T/C]6 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
5	1	OE_5	DIF[T/C]5 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	1	OE_2	DIF[T/C]2 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
1	1	OE_1	DIF[T/C]1 Output Enable 0 = Disabled (Tri-state) 1 = Enabled
0	1	Reserved	Reserved

Byte 2: Control Register 2

Bit	@pup	Name	Description
7	0	Reserved	Reserved
6	0	SRC_STP_DIF[T/C]6	Allow Control DIF[T/C]6 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
5	0	SRC_STP_DIF[T/C]5	Allow Control DIF[T/C]5 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	SRC_STP_DIF[T/C]2	Allow Control DIF[T/C]2 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
1	0	SRC_STP_DIF[T/C]1	Allow Control DIF[T/C]1 with assertion of SRC_STP 0 = Free-running 1 = Stopped with SRC_STP
0	0	Reserved	Reserved

**Byte 3: Control Register 3**

Bit	@pup	Name	Description
7	0		Reserved
6	0		Reserved
5	0		Reserved
4	0		Reserved
3	0		Reserved
2	0		Reserved
1	0		Reserved
0	0		Reserved

**Byte 4: Vendor ID Register**

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

**Byte 5: Control Register 5**

Bit	@Pup	Name	Description
7	0		Reserved
6	0		Reserved
5	0		Reserved
4	0		Reserved
3	0		Reserved
2	0		Reserved
1	0		Reserved
0	0		Reserved

**OE\_INV Clarification**

The OE\_INV pin is an input strap sampled at power-on. The functionality of this input is to set the active level polarities for OE\_1, OE\_6, PWRDWN, and SRC\_STP input pins. 'Active HIGH' indicates the functionality of the input is asserted when the input voltage level at the pin is high and deasserted when the voltage level at the input is low. 'Active LOW' indicates that the functionality of the input is asserted when the voltage level at the input is low and deasserted when the voltage level at the input pin is high. See V<sub>IH</sub> and V<sub>IL</sub> in the DC Electrical Specifications for input voltage high and low ranges.

OE_INV	PWRDWN	SRC	OE_1, OE_6
0	Active LOW	Active LOW	Active HIGH
1	Active HIGH	Active HIGH	Active LOW

**PWRDWN Clarification**

The PWRDWN pin is an asynchronous input used to shut off all clocks cleanly and instruct the device to evoke power savings mode. It may be active HIGH or active LOW depending on the strapped value of the OE\_INV input. The PWRDWN pin should be asserted prior to shutting off the input clock or power to ensure all clocks shut down in a glitch-free manner. This signal is synchronized internal to the device prior to powering down the clock buffer. PWRDWN is an asynchronous input for powering up the system. When the PWRDWN pin is asserted, all clocks will be held high or tri-stated (depending on the state of the control register drive mode and OE bits) prior to turning off the VCO. All clocks will start and stop without any abnormal behavior and meet all AC and DC parameters. This means no glitches, frequency shifting or amplitude abnormalities among others.

OE_INV	PWRDWN	Mode
0	0	Power Down
0	1	Normal
1	0	Normal
1	1	Power Down

**PWRDWN—Assertion**

When the power-down pin is sampled as being asserted by two consecutive rising edges of DIFC, all DIFT outputs will be held high or tri-stated (depending on the state of the control register drive mode and OE bits) on the next DIFC high to low transition. When the SMBus PWRDWN Drive Mode bit is

programmed to '0', all clock outputs will be held with the DIFT pin driven high at 2 x Iref and DIFC tri-stated. However, if the control register PWRDWN Drive Mode bit is programmed to '1', then both DIFT and the DIFC are tri-stated.

**PWRDWN—Deassertion**

The power-up latency is less than 1 ms. This is the time from the deassertion of the PWRDWN pin or the ramping of the power supply or the time from valid SRC\_IN input clocks until the time that stable clocks are output from the buffer chip (PLL locked). IF the control register PWRDWN Drive Mode bit is programmed to '1', all differential outputs must be driven high in less than 300 μs of the power down pin deassertion to a voltage greater than 200 mV.

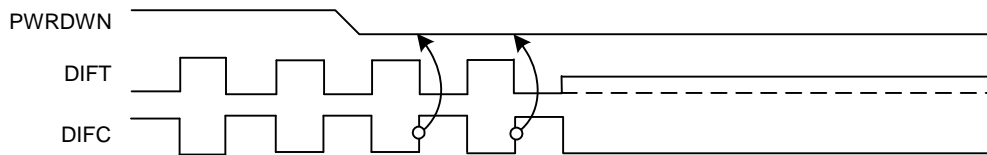


Figure 1. PWRDWN Assertion Diagram, OE\_INV = 0

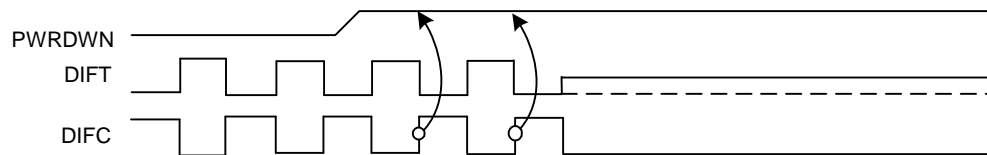


Figure 2. PWRDWN Assertion Diagram, OE\_INV = 1

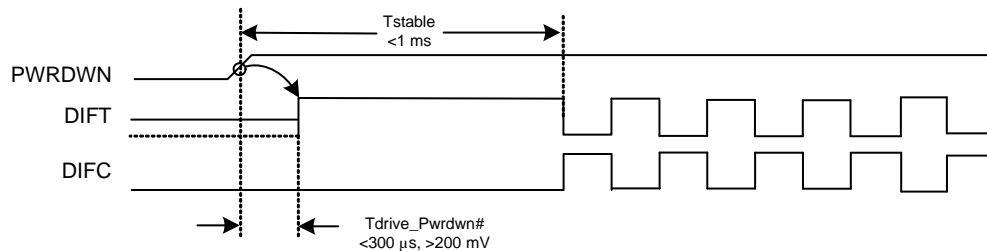


Figure 3. PWRDWN Deassertion Diagram, OE\_INV = 0

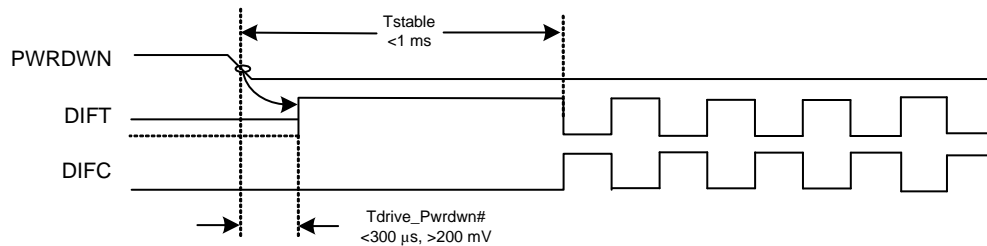


Figure 4. PWRDWN Deassertion Diagram, OE\_INV = 1

Table 4. Buffer Power-up State Machine

State	Description
0	3.3V Buffer power off
1	After 3.3V supply is detected to rise above 1.8V - 2.0V, the buffer enters state 1 and initiates a 0.2-ms–0.3-ms delay
2 <sup>[1]</sup>	Buffer waits for PWRDWN deassertion (and <b>waits for a valid clock on the SRC_IN input in PLL mode</b> )
3 <sup>[2,3,4]</sup>	Once the PLL is locked to the SRC_IN input clock, the buffer enters state 3 and enables outputs for normal operation

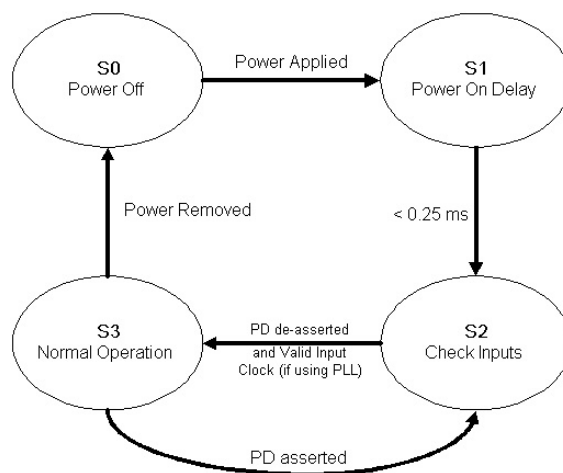


Figure 5. Buffer Power-up State Diagram

### SRC\_STP Clarification

The SRC\_STP signal is an asynchronous input used for clean stopping and starting the DIFT/C outputs. This input can be Active HIGH or Active LOW based on the strapped value of the OE\_INV input. The SRC\_STP signal is a debounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.) In the case where the output is disabled via OE control, the output will always be tri-stated regardless of the SRC\_STP Drive Mode register bit state.

### SRC\_STP Assertion

The impact of asserting the SRC\_STP pin is that all DIF outputs that are set in the control registers to stoppable via assertion of SRC\_STP are stopped after their next transition. When the control register SRC\_STP tri-state bit is programmed to '0', the final state of all stopped DIFT/C signals is DIFT clock = High and DIFC = Low. There will be no change to the output drive current values, DIFT will be driven high with a current value equal 6 x Iref, and DIFC will not be driven. When the control register SRC\_STP three-state bit is programmed to '1', the final state of all stopped DIF signals is low, both DIFT clock and DIFC clock outputs will not be driven.

Table 5. SRC\_STP Functionality<sup>[4]</sup>

OE_INV	SRC_STP	DIFT	DIFC
0	1	Normal	Normal
0	0	Iref * 6 or Float	Low
1	1	Iref * 6 or Float	Low
1	0	Normal	Normal

**Notes:**

1. Disabling of the SRC\_IN input clock prior to assertion of PWRDWN is an undefined mode and not recommended. Operation in this mode may result in glitches excessive frequency shifting.
2. The total power up latency from power-on to all outputs active is less than 1 ms (assuming a valid clock is present on SRC\_IN input).
3. In PLL Mode, if power is valid and PWRDWN is deasserted but no input clocks are present on the SRC\_IN input, DIF clocks will remain disabled. Only after valid input clocks are detected, valid power, PWRDWN deasserted with the PLL locked and stable, are the DIF outputs enabled.
4. In the case where OE is asserted low, the output will always be three-stated regardless of SRC\_STP drive mode register bit state.



### SRC\_STP Deassertion

All differential outputs that were stopped will resume normal operation in a glitch-free manner. The maximum latency from the deassertion to active outputs is between 2–6 DIFT/C clock periods (2 clocks are shown) with all DIFT/C outputs resuming simultaneously. If the control register tri-state bit is programmed to '1' (tri-state), then all stopped DIFT outputs will be driven high within 15 ns of SRC\_STP deassertion to a voltage greater than 200 mV.

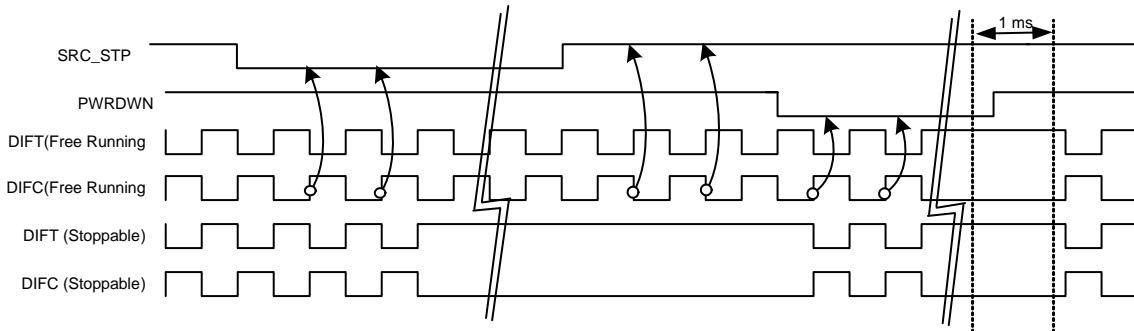


Figure 6. SRC\_STP = Driven, PWRDWN = Driven, OE\_INV = 0

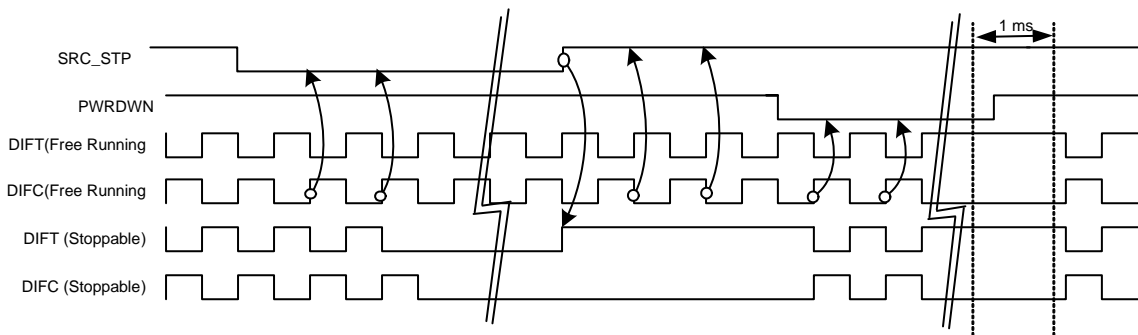


Figure 7. SRC\_STP = Tri-state, PWRDWN = Driven, OE\_INV = 0

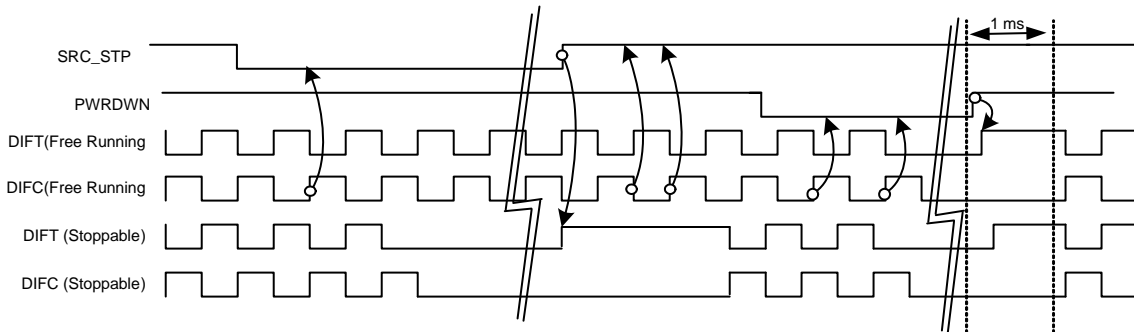


Figure 8. SRC\_STP = Tri-state, PWRDWN = Tri-state, OE\_INV = 0



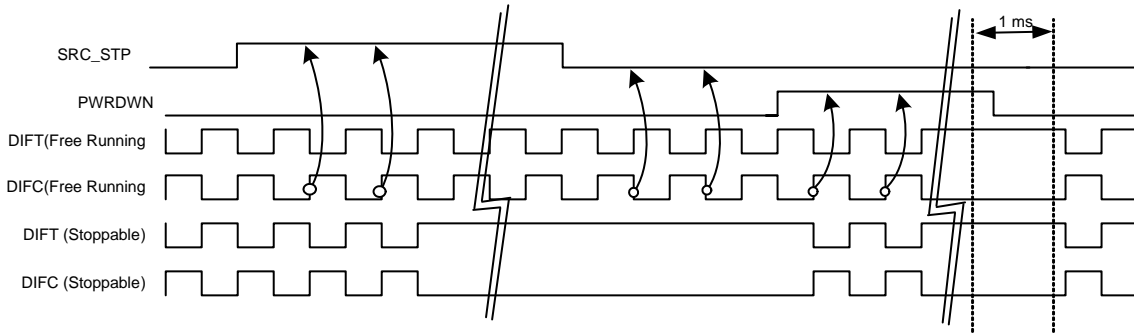


Figure 9. SRC\_STP = Driven, PWRDWN = Driven, OE\_INV = 1

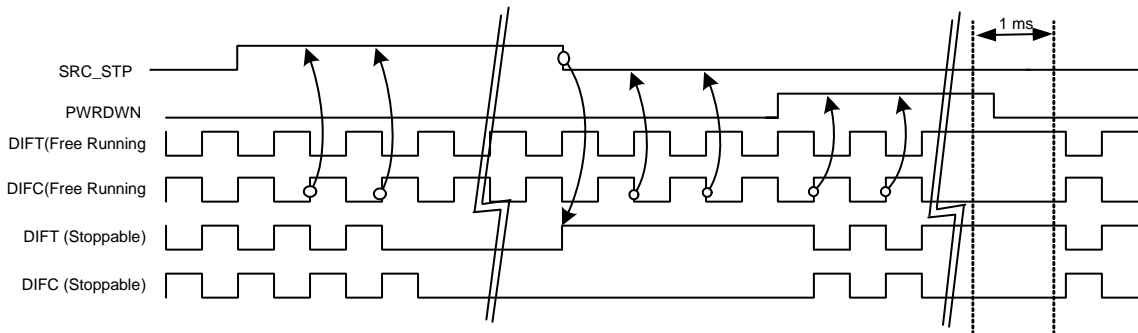


Figure 10. SRC\_STP = Tri-state, PWRDWN = Driven, OE\_INV = 1

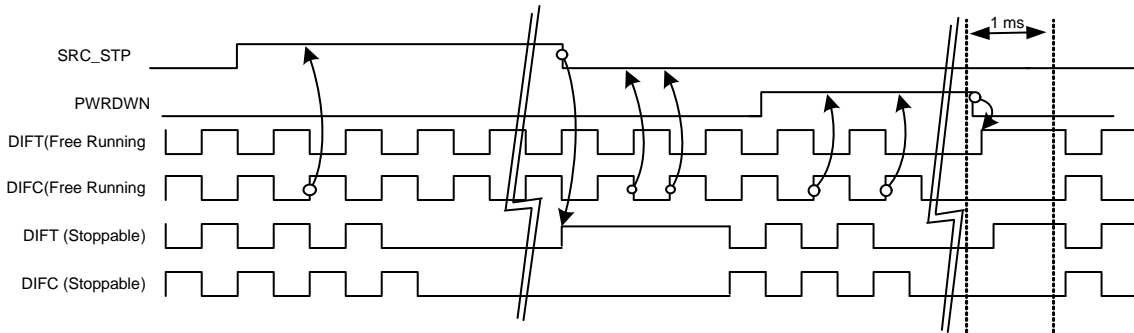


Figure 11. SRC\_STP = Tri-state, PWRDWN = Tri-state, OE\_INV = 1

### Output Enable Clarification

OE functionality allows for enabling and disabling individual outputs. OE\_1 and OE\_6 are Active HIGH or Active LOW inputs depending on the strapped value of the OE\_INV input. Disabling the outputs may be implemented in two ways, via writing a '0' to SMBus register bit corresponding to output of interest or by deasserting the OE input pin. In both methods, if SMBus registered bit has been written low or the OE pin is deasserted or both, the output of interest will be tri-stated. (The assertion and deassertion of this signal is absolutely asynchronous.)

Table 6. OE Functionality

OE_INV	OE (Pin)	OE (SMBus Bit)	DIF[T/C]
0	0	0	Tri-State
0	0	1	Tri-State
0	1	0	Tri-State
0	1	1	Enabled
1	0	0	Tri-State
1	0	1	Enabled
1	1	0	Tri-State
1	1	1	Tri-State

### **OE Assertion**

All differential outputs that were tri-stated will resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2–6 DIF clock periods. In addition, DIFT clocks will be driven high within 15 ns of OE assertion to a voltage greater than 200 mV.

### **OE Deassertion**

The impact of deasserting OE is that each corresponding output will transition from normal operation to tri-state in a glitch-free manner. The maximum latency from the deassertion to tri-stated outputs is between 2–6 DIF clock periods.

### **SRC\_DIV2# Clarification**

The SRC\_DIV2# input is used to configure the DIF output mode to be equal to the SRC\_IN input frequency or half the input frequency in a glitch-free manner. The SRC\_DIV2# function may be implemented via writing a '0' to SMBus register bit.

### **SRC\_DIV2# Assertion**

The impact of asserting the SRC\_DIV2# is that all DIF outputs will transition cleanly in a glitch-free manner from normal operation (output frequency equal to input) to half the input frequency within 2–6 DIF clock periods.

### **SRC\_DIV2# Deassertion**

The impact of deasserting the SRC\_DIV2# is that all DIF outputs will transition cleanly in a glitch-free manner from divide by 2 mode to normal (output frequency is equal to the input frequency) operation within 2–6 DIF clock periods.

### **PLL/BYPASS# Clarification**

The PLL/Bypass# input is used to select between bypass mode (no PLL) and PLL mode. In bypass mode, the input clock is passed directly to the output stage resulting in 50-ps additive jitter (50 ps + input jitter) on DIF outputs. In the case of PLL mode, the input clock is pass through a PLL to reduce high frequency jitter. The BYPASS# mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the PLL/BYPASS# pin low. In both methods, if the SMBus register bit has been written to '0' or PLL/BYPASS# pin is low or both, the device will be configure for BYPASS operation.

### **HIGH\_BW# Clarification**

The HIGH\_BW# input is used to set the PLL bandwidth. This mode is intended to minimize PLL peaking when two or more buffers are cascaded by staggering device bandwidths. The PLL high bandwidth mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the HIGH\_BW# pin is low or both, the device will be configured for high-bandwidth operation.

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage		-0.5	4.6	V
V <sub>DD_A</sub>	Analog Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	VDC
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	+150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	70	°C
T <sub>J</sub>	Temperature, Junction	Functional		150	°C
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000		V
UL-94	Flammability Rating	At 1/8 in.		V-0	
MSL	Moisture Sensitivity Level			1	

**DC Electrical Specifications**

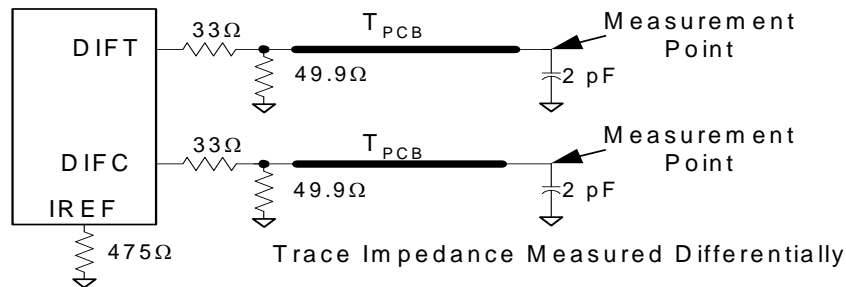
Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD_A</sub> , V <sub>DD</sub>	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V <sub>IL12C</sub>	Input Low Voltage	SDATA, SCLK	-	1.0	V
V <sub>IH12C</sub>	Input High Voltage	SDATA, SCLK	2.2	-	V
V <sub>IL</sub>	3.3V Input Low Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	3.3V Input High Voltage		2.0	V <sub>DD</sub> + 0.5	V
V <sub>OL</sub>	3.3V Output Low Voltage	I <sub>OL</sub> = 1 mA	-	0.4	V
V <sub>OH</sub>	3.3V Output High Voltage	I <sub>OH</sub> = -1 mA	2.4	-	V
I <sub>IL</sub>	Input Low Leakage Current	except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	-5		μA
I <sub>IH</sub>	Input High Leakage Current	except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>		5	μA
C <sub>IN</sub>	Input Pin Capacitance		1.5	5	pF
C <sub>OUT</sub>	Output Pin Capacitance		--	6	pF
L <sub>IN</sub>	Pin Inductance		-	7	nH
I <sub>DD3.3V</sub>	Dynamic Supply Current	At max. load, Full Active Bypass Mode	-	92	mA
		At max. load, Full Active PLL Mode	-	115	mA
		OE1 and OE6 deasserted, Bypass	-	60	mA
		SRC_STP asserted, Outputs Driven, Bypass	-	80	mA
		SRC_STP asserted, Outputs Tri-state, Bypass	-	2	mA
		SRC_STP asserted, Outputs Driven, PLL	-	85	mA
		SRC_STP asserted, Outputs Tri-State, PLL	-	2	mA
I <sub>PD3.3V</sub>	Power-down Supply Current	PWRDWN asserted, Outputs driven	-	40	mA
		PWRDWN asserted, Outputs Tri-stated	-	4	mA

**AC Electrical Specifications** (Measured in High Bandwidth Mode)

Parameter	Description	Condition	Min.	Max.	Unit
<b>SRC_IN at 0.7V</b>					
T <sub>PERIOD</sub>	Average Period	Measured at crossing point V <sub>OX</sub>	9.9970	10.0533	ns
T <sub>ABSMIN-IN</sub>	Absolute minimum clock periods	Measured at crossing point V <sub>OX</sub>	9.8720		ns
T <sub>R</sub> / T <sub>F</sub>	DIFT and DIFC Rise and Fall Times	Single ended measurement: V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V (Averaged)	0.6	4	V/ns
V <sub>IH</sub>	Differential Input High Voltage		150		mV
V <sub>IL</sub>	Differential Input Low Voltage			-150	mV
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing	Measured SE	250	550	mV

**AC Electrical Specifications** (continued) (Measured in High Bandwidth Mode)

Parameter	Description	Condition	Min.	Max.	Unit
$\Delta V_{OX}$	Vcross Variation over all edges	Measured SE		140	mV
$V_{RB}$	Differential Ringback Voltage		-100	100	mV
$T_{STABLE}$	Time before ringback allowed		500		ps
$V_{MAX}$	Absolute maximum input voltage			1.15	V
$V_{MIN}$	Absolute minimum input voltage		-0.3		V
$T_{DC}$	DIFT and DIFC Duty Cycle	Measured at crossing point $V_{OX}$	45	55	%
$T_{RFM}$	Rise/Fall Matching	Determined as a fraction of $2 * (T_R - T_F) / (T_R + T_F)$	-	20	%
<b>DIF at 0.7V</b>					
$F_{IN}$	Input Frequency	Bypass or PLL 1:1	90	210	MHz
$F_{ERROR}$	Input/Output Frequency Error	Bypass or PLL 1:1	-	0	ppm
$T_{DC}$	DIFT and DIFC Duty Cycle	Measured at crossing point $V_{OX}$	45	55	%
$T_{PERIOD}$	Average Period	Measured at crossing point $V_{OX}$ at 100 MHz	9.9970	10.0533	ns
$T_R / T_F$	DIFT and DIFC Rise and Fall Times	Single ended measurement: $V_{OL} = 0.175$ to $V_{OH} = 0.525V$ (Averaged)	175	700	ps
$T_{RFM}$	Rise/Fall Matching	Determined as a fraction of $2 * (T_R - T_F) / (T_R + T_F)$	-	20	%
$\Delta T_R / \Delta T_F$	Rise and Fall Time Variation Variation	Single ended measurement: $V_{OL} = 0.175$ to $V_{OH} = 0.525V$ (Real Time)	-	125	ps
$V_{HIGH}$	Voltage High	Measured SE	660	850	mv
$V_{LOW}$	Voltage Low	Measured SE	-150	-	mv
$V_{OX}$	Crossing Point Voltage at 0.7V Swing	Measured SE	250	550	mv
$\Delta V_{OX}$	Vcross Variation over all edges	Measured SE	-	140	mV
$V_{OVS}$	Maximum Overshoot Voltage	Measured SE	-	$V_{HIGH} + 0.3$	V
$V_{UDS}$	Minimum Undershoot Voltage	Measured SE	-	-0.3	V
$V_{RB}$	Ring Back Voltage	Measured SE	0.2	N/A	V
$T_{CCJ}$	Cycle to Cycle Jitter	PLL Mode	-	50	ps
		Bypass Mode (Jitter is additive)	-	50	ps
$T_{SKEW}$	Any DIFT/C to DIFT/C Clock Skew	Measured at crossing point $V_{OX}$	-	50	ps
$T_{PD}$	Input to output skew in PLL mode	Measured at crossing point $V_{OX}$	-	$\pm 250$	ps
	Input to output skew in Non-PLL mode	Measured at crossing point $V_{OX}$	2.5	4.5	ns



**Figure 12. Differential Clock Termination**



Switching Waveforms

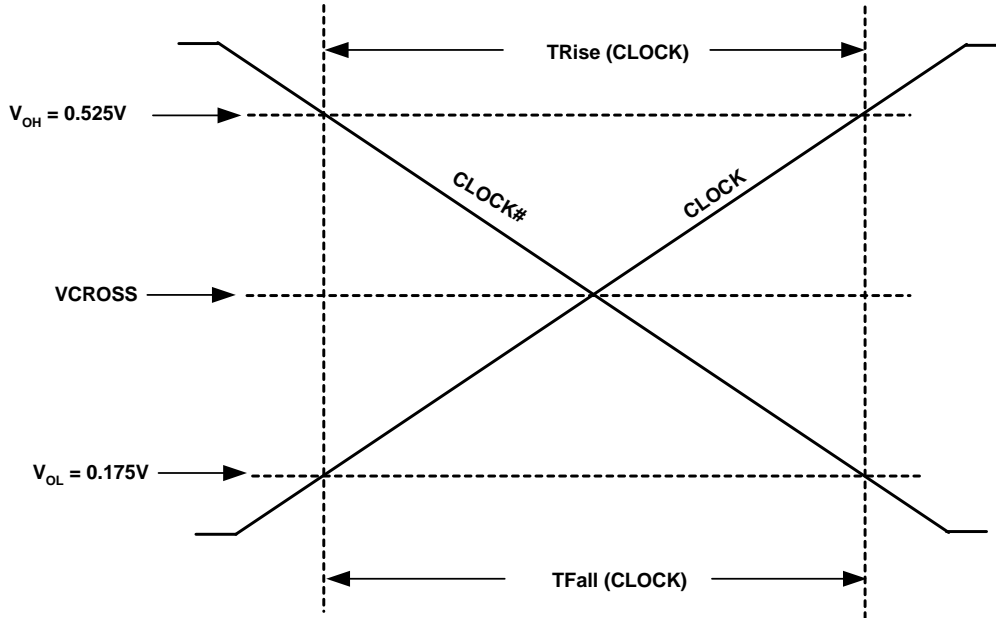


Figure 13. Single-Ended Measurement Points for TRise and TFall

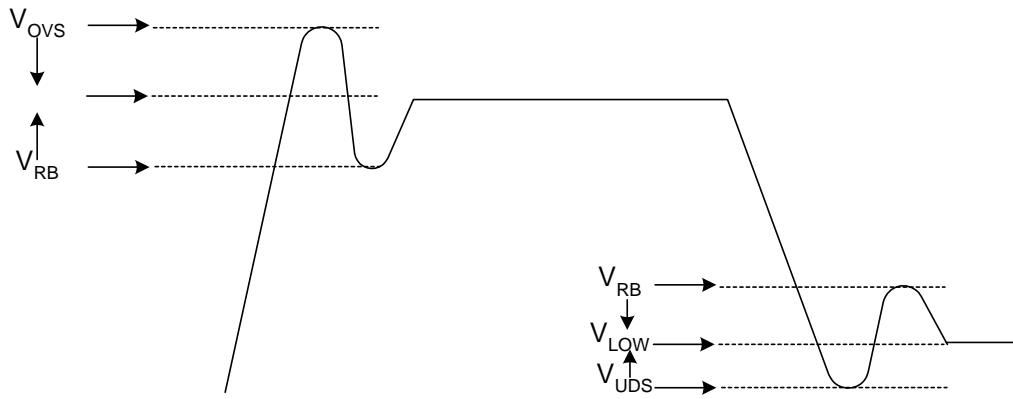


Figure 14. Single-ended Measurement Points for  $V_{OVS}$ ,  $V_{UDS}$  and  $V_{RB}$

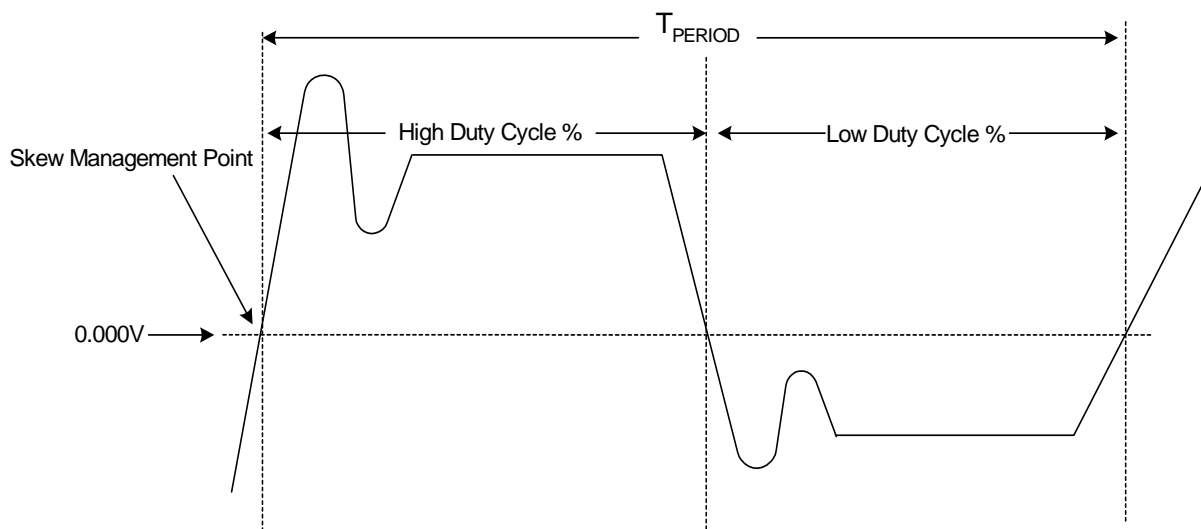


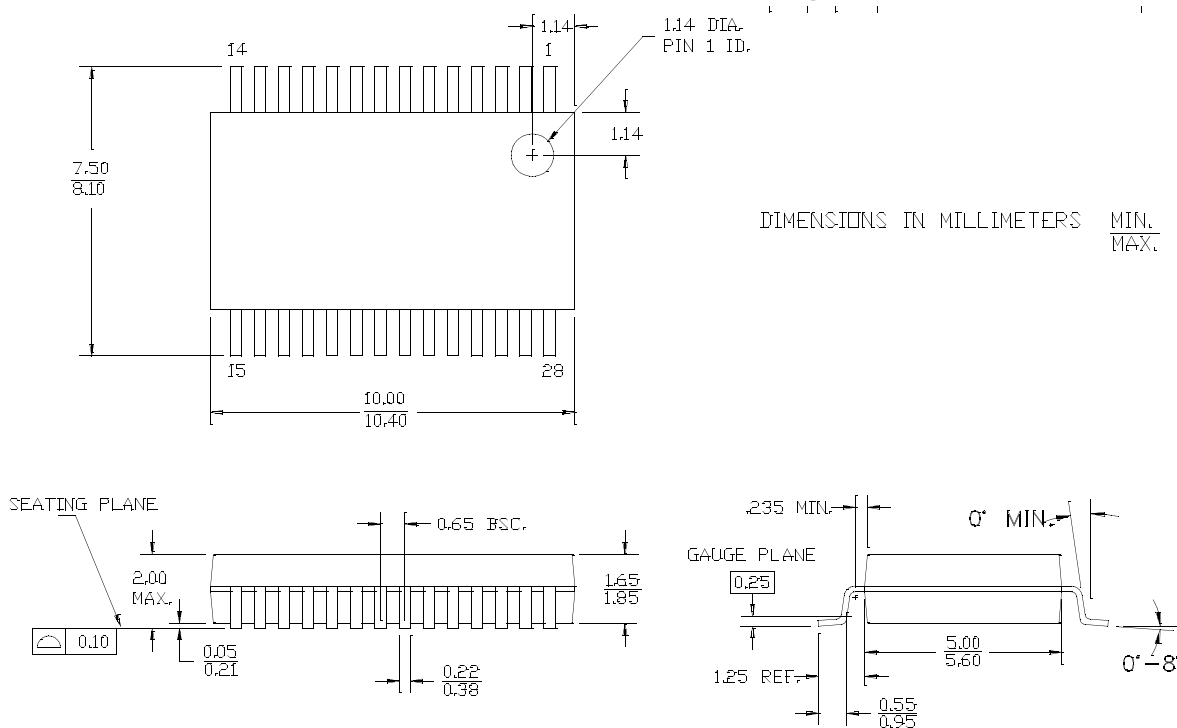
Figure 15. Differential (Clock-Clock#) Measurement Points (Tperiod, Duty Cycle and Jitter)

**Ordering Information**

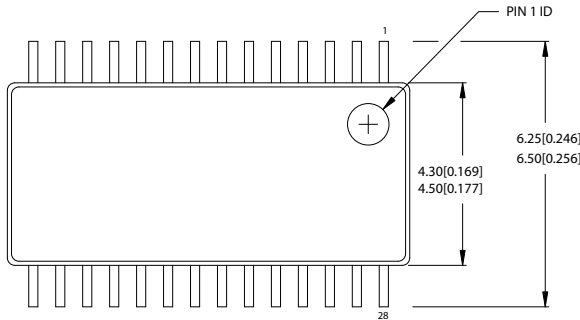
Ordering Code	Package Type	Operating Range
<b>Lead-free</b>		
CY28400OXC-2	28-pin SSOP	Commercial, 0°C to 70°C
CY28400OXC-2T	28-pin SSOP—(Tape and Reel)	Commercial, 0°C to 70°C
CY28400ZXC-2	28-pin TSSOP	Commercial, 0°C to 70°C
CY28400ZXC-2T	28-pin TSSOP—(Tape and Reel)	Commercial, 0°C to 70°C

**Package Drawing and Dimensions**

**28-Lead (5.3 mm) Shrunken Small Outline Package O28**



**28-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z28.173**

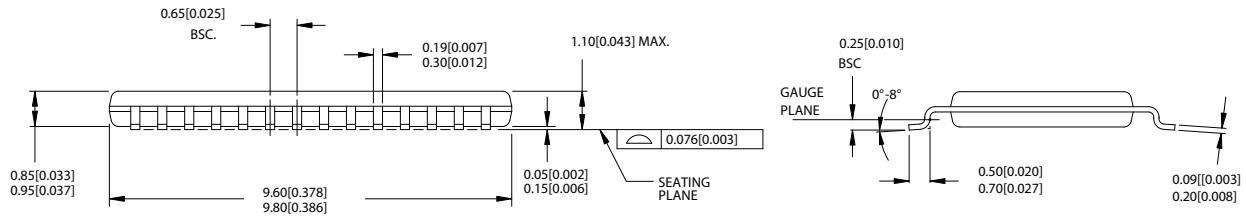


DIMENSIONS IN MM[INCHES] MIN.  
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.16 gms

PART #	
Z28.173	STANDARD PKG.
ZZ28.173	LEAD FREE PKG.



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