成越科技股份有限公司
Cheng Yue Technology Inc.

CY2890-F02.

Digital TFT-LCD Panel Timing Controller

Resolution : 800x480, 640x480, 800x600, 1024x600
1024x768, 720x480, 320x240, 480x272

Room 2, 4F., No. 128, Minsheng Rd.,
Hsin-Chu City 30043, Taiwan, R.O.C.
Tel : 886-3-531-3216
Fax : 886-3-531-2523
http://www.cyti.com.tw/

30043 新竹市民生路 128 號 4F-2
Tel : (03) 531-3216
Fax : (03) 531-2523
http://www.cyti.com.tw/

Revision History

Version	DATE	Description
2.1	2007/09/30	P4, update package as LQFP64
2.2	2007/11/20	P10, update pull-up/pull-down resistor as TYP 80K
2.3	2008/12/02	P4, remove 5V tolerant function. P35, remove CY2890-F01, Outline 10x10x1.4mm package
2.4	2009/01/16	P4,P10 supply voltage update as 2.7 V ~ 3.6 V

Ordering Information

Part No.	Package	Descriptions
CY2890-F02	64pin LQFP, Green package	Outline as 7x7x1.4mm

Content

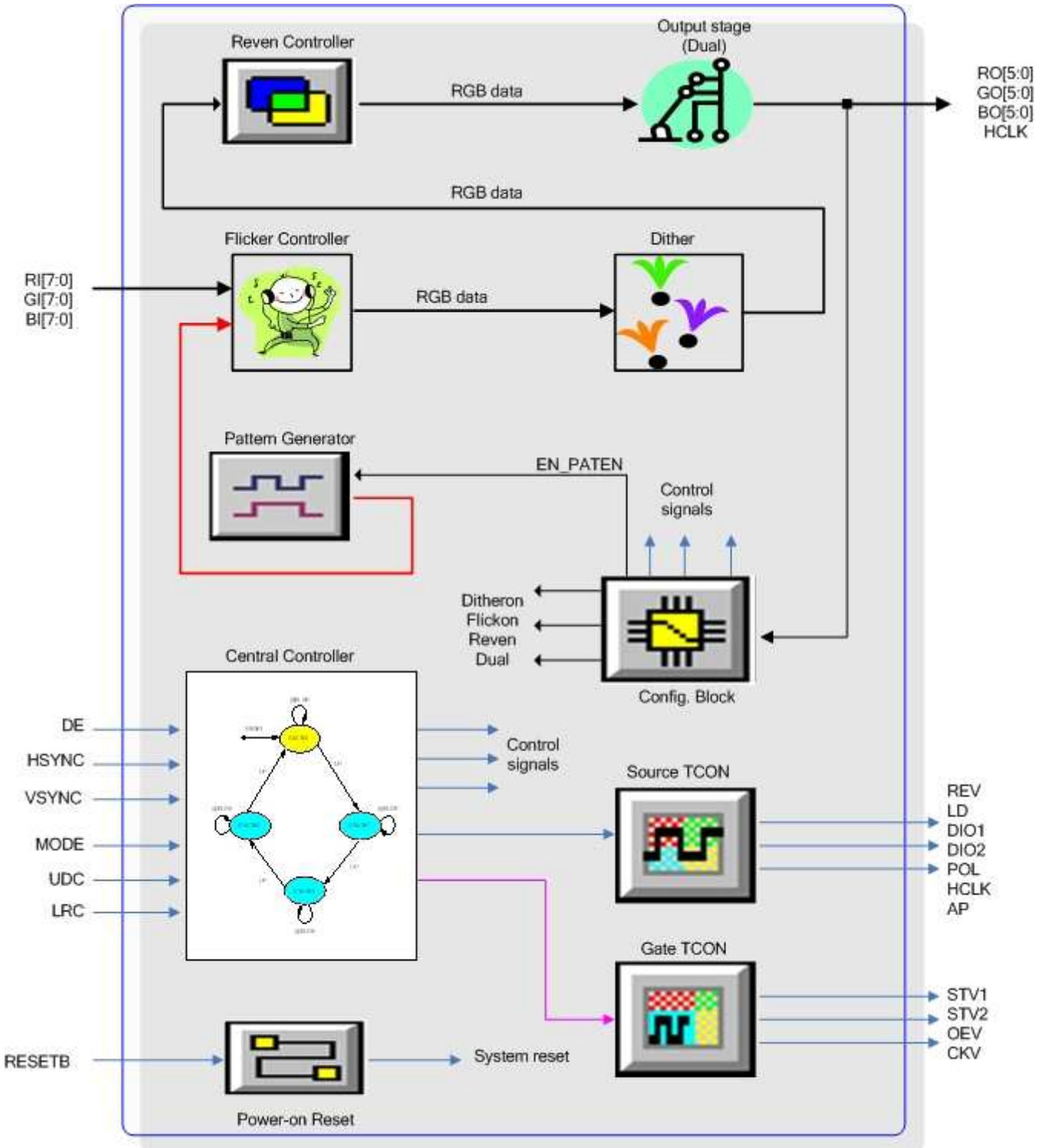
1. General Description

The CY2890-F02 is a digital TFT-LCD timing controller with built-in “dithering”, “reverse”, “dual”, “flicker” and “pattern generator” functions. The input signal is digital R/G/B with HSYNC/VSYNC or DE. User can use the MODE pin to select input signal to be either HSYNC mode or DE mode. The R/G/B input is fixed to 8 bits data width and the output is always 6 bits. The convert from 8 bits RGB to 6 bits RGB can be either directly truncated or dithering depends on the “DITHER” function is on or off. When DITHER is on CY2890 will emulate 8 bits gray level on 6 bits RGB bus. The users will have a more vivid picture with dither function on. The “Reverse” function is designed for reducing EMI. The key is to lower down the R/G/B transition count. The “dual” function can set the output HCLK to latch the output data at both edges. Set “dual” on can lower down the HCLK frequency to half. With the “Reverse” and “dual” functions, the board level system design can be relaxed. We also have a built-in test pattern generator for users to do a quick final test or aging burning test. The built-in test pattern generator has 24 very popular patterns. It will be free running when MODE = 1, HSYNC = 1 or MODE = 0, DE = 1. You can stop the free-running built-in test pattern at any time. The “flicker” function is used to reduce the flicker phenomenon. Beside all the functions we just mentioned, we also support 8 different panel resolutions, which can be selected by external strap resistors. Through CY2890, all the necessary horizontal and vertical control signals to TFT-LCD are handled automatically. This includes the polarity invert control. There is a built-in power-on reset circuit in the chip, no need for user to add external reset circuit. If users want to extend the power-on reset, an external capacitor can be added.

2. Features

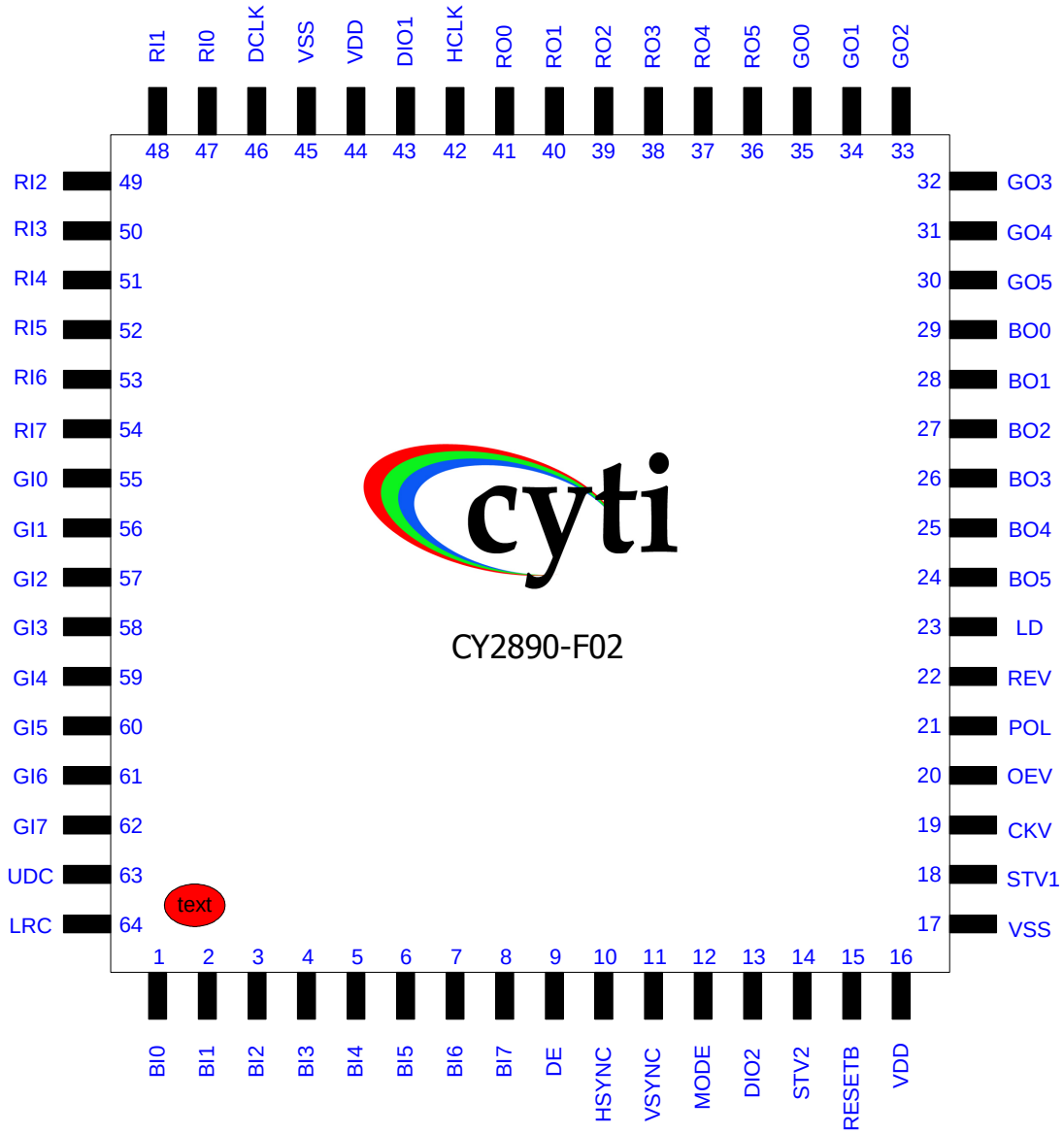
- Supporting 8 kinds of different digital TFT-LCD panels
  800 x 480 (*), 640 x 480, 800 x 600, 1024 x 600, 1024 x 768, 720 x 480, 320 x 240, 480 x 272
- Input can be HSYNC mode or DE mode
- Support 16.7M colors dither function
- Support FLICKER reduction function.
- Support DUAL edge function
- Support up/down, left/right scan control
- Support REVERSE function.
- Built-in test pattern generator with 24 popular patterns
- Built-In Power-On reset circuit
- Built-in polarity inverted function.
- Provide source and gate drivers control timing.
- Master clock frequency: 70 MHz max.
- Single supply voltage : +2.7V to +3.6V
- Wide temperature operation range -40°C / +95°C
- ESD meet class3 criteria
  HBM 4KV, MM 400V, LATCH-UP 100mA
- 64 LQFP Green Package

3. Block Diagram



CY2890-F0X Block Diagram

4. Pin Assignment



5. Pin Description

Pin No.	Symbol	I/O	Description	Internal
1	BI0	I	Blue color data input, bit0 (LSB)	pull-down
2	BI1	I	Blue color data input, bit1	pull-down
3	BI2	I	Blue color data input, bit2.	
4	BI3	I	Blue color data input, bit3.	
5	BI4	I	Blue color data input, bit4.	
6	BI5	I	Blue color data input, bit5.	
7	BI6	I	Blue color data input, bit6.	
8	BI7	I	Blue color data input, bit7 (MSB).	
9	DE / TEST	I	MODE = H : Data enable signal input, active high MODE = L : enable built-in patterns when DE = H, Stop when DE = L	pull-down
10	HSYNC / TEST	I	MODE = L : Negative polarity horizontal sync input MODE = H :enable built-in patterns when HSYNC = H, Stop when HSYNC = L	pull-down
11	VSYNC	I	Negative polarity vertical sync input	pull-down
12	MODE	I	DE / SYNC mode select H : DE mode L : SYNC mode	pull-up
13	DIO2	I/O	Source driver start pulse 2 LRC = 0, output LRC = 1, Tri-state	
14	STV2	I/O	Gate driver start pulse 2. UDC = 0, output UDC = 1, Tri-state	
15	RESETB	I	Active low system reset pin	pull-up
16	VDD	I	Power supply voltage.	
17	VSS	I	Power supply ground.	
18	STV1	I/O	Gate driver start pulse 1. UDC = 0, Tri-state UDC = 1, Output	
19	CKV	O	Gate driver shift clock.	
20	OEV	O	Gate driver output enable	
21	POL	O	Source driver polarity select	
22	REV	O	Source driver data reverse control.	
23	LD	O	Source driver latch pulse and output enable.	
24	BO5	O	Blue color data output, bit5 (MSB).	
25	BO4	O	Blue color data output, bit4.	
26	BO3	O	Blue color data output, bit3.	
27	BO2	O	Blue color data output, bit2.	
28	BO1	O	Blue color data output, bit1.	
29	BO0	O	Blue color data output, bit0 (LSB).	
30	GO5	O	Green color data output, bit5 (MSB).	
31	GO4	O	Green color data output, bit4.	
32	GO3	O	Green color data output, bit3.	
33	GO2	O	Green color data output, bit2.	

Pin No.	Symbol	I/O	Description	Internal
34	GO1	O	Green color data output, bit1.	
35	GO0	O	Green color data output, bit0 (LSB).	
36	RO5	I/O	Red data output, bit5 (MSB). Reven on/off setting	pull-up
37	RO4	I/O	Red color data output, bit4. Dual on/off setting	pull-up
38	RO3	I/O	Red color data output, bit3 Dither on /off setting	pull-up
39	RO2	I/O	Red color data output, bit2. Panel resolution select bit 2, RES[2],	pull-up
40	RO1	I/O	Red color data output, bit1. Panel resolution select bit 1, RES[1],	pull-up
41	RO0	I/O	Red color data output, bit0. (LSB) Panel resolution select bit 0, RES[0],	pull-up
42	HCLK	O	Source driver clock	
43	DIO1	I/O	Source driver start pulse 1 LRC = 0, Tri-state LRC = 1, Output	
44	VDD	I	Power supply voltage.	
45	VSS	I	Power supply ground.	
46	DCLK	I	Clock signal; latch input data at DCLK falling edge.	
47	RI0	I	Red color data input, bit0 (LSB)	pull-down
48	RI1	I	Red color data input, bit1.	pull-down
49	RI2	I	Red color data input, bit2.	
50	RI3	I	Red color data input, bit3.	
51	RI4	I	Red color data input, bit4.	
52	RI5	I	Red color data input, bit5.	
53	RI6	I	Red color data input, bit6.	
54	RI7	I	Red color data input, bit7 (MSB).	
55	GI0	I	Green color data input, bit0 (LSB)	pull-down
56	GI1	I	Green color data input, bit1	pull-down
57	GI2	I	Green color data input, bit2.	
58	GI3	I	Green color data input, bit3.	
59	GI4	I	Green color data input, bit4.	
60	GI5	I	Green color data input, bit5.	
61	GI6	I	Green color data input, bit6.	
62	GI7	I	Green color data input, bit7 (MSB).	
63	UDC	I	Up / Down scan control.	pull-up
64	LRC	I	Left / Right scan control.	pull-up

6. Function Description

◆ Panel Select Table for CY2890-F02

CY2890 can support 8 different kind panel resolutions. To select different panel resolution users have to add an external pull-up resistors at pin39, 40 or 41. At power-on, CY2890 will read in pin39, 40 and 41 as RES[2:0]. In the table below, we mark “x” mean don’t do anything. We mark “pull-down” mean you have to add an external resistor to GROUND.

RES[2:0] (RO[2:0])				RESOLUTION	CONNECTED TO PIN EXTERNAL PULL-DOWN RESISTOR VALUE
Value	Pin39 (RO2)	Pin40 (RO1)	Pin41 (RO0)		
0	x	x	x	800x480	No External Resistors
1	x	x	Pull-down	640x480	10K
2	x	Pull-down	X	800x600	10K
3	x	Pull-down	Pull-down	1024x600	10K
4	Pull-down	x	X	1024x768	10K
5	Pull-down	x	Pull-down	720x480	10K
6	Pull-down	Pull-down	X	320x240	10K
7	Pull-down	Pull-down	Pull-down	480x272	10K

◆ Dither/Dual/Reven Enable or Disable Setting Table for CY2890-F02

The 3 major function blocks, dither, dual and reven. They can be enabled or disabled by using an external strap resistor. This strap resistor will be read into CY2890 during the power-on reset period. That means once you make a change, in order to make the change activated, you have to redo the power on step.

PIN NUMBER	NAME	STRAP FUNCTION	DESCRIPTION	CONNECTED TO PIN EXTERNAL PULL-DOWN RESISTOR VALUE
36	RO5	REVEN	REVEN function enable/disable No connect : enable (internal pull-up) Connect Pull-down : disable	10K
37	RO4	DUAL	DUAL function enable/disable No connect : enable (internal pull-up) Connect Pull-down : disable	10K
38	RO3	DITHER	DITHER function enable/disable No connect : disable (internal pull-up) Connect Pull-down : enable	10K

7. DC Characteristics

◆ Absolute maximum ratings

PARAMETER	SYMBOL	RATING	UNIT
Power supply	V_{DD}	2.5 to 3.8	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to 125	℃

◆ Recommended operating conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply	V_{DD}	2.7	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating temperature	T_{OPR}	-40	-	95	℃

◆ DC Electrical characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA	
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA	
Tri-state leakage current	I_{OZ}		-10	-	10	μA	
Logic input low voltage	V_{IL}	CMOS	-	-	$0.3V_{DD}$	V	Note 1
Schmitt input low voltage	V_{SIL}	CMOS	-	-	$0.3V_{DD}$	V	Note 2
Logic input high voltage	V_{IH}	CMOS	$0.7V_{DD}$	-	-	V	Note 1
Schmitt input high voltage	V_{SIH}	CMOS	$0.7V_{DD}$	-	-	V	Note 2
Output low voltage	V_{OL}	I_{OL} = 4mA	-	-	$0.3V_{DD}$	V	Note 3
Output high voltage	V_{OH}	I_{OH} = -4mA	$0.7V_{DD}$	-	-	V	Note 3
Output low voltage	V_{OL}	I_{OL} = 8mA	-	-	$0.3V_{DD}$	V	Note 4
Output high voltage	V_{OH}	I_{OH} = -8mA	$0.7V_{DD}$	-	-	V	Note 4
Input pull up / down resistance	R_I	V_{IL} = 0V or V_{IH} = V_{DD}	-	80	-	KΩ	Note 5

Note 1: MODE, UDC, LRC, RI0~RI7, GI0~GI7, BI0~BI7.
Note 2: DCLK, HSYNC, VSYNC, DE, RESETB
Note 3: CKV, POL, REV, LD, DIO1, DIO2, STV1, STV2, OEV, AP, RO0~RO5, GO0~GO5, BO0~BO5.
Note 4: HCLK
Note 5: RESETB, HSYNC, VSYNC, DE, MODE, UDC, LRC, RI0, RI1, GI0, GI1, BI0, BI1, RO0~RO5

8. AC Characteristics

◆ SYNC mode Input signal characteristic, 800 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	34	-	NS	
CLOCK FREQUENCY	FCLK	-	29.5	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	11.2	-	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	11.2	-	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	890	928	1600	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	88			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	800			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	514	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	29			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 800 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	34	-	NS	
	FREQUENCY	FCLK	-	29.5	40	MHZ	
	LOW LEVEL WIDTH	TWCL	11.2	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	11.2	-	-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	6	NS	
	HORIZONTAL PERIOD	THP	820	928	1600	TCLK	
	HORIZONTAL VALID	THV	800			TCLK	
	HORIZONTAL BLANK	THBK	THP - THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	6	NS	

◆ Output Signal Characteristics, 800 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN).	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 640 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	34	-	NS	
CLOCK FREQUENCY	FCLK	-	29.5	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	11.2	-	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	11.2	-	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	790	900	1280	TCLK	
HSYNC PULSE WIDTH	THW	-	96	-	TCLK	
HSYNC BACK PORCH	THBP	-	48	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	144			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	640			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	518	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	33			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 640 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	34	-	NS	
	FREQUENCY	FCLK	-	29.5	40	MHZ	
	LOW LEVEL WIDTH	TWCL	11.2	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	11.2	-	-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	6	NS	
	HORIZONTAL PERIOD	THP	660	800	1280	TCLK	
	HORIZONTAL VALID	THV	640			TCLK	
	HORIZONTAL BLANK	THBK	THP - THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	6	NS	

◆ Output Signal Characteristics, 640 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 800 x 600

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	20	25	-	NS	
CLOCK FREQUENCY	FCLK	-	40	50	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	9		-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	9		-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	890	1000	1600	TCLK	
HSYNC PULSE WIDTH	THW	-	48	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	88			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	800			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	640	660	1200	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	36			THP	
VERTICAL DATA VALID WIDTH	TW	600			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 800 x 600

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	20	25	-	NS	
	FREQUENCY	FCLK	-	40	50	MHZ	
	LOW LEVEL WIDTH	TWCL	9	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	9	-	-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDEF	-	-	6	NS	
	HORIZONTAL PERIOD	THP	820	1000	1600	TCLK	
	HORIZONTAL VALID	THV	800			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	605	660	1200	THP	
	VERTICAL VALID	TW	600			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	6	NS	

◆ Output Signal Characteristics, 800 x 600

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	100	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 1024 x 600

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	14.3	15.4	-	NS	
CLOCK FREQUENCY	FCLK	-	65	70	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	6.5		-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	6.5		-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	1190	1280	2047	TCLK	
HSYNC PULSE WIDTH	THW	-	80	-	TCLK	
HSYNC BACK PORCH	THBP	-	80	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	160			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	1024			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	640	660	1200	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	36			THP	
VERTICAL DATA VALID WIDTH	TW	600			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 1024 x 600

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	14.3	15.4	-	NS	
	FREQUENCY	FCLK	-	65	70	MHZ	
	LOW LEVEL WIDTH	TWCL	6.5		-	NS	
	HIGH LEVEL WIDTH	TWCH	6.5		-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	4	NS	
	HORIZONTAL PERIOD	THP	1044	1280	2047	TCLK	
	HORIZONTAL VALID	THV	1024			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	605	660	1200	THP	
	VERTICAL VALID	TW	600			THP	
	VERTICAL BLANK	TVBK	TVP - TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	4	NS	

◆ Output Signal Characteristics, 1024 x 600

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	160	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 1024 x 768

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	14.3	15.4	-	NS	
CLOCK FREQUENCY	FCLK	-	65	70	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	6.5		-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	6.5		-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	1190	1280	2047	TCLK	
HSYNC PULSE WIDTH	THW	-	80	-	TCLK	
HSYNC BACK PORCH	THBP	-	80	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	160			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	1024			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	812	845	1536	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	40			THP	
VERTICAL DATA VALID WIDTH	TW	768			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 1024 x 768

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	14.3	15.4	-	NS	
	FREQUENCY	FCLK	-	65	70	MHZ	
	LOW LEVEL WIDTH	TWCL	6.5		-	NS	
	HIGH LEVEL WIDTH	TWCH	6.5		-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	4	NS	
	HORIZONTAL PERIOD	THP	1044	1280	2047	TCLK	
	HORIZONTAL VALID	THV	1024			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	773	845	1536	THP	
	VERTICAL VALID	TW	768			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	4	NS	

◆ Output Signal Characteristics, 1024 x 768

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	160	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 720 x 480

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	25	34	-	NS	
CLOCK FREQUENCY	FCLK	-	29.5	40	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	11.2	-	-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	11.2	-	-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	804	900	1440	TCLK	
HSYNC PULSE WIDTH	THW	-	40	-	TCLK	
HSYNC BACK PORCH	THBP	-	40	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	80			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	720			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	515	525	960	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	29			THP	
VERTICAL DATA VALID WIDTH	TW	480			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 720 x 480

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	25	34	-	NS	
	FREQUENCY	FCLK	-	29.5	40	MHZ	
	LOW LEVEL WIDTH	TWCL	11.2	-	-	NS	
	HIGH LEVEL WIDTH	TWCH	11.2	-	-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	6	NS	
	HORIZONTAL PERIOD	THP	740	900	1440	TCLK	
	HORIZONTAL VALID	THV	720			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	485	525	960	THP	
	VERTICAL VALID	TW	480			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	6	NS	

◆ Output Signal Characteristics, 720 x 480

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	66	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 320 x 240

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	28.6	93	-	NS	
CLOCK FREQUENCY	FCLK	-	10.7	35	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	12.8		-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	12.8		-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	370	416	512	TCLK	
HSYNC PULSE WIDTH	THW	-	26	-	TCLK	
HSYNC BACK PORCH	THBP	-	20	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	46			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	320			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	260	288	360	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	15			THP	
VERTICAL DATA VALID WIDTH	TW	240			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

◆ DE mode Input signal characteristics, 320 x 240

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	28.6	93	-	NS	
	FREQUENCY	FCLK	-	10.7	35	MHZ	
	LOW LEVEL WIDTH	TWCL	12.8		-	NS	
	HIGH LEVEL WIDTH	TWCH	12.8		-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	6	NS	
	HORIZONTAL PERIOD	THP	340	416	512	TCLK	
	HORIZONTAL VALID	THV	320			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	245	288	360	THP	
	VERTICAL VALID	TW	240			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	6	NS	

◆ Output Signal Characteristics, 320 x 240

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	50	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

◆ SYNC mode Input signal characteristic, 480 x 272

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
CLOCK PERIOD	TCLK	28.6	93	-	NS	
CLOCK FREQUENCY	FCLK	-	10.7	35	MHZ	
CLOCK LOW LEVEL WIDTH	TWCL	12.8		-	NS	
CLOCK HIGH LEVEL WIDTH	TWCH	12.8		-	NS	
CLOCK RISE, FALL TIME	TCLKR, TCLKF	-	-	3	NS	
HSYNC PERIOD	THP	550	600	960	TCLK	
HSYNC PULSE WIDTH	THW	-	36	-	TCLK	
HSYNC BACK PORCH	THBP	-	30	-	TCLK	
HSYNC WIDTH + BACK PORCH	THW+ THBP	66			TCLK	
HORIZONTAL VALID DATA WIDTH	THV	480			TCLK	
HSYNC FRONT PORCH	THFP	THP – THW - THBP - THV			TCLK	
HORIZONTAL BLANK	THBK	THP – THV			TCLK	
VSYNC PERIOD	TVP	297	299	544	THP	
VSYNC PULSE WIDTH	TVW	-	3	-	THP	
VSYNC BACK PORCH	TVBP	19			THP	
VERTICAL DATA VALID WIDTH	TW	272			THP	
VSYNC FRONT PORCH	TVFP	TVP – TVW - TVBP - TW			THP	
VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA SETUP TIME	TDS	5	-	-	NS	
DATA HOLD TIME	TDH	5	-	-	NS	

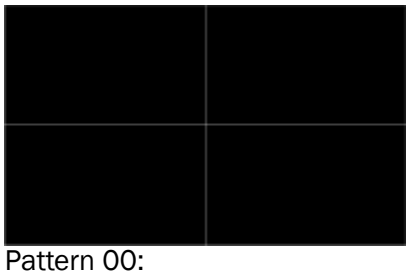
◆ DE mode Input signal characteristics, 480 x 272

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK	PERIOD	TCLK	28.6	93	-	NS	
	FREQUENCY	FCLK	-	10.7	35	MHZ	
	LOW LEVEL WIDTH	TWCL	12.8		-	NS	
	HIGH LEVEL WIDTH	TWCH	12.8		-	NS	
	RISE, FALL TIME	TCLKR, CLKF	-	-	3	NS	
	DUTY	-	0.45	0.50	0.55	-	
DE	SETUP TIME	TDES	5	-	-	NS	
	HOLD TIME	TDEH	5	-	-	NS	
	RISE, FALL TIME	TDER, TDEF	-	-	6	NS	
	HORIZONTAL PERIOD	THP	500	600	960	TCLK	
	HORIZONTAL VALID	THV	480			TCLK	
	HORIZONTAL BLANK	THBK	THP – THV			TCLK	
	VERTICAL PERIOD	TVP	277	299	544	THP	
	VERTICAL VALID	TW	272			THP	
	VERTICAL BLANK	TVBK	TVP – TW			THP	
DATA	SETUP TIME	TDS	5	-	-	NS	
	HOLD TIME	TDH	5	-	-	NS	
	RISE, FALL TIME	TDR, TDF	-	-	6	NS	

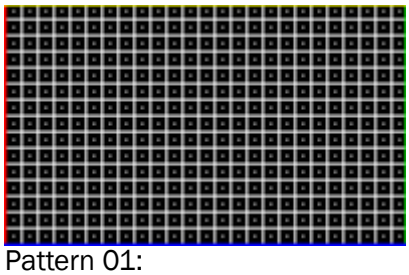
◆ Output Signal Characteristics, 480 x 272

PARAMETER		SYMBOL	VALUE	UNIT
HCLK FREQUENCY	NORMAL	FHCLK	1	FCLK
HCLK FREQUENCY	DUAL	1/2FHCLK	0.5	FCLK
HCLK PERIOD	NORMAL	THCLK	1	TCLK
HCLK PERIOD	DUAL	2THCLK	2	TCLK
DATA, REV DIO VALID TO HCLK RISING		TSU	4 (MIN.)	NS
HCLK RISING TO DATA, REV, DIO VALID		THD	4 (MIN.)	NS
POL PULSE WIDTH		TPOL	1	THP
POL VALID TO LD RISING		TPSU	0.5 THP + 12	THCLK
LD RISING TO POL VALID		TPHD	THP - TPSU	THCLK
STV PULSE WIDTH		TSTV	1	THP
STV VALID TO CKV RISING		TVSU	0.5	THP
CKV RISING TO STV VALID		TVHD	0.5	THP
DIO PULSE WIDTH		TDIOW	1	THCLK
LD PULSE WIDTH		TLDW	4	THCLK
OEV PULSE WIDTH		TOEV	50	THCLK
CKV PULSE WIDTH		TCKV	0.5	THP
TIME FROM LD TO CKV		TGS	1	THCLK
TIME FROM LD TO DIO		TLDO	THBK – 9	THCLK
TIME FROM THE LAST DATA TO LD		TED	9	THCLK

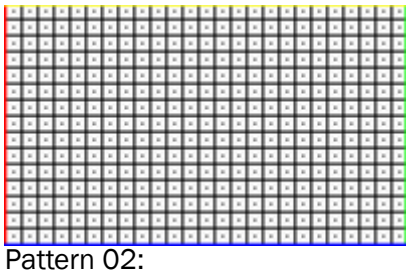
9. Built-in Patterns



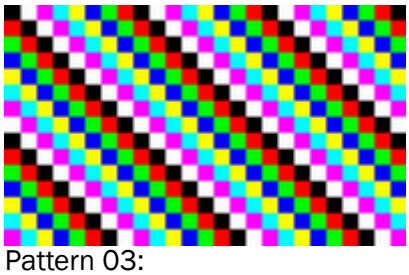
Pattern 00:
Black background with white cross line,
White line boundary./one pixel



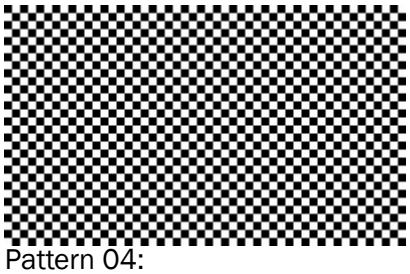
Pattern 01:
White cross hatch and dot
4 border lines
Left-red, right-green,up-blue,dn-yellow



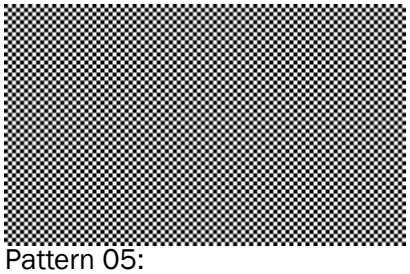
Pattern 02:
Black cross hatch and dot
4 border lines
Left-red, right-green,up-blue,dn-yellow



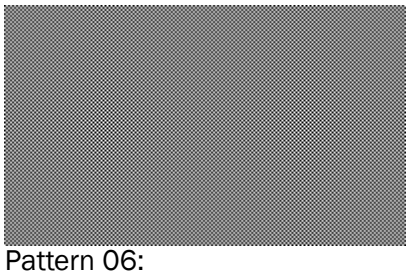
Pattern 03:
Diagonal color



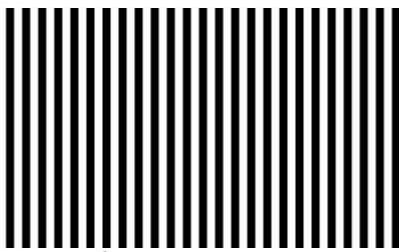
Pattern 04:
Black and white checkerboard
four pixels



Pattern 05:
Black and white checkerboard
two pixels



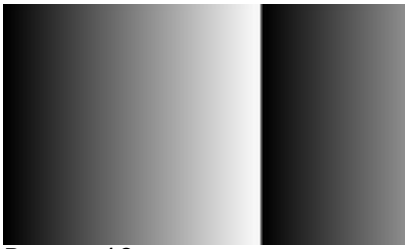
Pattern 06:
Black and white checkerboard
one pixel



Pattern 07:
Vertical black and white bar
Two pixels
.

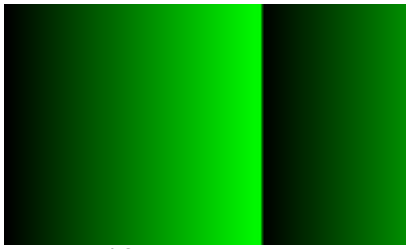
Pattern 08:
2 gray levels, dither off => 61,62
8 gray levels, dither on => 240 to 247

Pattern 09:
32 white gray levels
From 0 to 255

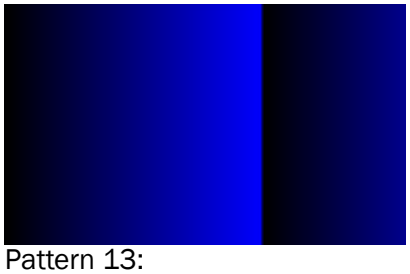


Pattern 10:
256 white grayscale / two pixels
From 0 to 255

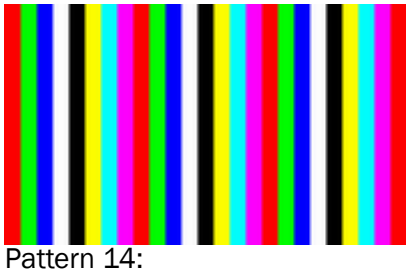
Pattern 11:
256 red grayscale / two pixels
From 0 to 255



Pattern 12:
256 green grayscale / two pixels
From 0 to 255



Pattern 13:
256 blue grayscale / two pixels
From 0 to 255

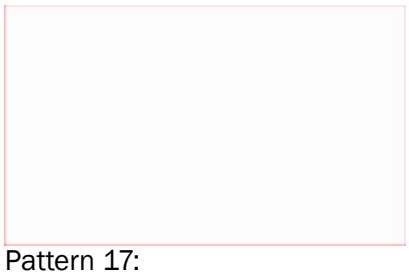


Pattern 14:
Vertical colors bar.

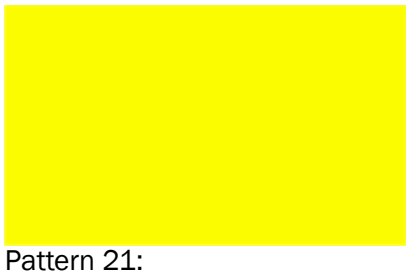
Pattern 15:
Horizontal colors bar.

Pattern 16:
Black with white line boundary.

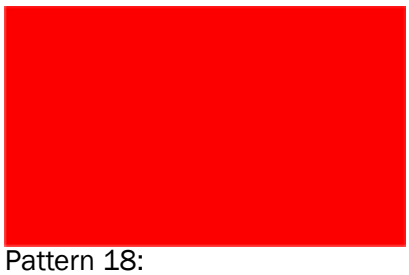
Pattern 20:
Blue with white line boundary.



Pattern 17:
White with red line boundary.

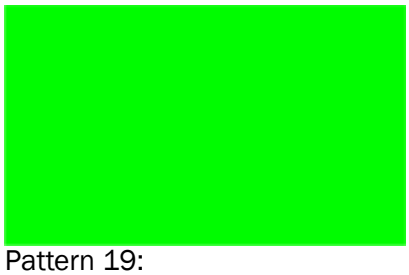


Pattern 21:
Yellow with white line boundary.

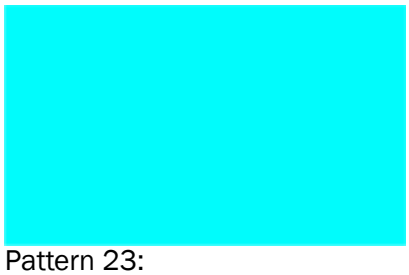


Pattern 18:
Red with white line boundary.

Pattern 22:
Magenta with white line boundary.



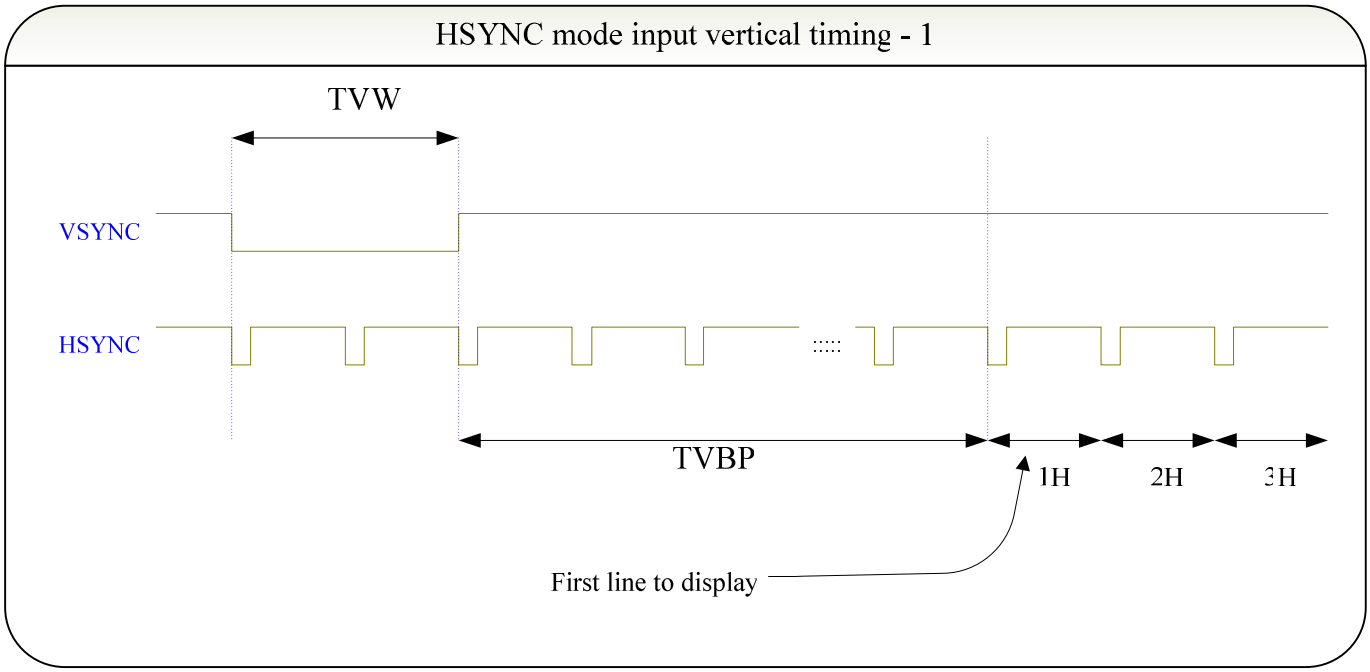
Pattern 19:
Green with white line boundary.



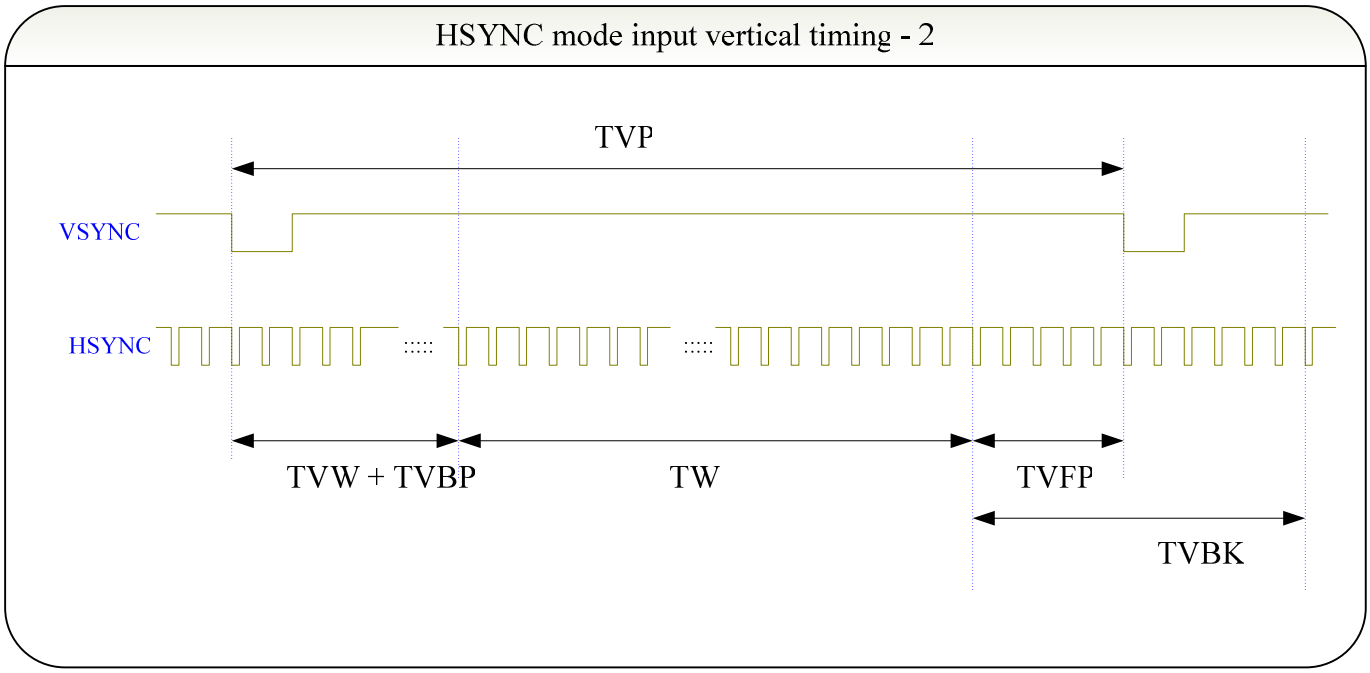
Pattern 23:
Cyan with white line boundary.

10. Waveforms

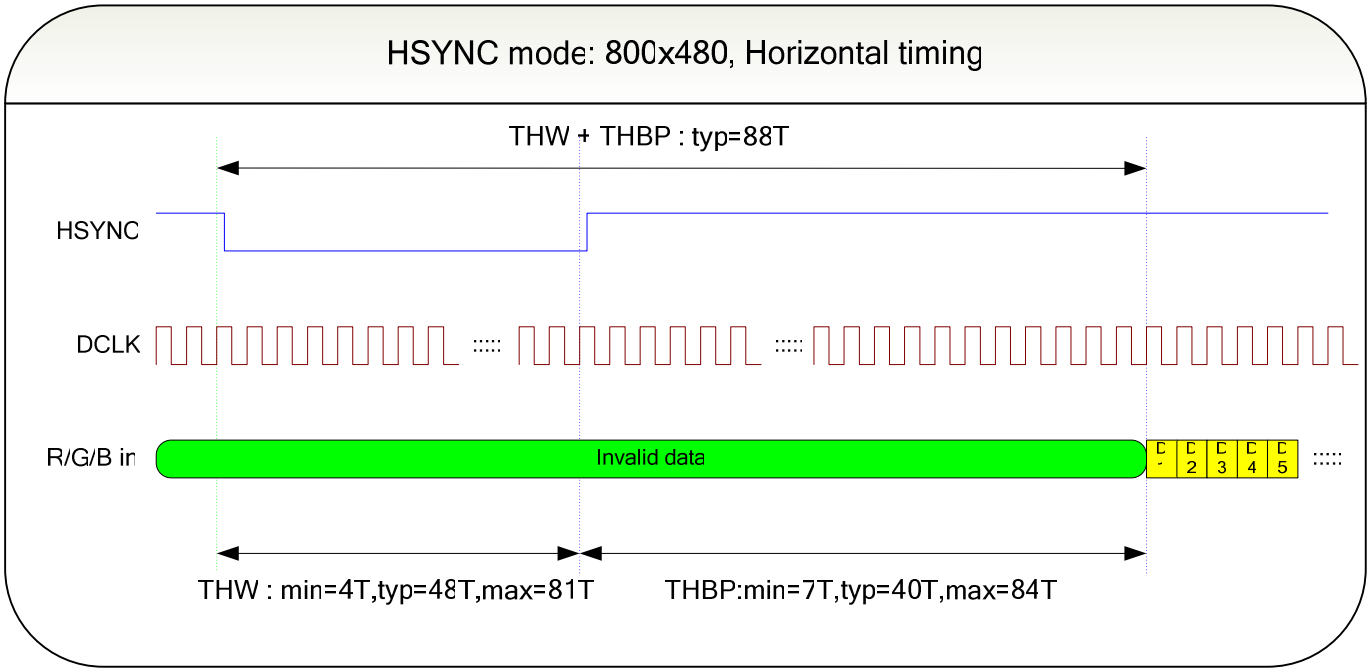
◆ Waveform 1: HSYNC mode input vertical timing - 1



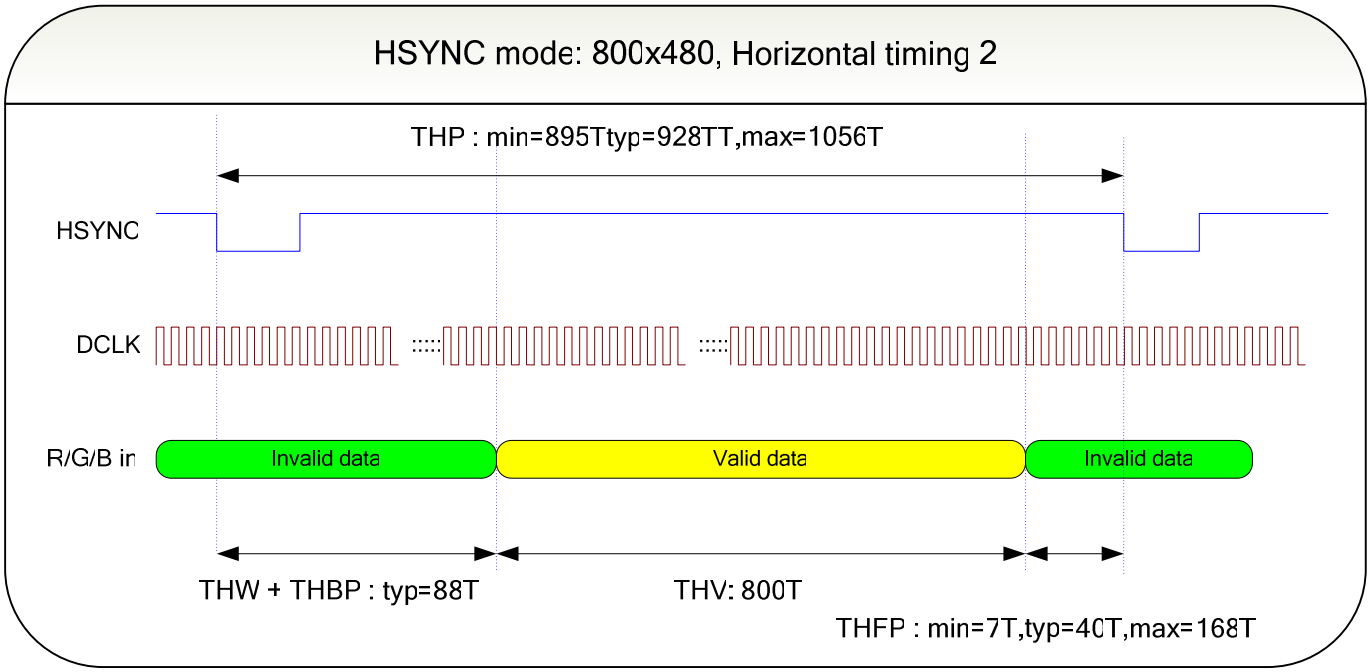
◆ Waveform 2: HSYNC mode input vertical timing - 2



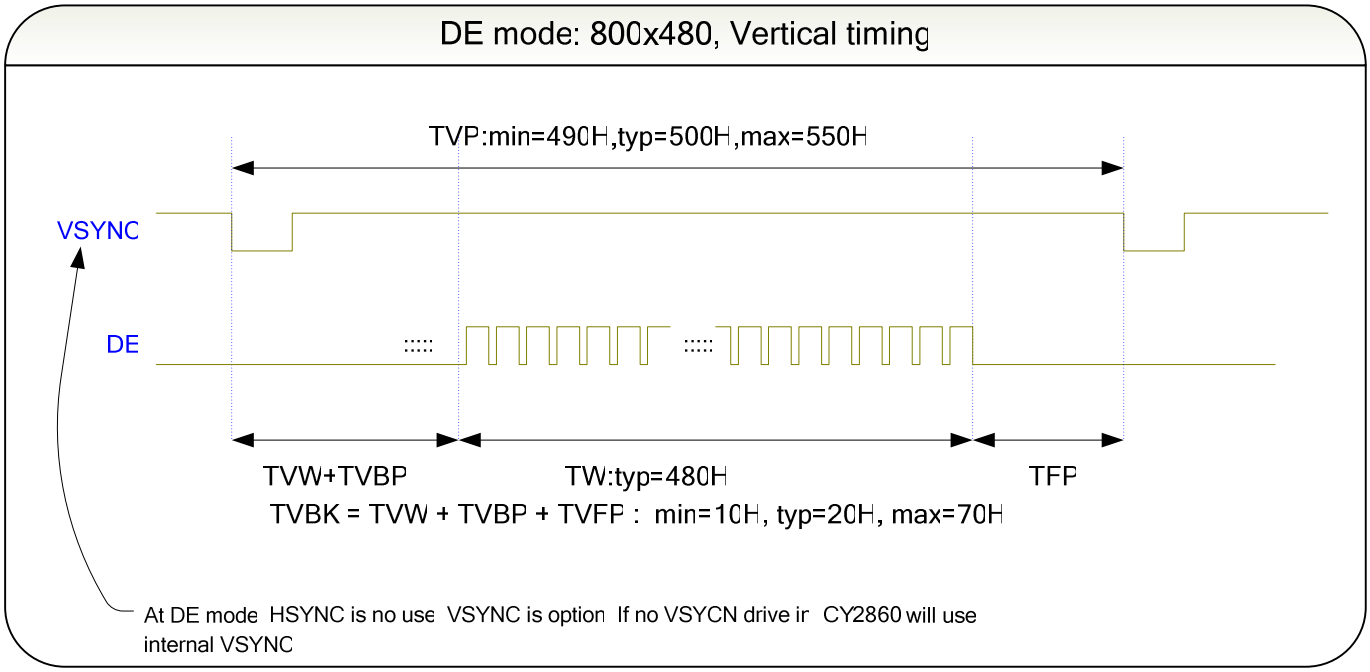
◆ Waveform 3 : HSYNC mode, 800x480, Horizontal timing 1



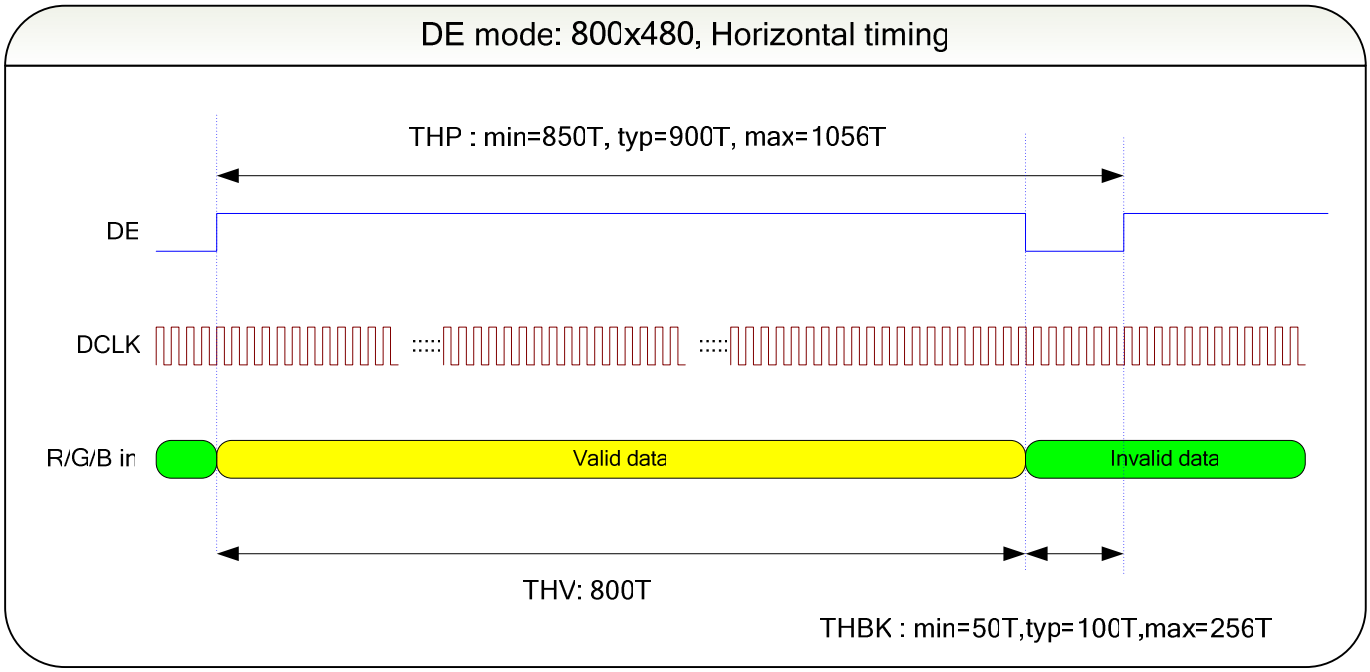
◆ Waveform 4 : HSYNC mode, 800x480, Horzontal timing 2



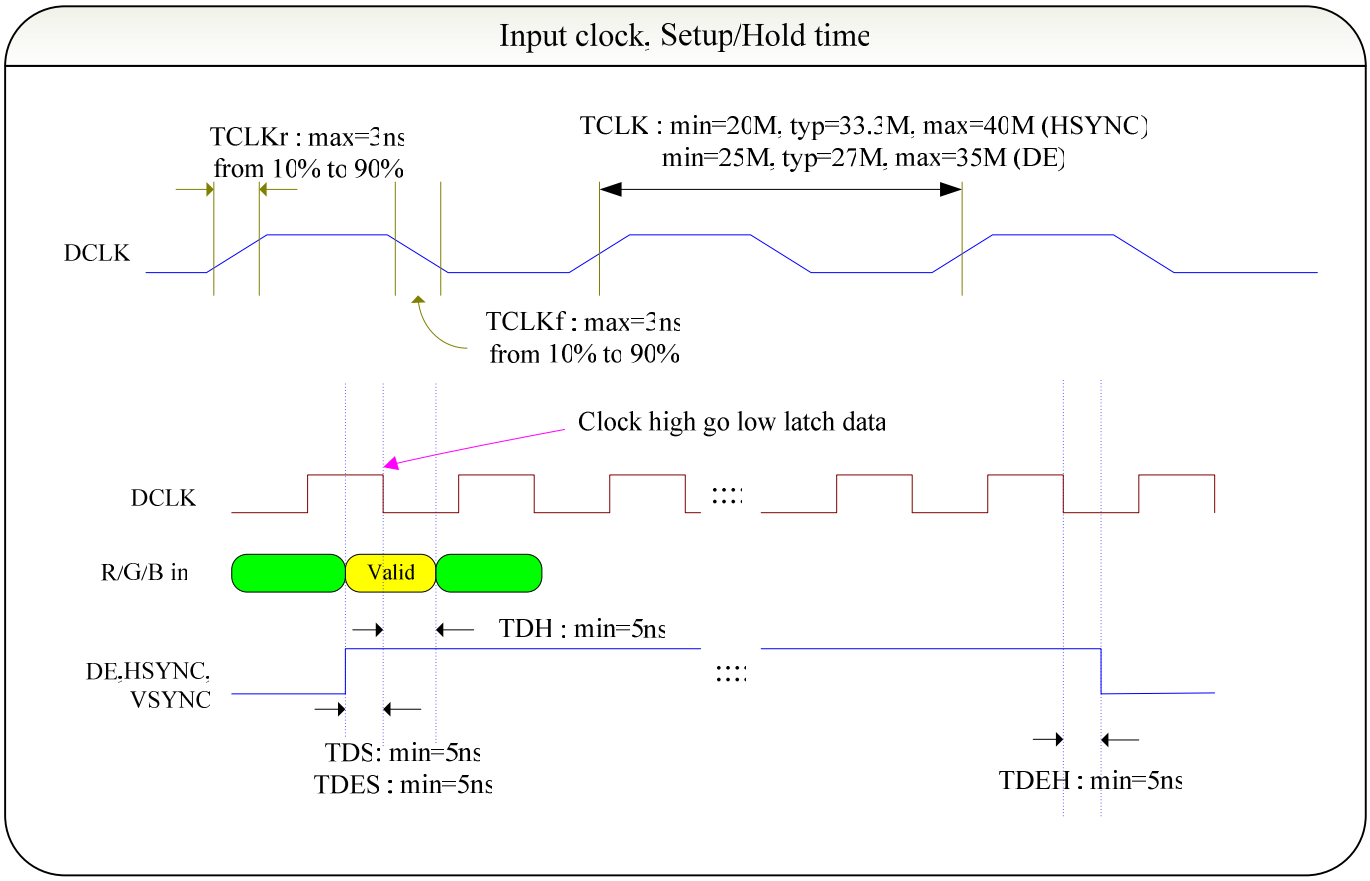
◆ Waveform 5 : DE mode, 800x480, Vertical timing



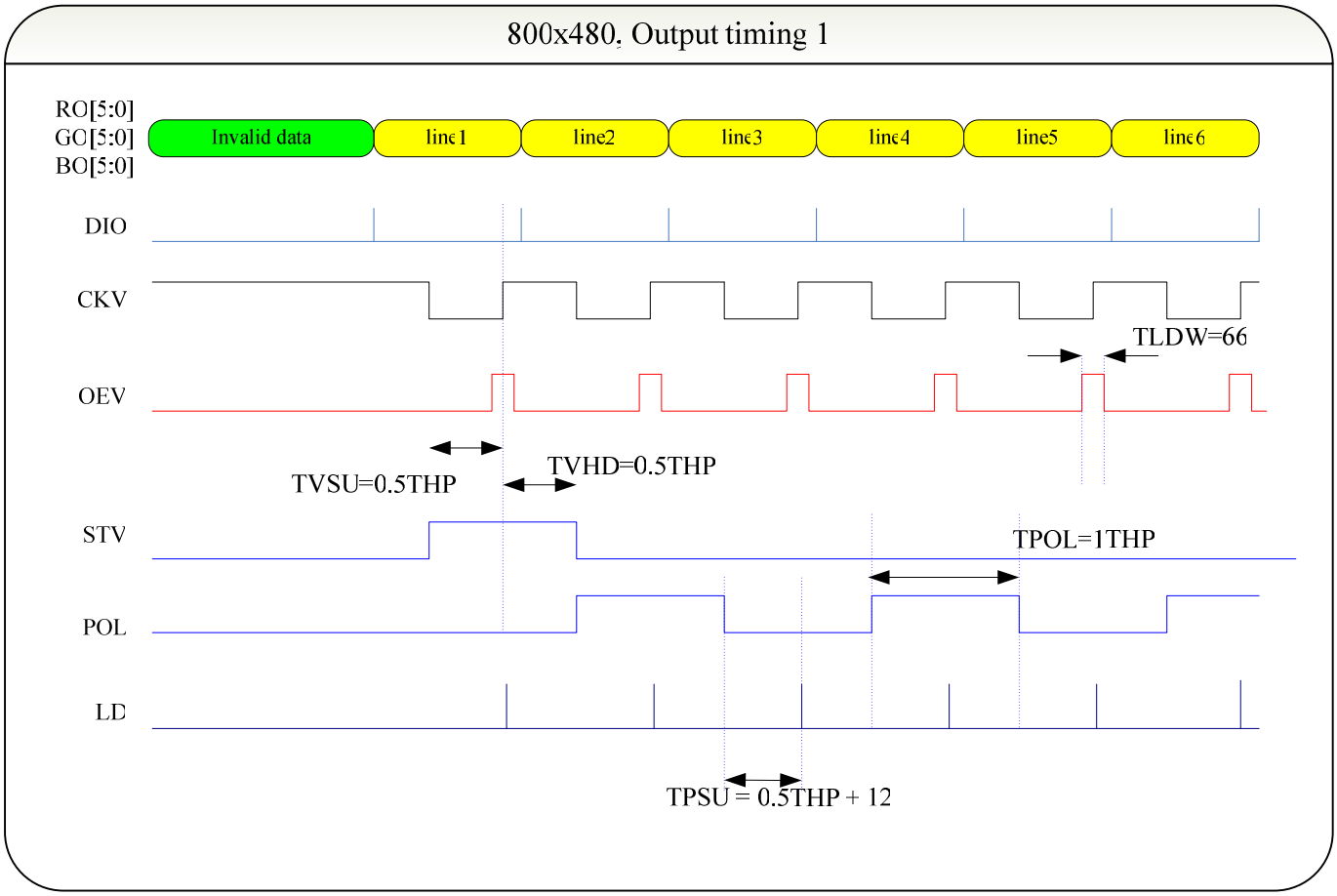
◆ Waveform 6 : DE mode, 800x480, Horizontal timing



◆ Waveform 7: input clock, setup/hold time

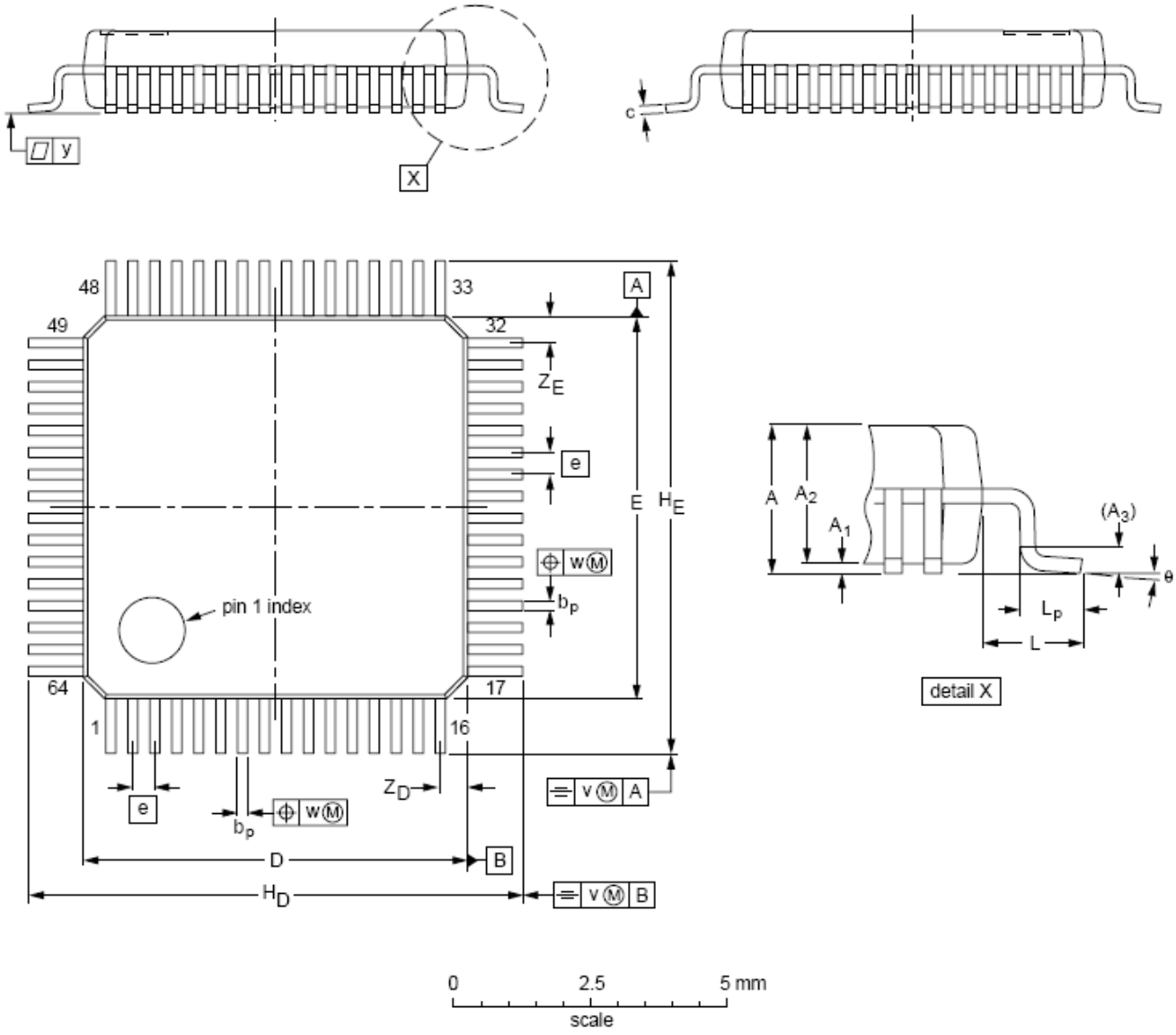


◆ Waveform 8 : 800 x 480, Output timing – 1



11. Package Information

CY2890-F02 : LQFP 64 pins (7x7x1.4mm)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	7.1 6.9	7.1 6.9	0.4	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.08	0.08	0.64 0.36	0.64 0.36	7° 0°