PRELIMINARY

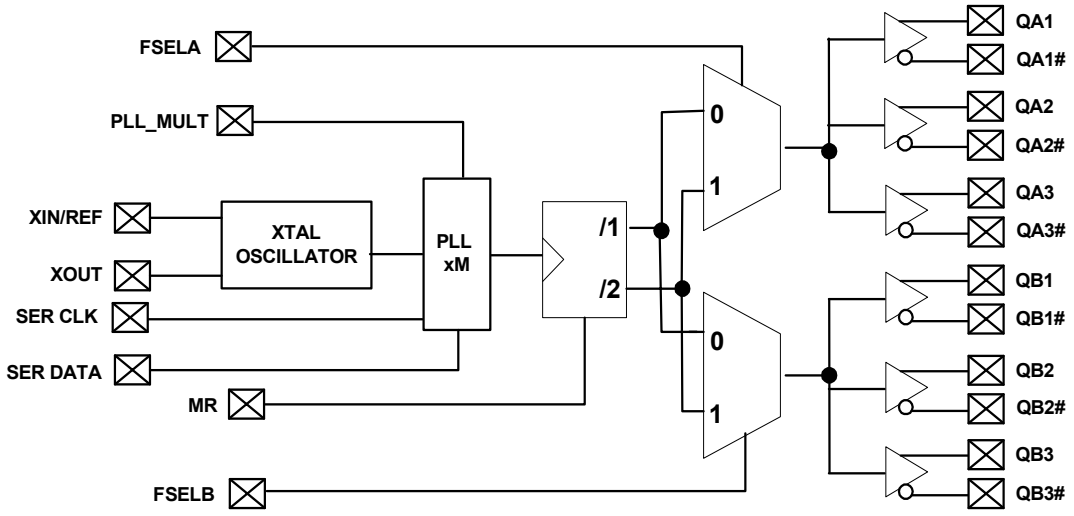
CY2XP306

High-frequency Programmable PECL Clock Generation Module

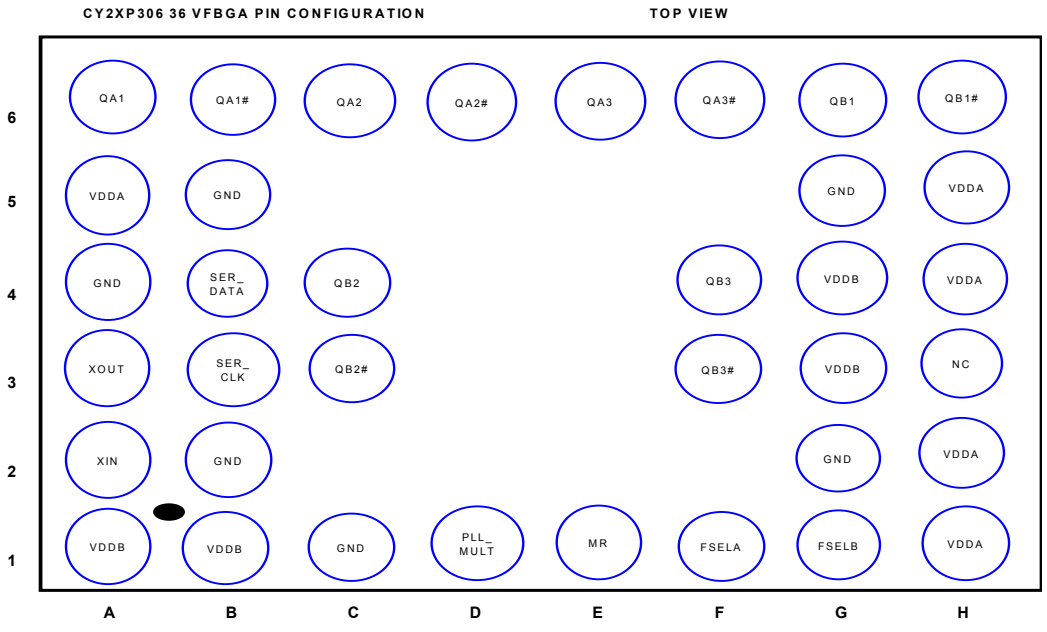
Features

- 60 ps typical Cycle-to-Cycle Jitter
- 30 ps typical Output-Output Skew
- Phase-locked loop (PLL) multiplier select
- LVTTL or XO Input; Six LVPECL Outputs
- Selectable Output Divider (/2)
- 1–133 MHz Input Frequency Range
- 62.5–500 MHz Output Frequency Range
- 36-pin VFBGA, 6 × 8 × 1 mm
- 3.3V operation
- Serially Configurable Multiply Ratios

Block Diagram



Pin Configuration (Top View)



Pin Definitions

Pin #	Pin Name	Pin Description
A2	XIN/REF	Reference Crystal Input or LVTTL
A3	XOUT	Reference Crystal Feedback
B2,B5,C1,G2,G5,A4	GND	Ground
A5,H1,H2,H4,H5	VDDA	3.3V Power Supply
A1,B1,G3,G4	VDDB	3.3V Power Supply
A6	QA1	LVPECL Clock Output
B6	QA1#	LVPECL Clock Output (Complement)
C6	QA2	LVPECL Clock Output
D6	QA2#	LVPECL Clock Output (Complement)
E6	QA3	LVPECL Clock Output
F6	QA3#	LVPECL Clock Output (Complement)
G6	QB1	LVPECL Clock Output
H6	QB1#	LVPECL Clock Output (Complement)
C4	QB2	LVPECL Clock Output
C3	QB2#	LVPECL Clock Output (Complement)
F4	QB3	LVPECL Clock Output
F3	QB3#	LVPECL Clock Output (Complement)
D1	PLL_MULT	PLL Multiplier Select Input, Internal pull-up resistor, see *Frequency Table*
E1	MR	LVPECL Reset; Internal Pull-Down, see *Function Table*
F1	FSELA	LVPECL Output Divider Select; Internal Pull-Down, see *Output Frequency Table*
G1	FSELB	LVPECL Output Divider Select; Internal Pull-Down, see *Output Frequency Table*
H3	NC	No Connect
B4	SER_DATA	Serial Interface Data
B3	SER_CLK	Serial Interface Clock

Table 1. Frequency Table

PLL_Mult	M (PLL Multiplier)	Example Input Frequency	Example *PLL* Output Frequency
0	x16	19.44 MHz	311.04 MHz
		19.53 MHz	312.5 MHz
1	x8	19.44 MHz	155.52 MHz
		19.53 MHz	156.25 MHz
		38.88 MHz	311.04 MHz

Table 2. Output Frequency Table

Control Pin	0	1
FSELA	QAx = PLL Output Frequency	QAx = PLL Output Frequency/2
FSELB	QBx = PLL Output Frequency	QBx = PLL Output Frequency/2

Table 3. Function Table

Control Pin	0	1
MR (Asynchronous)	Active	Reset (QX = Low, QX# = High)

Two-Wire Serial Interface

Introduction

The CY2XP306 has a two-wire serial interface designed for data transfer operations, and is used for programming the P and Q values for frequency generation. S_{clk} is the serial clock line controlled by the master device. S_{data} is a serial bidirectional data line. The CY2XP306 is a slave device and can either read or write information on the dataline upon request from the master device.

Figure 1 shows the basic bus connections between master and slave device. The buses are shared by a number of devices and are pulled high by a pull-up resistor.

Serial Interface Specifications

Figure 2 shows the basic transmission specification. To begin and end a transmission, the master device generates a start signal (S) and a stop signal (P). Start (S) is defined as switching the S_{data} from HIGH to LOW while the S_{clk} is at HIGH. Similarly, stop (P) is defined as switching the S_{data} from LOW to HIGH while holding the S_{clk} HIGH. Between these two signals, data on S_{data} is synchronous with the clock on the S_{clk}.

Data is allowed to change only at LOW period of clock, and must be stable at the HIGH period of clock. To acknowledge, drive the S_{data} LOW before the S_{clk} rising edge and hold it LOW until the S_{clk} falling edge.

Serial Interface Format

Each slave carries an address. The data transfer is initiated by a start signal (S). Each transfer segment is one byte in length. The slave address and the read/write bit are first sent from the master device after the start signal. The addressed slave device must acknowledge (Ack) the master device. Depending on the Read/Write bit, the master device will either write data into (logic 0) or read data (logic 1) from the slave device. Each time a byte of data is successfully transferred, the receiving device must acknowledge. At the end of the transfer, the master device will generate a stop signal (P).

Serial Interface Transfer Format

Figure 2 shows the serial interface transfer format used with the CY2XP306. Two dummy bytes must be transferred before the first data byte. The CY2XP306 has only three bytes of latches to store information, and the third byte of data is reserved. Extra data will be ignored.

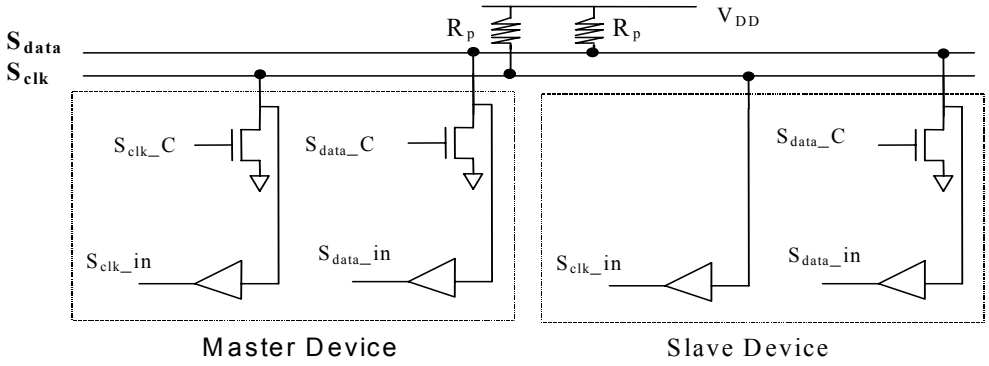


Figure 1. Device Connections

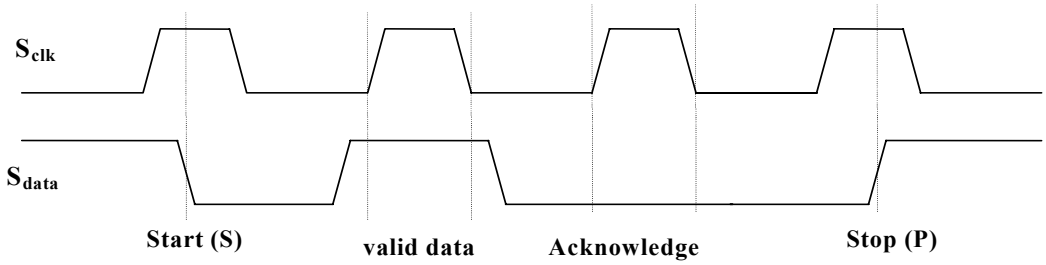


Figure 2. Serial Interface Specifications

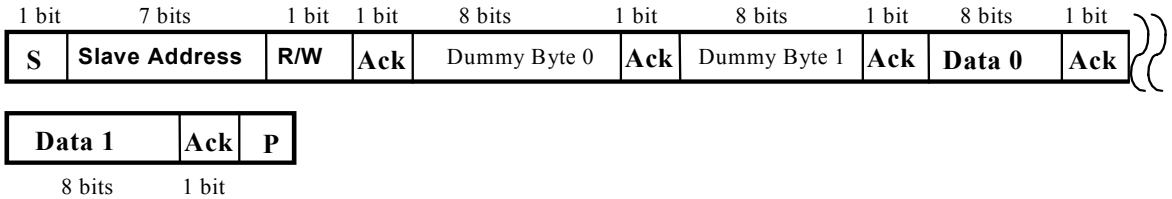


Figure 3. CY2XP306 Transfer Format

Serial Interface Address for the CY2XP306

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	0	1	0

Serial Interface Programming for the CY2XP306

	b7	b6	b5	b4	b3	b2	b1	b0
Data0	QCNTBYP	SELPQ	Q<5>	Q<4>	Q<3>	Q<2>	Q<1>	Q<0>
Data1	P<7>	P<6>	P<5>	P<4>	P<3>	P<2>	P<1>	P<0>
Data2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

To program the CY2XP306 using the two-wire serial interface, set the SELPQ bit HIGH. The default setting of this bit is LOW. The P and Q values are determined by the following formulas:

$P_{final} = (P_{7..0} + 3) * 2$

$Q_{final} = Q_{5..0} + 2.$

If the QCNTBYP bit is set HIGH, then Q_{final} defaults to a value of 1. The default setting of this bit is LOW.

If the SELPQ bit is set LOW, the PLL multipliers will be set using the values in the Select Function Table.

CyberClocks™ has been developed to generate P and Q values for stable PLL operation. This software is downloadable from www.cypress.com.

PLL Frequency = Reference x P/Q = Output

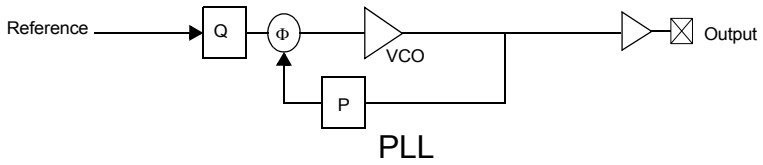


Figure 4. PLL Block Diagram

Functional Specifications

Crystal Input

The CY2XP306 receives its reference from an external reference input or external crystal. Pin XIN is the reference crystal input, and pin XOUT is the reference crystal feedback. The oscillator circuit requires external capacitors. Please refer to the application note entitled *Crystal Oscillator Topics* for details.

Select Input

There are four select input pins, the PLL_MULT, MR, FSELA and FSELB. PLL_MULT pin selects the frequency multiplier in the PLL. The PLL_MULT pin has an internal pull-up resistor. The multiplier selection is given on *Table 1*, *Frequency Table*.

The MR pin is a reset control pin. It has an internal pull-down resistor. Please see *Table 3* for detailed function.

The FSELA and FSELB pins are output dividers select pins, see *Table 2* for *Output Frequency Table*.

All of these four select pins are standard LVCMOS inputs.

State Transition Characteristics

Specifies the maximum settling time of the QA and QB bank outputs from device power-up. For V_{DD}, any sequences are allowed to power-up and power-down the CY2XP306.

Table 4. State Transition Characteristics Table

From	To	Transition Latency	Description
V_{DD} On	QA/QB Outputs Normal	3 ms	Time from V_{DD} is applied and settled to outputs settled.

Table 5. Operating Ambient Temperature

Parameter	Description	Min.	Max.	Unit
T_A	Commercial Temperature	0	70	°C
	Industrial Temperature	–40	85	°C

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage	Non-functional	–0.3	4.6	V
V_{DD}	Operating Voltage	Functional	3.135	3.465	V
VTT	Output Termination Voltage	Relative to V_{DD}[1]	V_{DD} – 2		V
V_{IN}	Input Voltage	Relative to V_{DD}[1]	–0.3	V_{DD} + 0.3	V
V_{OUT}	Output Voltage	Relative to V_{DD}[1]	–0.3	V_{DD} + 0.3	V
LU_I	Latch Up Immunity	Functional	100		mA
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Non-functional	–	150	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	11.48		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	85.8		°C/W
ESD_h	ESD Protection (Human Body Model)		2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.

Crystal Requirements

Requirements to use parallel mode fundamental xtal. External capacitors are required in the crystal oscillator circuit. Please refer to the application note entitled *Crystal Oscillator Topics* for details.

Crystal Requirements

Parameter	Description	Min.	Max.	Unit
X_F	Frequency	10	31.25	MHz

DC Specifications (V_{DD} = 3.3 V ± 5%, Commercial and Industrial Temperature)

Parameter	Description		Min.	Max.	Unit
V_{DD}	Supply voltage		3.135	3.465	V
V_{IL1}	Input signal low voltage at pin PLL_MULT		–	0.35	V_{DD}
V_{IH1}	Input signal high voltage at pin PLL_MULT		0.65	–	V_{DD}
V_{IL2}	Input signal low voltage at pins REF		–	0.8	V
V_{IH2}	Input signal high voltage at pins REF		2.0	–	V
V_{IL3}	LVPECL input signal low voltage at pins MR, FSELA, FSELB		V_{DD} – 1.945	V_{DD} – 1.625[3]	V
V_{IH3}	LVPECL input signal high voltage at pins MR, FSELA, FSELB		V_{DD} – 1.165[3]	V_{DD} – 0.88	V
R_{PUP}	Internal pull-up resistance		10	100	kΩ
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)		0.05	500	ms
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current		–	150	mA
V_{OL}	LVPECL Output Low Voltage V_{DD} = 3.3V ± 5%	I_{OL} = –5 mA[2]	V_{DD} – 1.995	V_{DD} – 1.5	V
V_{OH}	LVPECL Output High Voltage	I_{OH} = –30 mA[2]	V_{DD} – 1.25	V_{DD} – 0.7	V

Note:
1. Where V_{DD} is 3.3V±5%
2. Equivalent to a termination of 50Ω to V_{TT}.
3. V_{IL3} will operate down to GND; V_{IH3} will operate up to V_{DD}.

AC Specifications (V_{DD} = 3.3 V ± 5%, Commercial and Industrial Temperature)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
f_{IN}	Input frequency	Limited by Max PLL Frequency	1	–	133	MHz
f_{XTALIN}	Crystal Input frequency		10	–	31.25	MHz
$C_{IN,CMOS}$	Input capacitance at PLL_MULT pin[4]		–	–	10	pF
f_O	Output Frequency		125	–	500	MHz
$Vo_{(P-P)}$	Differential output voltage (peak-to-peak)		0.5	–	–	V
V_{CMRO}	Output Common Voltage Range	Typical	V_{DD} – 1.425			V
$tsk_{(O)}$	Output-to-output skew	311 MHz 50% duty cycle Standard load Differential Operation	–	30	TBD	ps
$tsk_{(PP)}$	Part-to-part output skew	311 MHz 50% duty cycle Standard load Differential Operation	–	–	150	ps
T_R,T_F	Output Rise / Fall time	311 MHz 50% duty cycle Differential (20% to 80%)	–	–	0.3	ns
DC	Long-term average output duty cycle		45	–	55	%
J_{C2C}	Cycle-to-cycle Jitter (Peak)	peak; 311 MHz; Jitter Defined by JESD65B	–	60	TBD	ps

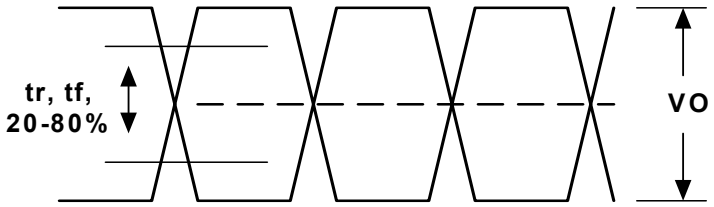


Figure 5. LVPECL Output

Notes:
4. Capacitance measured at freq. = 1 MHz, DC Bias = 0.9V, and VAC < 100 mV.

Test Configurations

Standard test load using a differential pulse generator and differential measurement instrument.

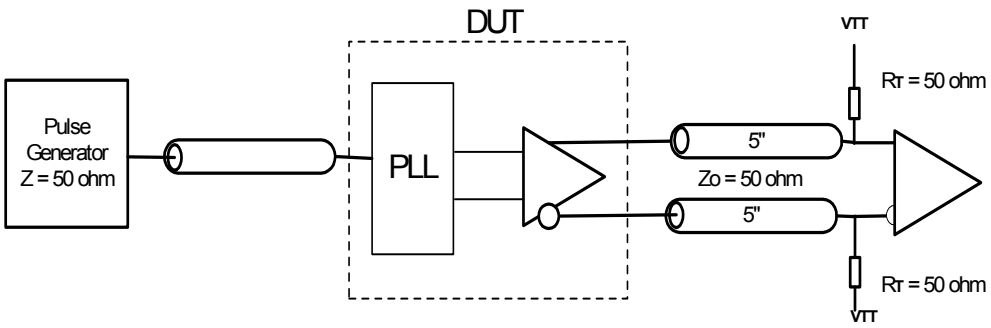


Figure 6. CY2XP306 AC Test Reference. One output LVPECL pair is shown for clarity.

Applications Information

Termination Example

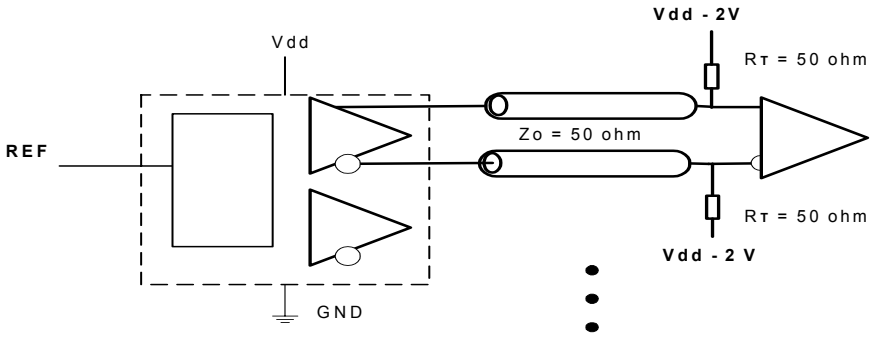


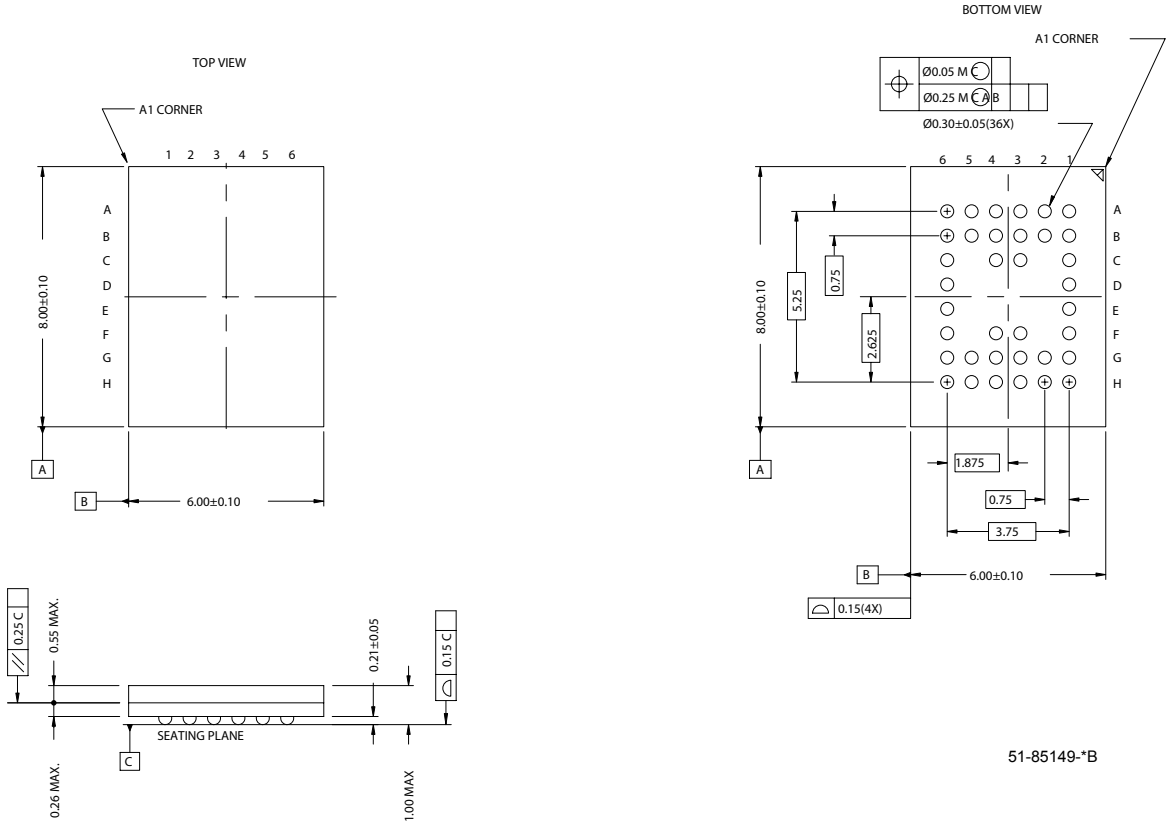
Figure 7. Standard LVPECL–PECL Output Termination. One output is shown for clarity.

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
Lead Free			
CY2XP306BVXI	36-lead VFBGA	Industrial Temp	3.3V
CY2XP306BVXIT	36-lead VFBGA - Tape and Reel	Industrial Temp	3.3V

Package Drawing and Dimensions

36-Lead VFBGA (6 x 8 x 1 mm) BV36A



Document History Page

Document Title: CY2XP306 High-frequency Programmable PECL Clock Generation Module Document Number: 38-07725				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	312633	See ECN	RGL	New Data Sheet
*A	349137	See ECN	RGL	Data sheet re-write