1-Mbit (64 K × 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with CE, and OE features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) Type II package

Functional Description

The CY62126ESL is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (CE HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH) or during a write operation (CE LOW and WE LOW).

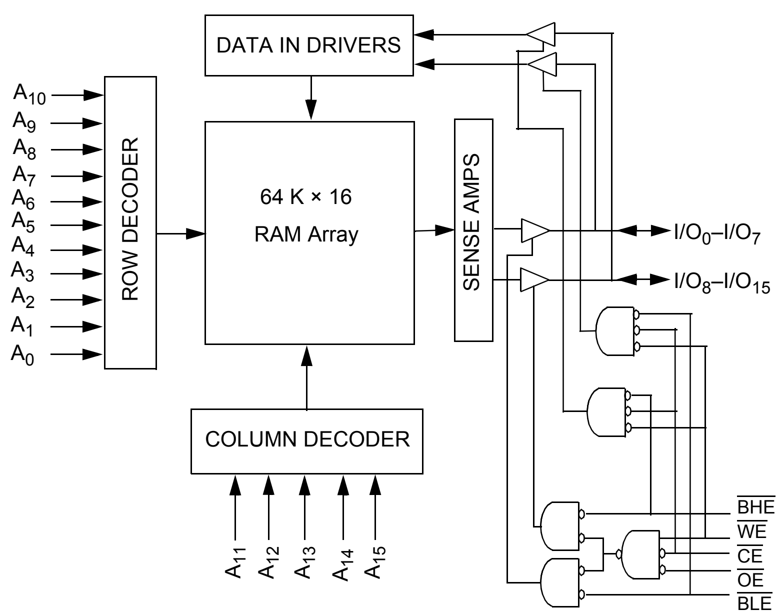
To write to the device, take Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

To read from the device, take Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

The CY62126ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related resources, click here.

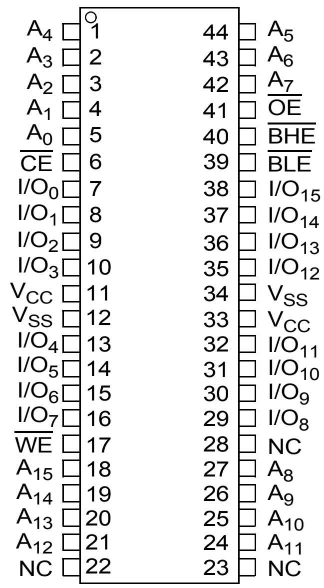
Logic Block Diagram



Contents

Pin Configuration

44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	Range	V_{CC} Range (V) [2]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1MHz		f = f_{max}			
				Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62126ESL	Industrial	2.2 V–3.6 V and 4.5 V–5.5 V	45	1.3	2	11	16	1	4

Notes
1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... 55 °C to +125 °C

Supply voltage to ground potential [4, 5] ....–0.5 V to 6.0 V

DC voltage applied to outputs in High Z State [4, 5] ....–0.5 V to 6.0 V

DC input voltage [4, 5] ....–0.5 V to 6.0 V

Output current into outputs (low) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch up current .... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62126ESL	Industrial	–40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [7]	Max	
V_{OH}	Output high voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –0.1 mA	–	–	3.4 [8]	
V_{OL}	Output low voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input high voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2	–	V_{CC} + 0.5	
V_{IL}	Input low voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	
		$4.5 \le V_{CC} \le 5.5$		–0.5	–	0.8	
I_{IX}	Input leakage current	$GND \le V_{IN} \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$, I_{OUT} = 0 mA, CMOS levels	–	11	16	mA
		f = 1 MHz		–	1.3	2.0	
I_{SB1} [9]	Automatic CE power down current – CMOS Inputs	$\overline{CE} \ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, $f = f_{max}$ (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	1	4	µA
I_{SB2} [9]	Automatic CE power down current – CMOS inputs	$\overline{CE} \ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		–	1	4	µA

Notes
4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
8. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
9. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

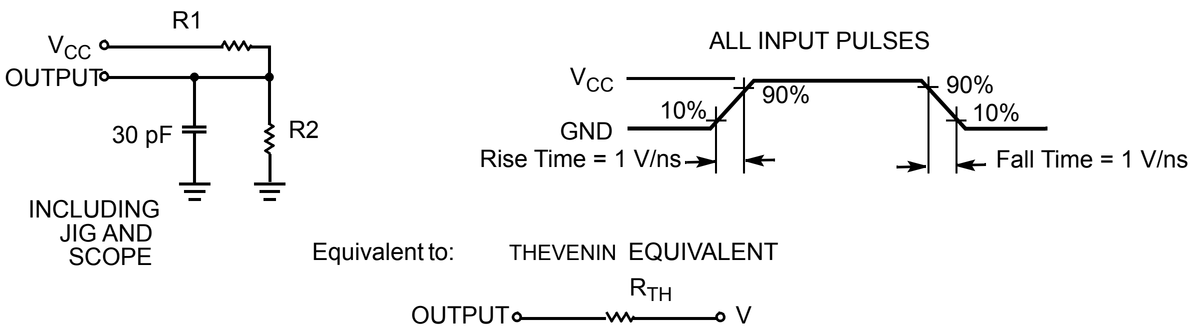
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	28.2	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.4	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	5.0 V	Unit
R1	16600	1103	1800	Ω
R2	15400	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.2	1.75	1.77	V

Note
10. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [12]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	$V_{CC} = 1.5$ V	–	–	3	µA
t_{CDR} [13]	Chip deselect to data retention time			0	–	–	ns
t_R [14]	Operation recovery time			45	–	–	ns

Data Retention Waveform

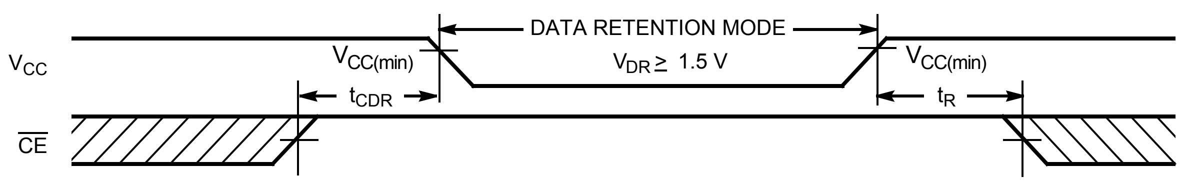


Figure 2. Data Retention Waveform

Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
12. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [15]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power up	–	45	ns
t_{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z [16]	5	–	ns
t_{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z [16, 17]	–	18	ns
Write Cycle [18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address Hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BHE}$ / $\overline{BLE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [16]	10	–	ns

Notes

15. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 1 on page 5.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [19, 20]

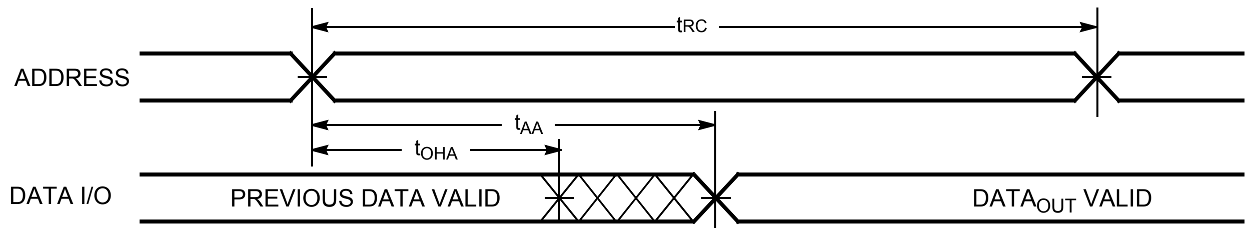
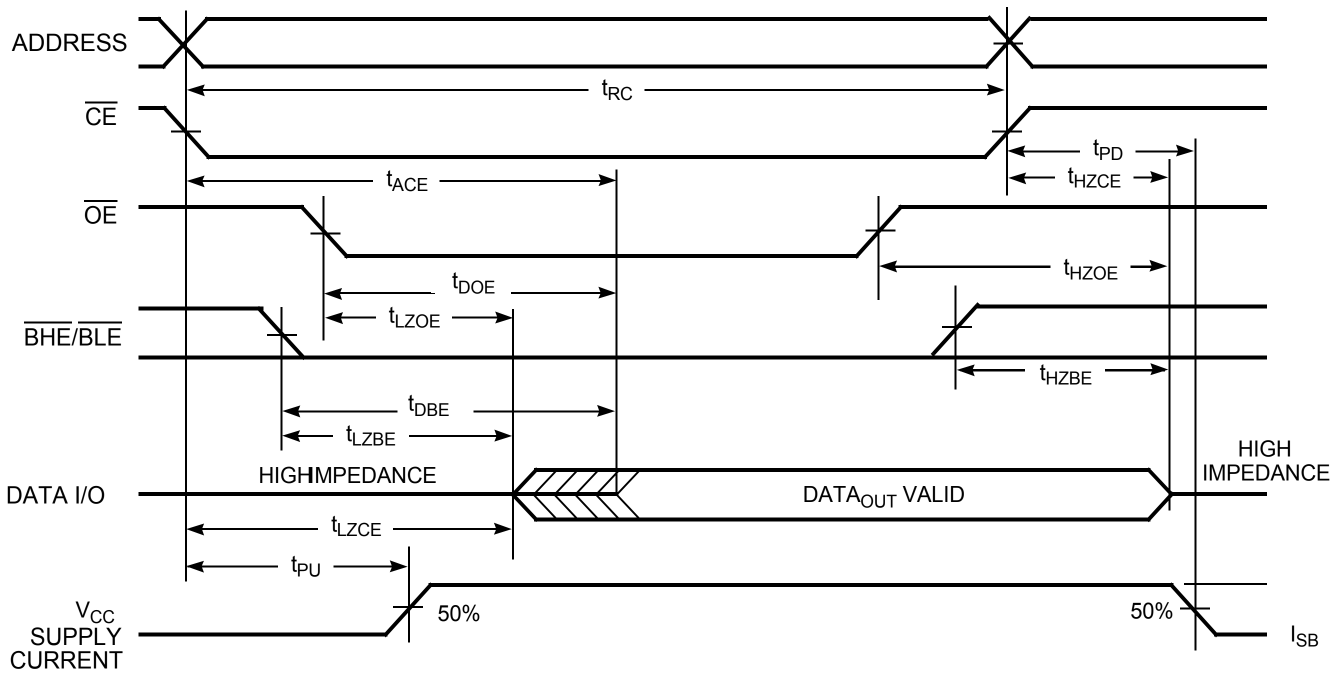


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [20, 21]



Notes

19. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
20. $\overline{WE}$ is high for read cycles.
21. Address valid before or similar to $\overline{CE}$ transition low.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH during Write) [22, 23]

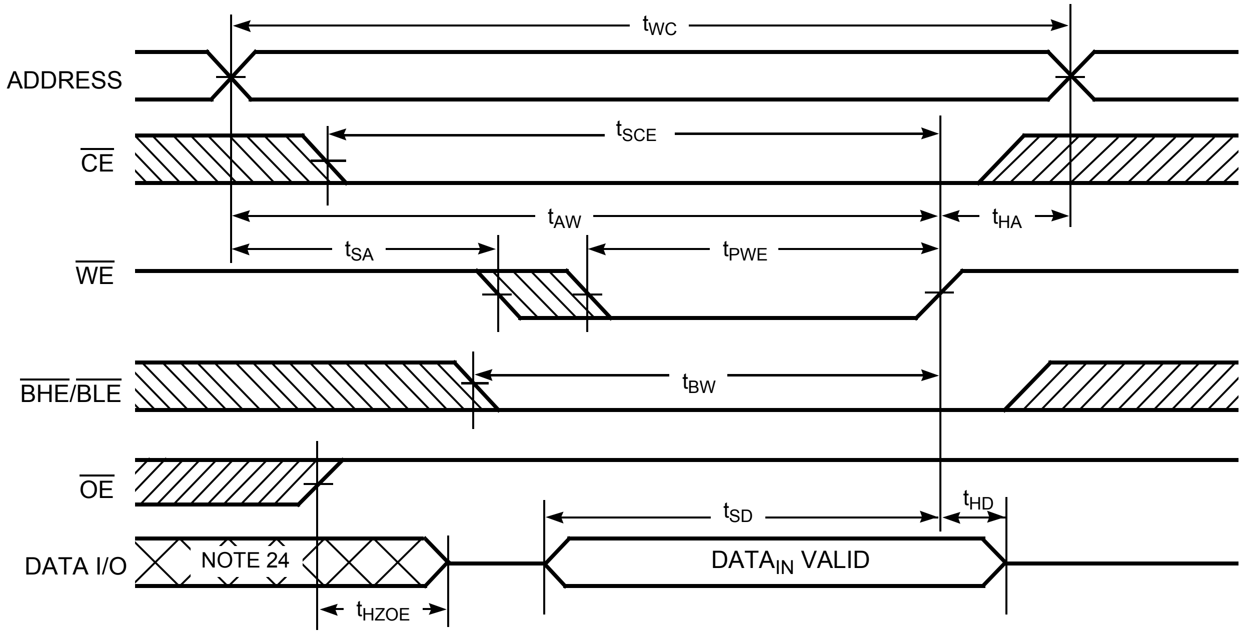
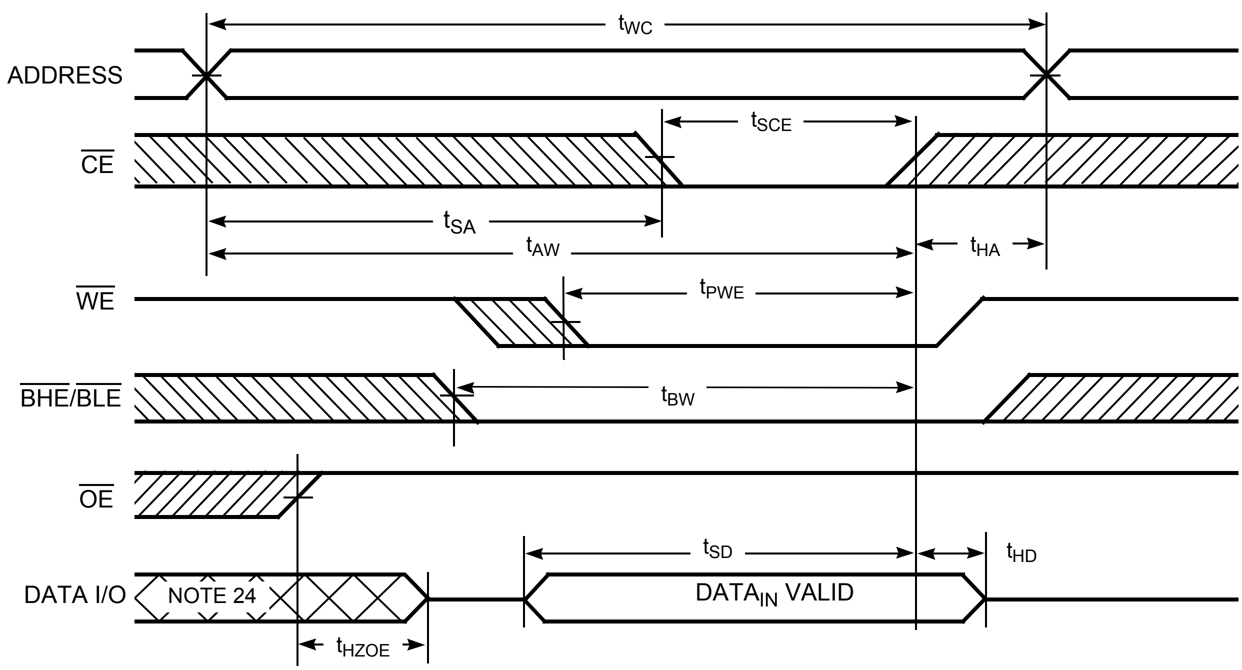


Figure 6. Write Cycle No. 2 ($\overline{CE}$ Controlled) [22, 23]



Notes

22. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
23. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 (WE Controlled, OE LOW) [25]

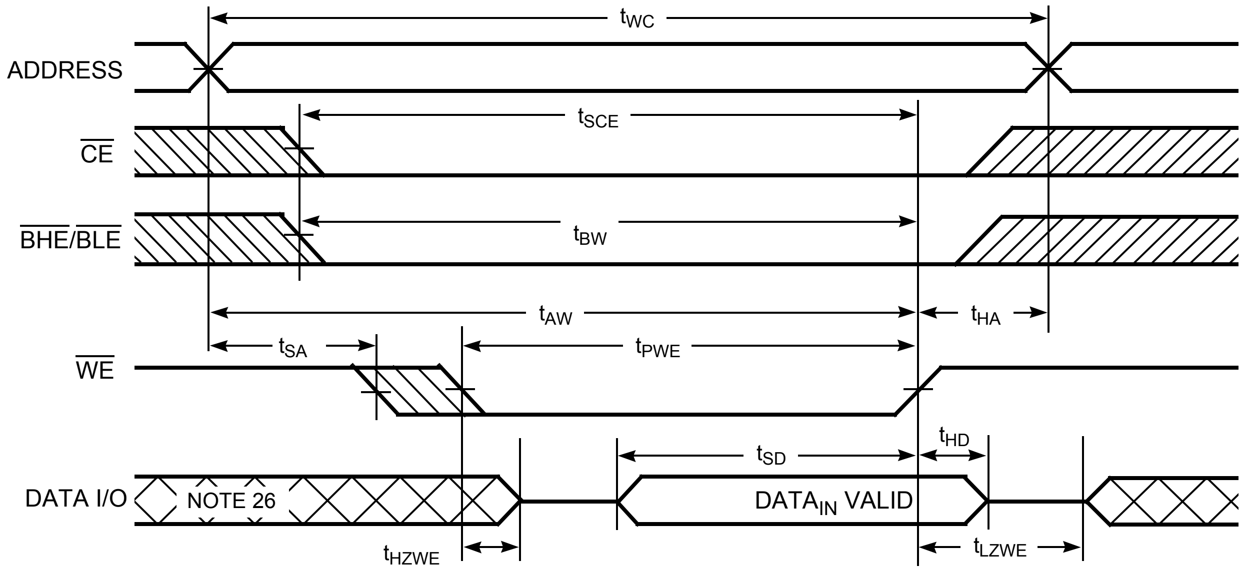
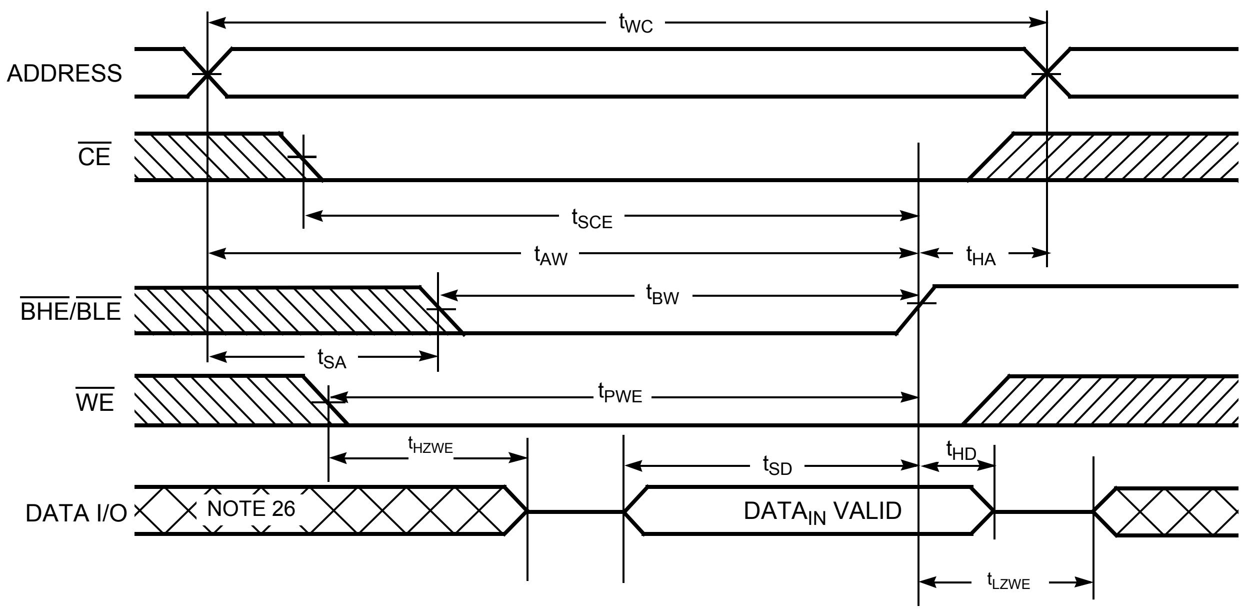


Figure 8. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [25]



Notes

25. If CE goes high simultaneously with WE high, the output remains in high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [27]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect or power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Note

27. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62126ESL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

Contact your local Cypress sales representative for availability of these parts.

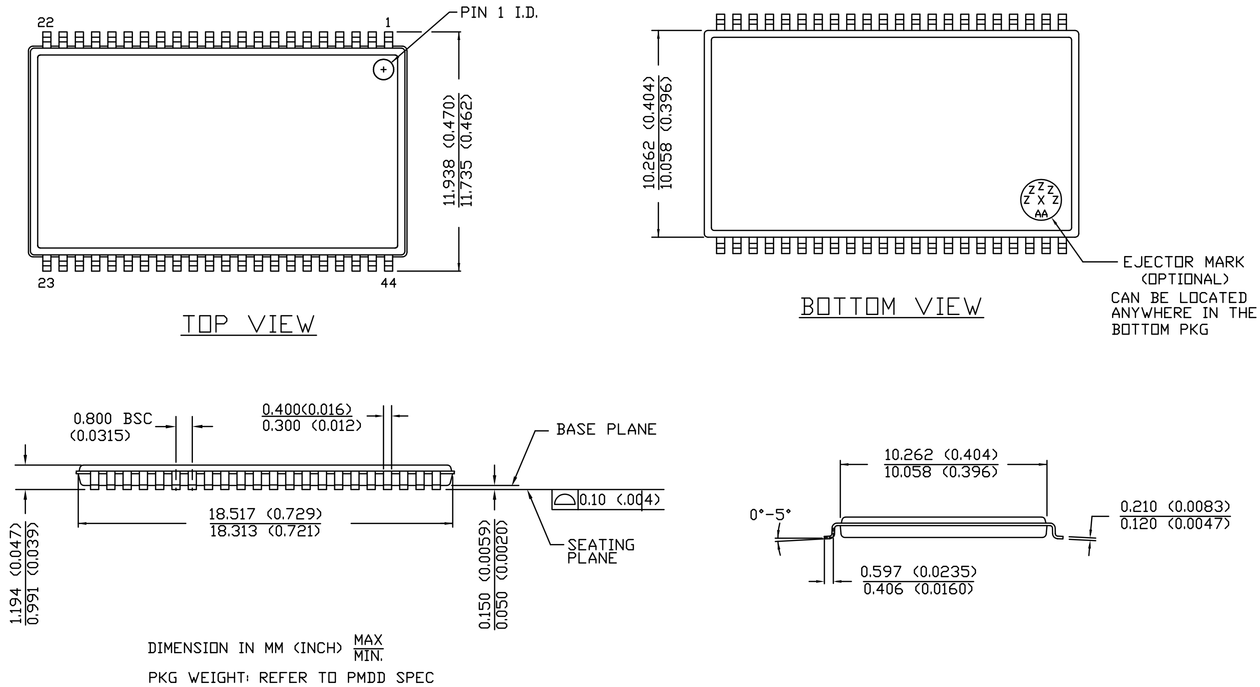
Ordering Code Definitions

CY 621 2 6 E SL - 45 ZS X I

- I: Temperature Grade: I = Industrial
- X: Pb-free
- ZS: Package Type: ZS = 44-pin TSOP Type II
- 45: Speed Grade: 45 ns
- SL: SL = Wide Voltage Range (3 V and 5 V)
- E: Process Technology: E = 90 nm Technology
- 6: Bus width: 6 = × 16
- 2: Density: 2 = 1-Mbit
- 621: Family Code: 621 = MoBL SRAM family
- CY: Company ID: CY = Cypress

Package Diagram

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Revision	ECN	Submission Date	Orig. of Change	Description of Change
Document Title: CY62126ESL MoBL®, 1-Mbit (64 K × 16) Static RAM **Document Number: 001-45076**				
**	2610988	11/21/08	VKN / PYRS	New data sheet.
*A	2718906	06/15/2009	VKN	Post to external web.
*B	2944332	06/04/2010	VKN	Added Contents Updated Electrical Characteristics (Added Note 9 and referred the same note in I_{SB2} parameter). Updated Truth Table (Added Note 27 and referred the same note in $\overline{CE}$ column). Updated Package Diagram. Updated links in Sales, Solutions, and Legal Information.
*C	3113720	12/17/2010	PRAS	Added Ordering Code Definitions.
*D	3292276	06/24/2011	RAME	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated Data Retention Characteristics (Changed the minimum value of t_R parameter). Updated to new template.
*E	3503697	01/20/2012	TAVA	Updated Electrical Characteristics (Replaced V_I with V_{IN} in Test Conditions of I_{IX} parameter). Updated Switching Waveforms. Updated Package Diagram.
*F	4013949	06/04/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition "$4.5 \leq V_{CC} \leq 5.5$, $I_{OH} = –0.1$ mA" for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 8 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition "$4.5 \leq V_{CC} \leq 5.5$, $I_{OH} = –0.1$ mA". Updated Package Diagram: spec 51-85087 – Changed revision from *D to *E.
*G	4241229	01/09/2014	VINI	Updated to new template. Completing Sunset Review.
*H	4576448	11/21/2014	VINI	Updated Functional Description: Added "For a complete list of related resources, click here." at the end.
*I	4592990	12/10/2014	VINI	Updated Maximum Ratings: Referred Notes 4, 5 in "Supply voltage to ground potential".
*J	6013882	01/04/2018	AESATP12	Updated logo and copyright.

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