**CY62127DV30 MoBL®**

# 1-Mbit (64K × 16) Static RAM

## Features

- Temperature ranges
  - ❐ Industrial: –40 °C to 85 °C
- Very high speed: 55 ns
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62127BV
- Ultra-low active power
  - ❐ Typical active current: 0.85 mA at f = 1 MHz
  - ❐ Typical active current: 5 mA at f = $f_{MAX}$
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Available in Pb-free 48-ball FBGA and 44-pin TSOP Type II packages

## Functional Description

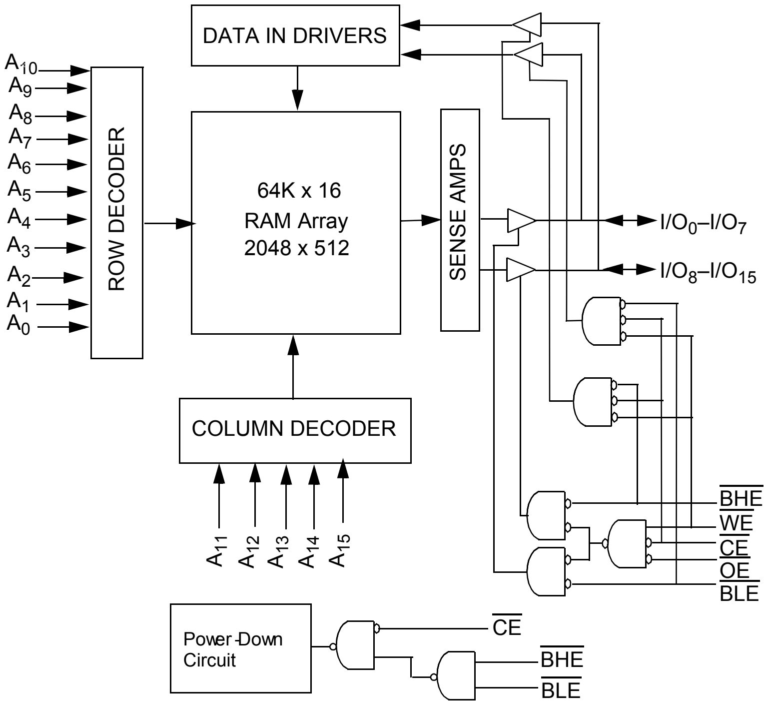
The CY62127DV30 is a high-performance CMOS static RAM organized as 64K words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both byte high enable and byte low enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins ($A_0$ through $A_{15}$). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{15}$).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O$_0$ to I/O$_7$. If byte high enable ($\overline{BHE}$) is LOW, then data from memory appear on I/O$_8$ to I/O$_{15}$. See the truth table at the back of this datasheet for a complete description of read and write modes.

For a complete list of related documentation, click here.

## Logic Block Diagram



## Contents

## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating, $I_{CC}$ (mA) | | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | f = 1 MHz | | f = $f_{MAX}$ | | | | |
| | Min | Typ | Max | | Typ[1] | Max | Typ[1] | Max | Range | Typ[1] | Max |
| CY62127DV30LL | 2.2 | 3.0 | 3.6 | 55 | 0.85 | 1.5 | 5 | 10 | Industrial | 1.5 | 4 |

## Pin Configurations

Figure 1. 48-ball FBGA pinout [2, 3]

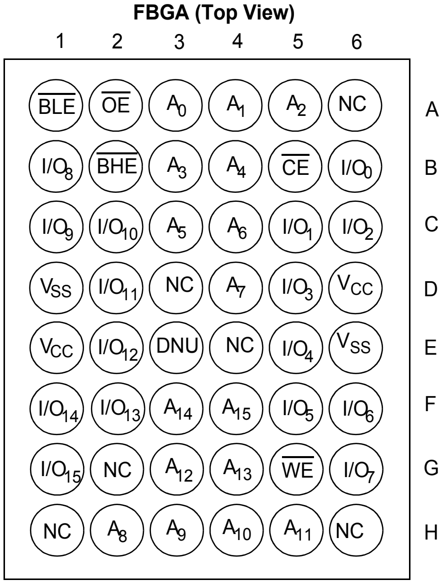
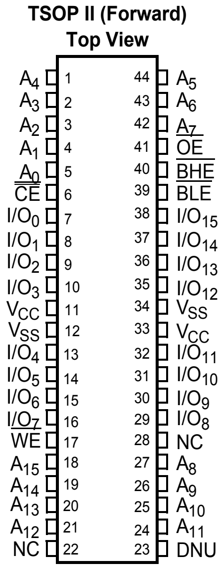


Figure 2. 44-pin TSOP Type II pinout [2, 3]



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**Notes**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C.
2. NC pins are not connected to the die. Expansion pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M
3. Pin #23 of TSOP-II and E3 ball of FBGA are DNU, which have to be left floating or tied to Vss to ensure proper application.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ................................ –65 °C to +150 °C

Ambient temperature
with power applied .................................. –55 °C to +125 °C

Supply voltage to ground potential ................–0.3 V to 3.9 V

DC voltage applied to outputs
in high Z State[4] ................................. –0.3 V to $V_{CC}$ + 0.3 V

DC input voltage[4] .............................. –0.3 V to $V_{CC}$ + 0.3 V

Output current into outputs (LOW) ............................. 20 mA

Static discharge voltage
(per MIL-STD-883, method 3015) ......................... > 2001 V

Latch-up current .................................................... > 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{CC}$[5] |
|---|---|---|
| Industrial | –40 °C to +85 °C | 2.2 V to 3.6 V |

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | -55 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[6] | Max | |
| $V_{OH}$ | Output HIGH voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OH} = -0.1$ mA | 2.0 | – | – | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OH} = -1.0$ mA | 2.4 | – | – | |
| $V_{OL}$ | Output LOW voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OL} = 0.1$ mA | – | – | 0.4 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OL} = 2.1$ mA | – | – | 0.4 | |
| $V_{IH}$ | Input HIGH voltage | $2.2 \le V_{CC} \le 2.7$ | | 1.8 | – | $V_{CC}$ + 0.3 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | 2.2 | – | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input LOW voltage | $2.2 \le V_{CC} \le 2.7$ | | –0.3 | – | 0.6 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | –0.3 | – | 0.8 | |
| $I_{IX}$ | Input leakage current | $GND \le V_I \le V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | $GND \le V_O \le V_{CC}$, Output disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | $f = f_{MAX} = 1/t_{RC}$ | $V_{CC} = 3.6$ V, $I_{OUT} = 0$ mA, CMOS level | – | 5 | 10 | mA |
| | | f = 1 MHz | | – | 0.85 | 1.5 | |
| $I_{SB1}$ | Automatic CE power-down current – CMOS Inputs | $\overline{CE} \ge V_{CC} - 0.2$ V,<br>$V_{IN} \ge V_{CC} - 0.2$ V, $V_{IN} \le 0.2$ V,<br>$f = f_{MAX}$ (Address and data only),<br>f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$) | | – | 1.5 | 4 | µA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS Inputs | $\overline{CE} \ge V_{CC} - 0.2$ V,<br>$V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V,<br>f = 0, $V_{CC} = 3.6$ V | | – | 1.5 | 4 | µA |

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**Notes**

[4] $V_{IL(min)} = -2.0$ V for pulse durations less than 20 ns., $V_{IH(max)} = V_{CC} + 0.75$ V for pulse durations less than 20 ns.

[5] Full device operation requires linear ramp of $V_{CC}$ from 0 V to $V_{CC(min)}$ and $V_{CC}$ must be stable at $V_{CC(min)}$ for 500 µs.

[6] Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

## Capacitance

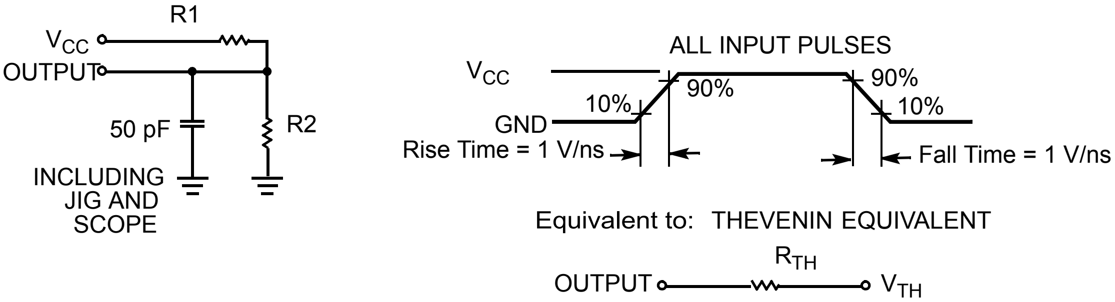
| Parameter [7] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 8 | pF |
| $C_{OUT}$ | Output capacitance | | 8 | pF |

## Thermal Resistance

| Parameter [8] | Description | Test Conditions | FBGA | TSOP-II | Unit |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 52.02 | 62.01 | °C/W |
| $\theta_{JC}$ | Thermal resistance (junction to case) | | 10.98 | 22.08 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**



| Parameters | 2.5 V (2.2 V–2.7 V) | 3.0 V (2.7 V–3.6 V) | Unit |
|---|---|---|---|
| R1 | 16600 | 1103 | Ω |
| R2 | 15400 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

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**Note**

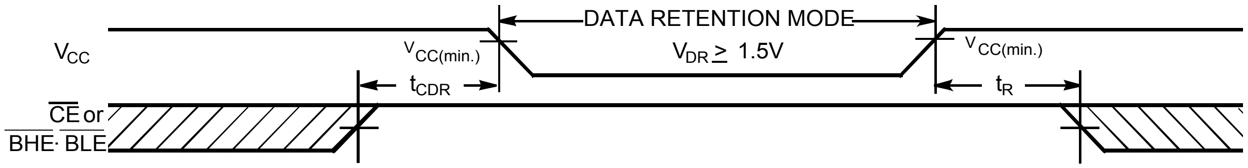
7. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

| Parameter | Description | Conditions | Min | Typ[9] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | 1.5 | – | – | V |
| $I_{CCDR}$ | Data retention current | $V_{CC}$ = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | | – | 3 | µA |
| $t_{CDR}$ | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R$[10] | Operation recovery time | | 55 | – | – | ns |

## Data Retention Waveform

Figure 4. Data Retention Waveform [11]



**Notes**

8. Tested initially and after any design or process changes that may affect these parameters.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C.
10. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)}$ > 200 µs.

## Switching Characteristics

Over the Operating Range

| Parameter [12] | Description | CY62127DV30-55 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 55 | – | ns |
| $t_{AA}$ | Address to data valid | – | 55 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z[13] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z[13, 14] | – | 20 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z[13] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z[13, 14] | – | 20 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 55 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to data valid | – | 55 | ns |
| $t_{LZBE}$[15] | $\overline{BLE}$/$\overline{BHE}$ LOW to low Z[13] | 5 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to high Z[13, 14] | – | 20 | ns |
| **Write Cycle**[16, 17] | | | | |
| $t_{WC}$ | Write cycle time | 55 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 40 | – | ns |
| $t_{AW}$ | Address setup to write end | 40 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 40 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 40 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z[13, 14] | – | 20 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z[13] | 10 | – | ns |

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**Notes**

11. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the Chip Enable signals or by disabling both byte enable pins.
12. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}$.
13. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
14. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
15. If both byte enables are toggled together, this value is 10 ns.
16. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
17. The minimum write pulse width for WRITE Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

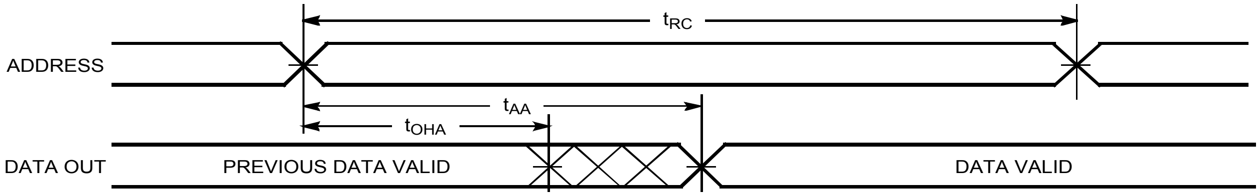

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [18, 19]

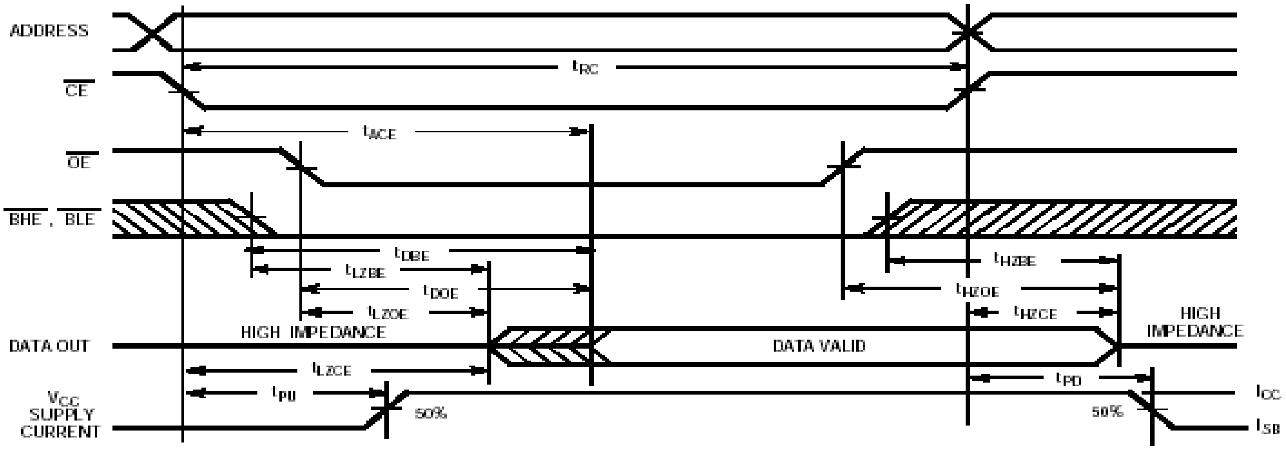

Figure 6. Read Cycle No. 2 (OE Controlled) [18, 19, 20]

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**Notes**

18. Device is continuously selected. OE, CE = $V_{IL}$, BHE, BLE = $V_{IL}$.
19. WE is HIGH for Read cycle.
20. Address valid prior to or coincident with CE, BHE, BLE transition LOW.

## Switching Waveforms *(continued)*

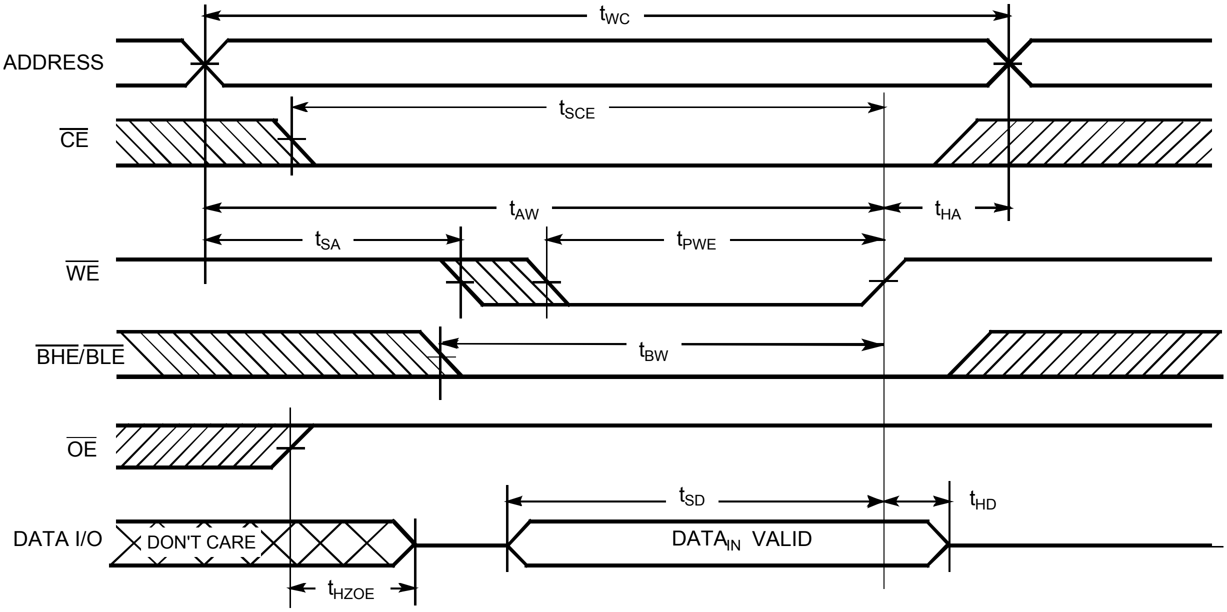

**Figure 7. Write Cycle No. 1 (WE Controlled)** [21, 22, 23, 24, 25]

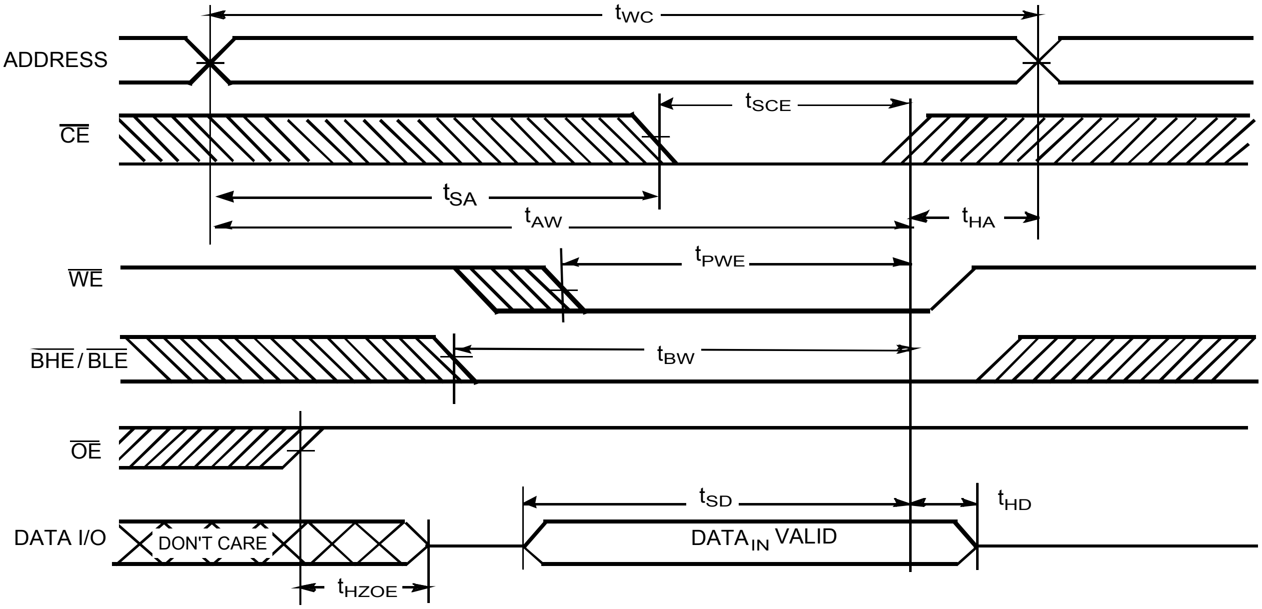

**Figure 8. Write Cycle No. 2 (CE Controlled)** [21, 22, 23, 24, 25]

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**Notes**

21. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
22. The internal Write time of the memory is defined by the overlap of WE, CE = $V_{IL}$, BHE and/or BLE = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. Data I/O is high-impedance if OE = $V_{IH}$.
24. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
25. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms *(continued)*

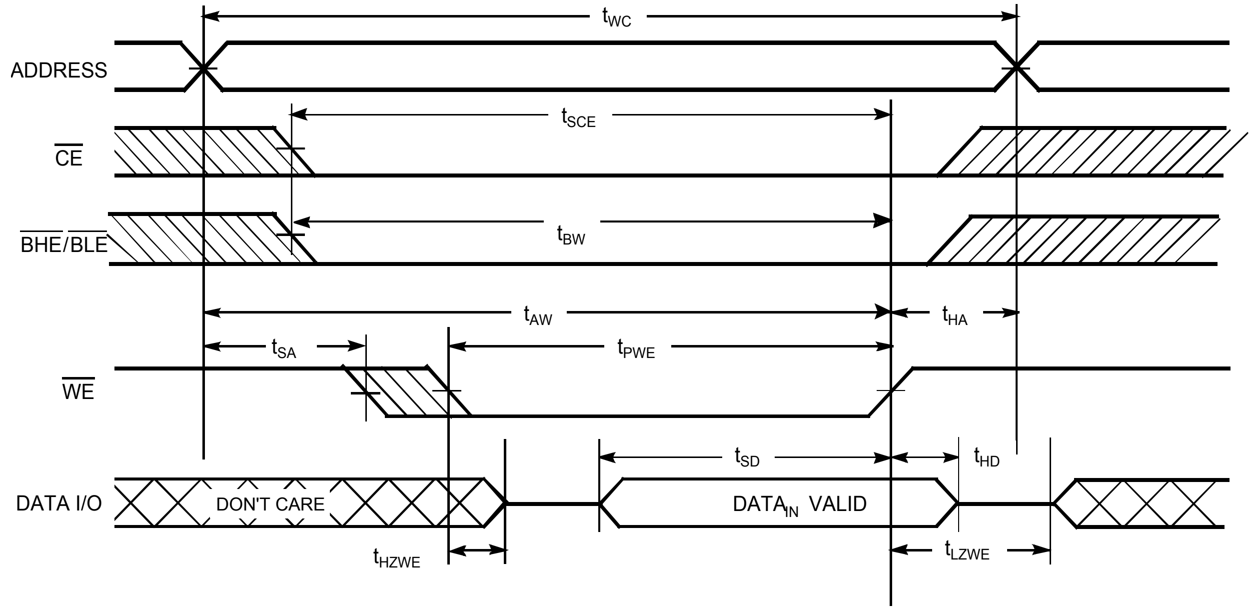

Figure 9. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [26, 27, 28]

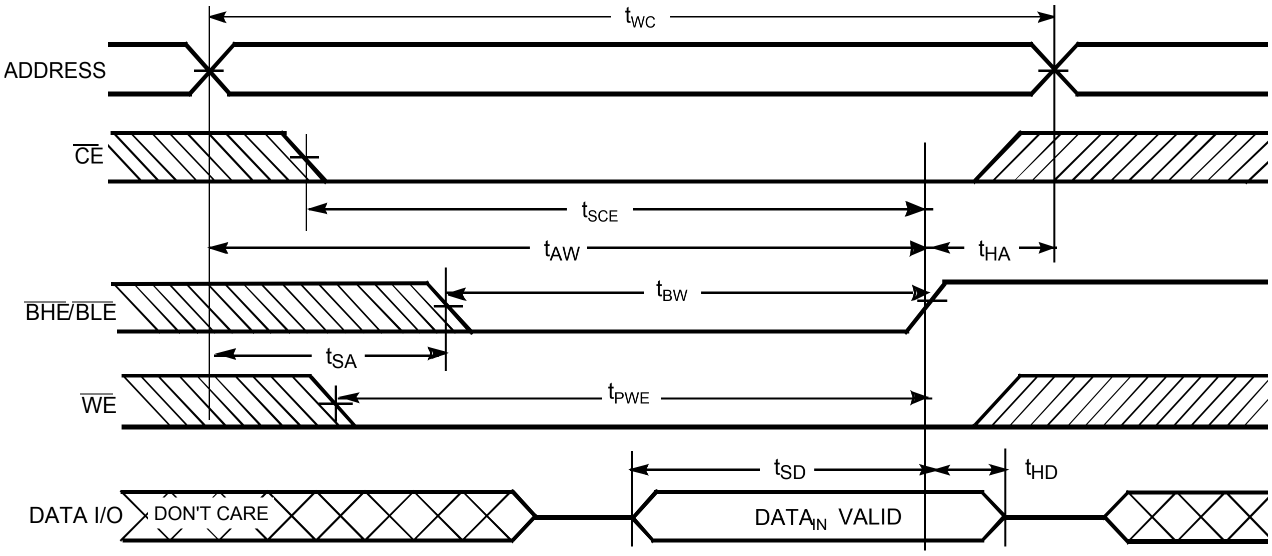

Figure 10. Write Cycle No. 4 ($\overline{\text{BHE}}$ / $\overline{\text{BLE}}$ Controlled) [26, 27]

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**Notes**

26. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
27. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.
28. The minimum write pulse width for WRITE Cycle No.3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of $t_{HZWE}$ and $t_{SD}$.

## Truth Table

| $\overline{\text{CE}}$ [29, 30] | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | $\overline{\text{BHE}}$ | $\overline{\text{BLE}}$ | $I/O_0$–$I/O_7$ | $I/O_8$–$I/O_{15}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | X | X | H | H | High Z | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out | Data Out | Read All Bits | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out | High Z | Read Lower Byte Only | Active ($I_{CC}$) |
| L | H | L | L | H | High Z | Data Out | Read Upper Byte Only | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | High Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data in | Data in | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data in | High Z | Write Lower Byte Only | Active ($I_{CC}$) |
| L | L | X | L | H | High Z | Data in | Write Upper Byte Only | Active ($I_{CC}$) |

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**Notes**

[29] If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

[30] During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

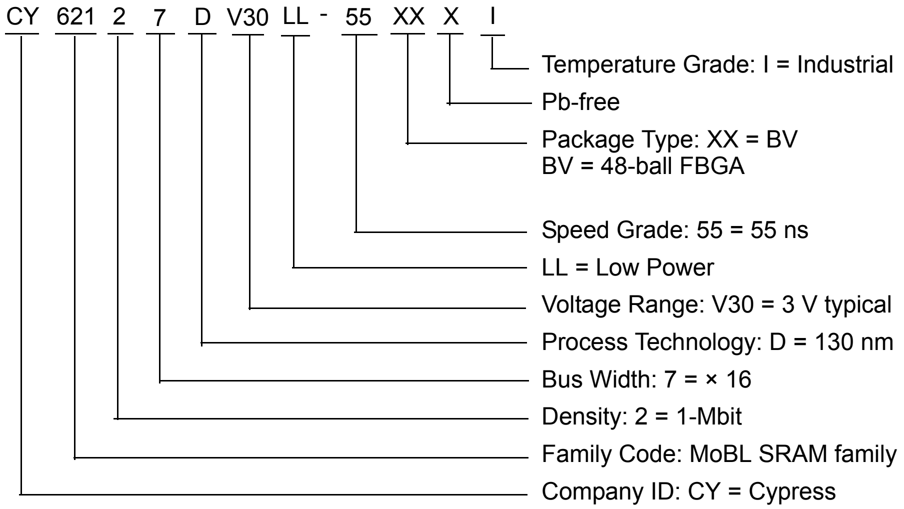
## Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and see product summary page at http://www.cypress.com/products or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62127DV30LL-55BVXI | 51-85150 | 48-ball FBGA (6 mm × 8 mm × 1 mm) (Pb-free) | Industrial |

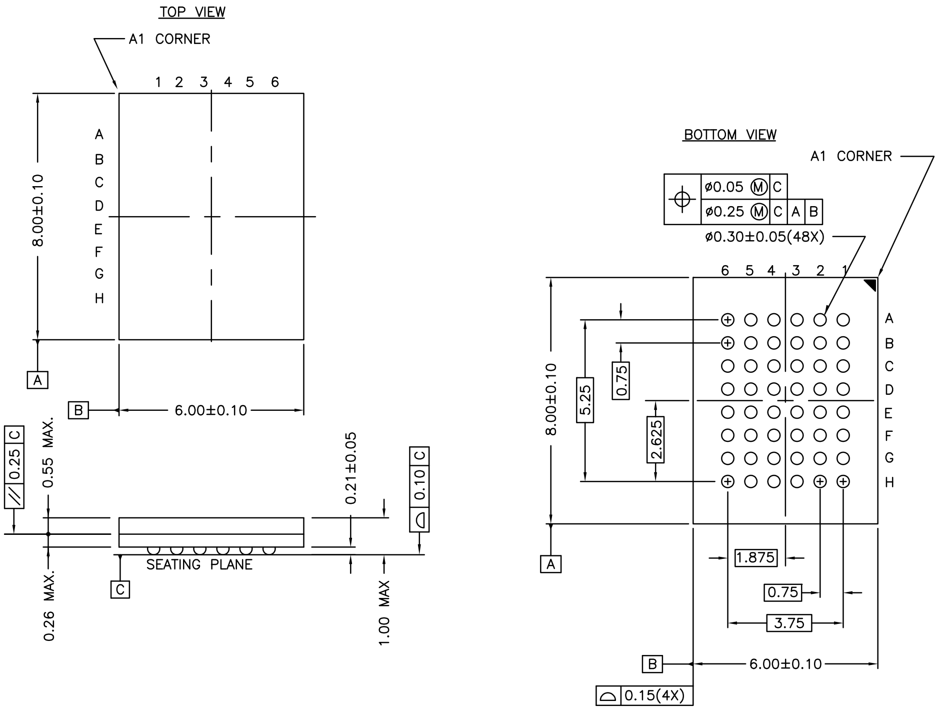
### Ordering Code Definitions



Temperature Grade: I = Industrial
Pb-free
Package Type: XX = BV
BV = 48-ball FBGA
Speed Grade: 55 = 55 ns
LL = Low Power
Voltage Range: V30 = 3 V typical
Process Technology: D = 130 nm
Bus Width: 7 = × 16
Density: 2 = 1-Mbit
Family Code: MoBL SRAM family
Company ID: CY = Cypress

## Package Diagrams

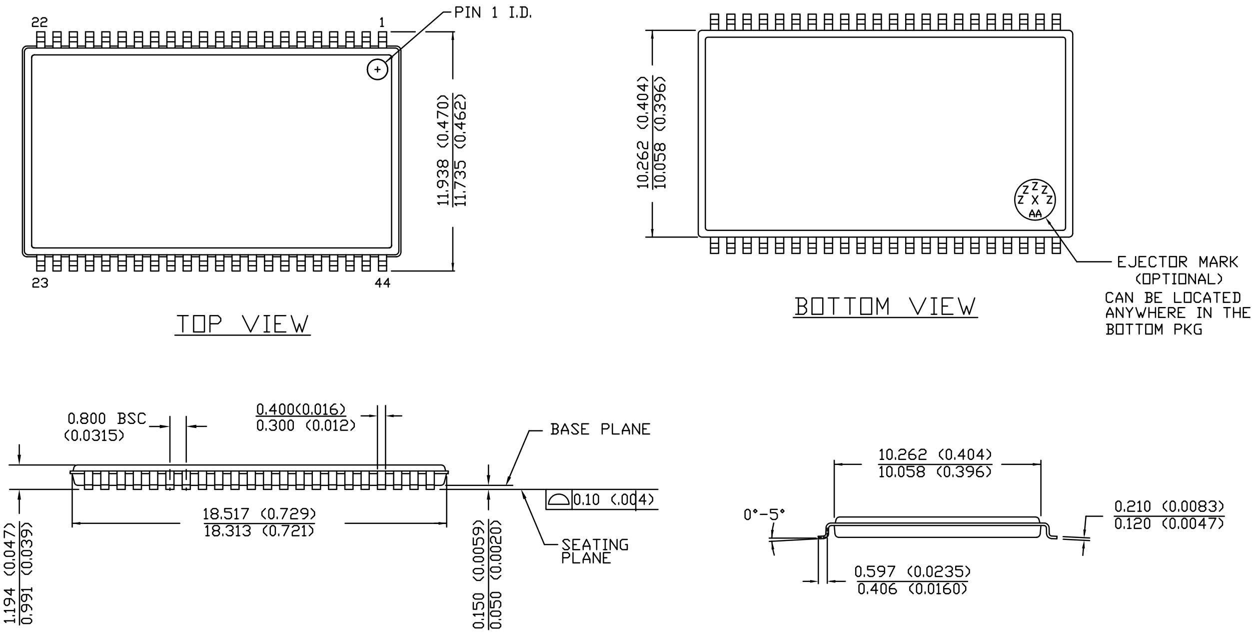
**Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

**Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087**



DIMENSION IN MM (INCH) $\frac{\text{MAX}}{\text{MIN.}}$

PKG WEIGHT: REFER TO PMDD SPEC

51-85087 *E

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{\text{BHE}}$ | Byte High Enable |
| $\overline{\text{BLE}}$ | Byte Low Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| $\overline{\text{CE}}$ | Chip Enable |
| FBGA | Fine-Pitch Ball Grid Array |
| I/O | Input/Output |
| $\overline{\text{OE}}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| $\overline{\text{WE}}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| µA | microampere |
| mA | milliampere |
| ns | nanosecond |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

**Document Title: CY62127DV30 MoBL®, 1-Mbit (64K × 16) Static RAM**
**Document Number: 38-05229**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 117690 | JUI | 08/27/02 | New data sheet |
| *A | 127311 | MPR | 06/13/03 | Changed status from Advanced to Preliminary.<br>Updated DC Electrical Characteristics:<br>Changed maximum value of $I_{SB2}$ parameter from 4 μA to 5 μA corresponding to Test Condition “L”.<br>Changed maximum value of $I_{SB2}$ parameter from 3 μA to 4 μA corresponding to Test Condition “LL”.<br>Updated Capacitance:<br>Changed value of $C_{IN}$ parameter from 6 pF to 8 pF.<br>Updated Data Retention Characteristics:<br>Changed maximum value of $I_{CCDR}$ parameter from 1.2 μA to 4 μA corresponding to Test Condition “L”.<br>Changed maximum value of $I_{CCDR}$ parameter from 0.8 μA to 3 μA corresponding to Test Condition “LL”. |
| *B | 128341 | JUI | 07/22/03 | Changed status from Preliminary to Final.<br>Add 70 ns speed related information in all instances across the document.<br>Updated Ordering Information. |
| *C | 129000 | CDY | 08/29/03 | Updated DC Electrical Characteristics:<br>Changed typical value of $I_{CC}$ parameter corresponding to Test Condition “f = 1 MHz” from 0.5 mA to 0.85 mA. |
| *D | 316039 | PCI | See ECN | Added 45 ns speed bin related information in all instances across the document.<br>Updated AC Test Loads and Waveforms:<br>Added Note “Test condition for the 45-ns part is a load capacitance of 30 pF.” and referred the same note in Figure 3.<br>Updated Ordering Information:<br>Updated part numbers.<br>Changed name of 44-lead TSOP-II package from Z44 to ZS44 in “Package Name” column. |
| *E | 346982 | AJU | See ECN | Added 56-pin QFN package related information in all instances across the document.<br>Updated Ordering Information. |
| *F | 369955 | SYT | See ECN | Added Automotive related information in all instances across the document.<br>Updated Features:<br>Added Temperature Ranges.<br>Updated Ordering Information:<br>Added Pb-free Automotive parts for 55 ns Speed bin. |
| *G | 457685 | NXR | See ECN | Removed 56-pin QFN package related information in all instances across the document.<br>Updated Ordering Information. |
| *H | 470383 | NXR | See ECN | Updated Pin Configurations:<br>Updated Figure 2 (Changed pin 23 of TSOP II from NC to DNU).<br>Updated Note 3. |
| *I | 2897885 | RAME / NIKM | 03/22/10 | Updated Ordering Information (Removed inactive parts).<br>Updated Package Diagrams. |

## Document History Page *(continued)*

**Document Title: CY62127DV30 MoBL®, 1-Mbit (64K × 16) Static RAM**
**Document Number: 38-05229**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| *J | 3010373 | AJU | 08/20/2010 | Updated Features.<br>Updated Product Portfolio.<br>Updated Operating Range.<br>Updated DC Electrical Characteristics.<br>Updated Data Retention Characteristics.<br>Updated Switching Characteristics.<br>Updated Ordering Information and added Ordering Code Definitions.<br>Minor edits.<br>Updated to new template. |
| *K | 3329789 | RAME | 07/27/11 | Updated Functional Description:<br>Removed the Note “For best practice recommendations, refer to the Cypress application note “System Design Guidelines” at http://www.cypress.com website.” and its reference.<br>Updated to new template. |
| *L | 3393183 | RAME | 10/03/11 | Post to web. |
| *M | 3861271 | TAVA | 01/08/2013 | Updated Ordering Information (Updated part numbers).<br>Updated Package Diagrams:<br>spec 51-85150 – Changed revision from *G to *H.<br>spec 51-85087 – Changed revision from *D to *E. |
| *N | 4499469 | MEMJ | 09/11/2014 | Updated Switching Characteristics:<br>Added Note 17 and referred the same note in “Write Cycle”.<br>Updated Switching Waveforms:<br>Added Note 28 and referred the same note in Figure 9.<br>Updated to new template.<br>Completing Sunset Review. |
| *O | 4576478 | MEMJ | 11/21/2014 | Updated Functional Description:<br>Added “For a complete list of related documentation, click here.” at the end. |
| *P | 4920942 | VINI | 09/15/2015 | Updated to new template.<br>Completing Sunset Review. |
| *Q | 5444200 | VINI | 09/21/2016 | Updated Thermal Resistance:<br>Replaced “two-layer” with “four-layer” in “Test Conditions” column.<br>Updated all values of $\theta_{JA}$ and $\theta_{JC}$ parameters.<br>Updated to new template.<br>Completing Sunset Review. |
| *R | 5997966 | AESATMP9 | 12/21/2017 | Updated logo and copyright. |

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