CY62136EV30
MoBL®

2-Mbit (128K x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62136CV30**
- **Ultra low standby power**
  - **— Typical standby current: 1μA**
  - **— Maximum standby current: 7μA**
- **Ultra-low active power**
  - **— Typical active current: 2 mA @ f = 1 MHz**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in a Pb-free 48-ball VFBGA and 44-pin TSOP II packages**

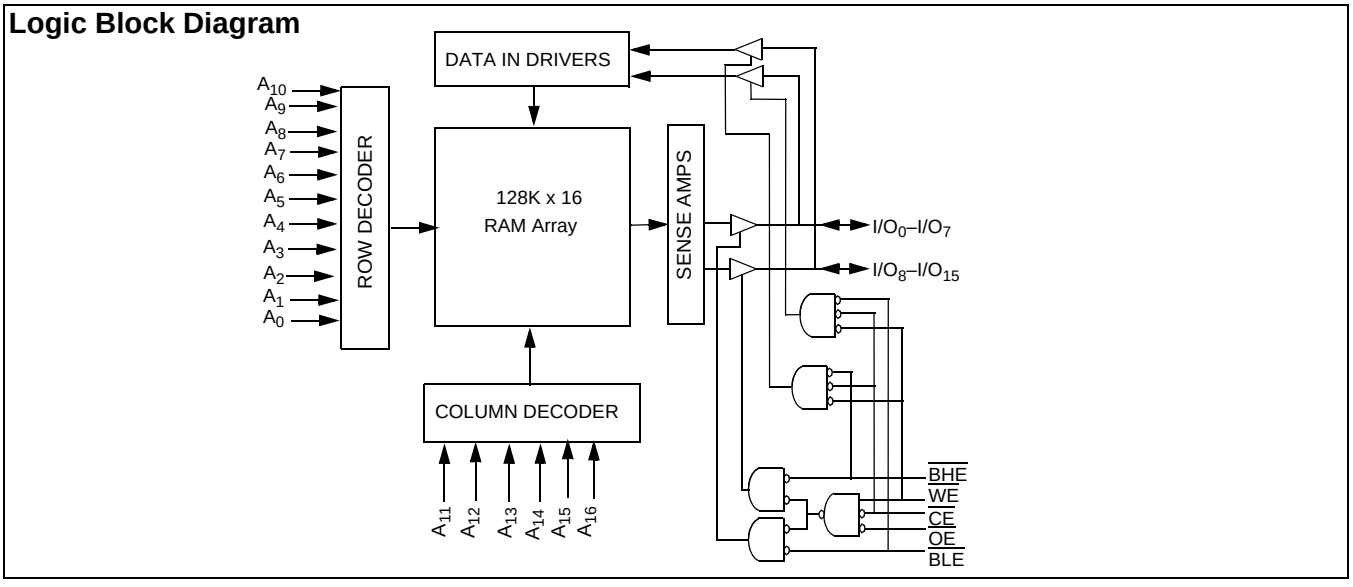
Functional Description[1]

The CY62136EV30 is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

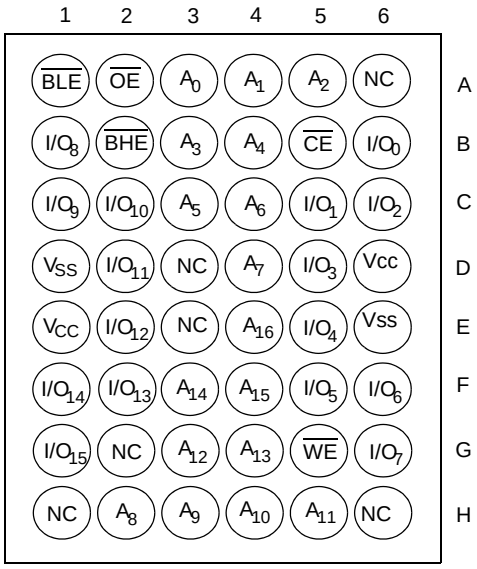
Logic Block Diagram



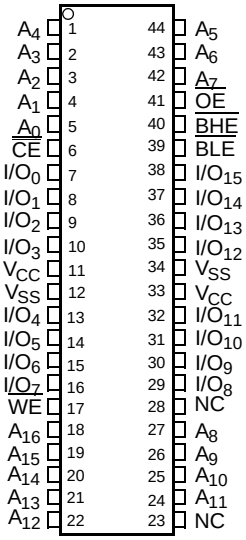
Note:
1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2, 3]

VFBGA (Top View)



44 TSOP II (Top View)



Product Portfolio[4]

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating ICC (mA)				Standby I_{SB2} (μA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[4]	Max.		Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.
CY62136EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes:
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, and H6 in the BGA package are address expansion pins for 4 Mbit, 8 Mbit, 16 Mbit and 32 Mbit, respectively.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied .....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.3V to 3.9V ($V_{CC\ MAX}$ + 0.3V)

DC Voltage Applied to Outputs in High-Z State[5,6].....–0.3V to 3.9V ($V_{CC\ MAX}$ + 0.3V)

DC Input Voltage[5,6]..... –0.3V to 3.9V ($V_{CC\ MAX}$ + 0.3V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current .....> 200 mA

Operating Range[7]

Device	Range	Ambient Temperature	V_{CC}[7]
CY62136EV30LL	Industrial	–40°C to +85°C	2.2V - 3.6V

Electrical Characteristics Over the Operating Range [5, 6, 7]

Parameter	Description	Test Conditions		45 ns Min.	45 ns Typ.[4]	45 ns Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V	2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V			0.4	V
		I_{OL} = 2.1mA	V_{CC} = 2.70V			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3	V
		V_{CC}= 2.7V to 3.6V		2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V		–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V		–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels		15	20	mA
		f = 1 MHz			2	2.5	
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC}–0.2V, V_{IN}≥V_{CC}–0.2V, V_{IN}≤0.2V) f = f_{MAX} (Address and Data Only), f = 0 (OE, and WE), V_{CC} = 3.60V			1	7	µA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V			1	7	µA

Capacitance (for all packages)[8]

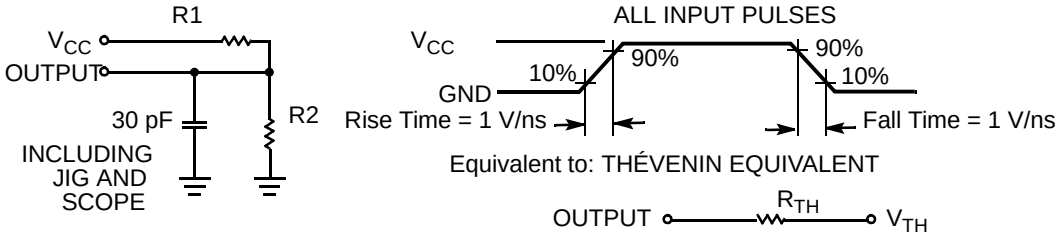
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$=V_{CC}+0.75V for pulse durations less than 20ns.
7. Full Device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after V_{CC} stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance[8]

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[8]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[8]		10	13	°C/W

AC Test Loads and Waveforms

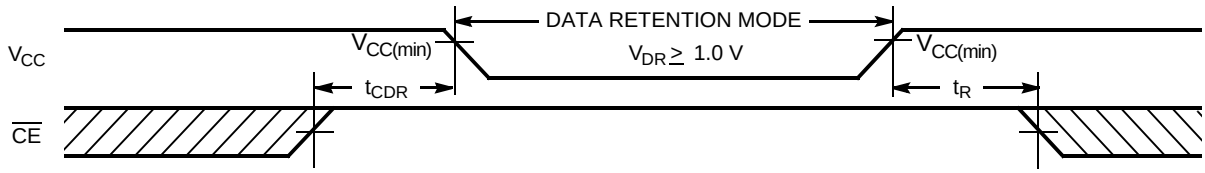


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)[8, 9]

Parameter	Description	Conditions	Min.	Typ.[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.0V $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.8	3	µA
t_{CDR}[8]	Chip Deselect to Data Retention Time		0			ns
t_R[9]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Notes:
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

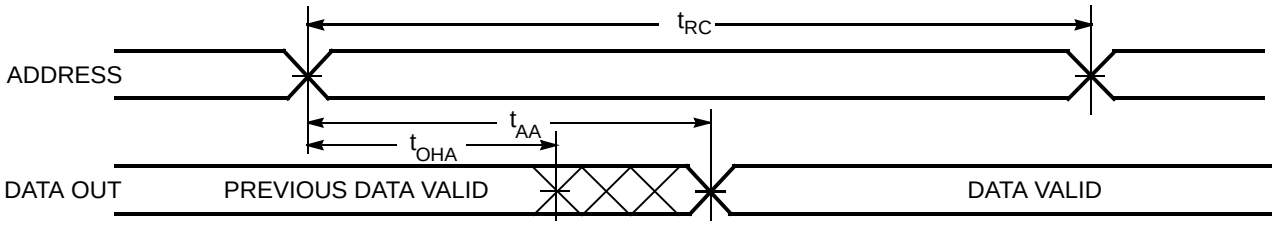
Switching Characteristics Over the Operating Range [10, 11, 12, 13]

Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[11]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[11, 12]		18	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid		22	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[11]	5		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z[11, 12]		18	ns
Write Cycle[13]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		ns
t_{AW}	Address Set-Up to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to Write End	35		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	10		ns

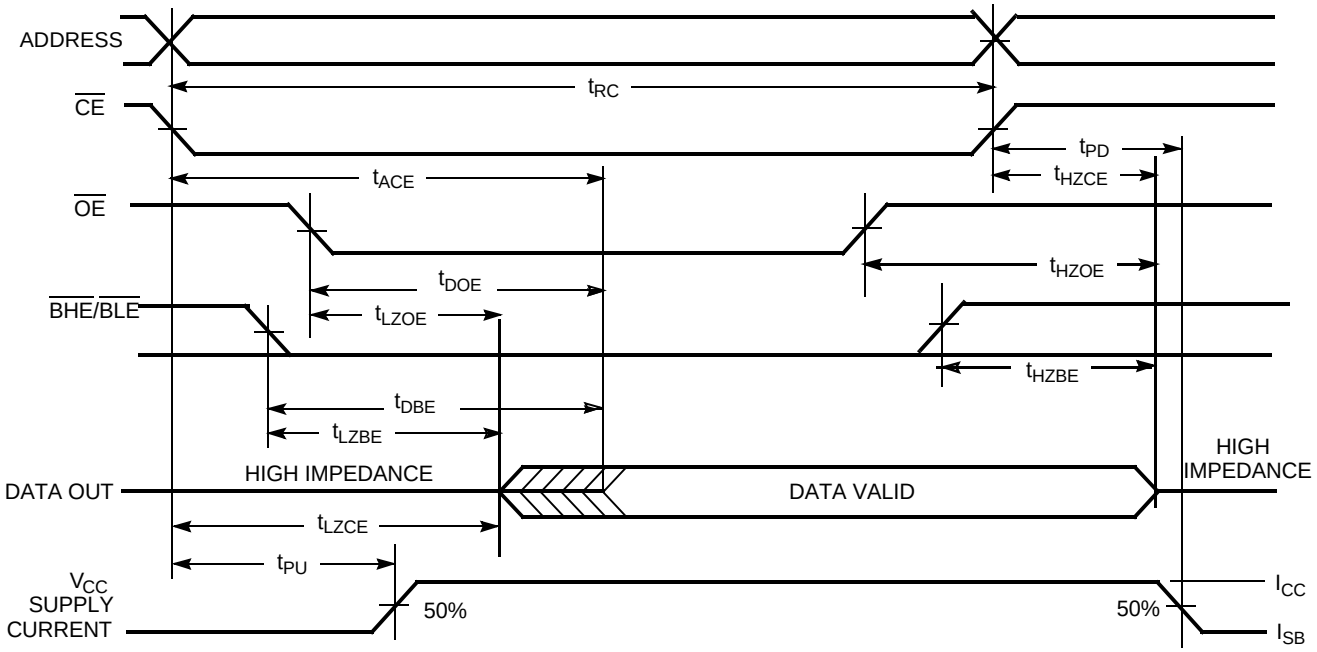
Notes:
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
13. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms [14, 15]

Read Cycle 1 (Address Transition Controlled)[14, 15]



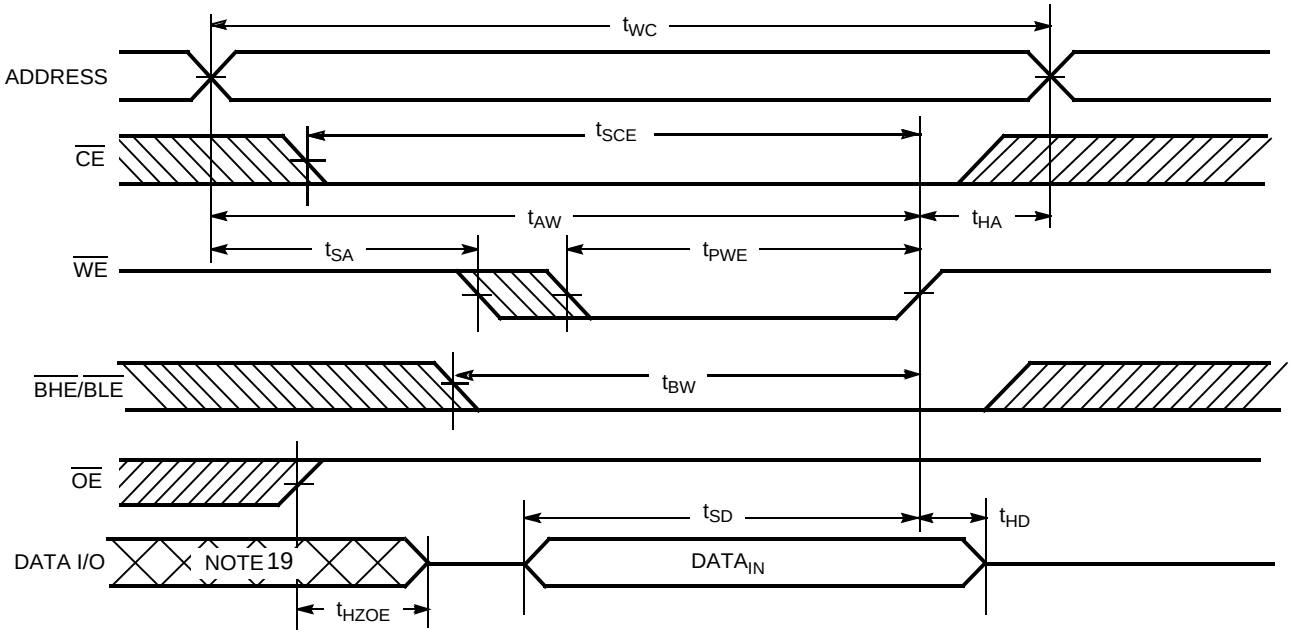
Read Cycle No. 2 (OE Controlled)[15, 16]



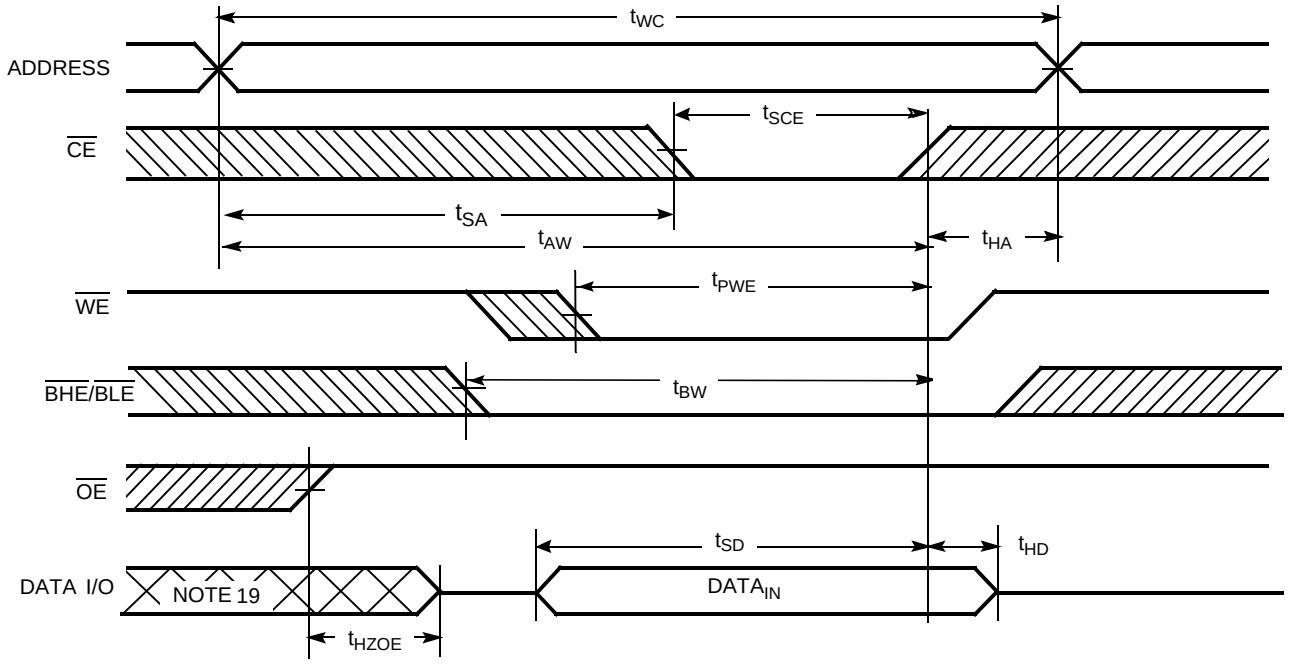
Notes:
14. The device is continuously selected. OE, CE = V_{IL}, BHE and/or BLE = V_{IL}.
15. WE is HIGH for read cycle.
16. Address valid prior to or coincident with CE and BHE, BLE transition LOW.

Switching Waveforms (continued)[14, 15]

Write Cycle No. 1 (WE Controlled)[13, 17, 18]



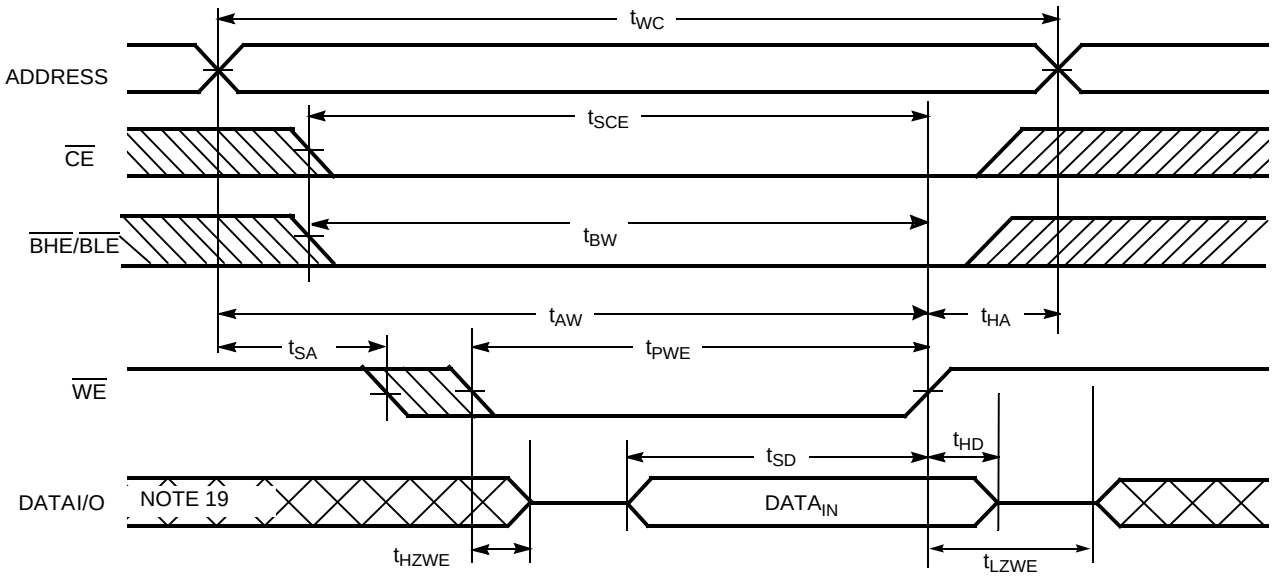
Write Cycle No. 2 (CE Controlled)[13, 17, 18]



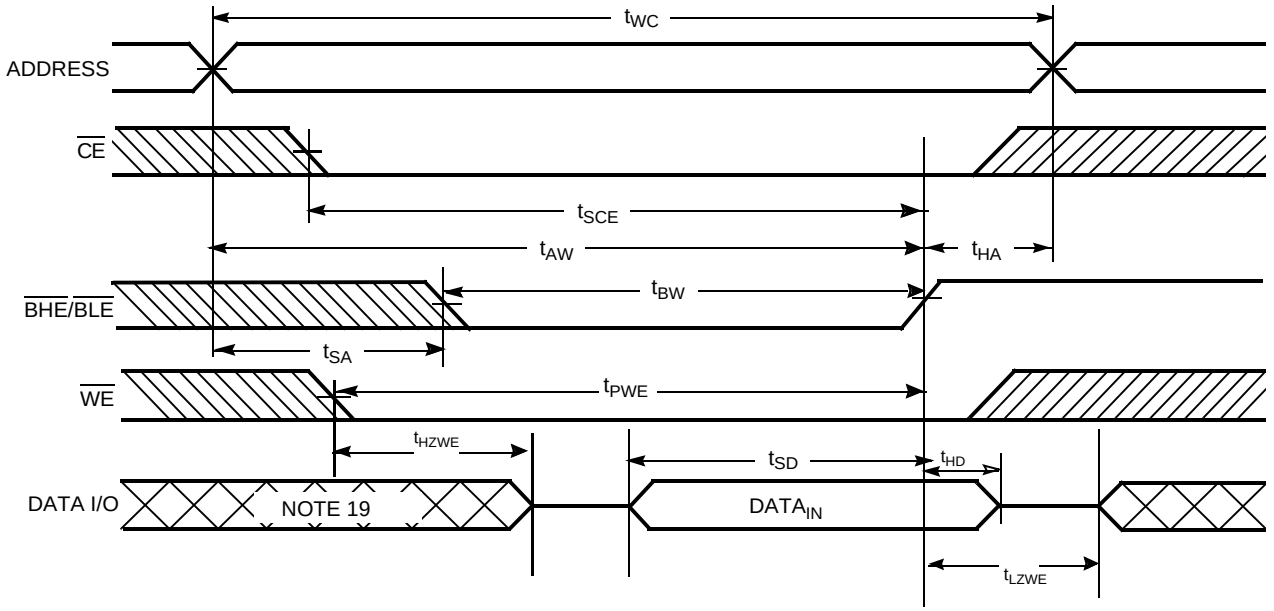
Notes:
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)[14, 15]

Write Cycle No. 3 (WE Controlled, OE LOW)[18]



Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)[18]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

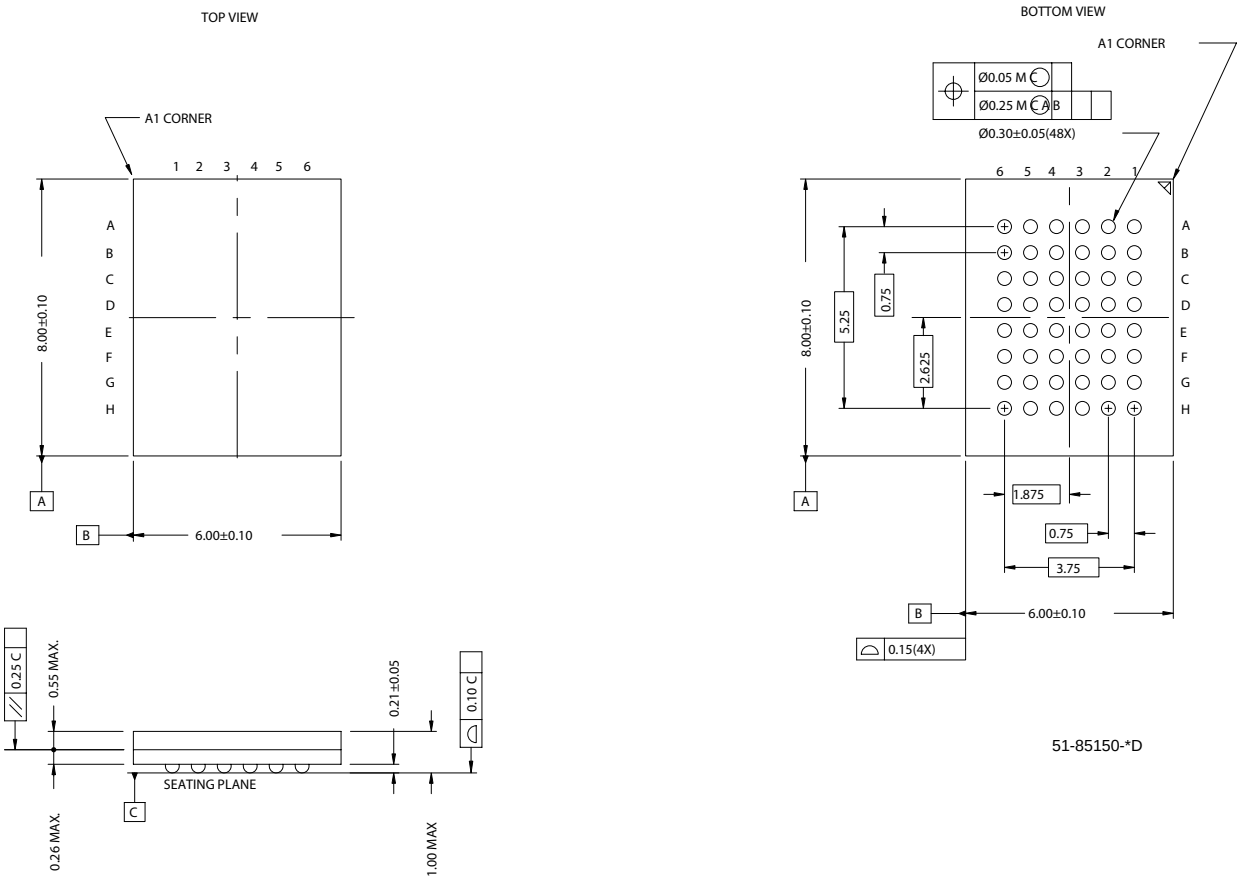
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62136EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package II (Pb-free)	

Please contact your local Cypress sales representative for availability of other parts

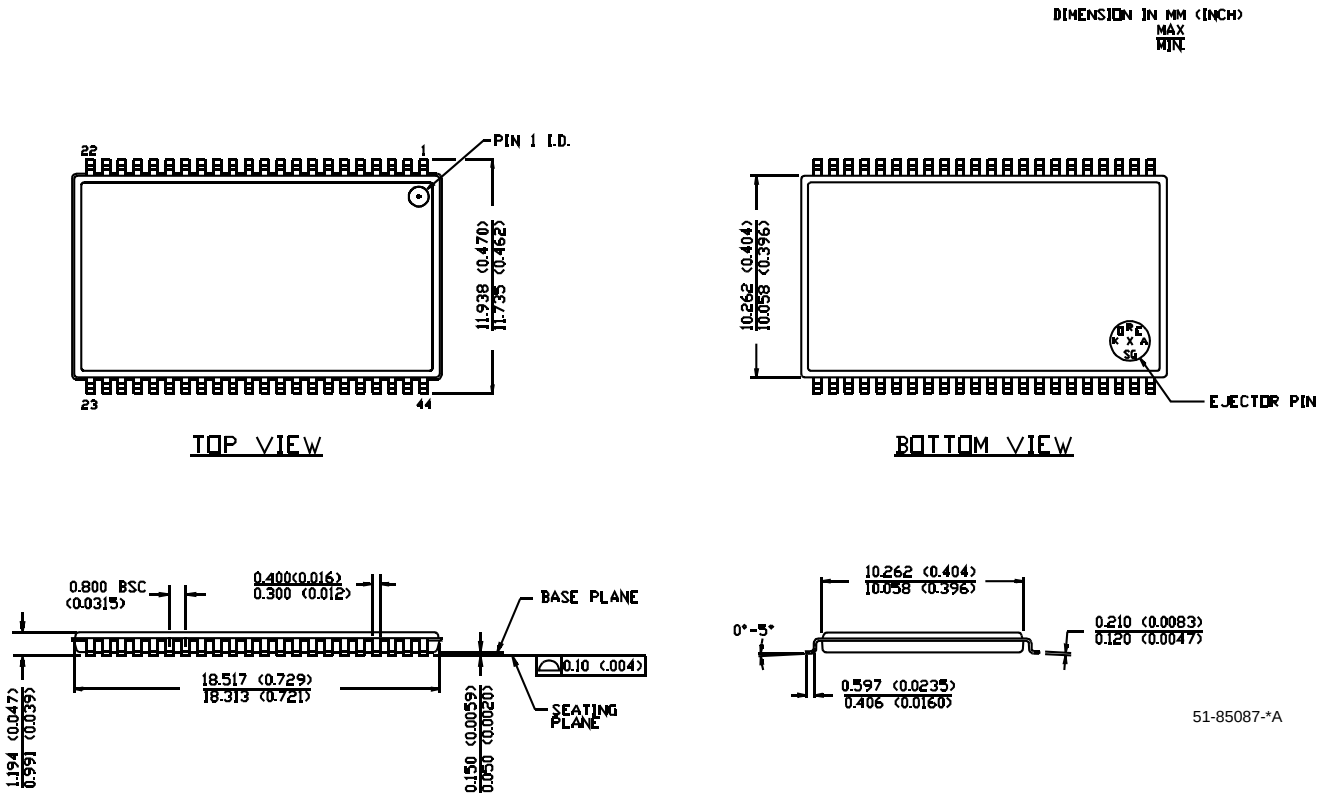
Package Diagrams

48-pin VFBGA (6 x 8 x 1 mm) (51-85150)



Package Diagrams (continued)

44-pin TSOP II (51-85087)



Document History Page

Document Title: CY62136EV30 MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 38-05569				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	237432	See ECN	AJU	New Data Sheet
*A	419988	See ECN	RXU	Converted from Advanced Information to Final. Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35ns Speed Bin Removed “L” version of CY62136EV30 Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ. values from 0.7 µA to 1 µA and Max. values from 2.5 µA to 7 µA. Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed V_{DR} from 1.5V to 1V on Page# 4. Changed I_{CCDR} from 2.5 µA to 3 µA. Added I_{CCDR} typical value. Changed t_{OHA}, t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{LZBE} from 6 ns to 5 ns Changed t_{LZOE} from 3 ns to 5 ns Changed t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE},t_{AW} and t_{BW} from 40 ns to 35 ns Changed t_{PWE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Corrected typo in the Truth Table on Page# 9 Updated the package diagram 48-pin VFBGA from *B to *D Updated the ordering Information table and replaced the Package Name column with Package Diagram.
*B	427817	See ECN	NXR	Minor change: Moved datasheet to external web