

## 2-Mbit (128K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Industrial:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-A:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-E:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- **High speed: 55 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in standard Pb-free 44-pin TSOP Type II, Pb-free and non Pb-free 48-ball FBGA packages**

### Functional Description<sup>[1]</sup>

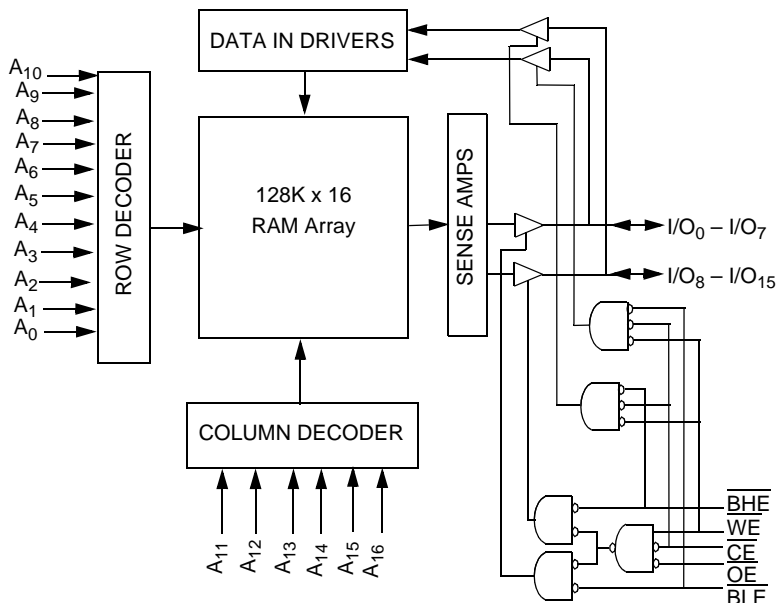
The CY62136VN is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{\text{CE}}$  HIGH). The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH),  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

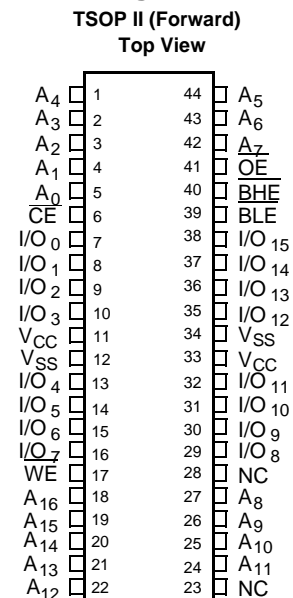
Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{16}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

### Logic Block Diagram



### PinConfigurations<sup>[3]</sup>

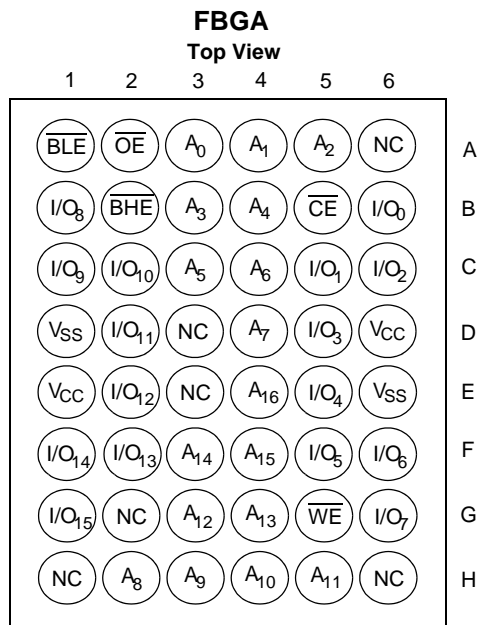


**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed	Ranges	Power Dissipation			
	Min	Typ. <sup>[2]</sup>	Max			Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
						Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62136VNLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
				55	Automotive-A	7	20	1	15
				70	Industrial	7	15	1	15
				70	Automotive-A	7	15	1	15
				70	Automotive-E	7	20	1	20

**Pin Configurations<sup>[3]</sup>**

**Notes:**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25°C.
3. NC pins are not connected on the die.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential .....	-0.5V to +4.6V
DC Voltage Applied to Outputs in High-Z State <sup>[4]</sup> .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage <sup>[4]</sup> .....	-0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	> 2001V (per MIL-STD-883, Method 3015)
Latch-up Current.....	> 200 mA

### Operating Range

Range	Ambient Temperature [T <sub>A</sub> ] <sup>[5]</sup>	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	$V_{CC} = 2.7V, I_{OH} = -1.0 mA$	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	$V_{CC} = 2.7V, I_{OL} = 2.1 mA$			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	$V_{CC} = 3.6V$	2.2		$V_{CC} + 0.5V$	2.2		$V_{CC} + 0.5V$	V
V <sub>IL</sub>	Input LOW Voltage	$V_{CC} = 2.7V$	-0.5		0.8	-0.5		0.8	V
I <sub>IX</sub>	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	Ind'l	-1	+1	-1	+1	$\mu A$	
			Auto-A	-1	+1	-1	+1	$\mu A$	
			Auto-E			-10	+10	$\mu A$	
I <sub>OZ</sub>	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	Ind'l	-1	+1	-1	+1	$\mu A$	
			Auto-A	-1	+1	-1	+1	$\mu A$	
			Auto-E			-10	+10	$\mu A$	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6V, I_{OUT} = 0 mA$ , CMOS Levels	Ind'l	7	20	7	15	mA
				Auto-A	7	20	7	15	
				Auto-E			7	20	
		$f = 1 MHz$		Ind'l	1	2	1	2	mA
				Auto-A	1	2	1	2	
				Auto-E			1	2	
I <sub>SB1</sub>	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V, V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = f_{MAX}$	Ind'l		100		100	$\mu A$	
			Auto-A		100		100	$\mu A$	
			Auto-E				100	$\mu A$	
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V, V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$	Ind'l	1	15	1	15	$\mu A$	
			Auto-A	1	15	1	15		
			Auto-E			1	20		

### Capacitance<sup>[6]</sup>

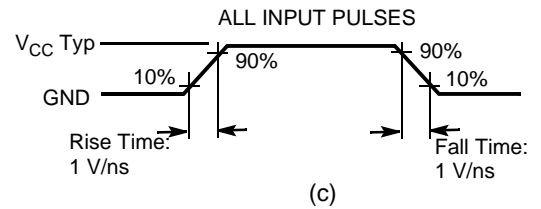
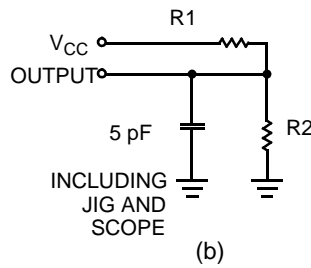
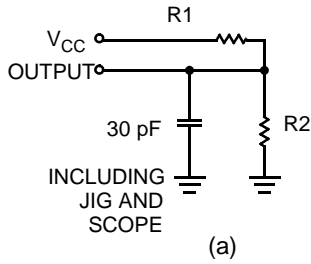
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	$T_A = 25^\circ C, f = 1 MHz, V_{CC} = V_{CC(typ)}$	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

#### Notes:

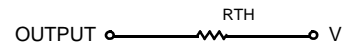
- V<sub>IL</sub>(min) = -2.0V for pulse durations less than 20 ns.
- T<sub>A</sub> is the "Instant-On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[6]</sup>**

Parameter	Description	Test Conditions	TSOPII	FBGA	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	60	55	$^{\circ}\text{C}/\text{W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		22	16	$^{\circ}\text{C}/\text{W}$

**AC Test Loads and Waveforms**


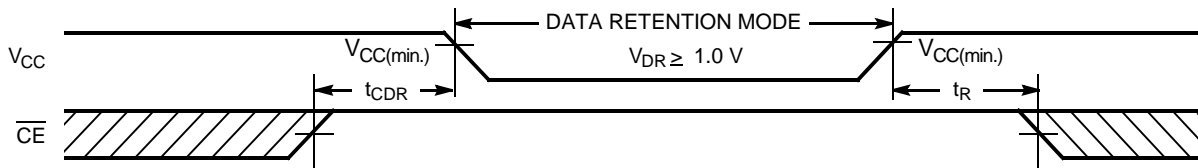
Equivalent to: THÉVENIN EQUIVALENT



Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
$R_{TH}$	645	Ohms
$V_{TH}$	1.75	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[9]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0\text{V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}$ ,		0.5	7.5	$\mu\text{A}$
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		70			ns

**Data Retention Waveform**

**Note:**

7. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100$  ms or stable at  $V_{CC(\text{min})} \geq 100$  ms.
8. No input may exceed  $V_{CC} + 0.3\text{V}$

**Switching Characteristics** Over the Operating Range <sup>[9]</sup>

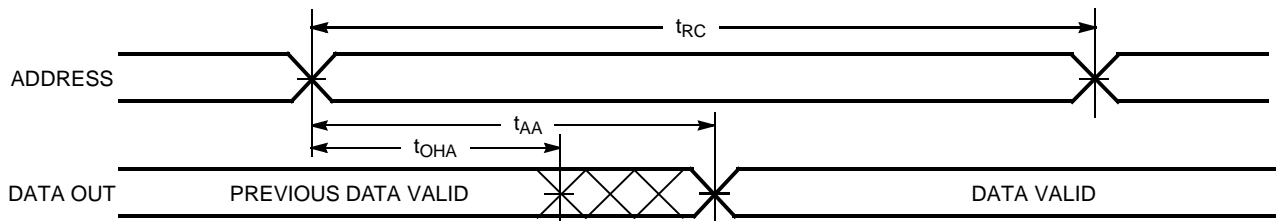
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[10]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[10, 11]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[10]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[10, 11]</sup>		25		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-down		55		70	ns
t <sub>DBE</sub>	$\overline{BLE} / \overline{BHE}$ LOW to Data Valid		25		35	ns
t <sub>LZBE</sub>	$\overline{BLE} / \overline{BHE}$ LOW to Low-Z <sup>[10, 11]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE} / \overline{BHE}$ HIGH to High-Z <sup>[12]</sup>		25		25	ns
<b>Write Cycle<sup>[12, 13]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>BW</sub>	$\overline{BLE} / \overline{BHE}$ LOW to Write End	50		60		ns
t <sub>SD</sub>	Data Set-up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[10, 11]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[10]</sup>	5		10		ns

**Notes:**

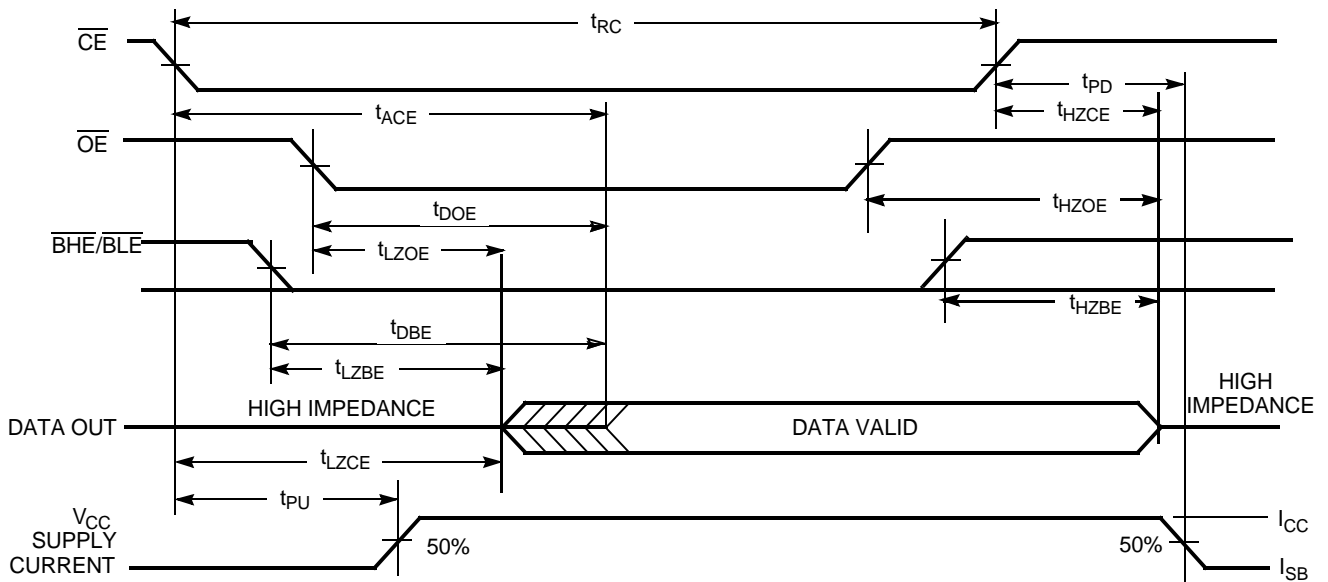
9. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
10. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
11. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
12. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for write cycle 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

### Switching Waveforms

#### Read Cycle No. 1<sup>[14, 15]</sup>



#### Read Cycle No. 2<sup>[15, 16]</sup>

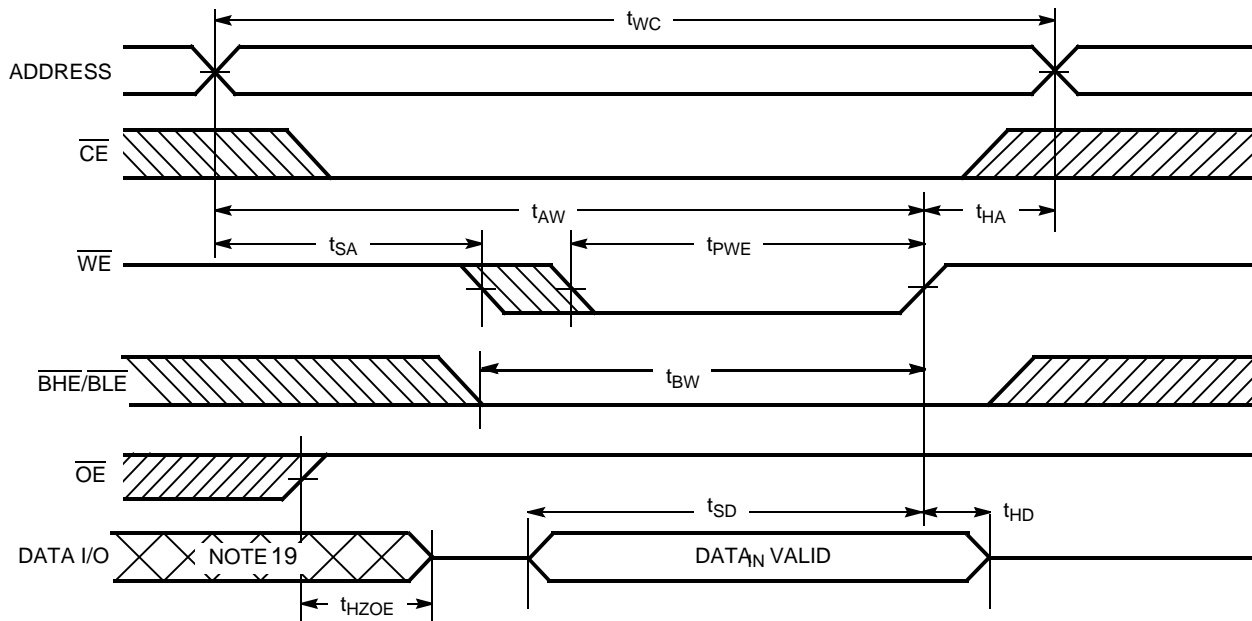


**Notes:**

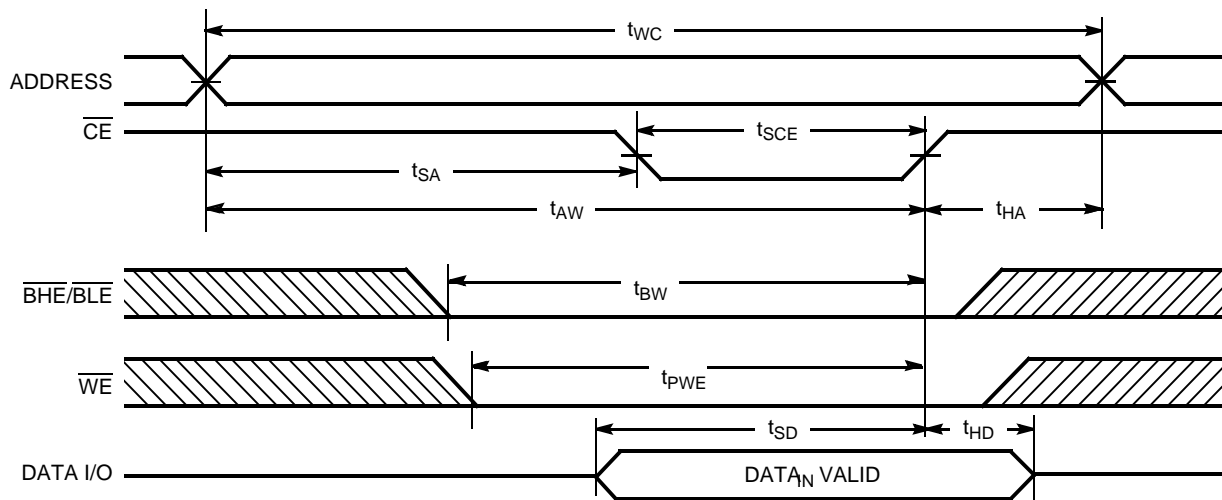
- 14. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 1 (WE Controlled)**<sup>[12, 17, 18]</sup>



**Write Cycle No. 2 (CE Controlled)**<sup>[12, 17, 18]</sup>

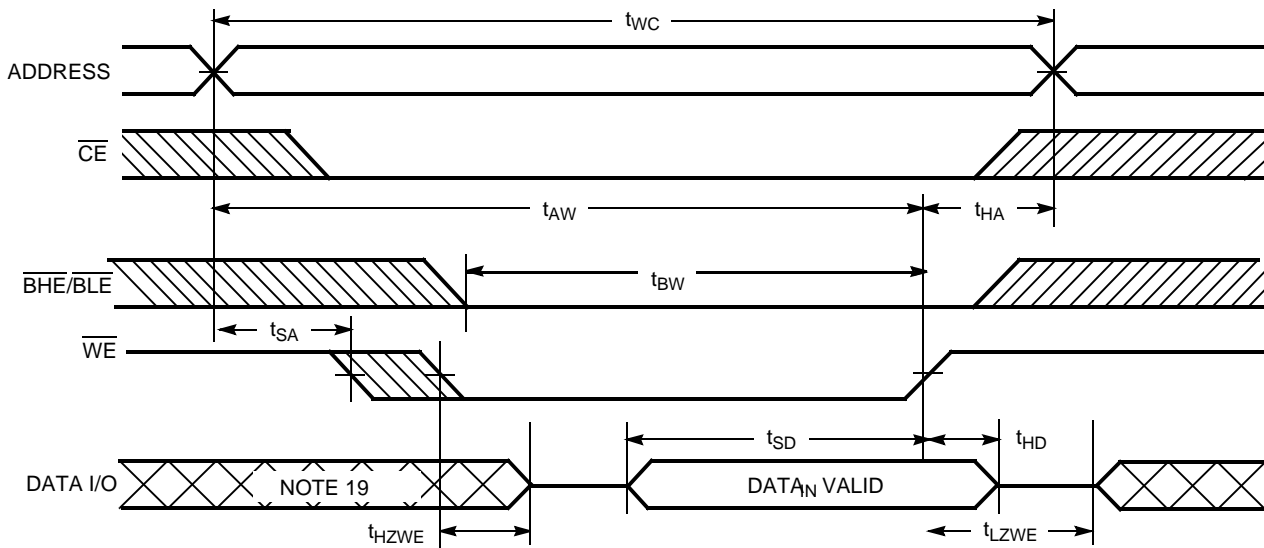


**Notes:**

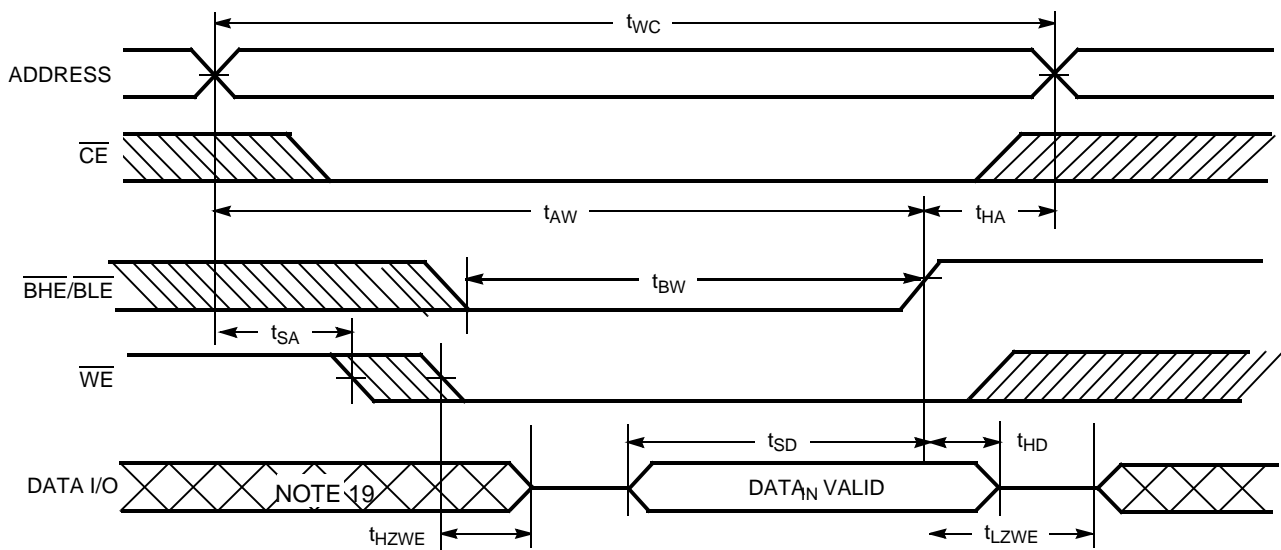
- 17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 18. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms** (continued)

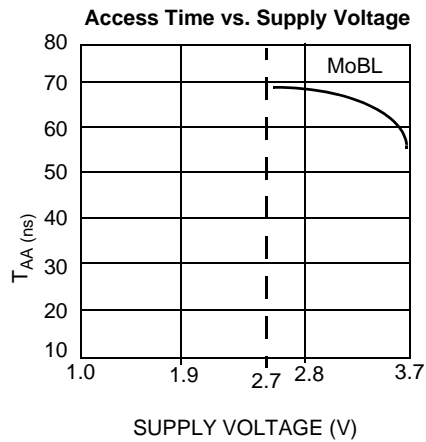
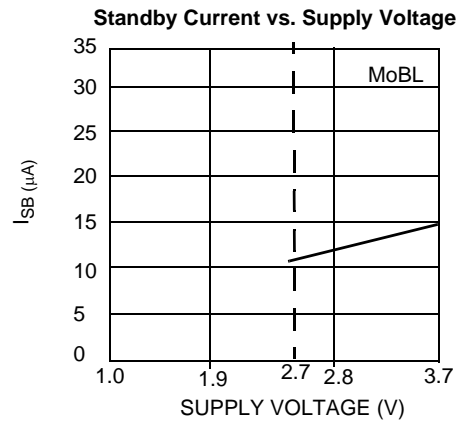
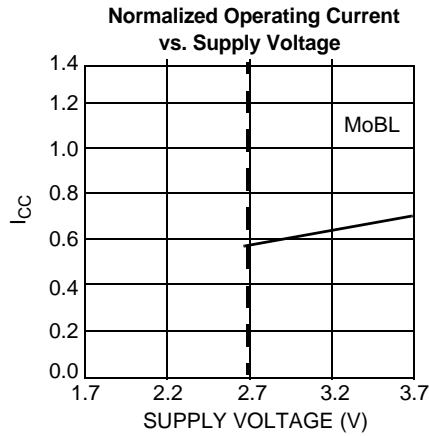
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[13, 18]</sup>**



**Write Cycle No. 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[19]</sup>**





**Typical DC and AC Characteristics**

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Write	Active ( $I_{CC}$ )

Ordering Information

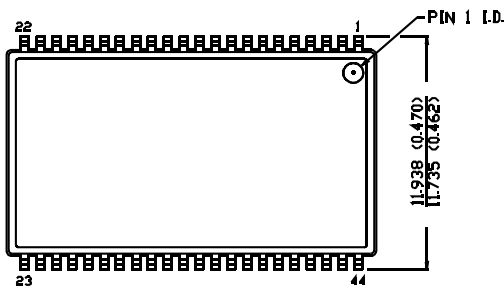
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62136VNLL-55ZXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial
	CY62136VNLL-55BAI	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA	
	CY62136VNLL-55ZSXA	51-85087	44-pin TSOP II (Pb-Free)	Automotive-A
70	CY62136VNLL-70ZXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial
	CY62136VNLL-70BAI	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA	Automotive-A
	CY62136VNLL-70BAXA	51-85096	48-Ball (7.00 mm x 7.00 mm) FBGA (Pb-Free)	
	CY62136VNLL-70ZSXA	51-85087	44-pin TSOP II (Pb-Free)	
	CY62136VNLL-70ZSXE	51-85087	44-pin TSOP II (Pb-Free)	Automotive-E

Please contact your local Cypress sales representative for availability of these parts

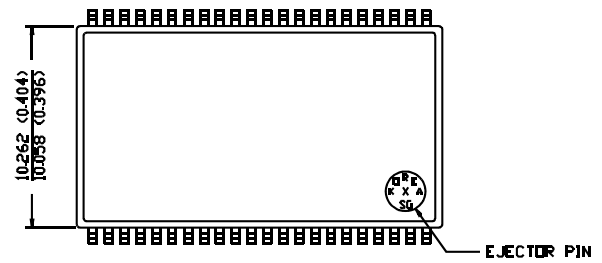
Package Diagrams

44-pin TSOP II (51-85087)

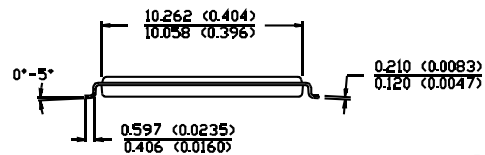
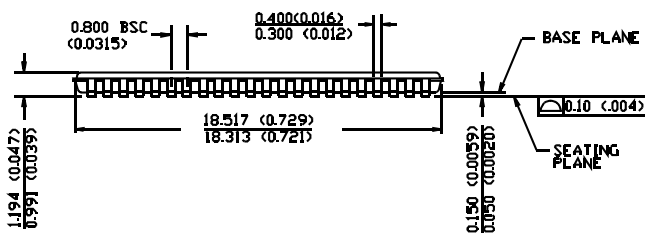
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



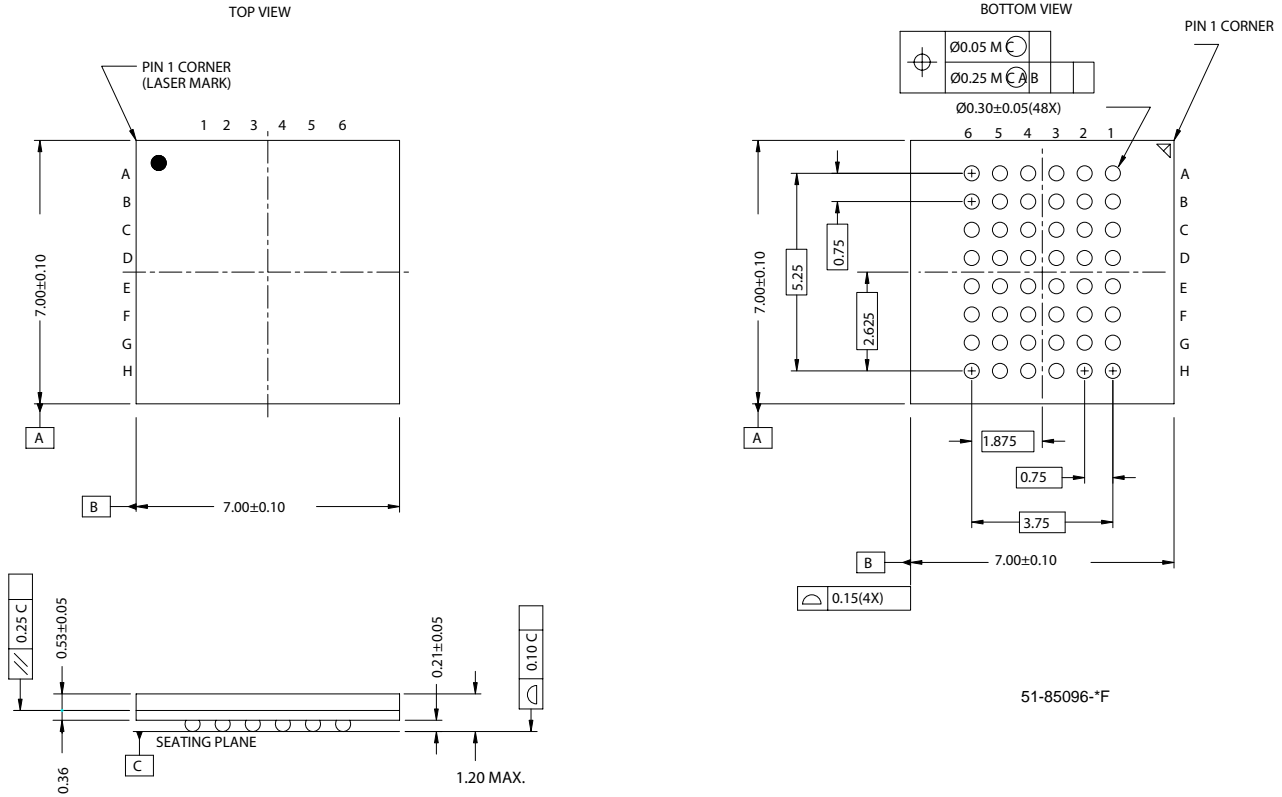
BOTTOM VIEW



51-85087-\*A

**Package Diagrams (continued)**

**48-Ball (7.00 mm x 7.00 mm) FBGA (51-85096)**



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**Document History Page**

<b>Document Title: CY62136VN MoBL<sup>®</sup> 2-Mbit (128K x 16) Static RAM</b> <b>Document Number: 001-06510</b>				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426503	See ECN	RXU	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table