# CY621472E30 MoBL®

# 4-Mbit (256 K × 16) Static RAM

## Features

- Very high speed: 45 ns
- Temperature range
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, $CE_2$, and $\overline{OE}$ Features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package
- Byte power down feature

## Functional Description

The CY621472E30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins ($I/O_0$ through $I/O_{15}$) are placed in a high impedance state when:

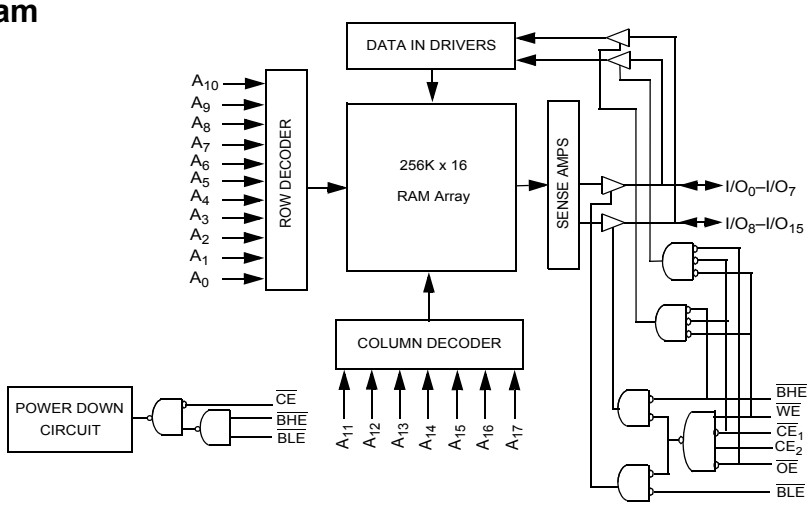
- Deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}_1$ LOW and $CE_2$ HIGH and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$) is written into the location specified on the address pins ($A_0$ through $A_{17}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{17}$).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and $CE_2$ HIGH and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $I/O_8$ to $I/O_{15}$. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

## Logic Block Diagram



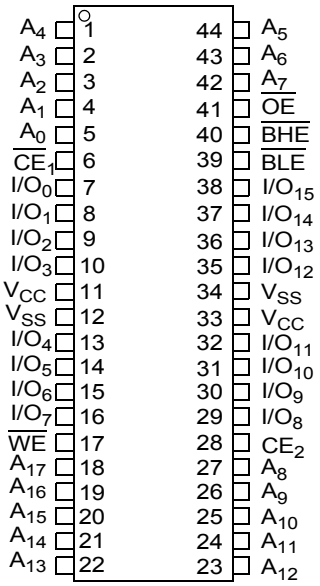
## Contents

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | | Min | Typ [1] | Max | | Typ [1] | Max | Typ [1] | Max | Typ [1] | Max |
| CY621472E30LL | Industrial | 2.2 | 3.0 | 3.6 | 45 | 2 | 2.5 | 15 | 20 | 1 | 7 |

## Pin Configuration

**Figure 1. 44-pin TSOP II pinout**




**Note**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to +3.9 V ($V_{CCmax}$ + 0.3 V)

DC Voltage Applied to Outputs in High Z State [2, 3] .....–0.3 V to 3.9 V ($V_{CCmax}$ + 0.3 V)

DC input voltage [2, 3] .....–0.3 V to 3.9 V ($V_{CCmax}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current..... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [4] |
|---|---|---|---|
| CY621472E30LL | Industrial | –40 °C to +85 °C | 2.2 V to 3.6 V |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [5] | Max | |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –0.1 mA | | 2.0 | – | – | V |
| | | $I_{OH}$ = –1.0 mA, $V_{CC} \geq$ 2.70 V | | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 0.1 mA | | – | – | 0.4 | V |
| | | $I_{OL}$ = 2.1 mA, $V_{CC}$ = 2.70 V | | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ = 2.2 V to 2.7 V | | 1.8 | – | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 2.2 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | $V_{CC}$ = 2.2 V to 2.7 V | | –0.3 | – | 0.6 | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | –0.3 | – | 0.8 | V |
| $I_{IX}$ | Input leakage current | GND $\leq V_I \leq V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | GND $\leq V_O \leq V_{CC}$, Output Disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | f = $f_{max}$ = $1/t_{RC}$ | $V_{CC}$ = $V_{CC(max)}$, $I_{OUT}$ = 0 mA, CMOS levels | – | 15 | 20 | mA |
| | | f = 1 MHz | | – | 2 | 2.5 | |
| $I_{SB1}$ [6] | Automatic CE power-down current – CMOS inputs | $\overline{CE_1} \geq V_{CC}$ – 0.2 V, $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), $V_{CC}$ = 3.60 V | | – | 1 | 7 | µA |
| $I_{SB2}$ [6] | Automatic CE Power down current – CMOS inputs | $\overline{CE_1} \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, $V_{CC}$ = 3.60 V | | – | 1 | 7 | µA |

**Notes**

2. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = $V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
4. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after $V_{CC}$ stabilization.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C.
6. Chip enables ($\overline{CE_1}$ and $CE_2$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.

## Capacitance

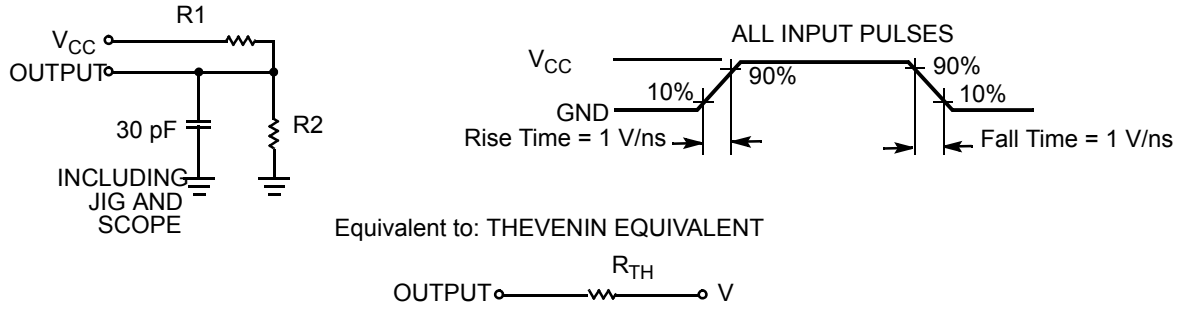
| Parameter [7] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [7] | Description | Test Conditions | 44-pin TSOP II Package | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 77 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 13 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**




| Parameters | 2.50 V | 3.0 V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

**Note**
7. Tested initially and after any design or process changes that may affect these parameters.

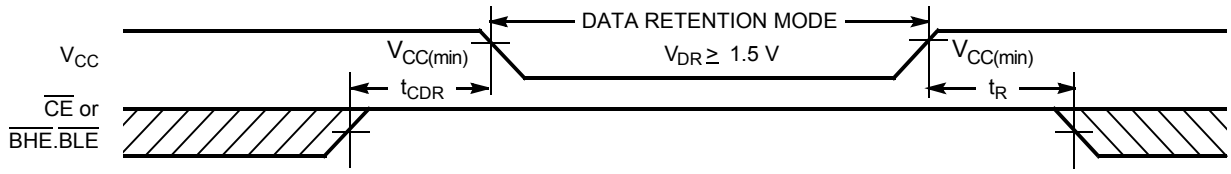
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ [8] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | 1.5 | – | – | V |
| $I_{CCDR}$[9] | Data retention current | $V_{CC}$ = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 0.8 | 7 | µA |
| $t_{CDR}$ [10] | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R$ [11] | Operation recovery time | | 45 | – | – | ns |

## Data Retention Waveform

**Figure 3. Data Retention Waveform** [12, 13]




**Notes**

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25 °C.
9. Chip enables ($\overline{CE}_1$ and $CE_2$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
12. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and $CE_2$ such that when $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range

| Parameter [14] | Description | 45 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 45 | – | ns |
| $t_{AA}$ | Address to data valid | – | 45 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to data valid | – | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [15] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [15, 16] | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to Low Z [15] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH/$CE_2$ LOW to High Z [15, 16] | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to Power-up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH/$CE_2$ LOW to Power-down | – | 45 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to data valid | – | 45 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [15, 17] | 5 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [15, 16] | – | 18 | ns |
| **Write Cycle** [18, 19] | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW/$CE_2$ HIGH to Write End | 35 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 35 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [15, 16] | – | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [15] | 10 | – | ns |

**Notes**

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the Figure 2 on page 5.
15. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
16. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
17. If both byte enables are together, this value is 10 ns.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for WRITE Cycle 4 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [20, 21]

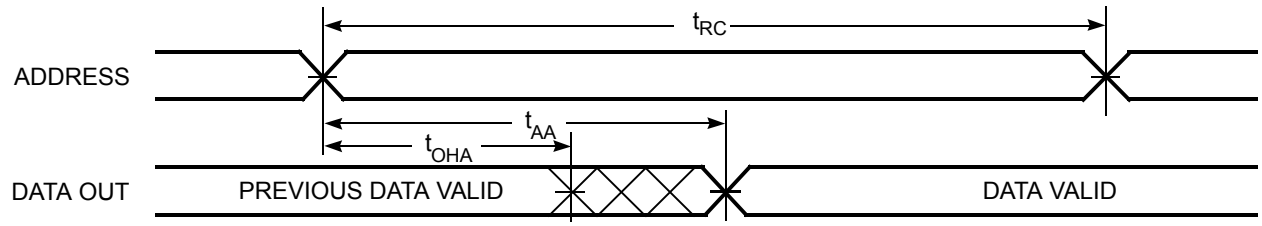
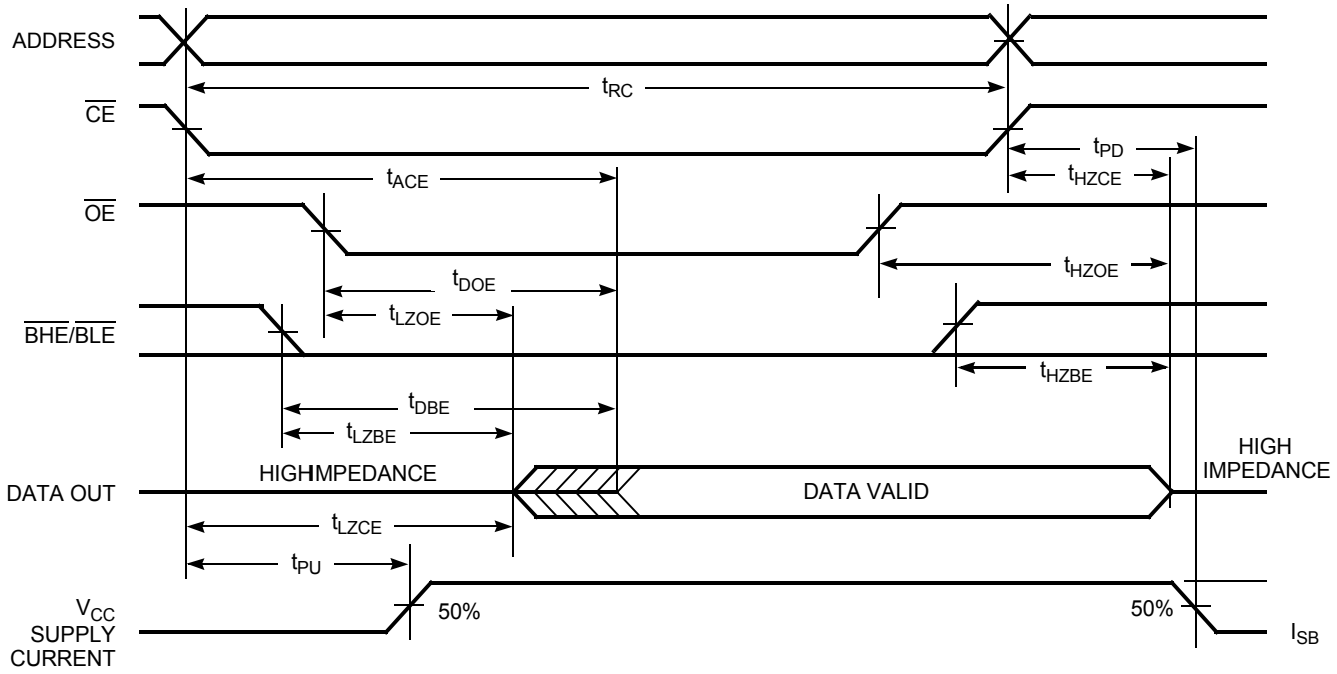



**Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [21, 22, 23]




**Notes**
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$.
21. $\overline{WE}$ is HIGH for read cycle.
22. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and $CE_2$ such that when $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
23. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 (WE Controlled)** [24, 25, 26, 27]

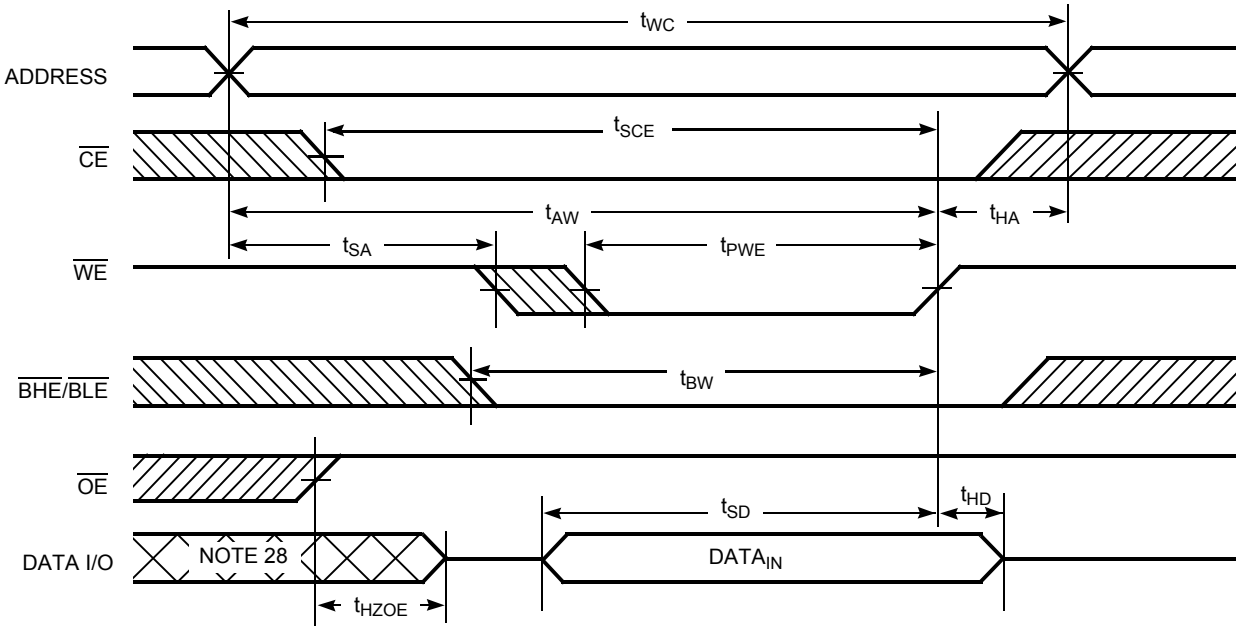
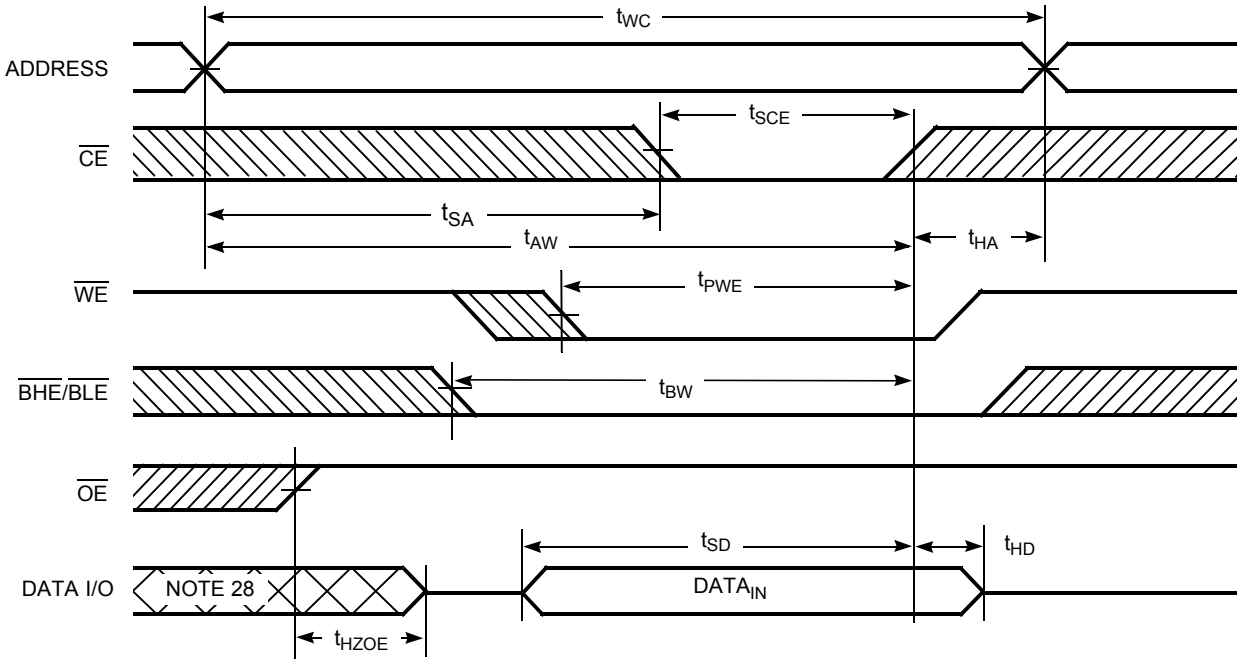



**Figure 7. Write Cycle No. 2 (CE Controlled)** [24, 25, 26, 27]




**Notes**

24. $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and $CE_2$ such that when $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW)** [29, 30, 31]

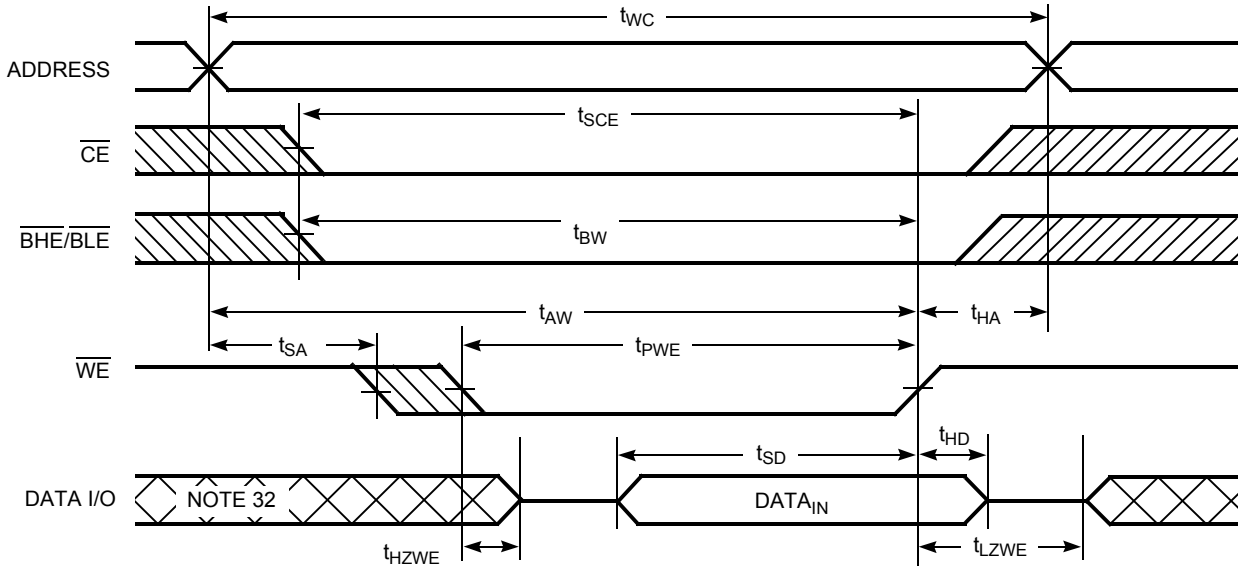
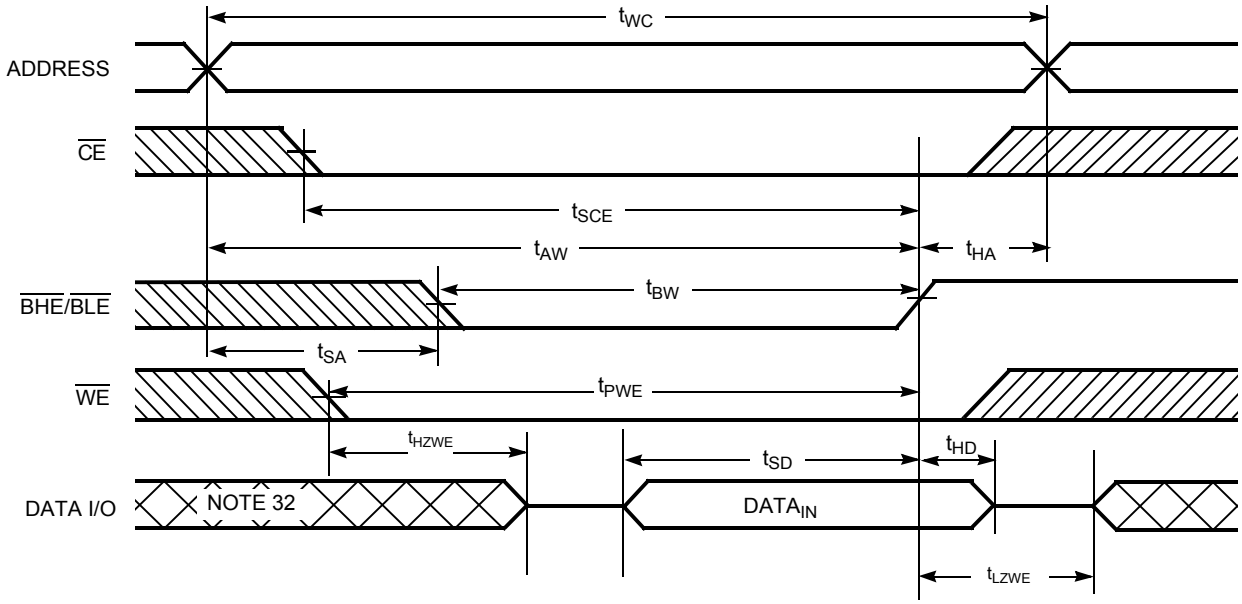



**Figure 9. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)** [29, 30]




**Notes**
29. CE refers to the internal logical combination of $\overline{CE}_1$ and $CE_2$ such that when $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, CE is LOW. For all other cases CE is HIGH.
30. If CE goes HIGH simultaneously with WE = $V_{IH}$, the output remains in a high impedance state.
31. The minimum write cycle pulse width should be equal to the sum of $t_{HZWE}$ and $t_{SD}$.
32. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

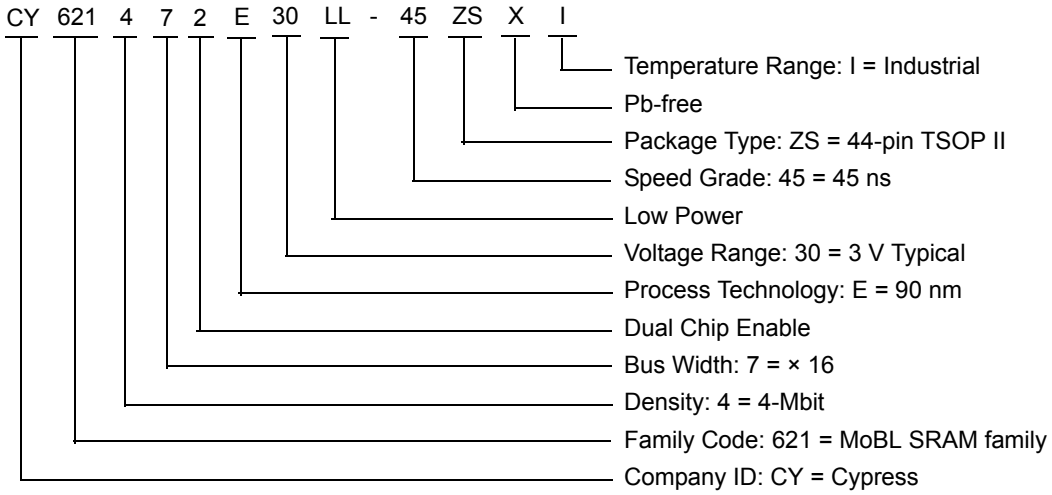
| $\overline{CE1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | I/Os | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X[33] | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X[33] | L | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X[33] | X[33] | X | X | H | H | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | H | L | L | L | Data out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | H | L | Data out ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | H | Data out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | H | L | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | H | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | H | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data in ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | H | L | X | H | L | Data in ($I/O_0$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | H | L | X | L | H | Data in ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Write | Active ($I_{CC}$) |

**Note**
33. The 'X' (Don't care) state for the chip enables ($\overline{CE}_1$ and $CE_2$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

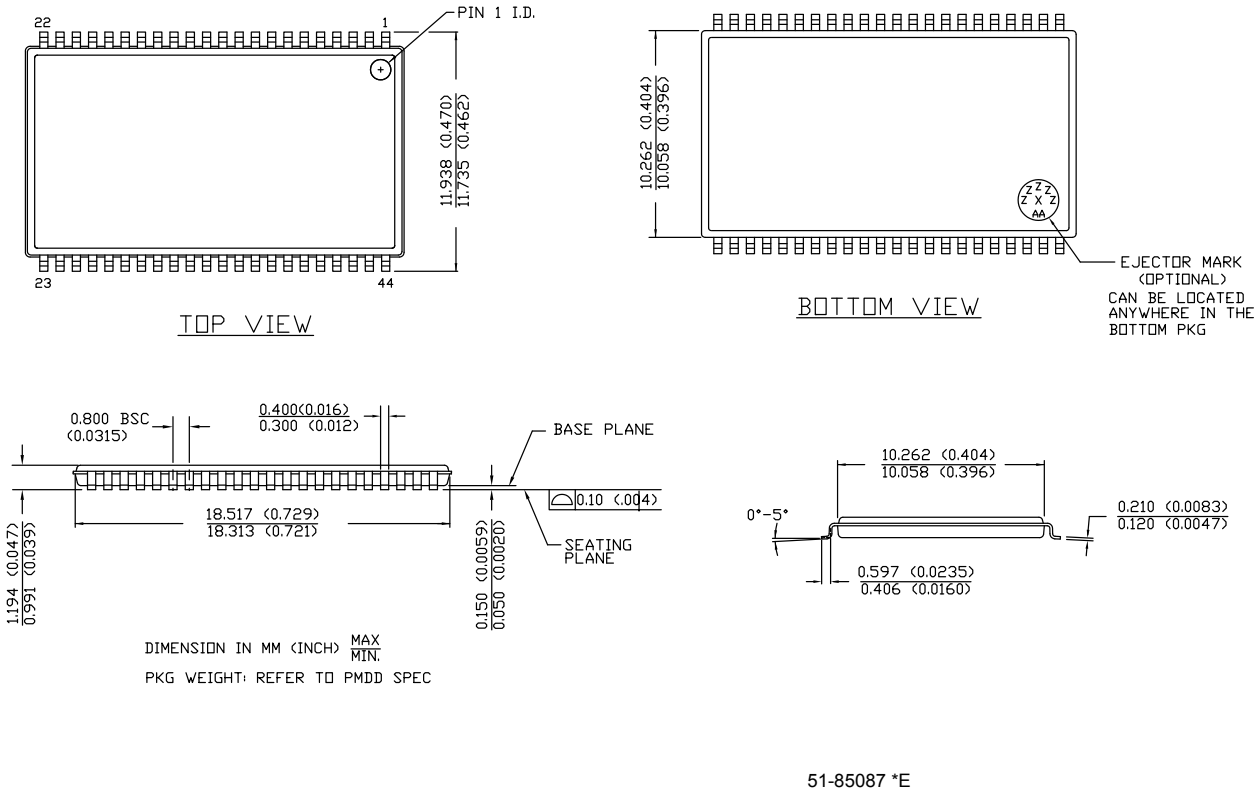
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY621472E30LL-45ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | Industrial |

### Ordering Code Definitions



## Package Diagram

**Figure 10. 44-pin TSOP II Package Outline, 51-85087**




51-85087 *E

## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY621472E30 MoBL®, 4-Mbit (256 K × 16) Static RAM<br>Document Number: 001-67798 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 3184883 | RAME | 03/01/2011 | New data sheet. |
| *A | 3223503 | RAME | 04/15/2011 | Overline bar $CE_2$ removed from the Truth table.<br>Updated all notes as per template. |
| *B | 3261142 | RAME | 05/19/2011 | Updated Switching Characteristics (corrected the Min value of $t_{LZBE}$ parameter).<br>Added Ordering Information and Ordering Code Definitions.<br>Added Acronyms and Units of Measure. |
| *C | 3365953 | AJU | 09/08/2011 | Changed datasheet status from Preliminary to Final.<br>Updated 44-pin TSOP II package spec. |
| *D | 3414567 | TAVA | 10/20/2011 | Replaced CY62147EV30 with CY621472E30 through out the data sheet. |
| *E | 4331825 | NILE | 04/03/2014 | Updated Switching Characteristics:<br>Added Note 19 and referred the same note in “Write Cycle”.<br>Updated Switching Waveforms:<br>Added Note 31 and referred the same note in Figure 8.<br>Updated Package Diagram:<br>spec 51-85087 – Changed revision from *D to *E.<br>Updated in new template.<br>Completing Sunset Review. |
| *F | 4573121 | NILE | 11/18/2014 | Added related documentation hyperlink in page 1. |

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