

256K x 16 Static RAM

Features

- **High Speed**
 - 55 ns and 70 ns availability
- **Voltage range:**
 - CY62147CV25: 2.2V–2.7V
 - CY62147CV30: 2.7V–3.3V
 - CY62147CV33: 3.0V–3.6V
- **Pin Compatible with CY62147V**
- **Ultra-low active power**
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 5.5 mA @ f = f_{max} (70 ns speed)
- **Low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The CY62147CV25/30/33 are high-performance CMOS static RAMs organized as 256K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that signifi-

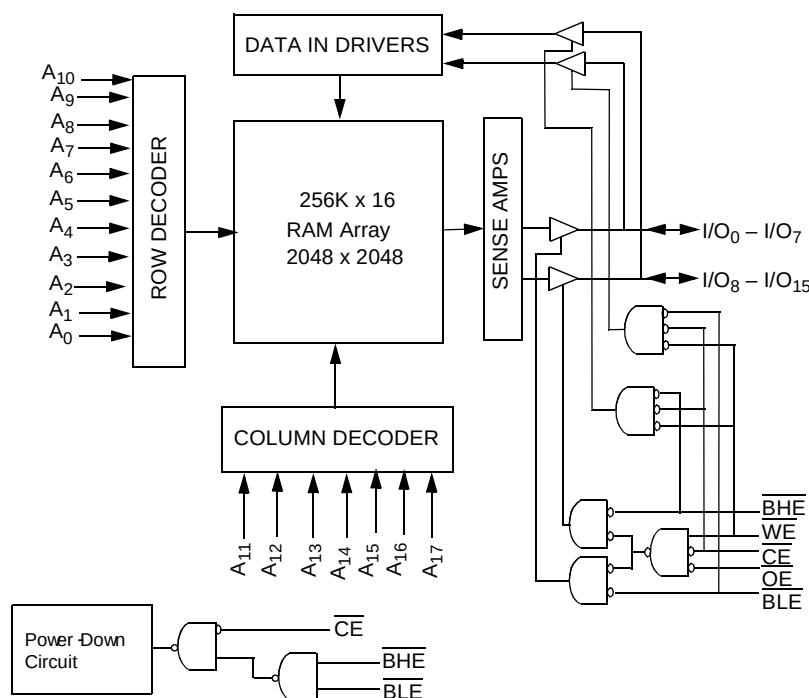
cantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH or both $\overline{\text{BLE}}$ and $\overline{\text{BHE}}$ are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

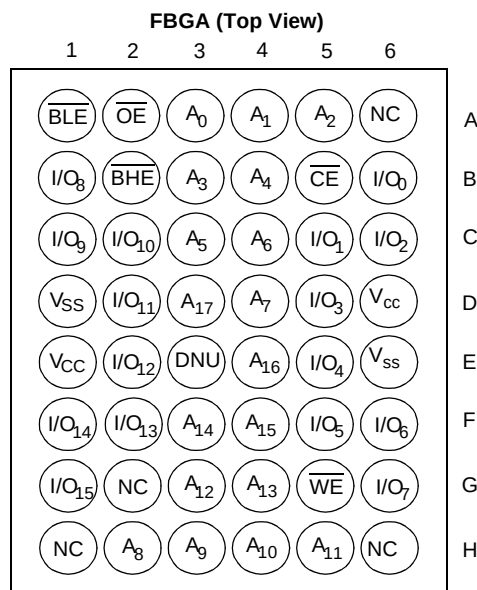
Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147CV25/30/33 are available in a 48-ball FBGA package.

Logic Block Diagram



Pin Configuration^[1, 2]



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential ... -0.5V to V_{CCmax} + 0.5V

DC Voltage Applied to Outputs

in High Z State^[3] -0.5V to V_{CC} + 0.3V

DC Input Voltage^[3] -0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62147CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62147CV30			2.7V to 3.3V
CY62147CV33			3.0V to 3.6V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating, I _{CC}				Standby (I _{SB2})	
					f = 1 MHz		f = f _{max}			
	V _{CC(min.)}	V _{CC(typ.)} ^[4]	V _{CC(max.)}		Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.
CY62147CV25	2.2V	2.5V	2.7V	55 ns	1.5 mA	3 mA	7 mA	15 mA	5 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62147CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	7 mA	15 mA	7 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62147CV33	3.0V	3.3V	3.6V	55 ns	1.5 mA	3 mA	7 mA	15 mA	8 μA	20 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		

Notes:

- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62147CV25-55			CY62147CV25-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 2.2V	2.0			2.0			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA V _{CC} = 2.2V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		1.8		V _{CC} + 0.3V	1.8		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.6	-0.3		0.6	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 2.7V I _{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = f _{max} (Address and Data Only), f=0 (OE,WE,BHE and BLE)		5	15		5	15	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} = 2.7V							

Parameter	Description	Test Conditions	CY62147CV30-55			CY62147CV30-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 2.7V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 2.7V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 3.3V I _{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = f _{max} (Address and Data Only), f=0 (OE,WE,BHE and BLE)		7	15		7	15	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} = 3.3V							

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62147CV33-55			CY62147CV33-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 3.0V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 3.0V			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 3.6V I _{OUT} = 0 mA CMOS Levels		7	15		5.5	12	mA
		f = 1 MHz		1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = f _{max} (Address and Data Only), f=0 (OE,WE,BHE and BLE)		8	20		8	20	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} = 3.6V							

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	6	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ.)}	8	pF

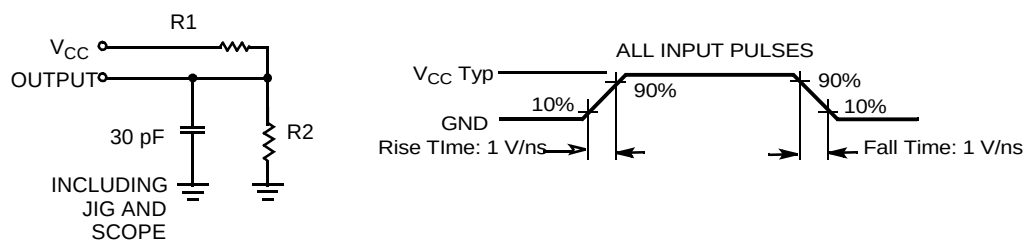
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[5]		Θ _{JC}	16	°C/W

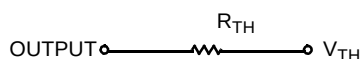
Note:

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

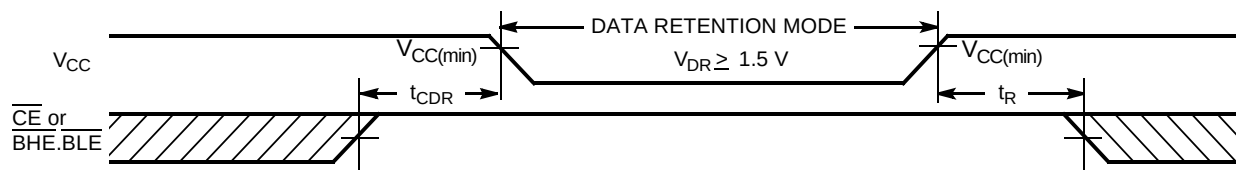


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	KΩ
R2	15.4	1.550	1.374	KΩ
R _{TH}	8	0.645	0.645	KΩ
V _{TH}	1.20	1.75	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5		V _{CCmax}	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		3	10	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time		0			ns
t _R ^[6]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform^[7]



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Note:

- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} > 100μs or stable at V_{CC(min.)} > 100 μs.
- BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics Over the Operating Range^[8]

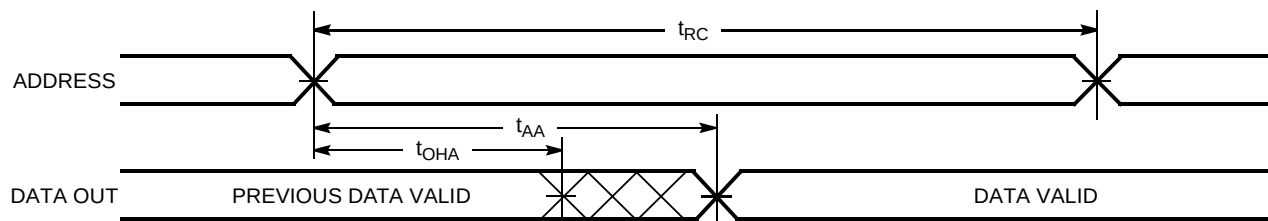
Parameter	Description	55 ns		70 ns		Unit
		Min	Max	Min	Max	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[9]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[9, 11]		20		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[9]	10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[9, 11]		20		25	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t _{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
t _{LZBE} ^[10]	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z ^[9]	5		5		ns
t _{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z ^[9, 11]		20		25	ns
WRITE CYCLE ^[12]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t _{BW}	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width	50		60		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[9, 11]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[9]	5		5		ns

Notes:

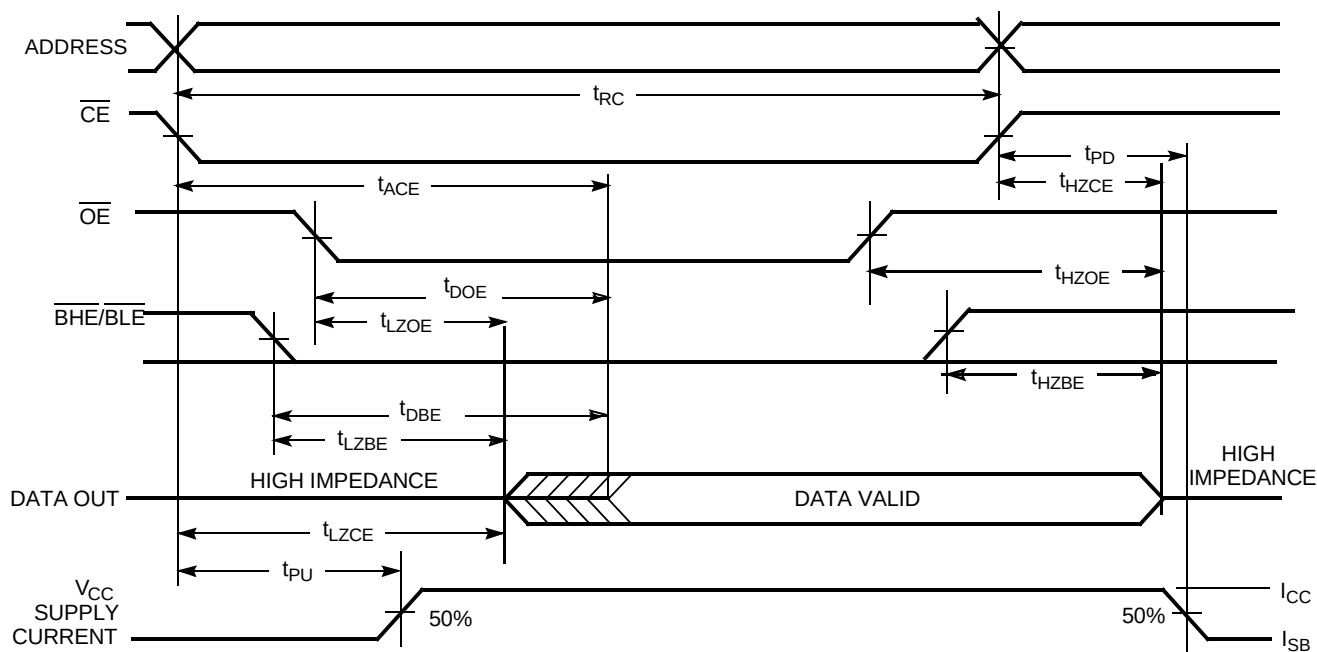
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- If both byte enables are toggled together this value is 10 ns.
- t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) ^[13, 14]

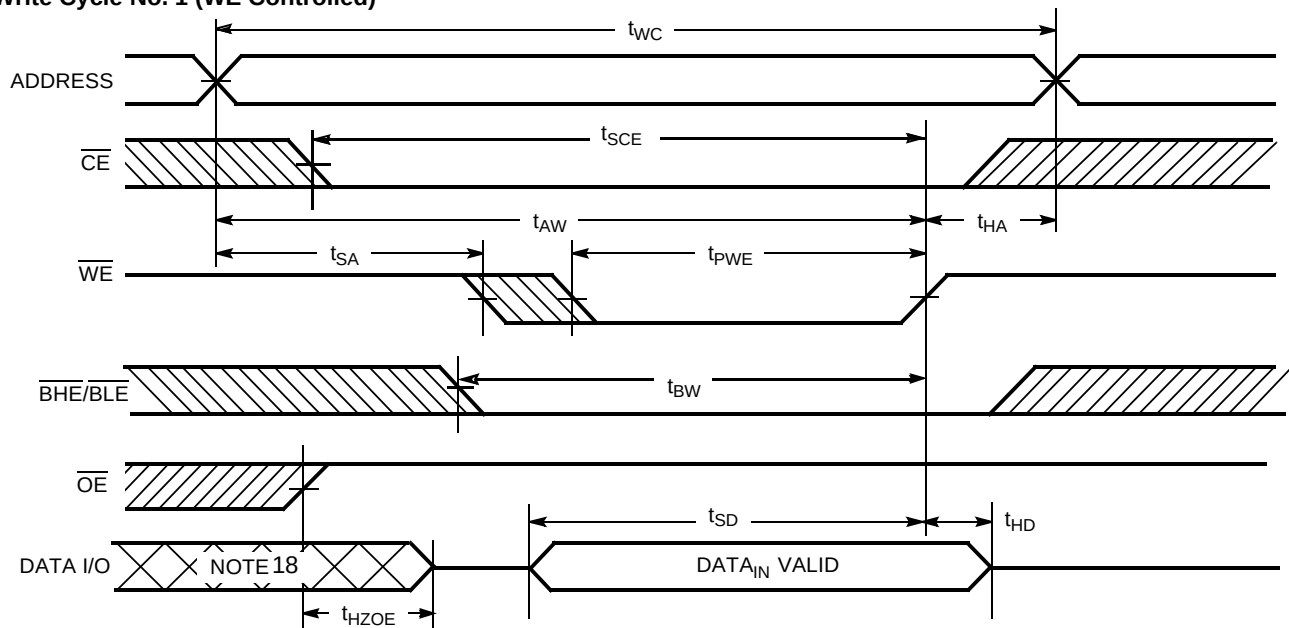
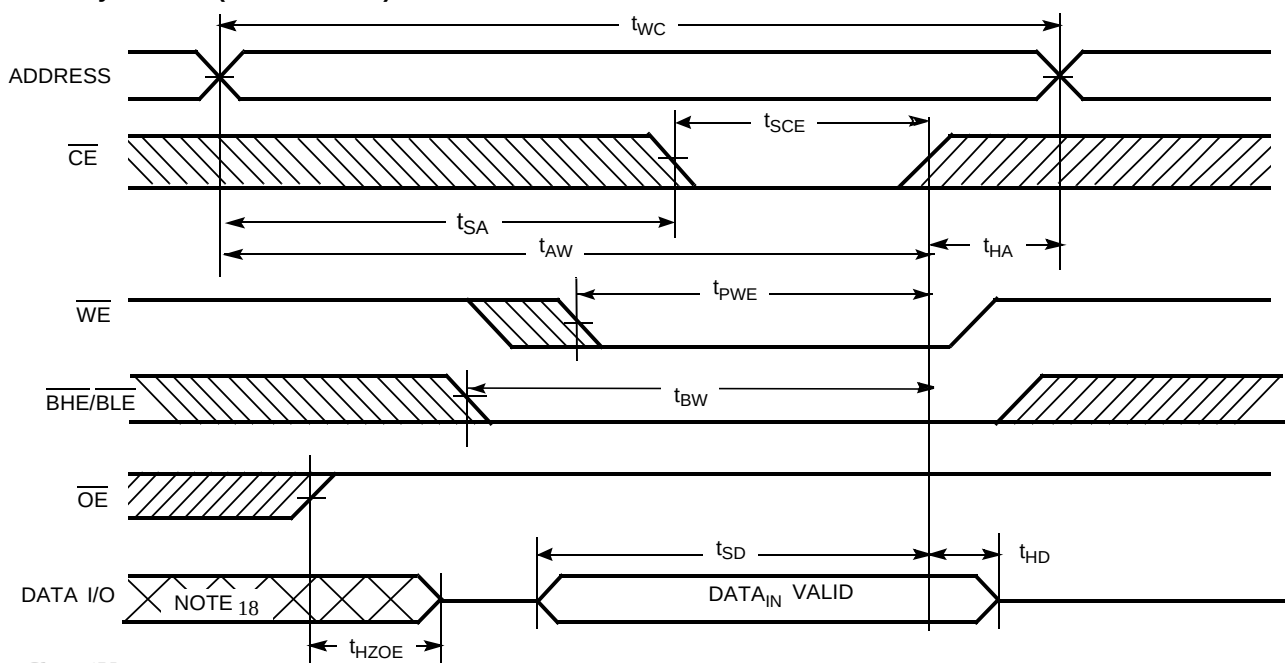


Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) ^[14, 15]



Notes:

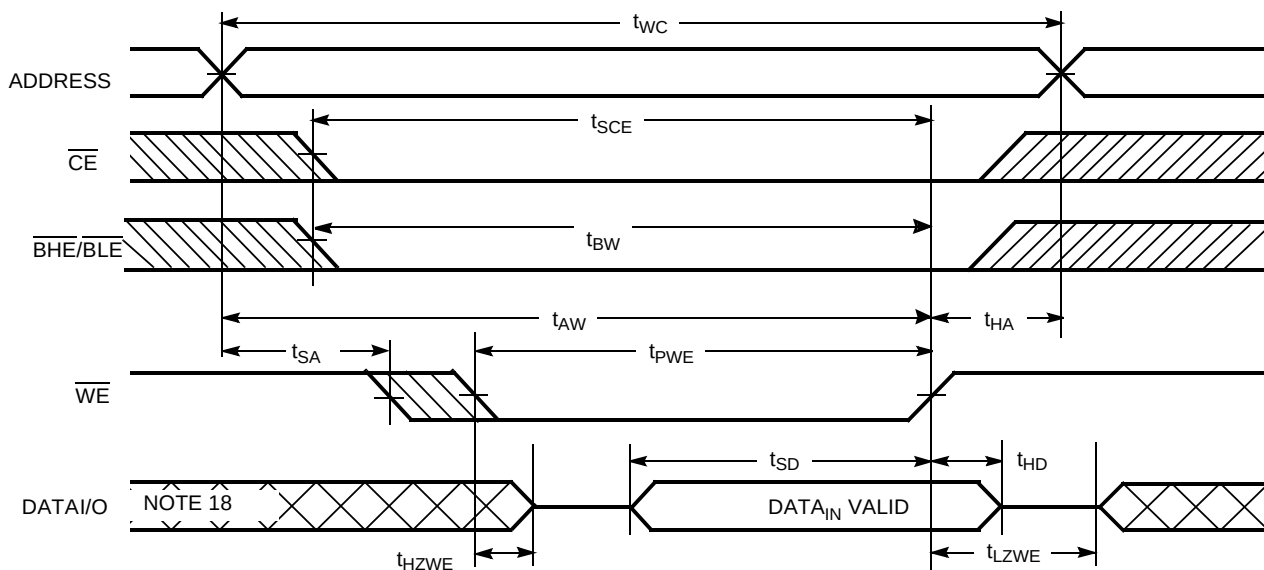
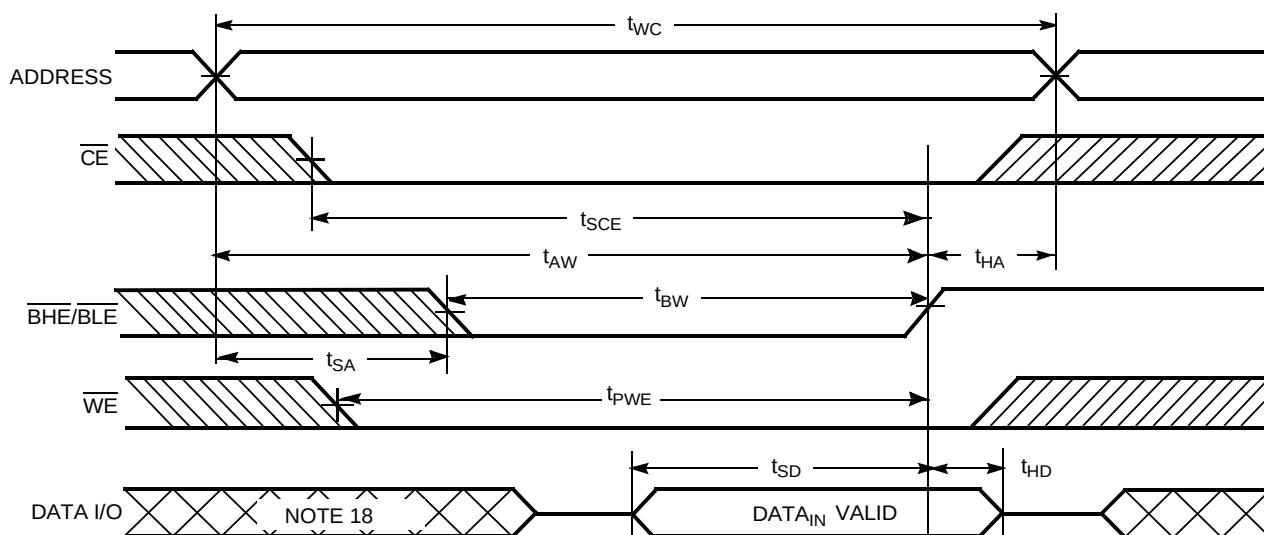
13. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}$ = V_{IL} , $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}}$ = V_{IL} .
14. $\overline{\text{WE}}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (WE Controlled) ^[12, 16, 17]

Write Cycle No. 2 (CE Controlled) ^[12, 16, 17]


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Notes:

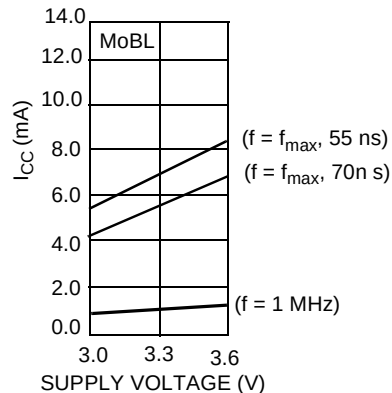
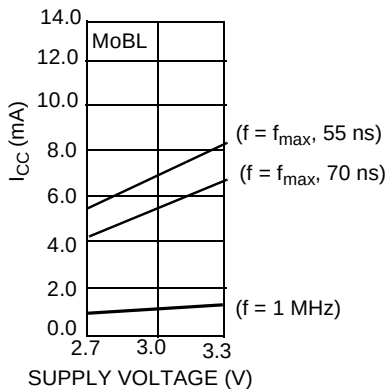
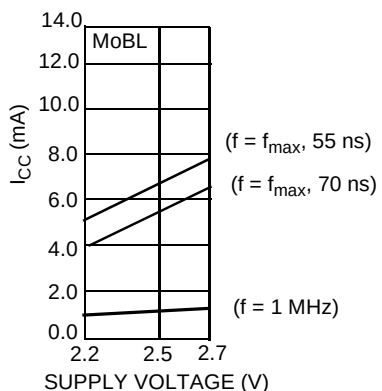
16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17]

Write Cycle No. 4 ($\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17]


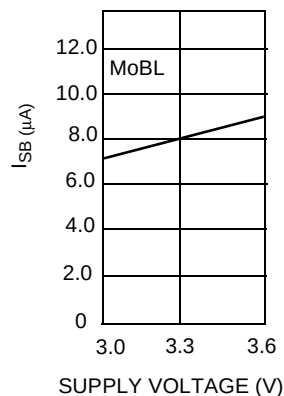
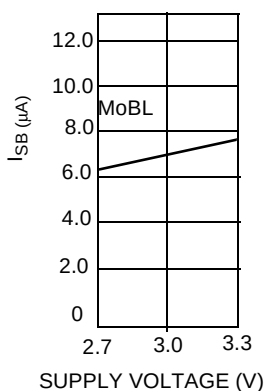
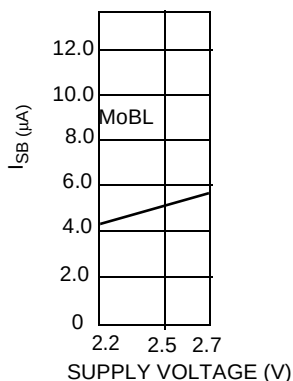
Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.)

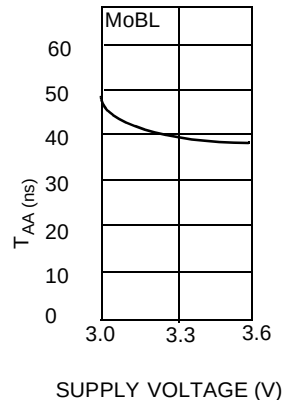
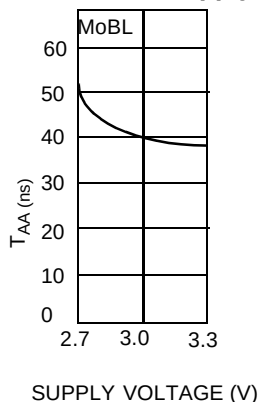
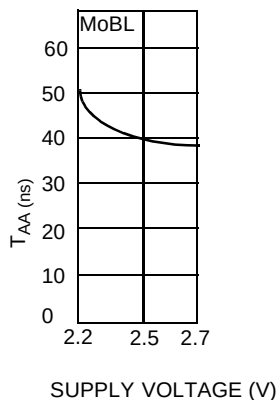
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

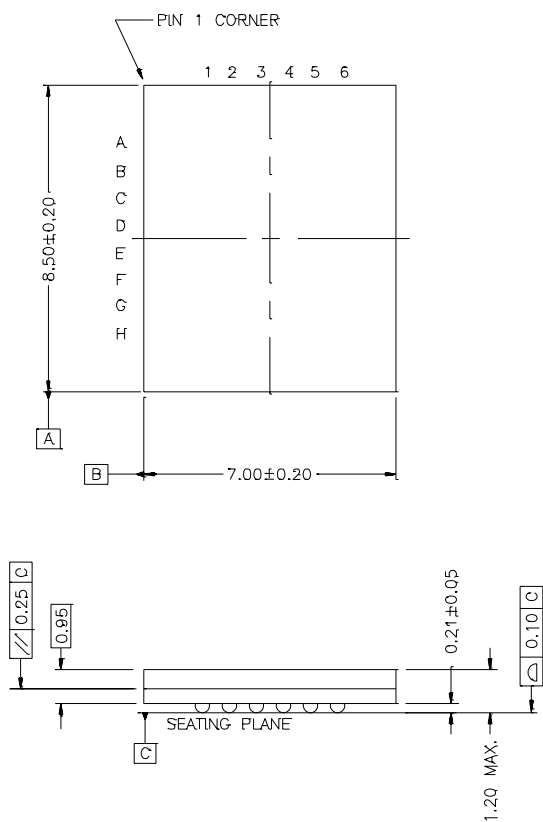
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV25LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62147CV25LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV30LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV30LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV33LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV33LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62147CV25LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV25LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV30LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV30LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62147CV33LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV33LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

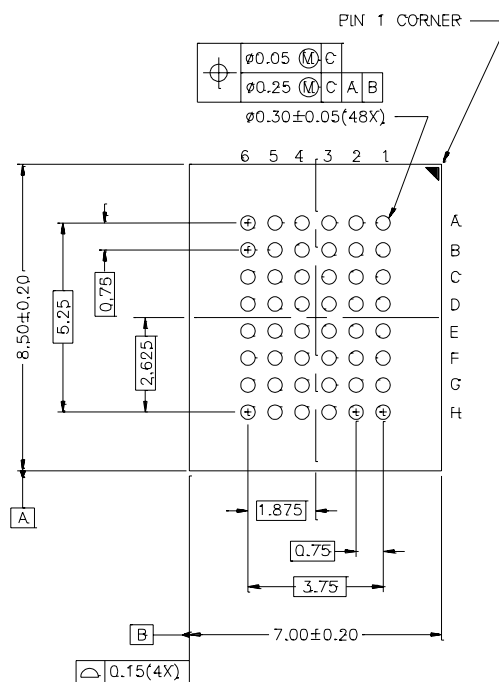
Package Diagrams

48-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA48B

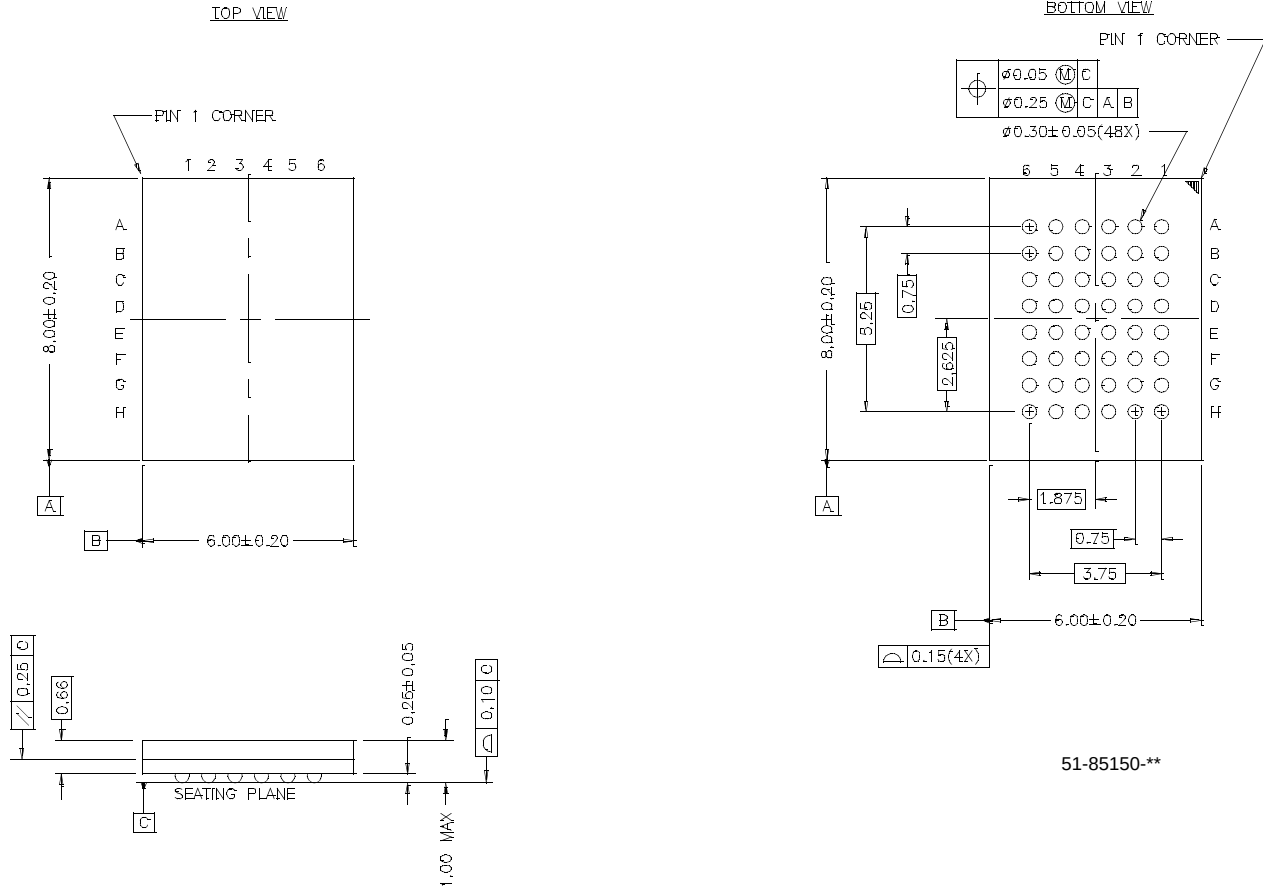
TOP VIEW



BOTTOM VIEW



51-85106-°C

Package Diagrams (continued)
48-Lead VFBGA (6 mm x 8 mm x 1 mm) BV48A


51-85150-**

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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112394	01/31/02	GAV	Converted from Spec# 38-01123 to 38-05202. Advance Information to Final
*A	114216	05/01/02	MGN/GUG	Improved Typical & Max Icc values