CY62148E MoBL®

4-Mbit (512K × 8) Static RAM

Features

- Very high speed: 45 ns
- Voltage range: 4.5 V to 5.5 V
- Pin compatible with CY62148B
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA (Industrial)
- Ultra low active power
  - Typical active current: 2.0 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC)[1] packages

Functional Description

The CY62148E is a high performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), Outputs are disabled ($\overline{OE}$ HIGH), or during an active Write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

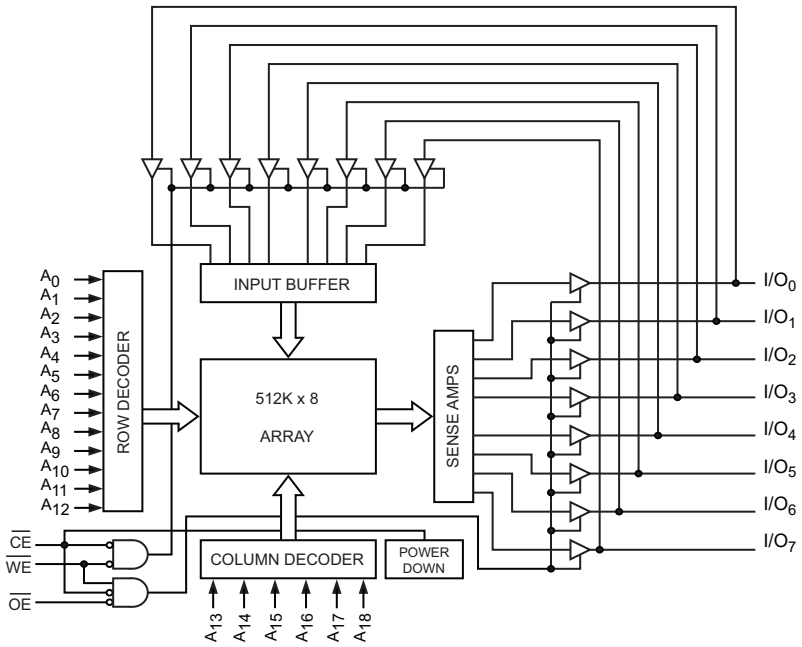
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

Logic Block Diagram



Note
1. SOIC package is available only in 55 ns speed bin.

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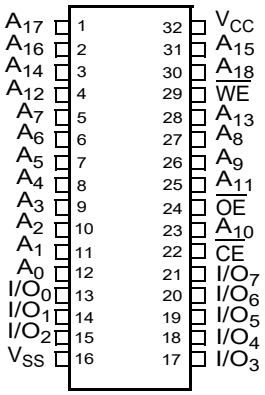
Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout [2]

Top View



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62148ELL	TSOP II	Industrial	4.5	5.0	5.5	45	2	2.5	15	20	1	7
CY62148ELL	SOIC	Industrial / Automotive-A	4.5	5.0	5.5	55	2	2.5	15	20	1	7

Notes
2. SOIC package is available only in 55 ns speed bin.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC voltage applied to outputs in high Z state [4, 5] ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC input voltage [4, 5] ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62148E	Industrial / Automotive-A	–40 °C to +85 °C	4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		45 ns			55 ns [7]			Unit
				Min	Typ [8]	Max	Min	Typ [8]	Max	
V_{OH} [9]	Output HIGH voltage	V_{CC} = 4.5 V, I_{OH} = –1 mA		2.4	–	–	2.4	–	–	V
		V_{CC} = 5.5 V, I_{OH} = –0.1 mA		–	–	3.4 [8]	–	–	3.4 [8]	V
V_{OL}	Output LOW voltage	I_{OL} = 2.1 mA		–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 4.5 V to 5.5 V		2.2	–	V_{CC} + 0.5	2.2	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage	V_{CC} = 4.5 V to 5.5 V	For TSOPII package	–0.5	–	0.8	–	–	–	V
			For SOIC package	–	–	–	–0.5	–	0.6 [10]	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	–	15	20	mA
		f = 1 MHz		–	2	2.5	–	2	2.5	
I_{SB2} [11]	Automatic $\overline{CE}$ power-down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	1	7	–	1	7	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns for I ≤ 30 mA.
5. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
7. SOIC package is available only in 55 ns speed bin.
8. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Please note that the maximum V_{OH} limit for this device does not exceed minimum CMOS V_{IH} of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
10. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.6 V. This is applicable to SOIC package only.
11. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

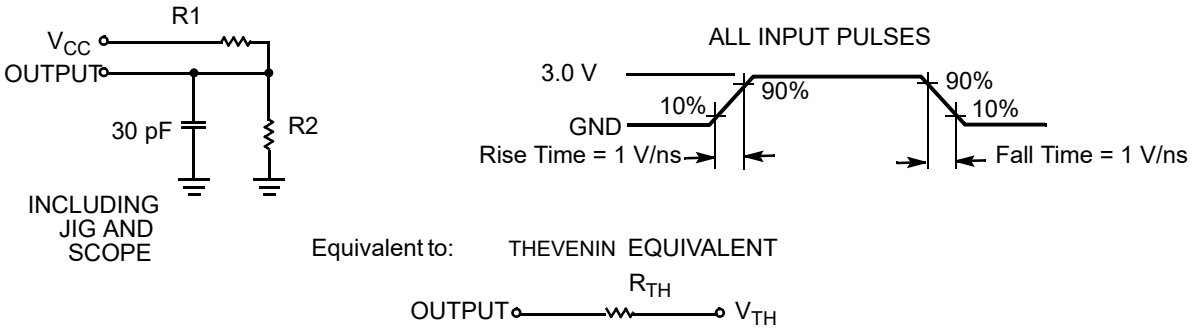
Parameter [12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.57	59.10	°C/W
Θ_{JC}	Thermal resistance (junction to case)		25.01	12.19	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter [12]	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Note
12. Tested initially and after any design or process changes that may affect these parameters.

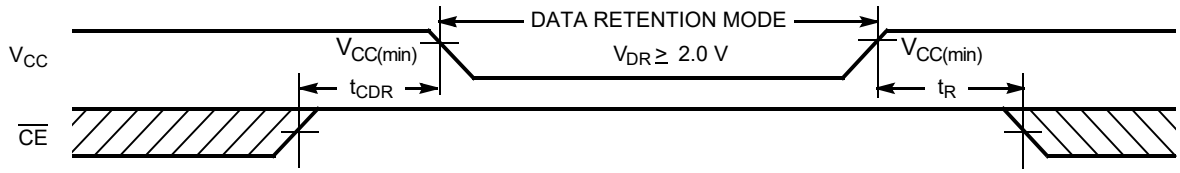
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ [13]	Max	Unit
V_{DR}	V_{CC} for data retention			2	–	–	V
I_{CCDR}[14]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial / Automotive-A	–	1	7	µA
t_{CDR}	Chip deselect to data retention time			0	–	–	ns
t_R[15]	Operation recovery time			45/55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
13. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
14. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.

Switching Characteristics

Over the operating range

Parameter [16, 17]	Description	45 ns		55 ns [18]		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [19]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [19, 20]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [19]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [19, 20]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle [21, 22]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [19, 20]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [19]	10	–	10	–	ns

Notes

16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
18. SOIC package is available only in 55 ns speed bin.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. The internal wre.ite time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
22. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [23, 24]

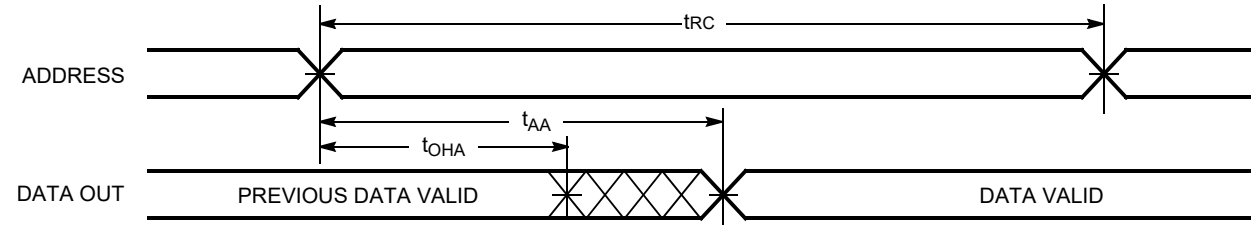


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [24, 25]

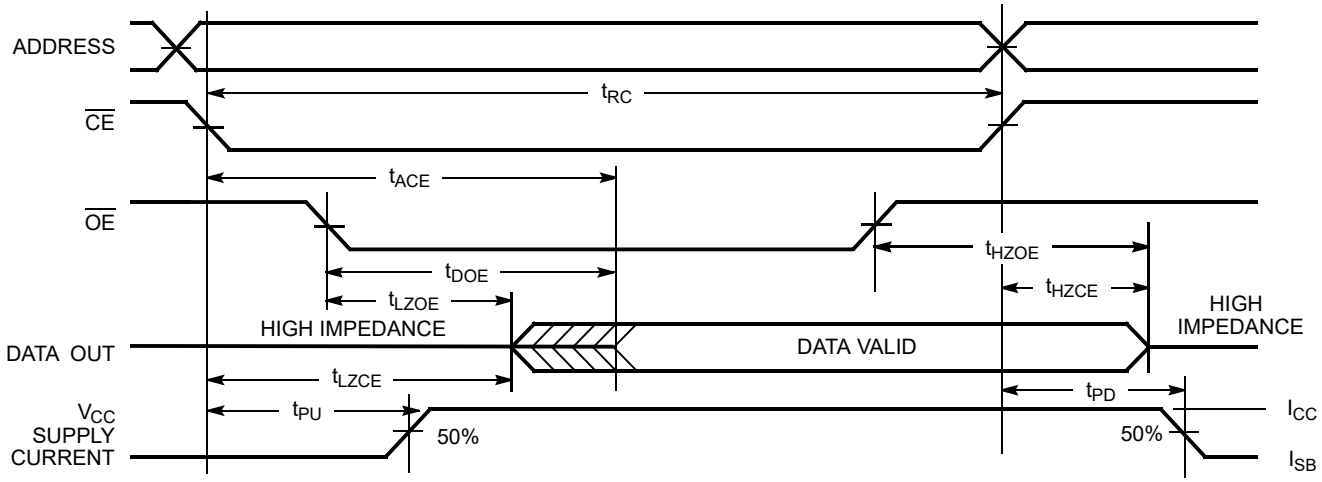
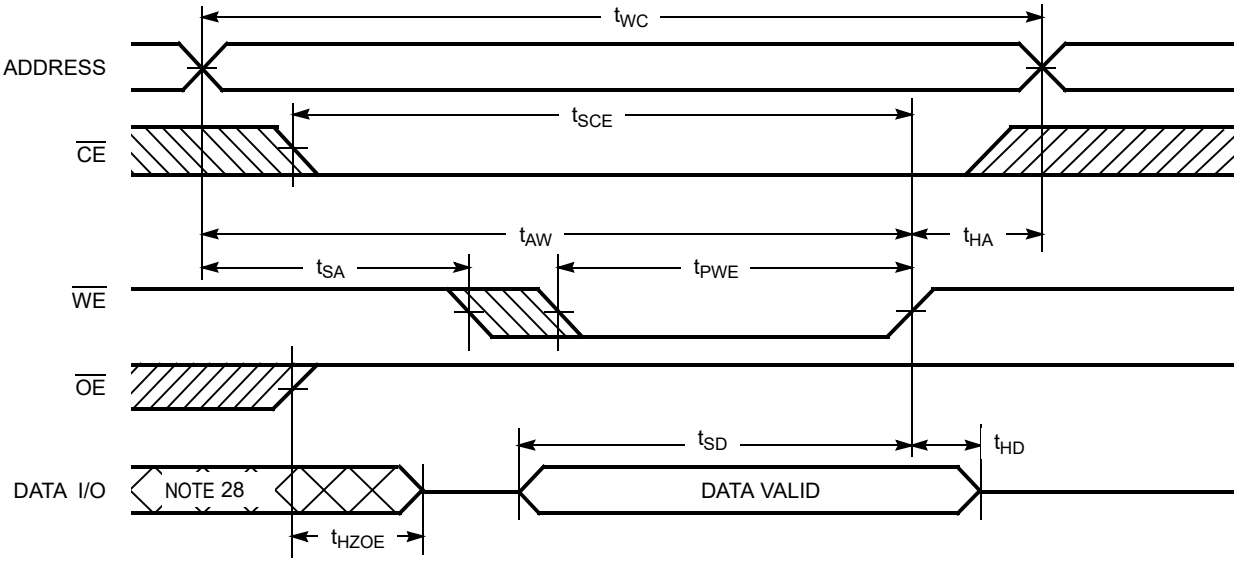


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [26, 27]



Notes
23. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
24. $\overline{WE}$ is HIGH for read cycles.
25. Address valid before or similar to $\overline{CE}$ transition LOW.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [29, 30]

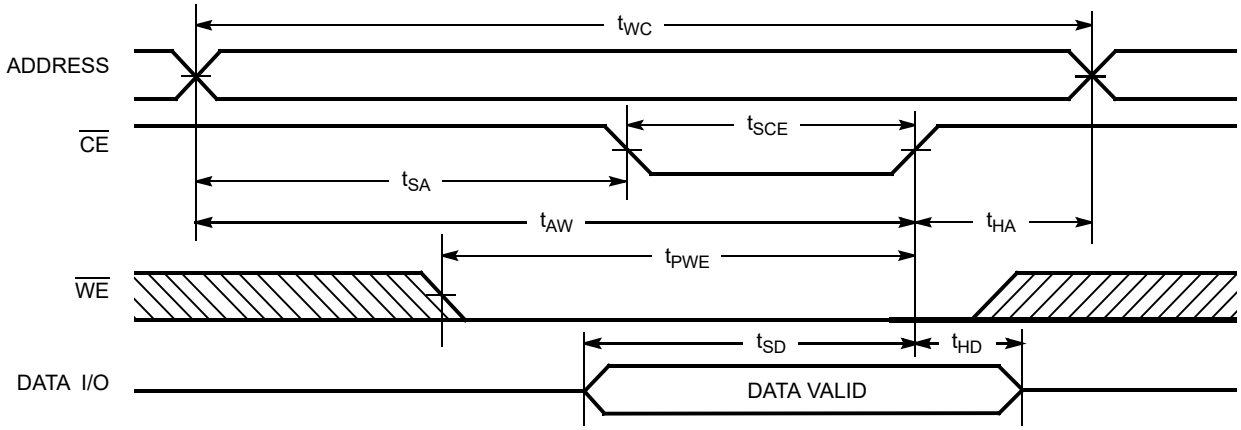
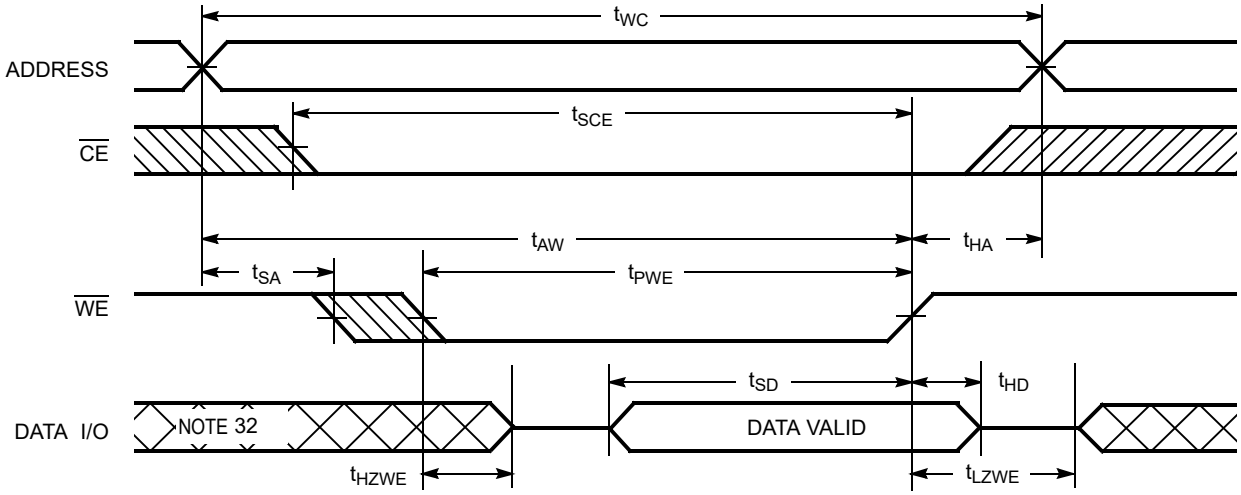


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [30, 31]



Notes
29. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
30. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
31. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
32. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H [33]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note
33. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Ordering Information

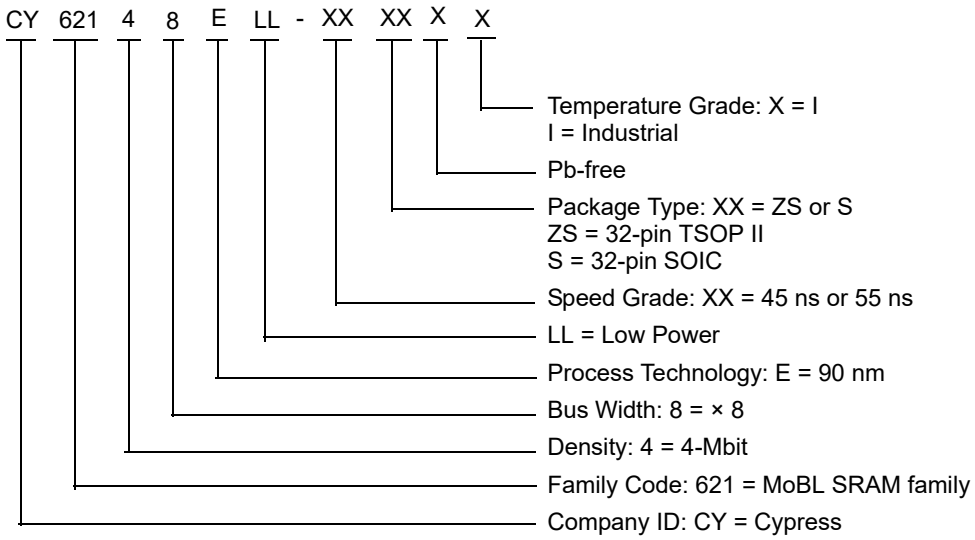
Table 1 lists the CY62148E MoBL® key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key features and Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148ELL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
55	CY62148ELL-55SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

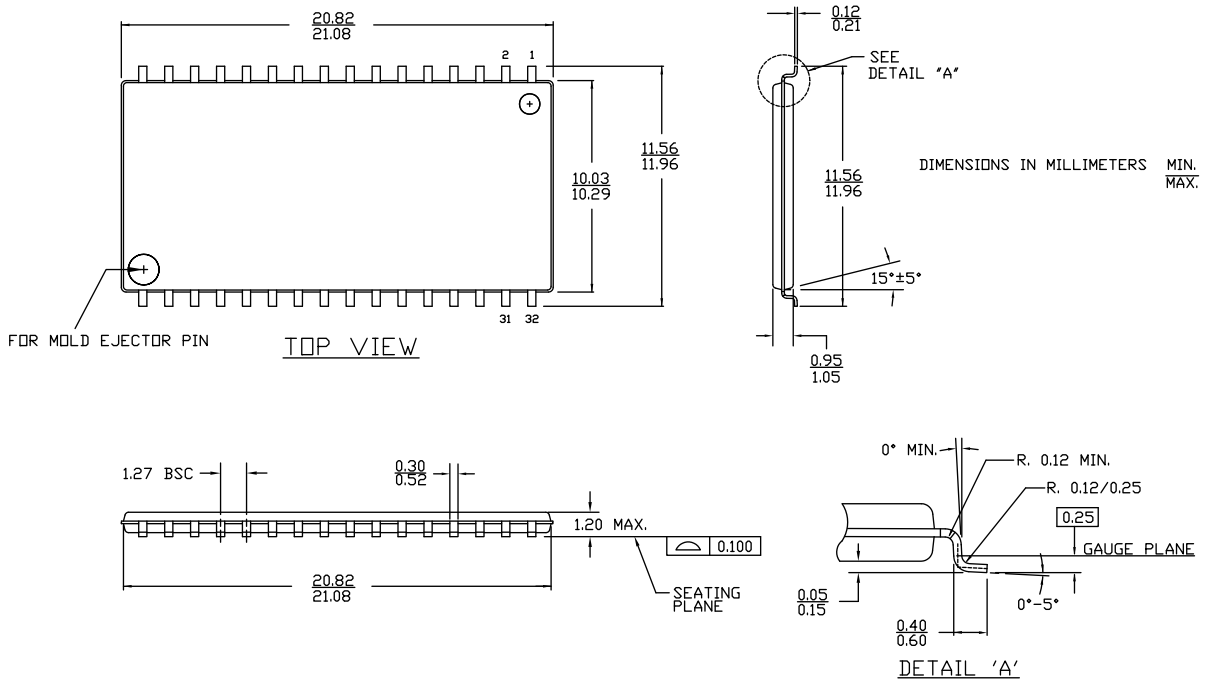
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

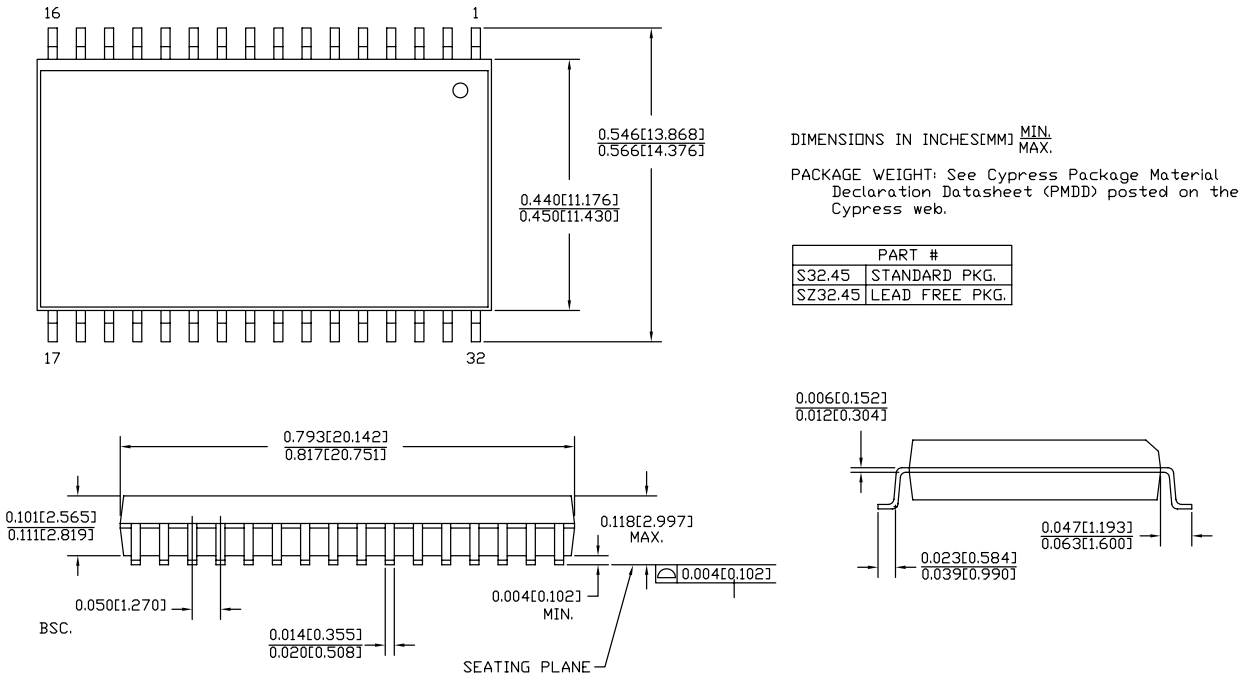
Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) Package Outline, 51-85095



51-85095 *D

Package Diagrams (continued)

Figure 10. 32-pin SOIC (450 Mils) Package Outline, 51-85081



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
MoBL	More Battery Life
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148E MoBL®, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	201580	AJU	01/08/2004	New data sheet.
*A	249276	SYT	08/03/2004	Changed status from Advance Information to Preliminary. Updated Features (Added RTSOP II and removed FBGA Package). Updated Functional Description (Added RTSOP II and removed FBGA Package). Updated Pin Configurations (Added RTSOP II and removed FBGA Package). Updated Operating Range (Updated Note 6 (Changed V_{CC} stabilization time from 100 μs to 200 μs)). Updated Data Retention Characteristics (Changed maximum value of I_{CCDR} parameter from 2.0 μA to 2.5 μA; changed minimum value of t_R parameter from 100 μs to t_{RC} ns). Updated Switching Characteristics (Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns for both 35 ns and 45 ns speed bin; changed maximum value of t_{DOE} parameter from 15 ns to 18 ns for 35 ns speed bin; changed maximum value of t_{HZOE}, t_{HZWE} parameters from 12 ns to 15 ns for 35 ns speed bin and 15 ns to 18 ns for 45 ns speed bin; changed minimum value of t_{SCE} parameter from 25 ns to 30 ns for 35 ns speed bin and 40 ns to 35 ns for 45 ns speed bin; changed maximum value of t_{HZCE} parameter from 12 ns to18 ns for 35 ns speed bin and 15 ns to 22 ns for 45 ns speed bin; changed minimum value of t_{SD} parameter from 15 ns to 18 ns for 35 ns speed bin and 20 ns to 22 ns for 45 ns speed bin). Updated Ordering Information (Corrected typo in Package Name column; also updated part numbers).
*B	414820	ZSD	12/16/2005	Changed status from Preliminary to Final. Changed the address of Cypress Semiconductor Corporation on Page 1 from “3901 North First Street” to “198 Champion Court”. Updated Features (Removed 35 ns speed bin). Updated Pin Configurations (Removed the Note “DNU pins have to be left floating or tied to V_{SS} to ensure proper application.” and its reference). Updated Product Portfolio (Removed 35 ns speed bin). Updated Maximum Ratings (Updated Note 4 (to include current limit)). Updated Electrical Characteristics (Removed “L” version of CY62148E; changed typical value of I_{CC} parameter from 1.5 mA to 2 mA at f = 1 MHz; changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA at f = 1 MHz; changed typical value of I_{CC} parameter from 12 mA to 15 mA at f = f_{max}; removed I_{SB1} parameter and its details; changed typical value of I_{SB2} parameter from 0.7 μA to 1 μA and maximum value of I_{SB2} parameter from 2.5 μA to 7 μA). Updated AC Test Loads and Waveforms (Changed the AC test load capacitance from 100 pF to 30 pF in Figure 2; changed test load parameters R_1, R_2, R_{TH} and V_{TH} from 1838 Ω, 994 Ω, 645 Ω and 1.75 V to 1800 Ω, 990 Ω, 639 Ω and 1.77 V). Updated Data Retention Characteristics (Changed maximum value of I_{CCDR} parameter from 2.5 μA to 7 μA; added typical value for I_{CCDR} parameter). Updated Switching Characteristics (Removed 35 ns speed bin; changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns; changed minimum value of t_{LZCE} and t_{LZWE} parameters from 6 ns to 10 ns; changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns; changed minimum value of t_{PWE} parameter from 30 ns to 35 ns; changed minimum value of t_{SD} parameter from 22 ns to 25 ns). Updated Ordering Information (Updated part numbers; also removed “Package Name” column and added “Package Diagram” column).

Document History Page (continued)

Document Title: CY62148E MoBL®, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C	464503	NXR	05/25/2006	Updated Product Portfolio (Included Automotive Range). Updated Operating Range (Included Automotive Range). Updated Electrical Characteristics (Included Automotive Range). Updated Data Retention Characteristics (Included Automotive Range). Updated Switching Characteristics (Included Automotive Range). Updated Ordering Information (Updated part numbers).
*D	485639	VKN	07/21/2006	Updated Operating Range (Replaced “2.2 V to 3.6 V” with “4.5 V to 5.5 V” in “V_{CC}” column).
*E	833080	VKN	03/09/2007	Updated Electrical Characteristics: Added SOIC package in “Test Conditions” of V_{IL} parameter and also added corresponding values. Added Note 10 and referred the same note in maximum value of V_{IL} parameter corresponding to SOIC package.
*F	890962	VKN	03/09/2007	Updated Pin Configurations (Added Note 2 and referred the same note in Figure 1). Updated Product Portfolio (Included Automotive-A range and removed Automotive-E range). Updated Operating Range (Included Automotive-A range and removed Automotive-E range). Updated Electrical Characteristics (Included Automotive-A range and removed Automotive-E range; added Note 11 (related to I_{SB2}) and referred the same note in I_{SB2} parameter). Updated Data Retention Characteristics (Included Automotive-A range and removed Automotive-E range). Updated Switching Characteristics (Included Automotive-A range and removed Automotive-E range). Updated Ordering Information (Updated part numbers).
*G	2947039	VKN	06/10/2010	Updated Truth Table (Added Note 33 and referred the same note in “$\overline{CE}$” column). Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85095 – Changed revision from ** to *A. spec 51-85081 – Changed revision from *B to *C. Updated to new template.
*H	3006318	AJU	08/23/2010	Updated Data Retention Characteristics (Added Note 14 and referred the same note in I_{CCDR} parameter). Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.
*I	3235744	RAME	04/20/2011	Updated Functional Description (Removed the line “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Package Diagrams: spec 51-85095 – Changed revision from *A to *B. Completing Sunset Review.
*J	3302815	RAME	07/14/2011	Updated to new template.
*K	3539544	TAVA	03/01/2012	Updated Electrical Characteristics (Updated Note 10). Updated Package Diagrams: spec 51-85081 – Changed revision from *C to *D. Completing Sunset Review.

Document History Page (continued)

Document Title: CY62148E MoBL®, 4-Mbit (512K × 8) Static RAM Document Number: 38-05442				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	3992135	MEMJ	05/06/2013	Updated Functional Description: Updated description. Updated Electrical Characteristics (Added one more Test Condition "V_{CC} = 5.5 V, I_{OH} = –0.1 mA" for V_{OH} parameter and also added corresponding values). Updated Package Diagrams: spec 51-85081 – Changed revision from *D to *E. Completing Sunset Review.
*M	4099045	VINI	08/19/2013	Updated Switching Characteristics: Added Note 16 and referred the same note in "Parameter" column. Updated to new template.
*N	4576526	VINI	11/21/2014	Updated Features: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 22 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 31 and referred the same note in Figure 8.
*O	4794169	NILE	06/11/2015	Updated Package Diagrams: spec 51-85095 – Changed revision from *B to *D. Updated to new template.
*P	5285890	VINI	06/01/2016	Updated Thermal Resistance: Replaced "two-layer" with "four-layer" in "Test Conditions" column. Updated all values in "32-pin SOIC Package" and "32-pin TSOP II Package" columns. Updated Data Retention Characteristics: Removed details in "Conditions" column corresponding to t_R parameter (To match the speed grade). Updated to new template. Completing Sunset Review.
*Q	6072272	VINI	02/15/2018	Updated Ordering Information: Updated part numbers. Updated to new template.
*R	6533264	VINI	04/04/2019	Updated to new template. Completing Sunset Review.

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