

4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
 - Typical standby current: 3.5 μ A
 - Maximum standby current: 8.7 μ A
- Embedded ECC for single-bit error correction^[1]
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 32-pin SOIC and 32-pin TSOP II packages

Functional Description

CY62148G is a high-performance CMOS low-power (MoBL) SRAM device with embedded ECC^[1]. This device is offered multiple pin configurations.

Device is accessed by asserting the chip enable ($\overline{CE}$) input LOW. Data writes are performed by asserting the Write Enable ($\overline{WE}$) input LOW, while providing the data on I/O₀ through I/O₇ and address on A₀ through A₁₈ pins.

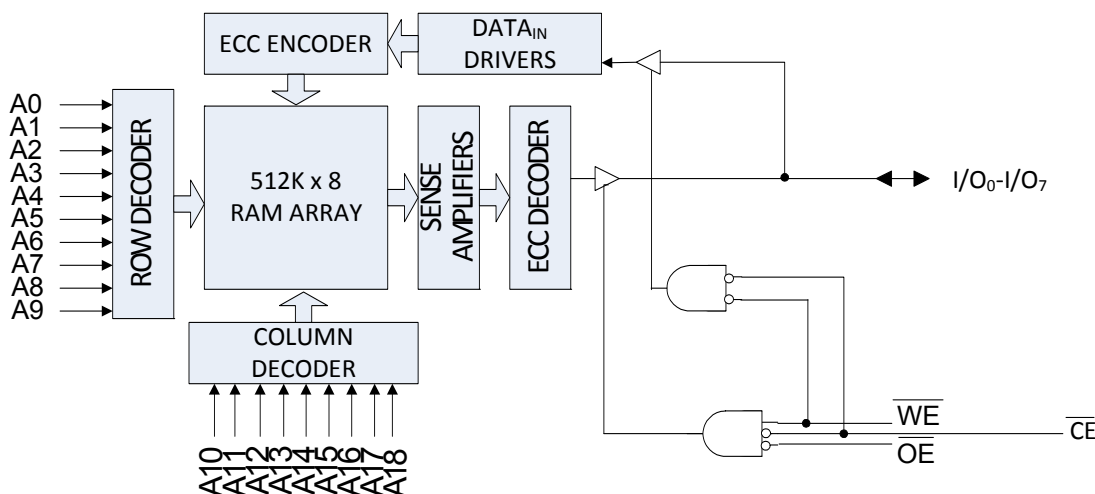
Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O₀ through I/O₇).

All I/Os (I/O₀ through I/O₇) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ HIGH or control signal $\overline{OE}$ is de-asserted).

See the [Truth Table – CY62148G](#) on page 12 for a complete description of read and write modes.

The logic block diagrams are on page 2.

Logic Block Diagram – CY62148G



Note

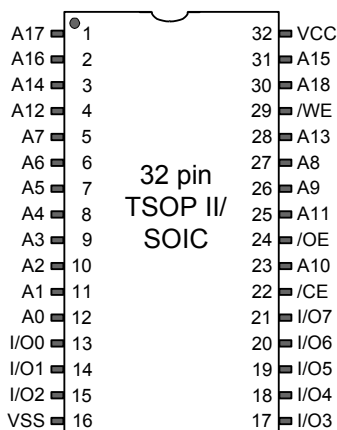
1. This device does not support automatic write-back on error detection.

Contents

Pin Configurations	3	Ordering Information	13
Product Portfolio	3	Ordering Code Definitions	13
Maximum Ratings	4	Package Diagrams	14
Operating Range	4	Acronyms	15
DC Electrical Characteristics	4	Document Conventions	15
Capacitance	6	Units of Measure	15
Thermal Resistance	6	Document History Page	16
AC Test Loads and Waveforms	6	Sales, Solutions, and Legal Information	17
Data Retention Characteristics	7	Worldwide Sales and Design Support	17
Data Retention Waveform	7	Products	17
AC Switching Characteristics	8	PSoC@Solutions	17
Switching Waveforms	9	Cypress Developer Community	17
Truth Table – CY62148G	12	Technical Support	17

Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout



Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I _{CC} , (mA)		Standby, I _{SB2} (μA)	
				f = f _{max}			
				Typ ^[2]	Max	Typ ^[2]	Max
CY62148G18	Industrial	1.65 V–2.2 V	55	–	20	–	10
CY62148G30		2.2 V–3.6 V	45	–	20	3.5	8.7
CY62148G		4.5 V–5.5 V					

Note

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage
to ground potential^[3] -0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs
in HI-Z state^[3] -0.5 V to V_{CC} + 0.5 V

DC input voltage^[3] -0.5 V to V_{CC} + 0.5 V

Output current into outputs (in low state) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) >2001 V

Latch-up current >140 mA

Operating Range

Grade	Ambient Temperature	V _{CC} ^[4]
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	45 ns / 55 ns			Unit
			Min	Typ	Max	
V _{OH}	Output HIGH voltage	1.65 V to 2.2 V V _{CC} = Min, I _{OH} = -0.1 mA	1.4	-	-	V
		2.2 V to 2.7 V V _{CC} = Min, I _{OH} = -0.1 mA	2	-	-	
		2.7 V to 3.6 V V _{CC} = Min, I _{OH} = -1.0 mA	2.2	-	-	
		4.5 V to 5.5 V V _{CC} = Min, I _{OH} = -1.0 mA	2.4	-	-	
		4.5 V to 5.5 V V _{CC} = Min, I _{OH} = -0.1 mA	V _{CC} - 0.5 ^[5]	-	-	
V _{OL}	Output LOW voltage	1.65 V to 2.2 V V _{CC} = Min, I _{OL} = 0.1 mA	-	-	0.2	V
		2.2 V to 2.7 V V _{CC} = Min, I _{OL} = 0.1 mA	-	-	0.4	
		2.7 V to 3.6 V V _{CC} = Min, I _{OL} = 2.1 mA	-	-	0.4	
		4.5 V to 5.5 V V _{CC} = Min, I _{OL} = 2.1 mA	-	-	0.4	
V _{IH}	Input HIGH voltage	1.65 V to 2.2 V -	1.4	-	V _{CC} + 0.2 ^[3]	V
		2.2 V to 2.7 V -	1.8	-	V _{CC} + 0.3 ^[3]	
		2.7 V to 3.6 V -	2	-	V _{CC} + 0.3 ^[3]	
		4.5 V to 5.5 V -	2.2	-	V _{CC} + 0.5 ^[3]	
V _{IL}	Input LOW voltage	1.65 V to 2.2 V -	-0.2 ^[3]	-	0.4	V
		2.2 V to 2.7 V -	-0.3 ^[3]	-	0.6	
		2.7 V to 3.6 V -	-0.3 ^[3]	-	0.8	
		4.5 V to 5.5 V -	-0.5 ^[3]	-	0.8	
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _{OUT} ≤ V _{CC} , Output disabled	-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	Max V _{CC} , I _{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	-	20	mA
			f = 18.18 MHz (55 ns)	-	20	mA
			f = 1 MHz	-	6	mA

Notes

3. V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.

4. Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.

5. This parameter is guaranteed by design and not tested.

DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45 ns / 55 ns			Unit
				Min	Typ	Max	
$I_{SB1}^{[6]}$	Automatic power down current – CMOS inputs; $V_{CC} = 2.2 \text{ V to } 3.6 \text{ V and } 4.5 \text{ V to } 5.5 \text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V},$ $f = f_{\max}$ (address and data only), $f = 0$ ($\overline{OE}$, and $\overline{WE}$), Max V_{CC}		–	–	8.7	μA
	Automatic power down current – CMOS inputs $V_{CC} = 1.65 \text{ V to } 2.2 \text{ V}$			–	–	10	
$I_{SB2}^{[6]}$	Automatic power down current – CMOS inputs $V_{CC} = 2.2 \text{ V to } 3.6 \text{ V and } 4.5 \text{ V to } 5.5 \text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V},$ $f = 0, \text{ Max } V_{CC}$	25 °C ^[7]	–	3.5	3.7	μA
			40 °C ^[7]	–	–	4.8	
			70 °C ^[7]	–	–	7	
			85 °C	–	–	8.7	
	Automatic power down current – CMOS inputs $V_{CC} = 1.65 \text{ V to } 2.2 \text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V},$ $f = 0, \text{ Max } V_{CC}$	25 °C ^[7]	–	3.5	4.3	
			40 °C ^[7]	–	–	5	
			70 °C ^[7]	–	–	7.5	
			85 °C	–	–	10	

Notes

6. Chip enables $\overline{CE}$ must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.

7. The I_{SB2} limits at 25 °C, 40 °C, 70 °C, and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

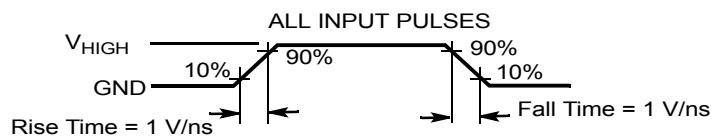
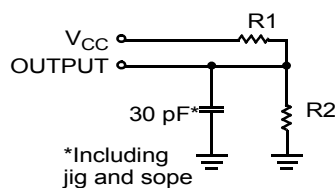
Parameter ^[8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

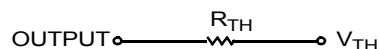
Parameter ^[8]	Description	Test Conditions	32-pin SOIC	32-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		25.12	17.44	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[9]



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.

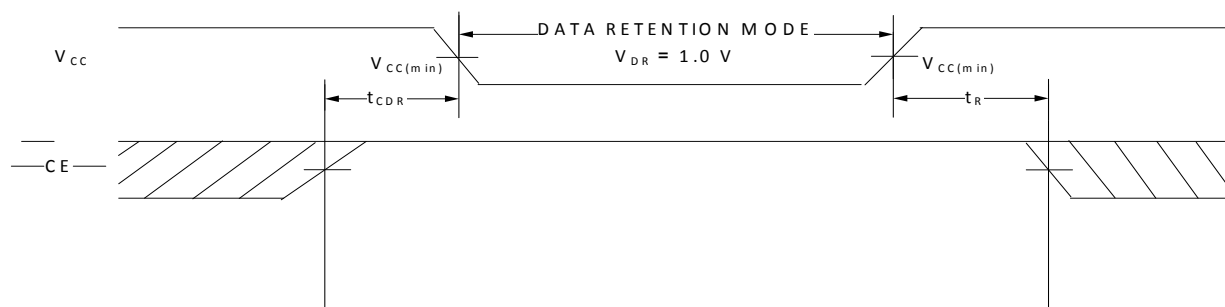
Data Retention Characteristics

Over the Operating range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1	—	—	V
$I_{CCDR}^{[11, 12]}$	Data retention current	$V_{CC} = 1.2 \text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	—	—	13	μA
$t_{CDR}^{[13, 14]}$	Chip deselect to data retention time		0	—	—	ns
$t_R^{[14]}$	Operation recovery time		45/55	—	—	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V–5.5 V), $T_A = 25^\circ\text{C}$.
11. Chip enables $\overline{CE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR} .
13. These parameters are guaranteed by design.
14. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu\text{s}$ or stable at $V_{CC(min)} \geq 100 \mu\text{s}$.

AC Switching Characteristics

Parameter ^[15, 16]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{RC}	Read cycle time	45	–	55	–	ns
t _{AA}	Address to data valid	–	45	–	55	ns
t _{OHA}	Data hold from address change	10	–	10	–	ns
t _{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t _{LZOE}	$\overline{OE}$ LOW to Low impedance ^[17]	5	–	5	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to HI-Z ^[17, 18]	–	18	–	18	ns
t _{LZCE}	$\overline{CE}$ LOW to Low impedance ^[17]	10	–	10	–	ns
t _{HZCE}	$\overline{CE}$ HIGH to HI-Z ^[17, 18]	–	18	–	18	ns
t _{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t _{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle ^[19, 20]						
t _{WC}	Write cycle time	45	–	55	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end	35	–	45	–	ns
t _{AW}	Address setup to write end	35	–	45	–	ns
t _{HA}	Address hold from write end	0	–	0	–	ns
t _{SA}	Address setup to write start	0	–	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t _{SD}	Data setup to write end	25	–	25	–	ns
t _{HD}	Data hold from write end	0	–	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to HI-Z ^[17, 18]	–	18	–	20	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low impedance ^[17]	10	–	10	–	ns

Notes

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

16. These parameters are guaranteed by design.

17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.

18. t_{HZOE} , t_{HZCE} and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.

19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

20. The minimum pulse width in Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [21, 22]

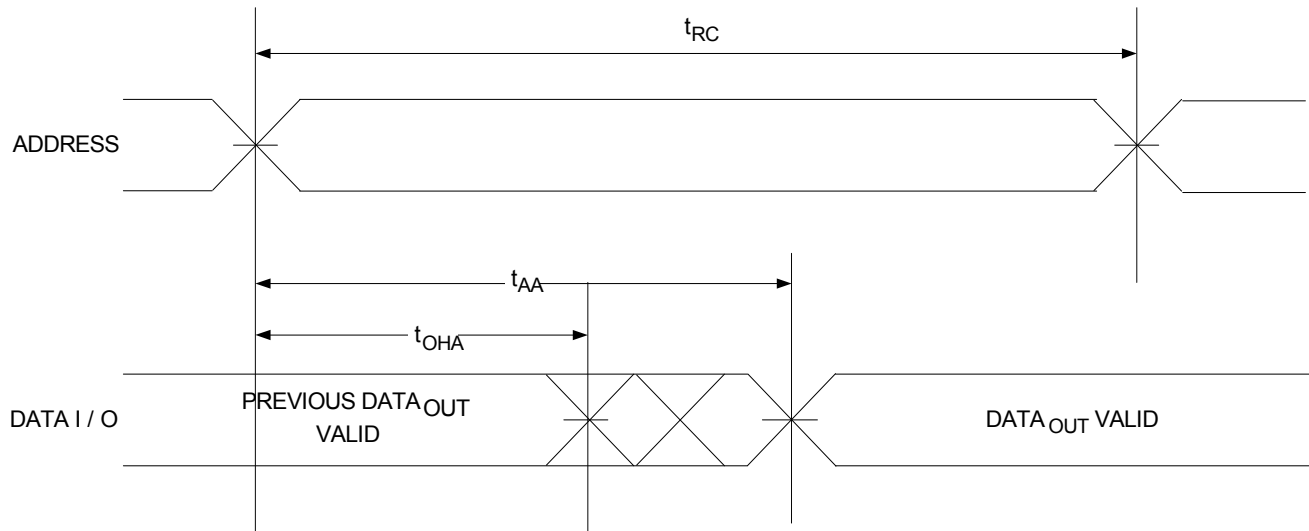
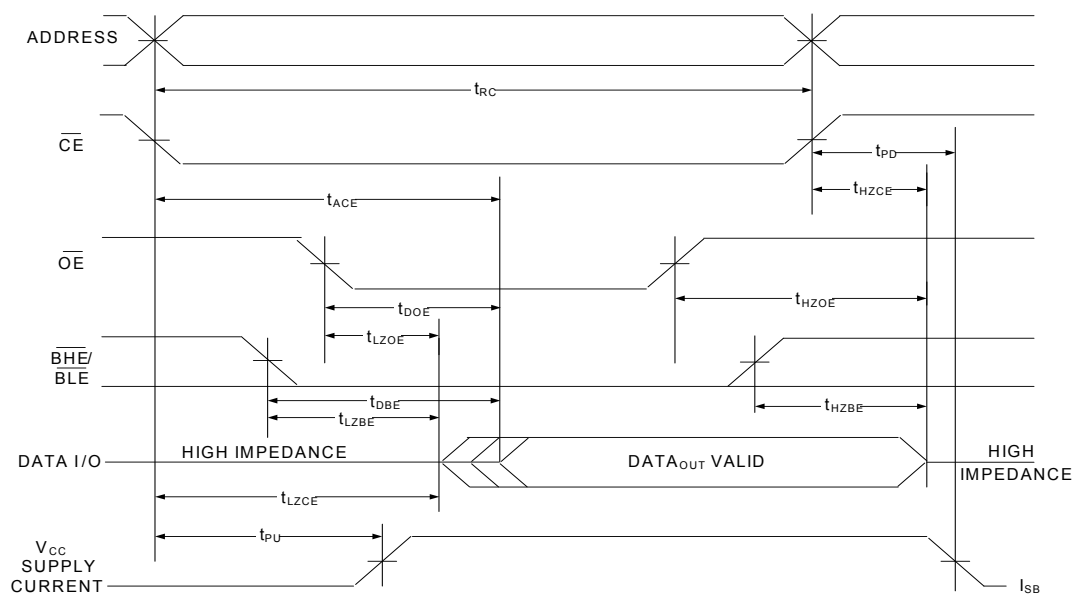


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [22, 23]

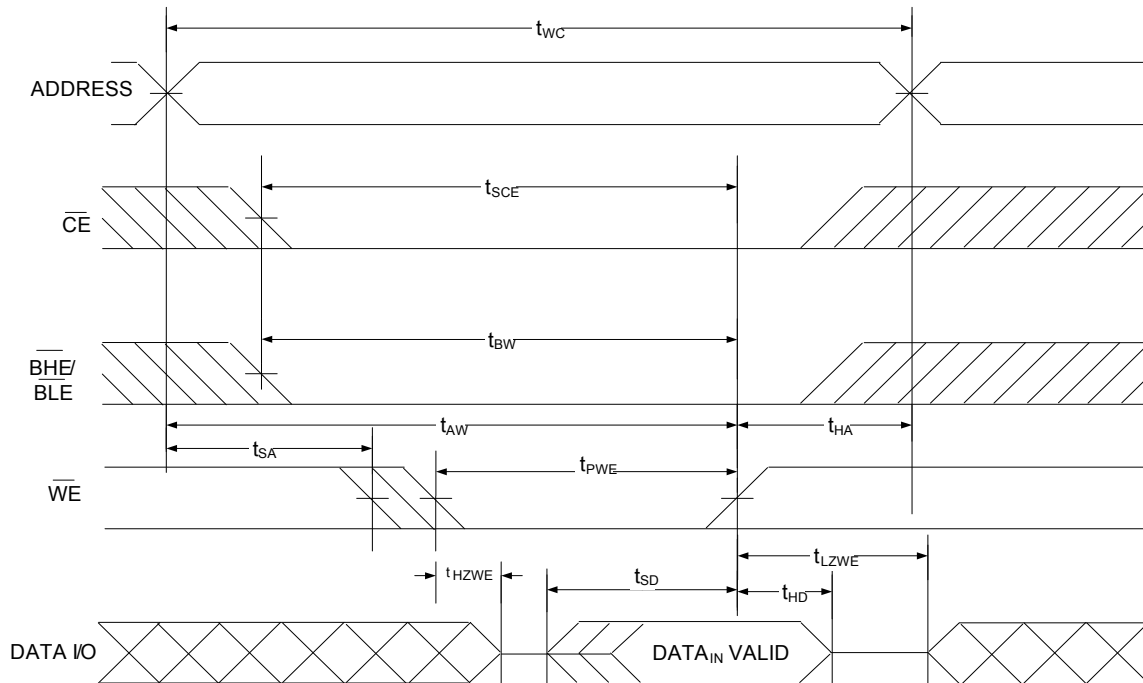


Notes

21. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
22. $\overline{WE}$ is HIGH for Read cycle.
23. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) [24, 25, 26]



Notes

24. $\overline{\text{WE}}$ is HIGH for Read cycle.

25. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

26. Data I/O is in a HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [27, 28]

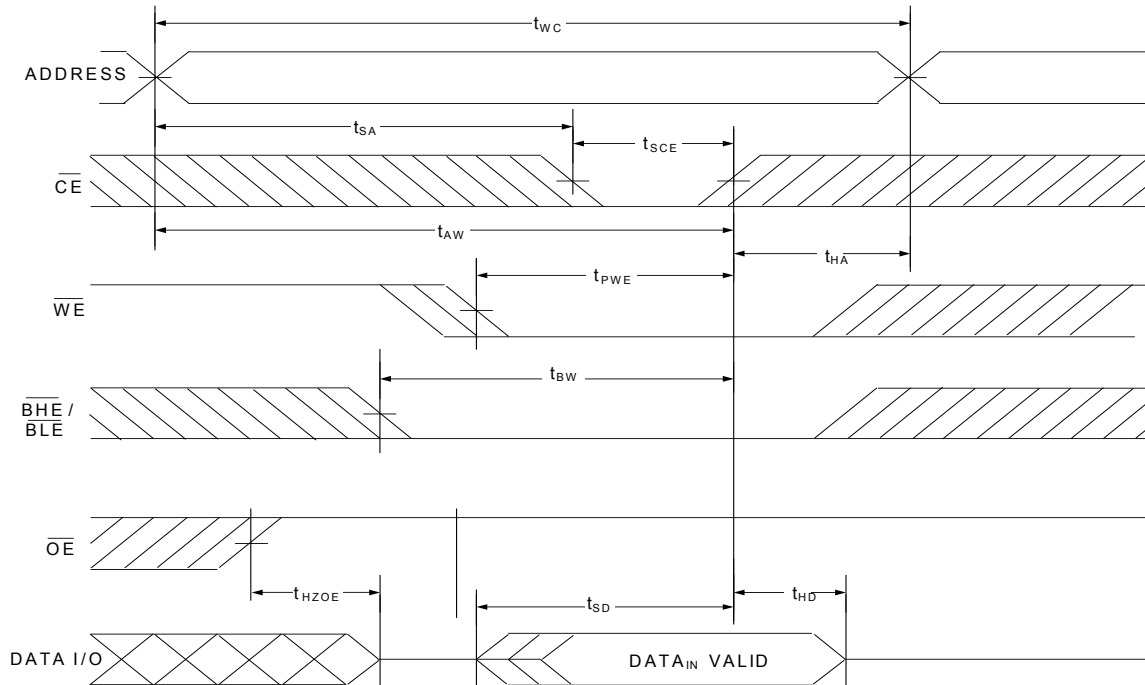
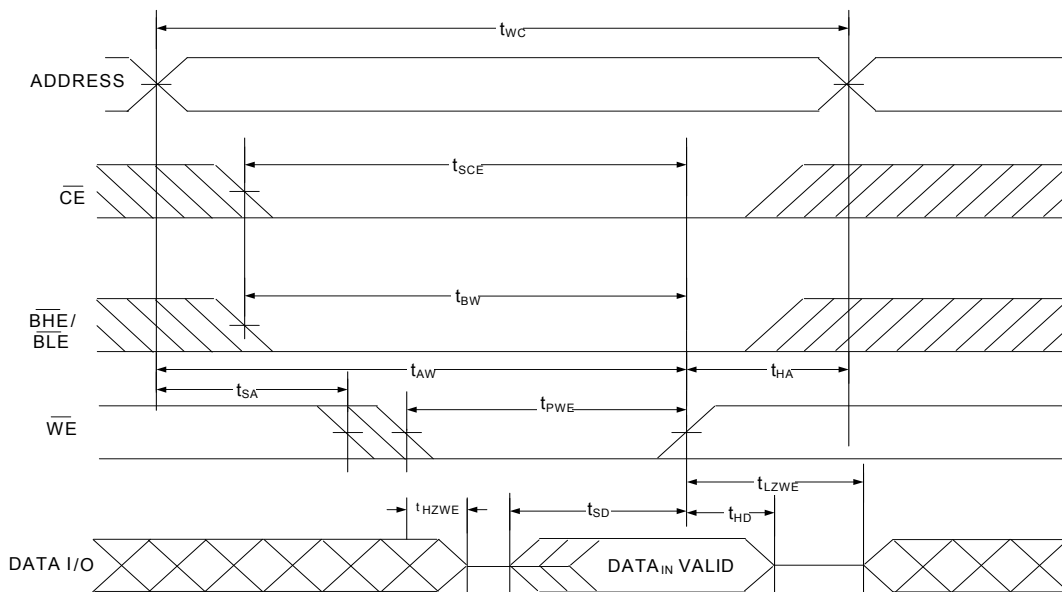


Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [27, 28, 29]



Notes

27. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

28. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$.

29. The minimum write pulse width for Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Truth Table – CY62148G

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power	Configuration
H	X ^[30]	X ^[30]	HI-Z	Deselect/Power-down	Standby (I_{SB})	512 K × 8
L	H	L	Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})	512 K × 8
L	H	H	HI-Z	Output disabled	Active (I_{CC})	512 K × 8
L	L	X ^[30]	Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})	512 K × 8

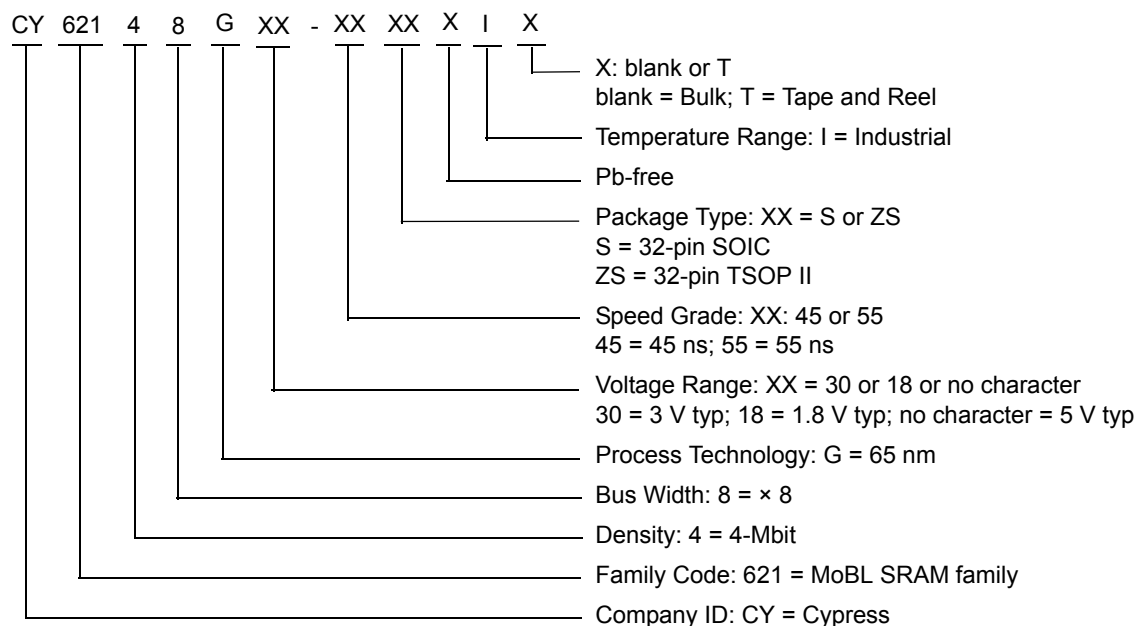
Note

30. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

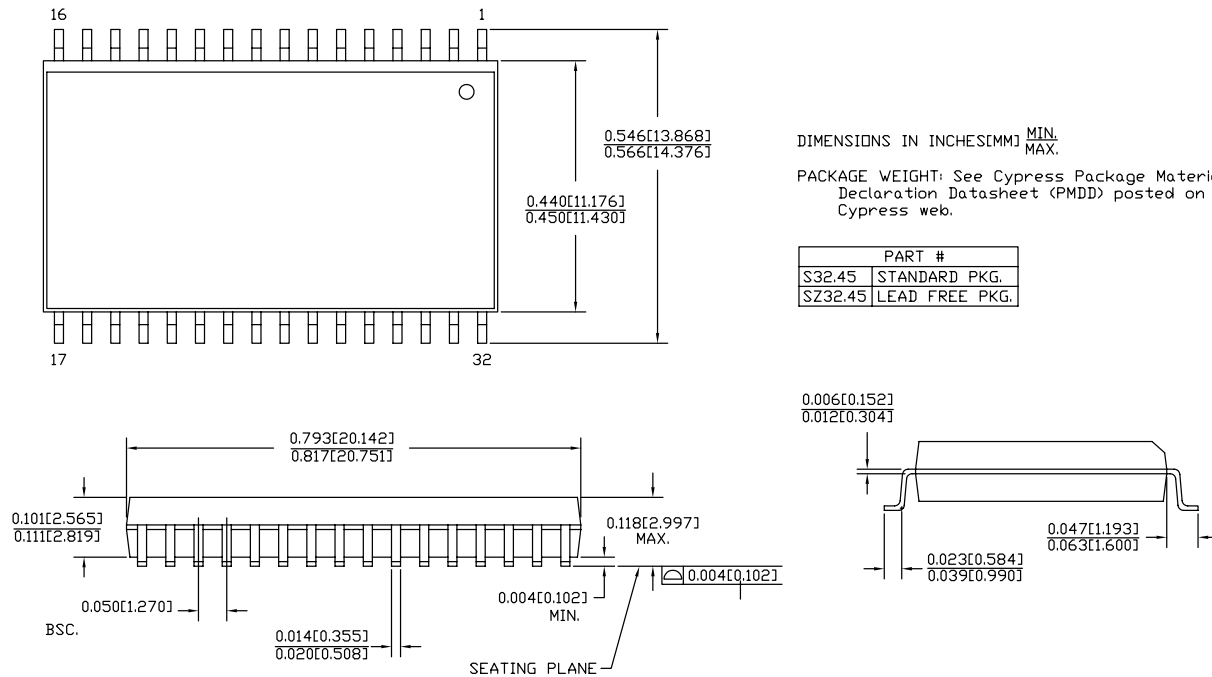
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62148G30-45SXI	51-85081	32-pin SOIC (450 Mils)	Industrial
		CY62148G30-45SXIT	51-85081	32-pin SOIC (450 Mils), Tape and Reel	
		CY62148G30-45ZSXI	51-85095	32-pin TSOP II	
		CY62148G30-45ZSXIT	51-85095	32-pin TSOP II, Tape and Reel	
	4.5 V–5.5 V	CY62148G-45SXI	51-85081	32-pin SOIC (450 Mils)	
		CY62148G-45SXIT	51-85081	32-pin SOIC (450 Mils), Tape and Reel	
		CY62148G-45ZSXI	51-85095	32-pin TSOP II	
		CY62148G-45ZSXIT	51-85095	32-pin TSOP II, Tape and Reel	
55	1.65 V–2.2 V	CY62148G18-55ZSXI	51-85095	32-pin TSOP II	
		CY62148G18-55ZSXIT	51-85095	32-pin TSOP II, Tape and Reel	

Ordering Code Definitions



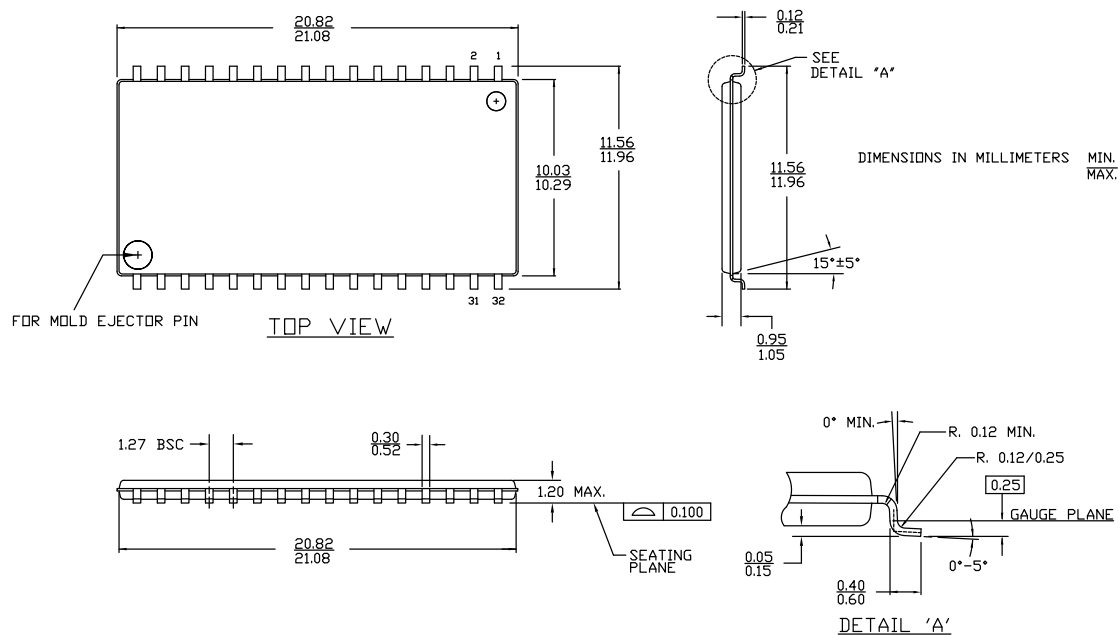
Package Diagrams

Figure 9. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



51-85081 *E

Figure 10. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



51-85095 *D

Acronyms

Acronym	Description
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62148G MoBL®, 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95415				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5054381	NILE	12/17/2015	Changed status from Preliminary to Final.
*C	5082528	NILE	01/12/2016	Updated Ordering Information : Updated part numbers. Completing Sunset Review.
*D	5432526	NILE	09/10/2016	Updated Maximum Ratings : Updated Note 3 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics : Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Ordering Information : Updated part numbers. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2015-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.