



8M (512K x 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65V to 2.2V
- Pin compatible with CY62157CV18
- Ultra low active power
 - Typical active current: 1 mA @ f = 1 MHz
 - Typical active current: 10 mA @ f = fmax
- Ultra low standby power
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Packages offered in a 48-ball FBGA

Functional Description^[1]

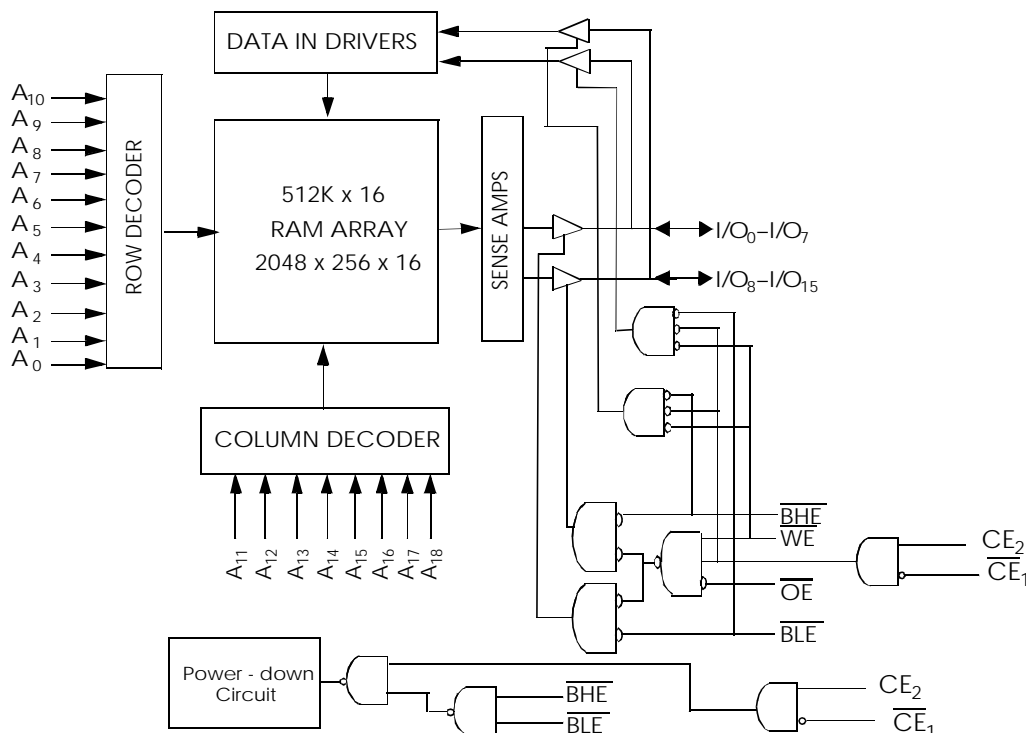
The CY62157DV20 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when

deselected Chip Enable 1 (\overline{CE}_1) HIGH or Chip Enable 2 (CE_2) LOW or both \overline{BHE} and \overline{BLE} are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected Chip Enable 1 (\overline{CE}_1) HIGH or Chip Enable 2 (CE_2) LOW, outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (CE_2) HIGH and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (CE_2) HIGH and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

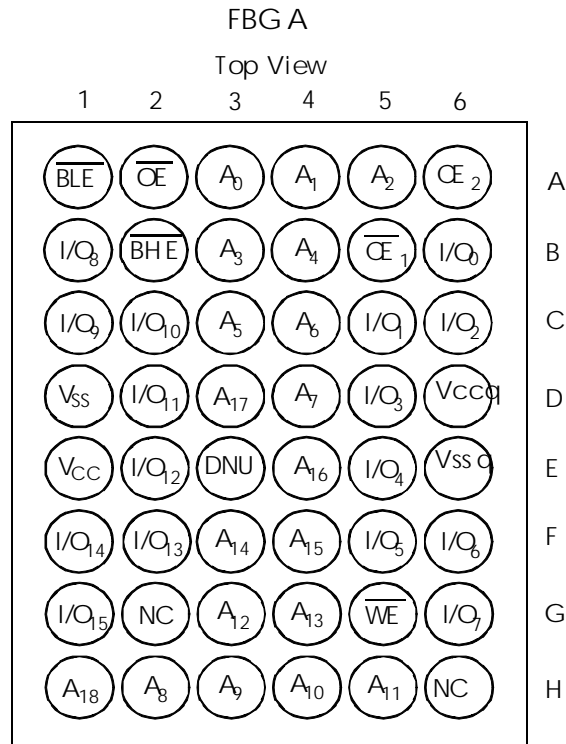
Reading from the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) LOW and Chip Enable 2 (CE_2) HIGH and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



Note:

1. For best practice recommendations, please refer to the Cypress application note *System Design Guidelines* on <http://www.cypress.com>.

Pin Configuration^[2, 3]

Notes:

2. NC pins are not connected to the die.
3. DNU pins are to be connected to V_{SS} or left open.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential. -0.2V to $V_{CCMAX} + 0.2V$
- DC Voltage Applied to Outputs

- in High-Z State^[4] -0.2V to $V_{CC} + 0.2V$
- DC Input Voltage^[4] -0.2V to $V_{CC} + 0.2V$
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Industrial	-40°C to +85°C	1.65V to 2.2V

Product Portfolio

Product	V _{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
	Min.	Typ. ^[5]	Max.		f = 1 MHz		f = f _{MAX}			
					Typ. ^[5]	Max.	Typ. ^[5]	Max.	Typ. ^[5]	Max.
CY62157DV20L	1.65	1.8	2.2	55	1	5	10	20	2	25
				70			8	15		
CY62157DV20LL	1.65	1.8	2.2	70	1	5	8	15	2	17
				55			10	20		

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	CY62157DV20-55			CY62157DV20-70			Unit	
			Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA, V _{CC} = 1.65V	1.4			1.4			V	
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA, V _{CC} = 1.65V			0.2			0.2	V	
V _{IH}	Input HIGH Voltage		1.4		V _{CC} + 0.2	1.4		V _{CC} + 0.2	V	
V _{IL}	Input LOW Voltage		-0.2		0.4	-0.2		0.4	V	
I _{Ix}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA	
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} , V _{CC} = 2.2V, I _{OUT} = 0 mA, CMOS level		10	20		8	15	mA	
		f = 1 MHz		1	5		1	5		
I _{SB1}	Automatic CE Power-down Current – CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	L		2	25		2	25	μA
			LL		2	17		2	17	
I _{SB2}	Automatic CE Power-down Current – CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 2.2V	L		2	25		2	25	μA
			LL		2	17		2	17	

Capacitance^[6]

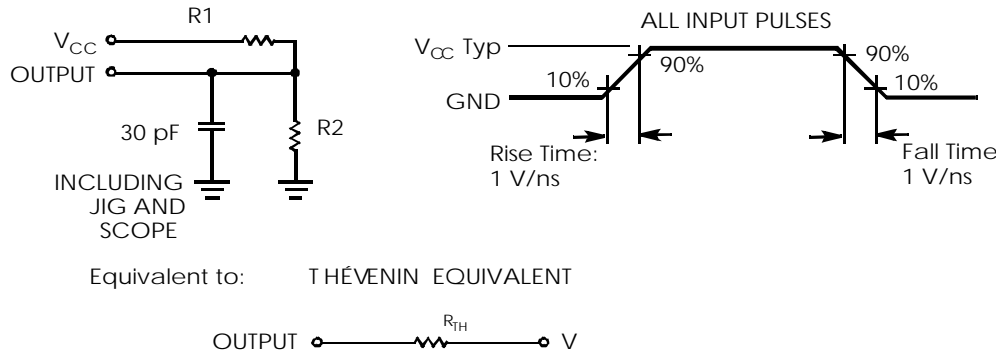
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	TA = 25°C, f = 1 MHz	6	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	8	pF

Notes:

- 4. V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- 5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

Thermal Resistance

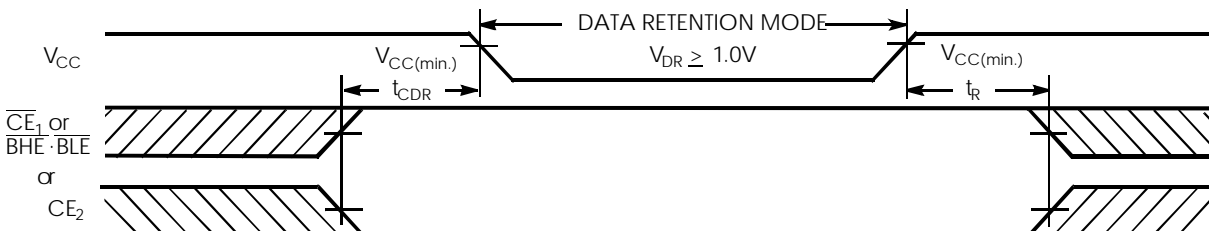
Parameter	Description	Test Conditions	BGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient) ^[6]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	C/W
θ_{JC}	Thermal Resistance (Junction to Case) ^[6]		16	C/W

AC Test Loads and Waveforms


Parameters	1.8V	UNIT
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

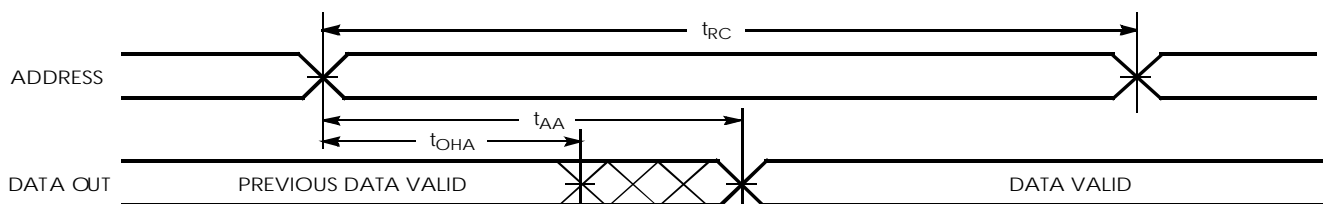
Parameter	Description	Conditions	Min.	Typ. ^[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		2.2	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V, CE_1 \geq V_{CC} - 0.2V, CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	10	μA
		L			3	
		LL				
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[8]

Notes:

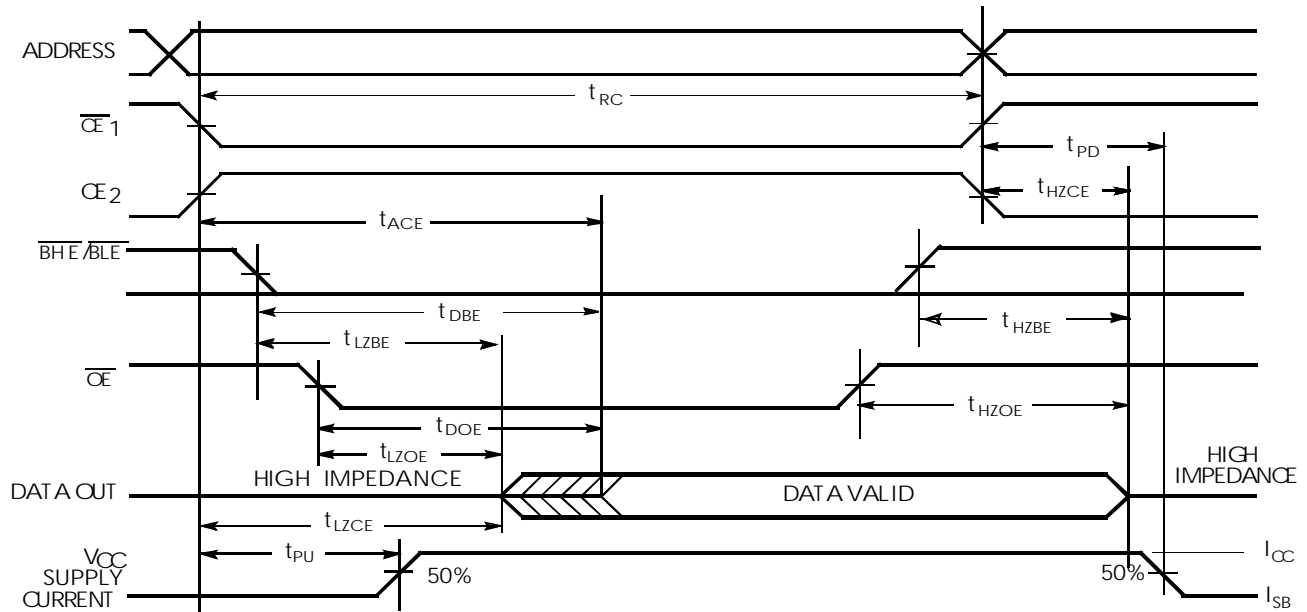
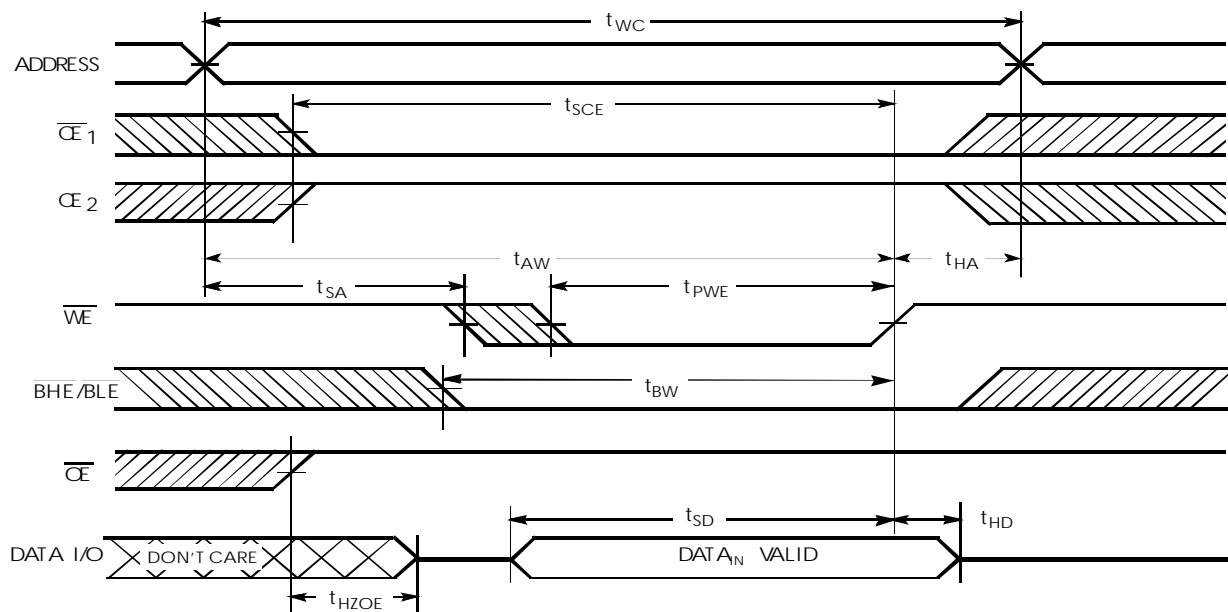
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 100 \mu s$ or stable at $V_{CC(min.)} > 100 \mu s$.
- $\overline{BHE} \cdot \overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics (Over the Operating Range)^[9]

Parameter	Description	CY62157DV20-55		CY62157DV20-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	\overline{CE}_1 LOW or CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[10]	5		5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[10, 12]		20		25	ns
t_{LZCE}	\overline{CE}_1 LOW or CE_2 HIGH to Low Z ^[10]	10		10		ns
t_{HZCE}	\overline{CE}_1 HIGH or CE_2 LOW to High Z ^[10, 12]		20		25	ns
t_{PU}	\overline{CE}_1 LOW or CE_2 HIGH to Power-up	0		0		ns
t_{PD}	\overline{CE}_1 HIGH or CE_2 LOW to Power-down		55		70	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		70	ns
$t_{LZBE}^{[11]}$	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[10]	5		5		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[10, 12]		20		25	ns
Write Cycle^[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	\overline{CE}_1 LOW or CE_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	45		50		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	45		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[10, 12]		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[10]	10		10		ns

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[14, 15]

Notes:

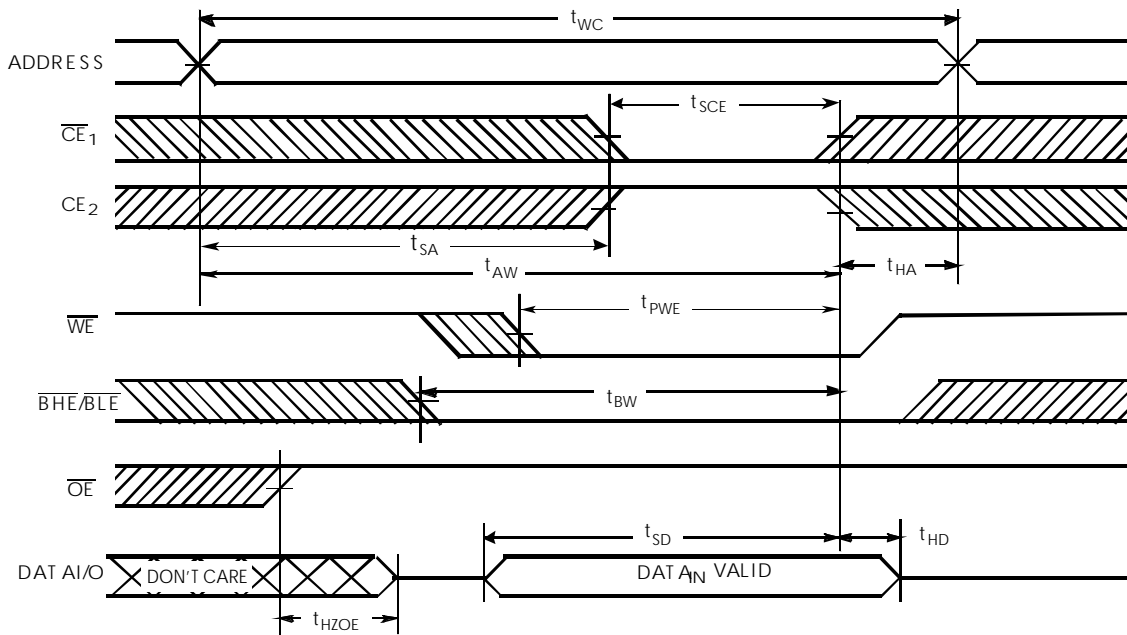
9. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)/2}$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} .
11. If both byte enables are toggled together, this value is 10 ns.
12. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. The internal Write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
14. Device is continuously selected. \overline{OE} , $CE_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, $CE_2 = V_{IH}$.
15. \overline{WE} is HIGH for Read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled)^[15, 16]

Write Cycle No. 1 (\overline{WE} Controlled)^[13, 17, 18, 19]

Notes:

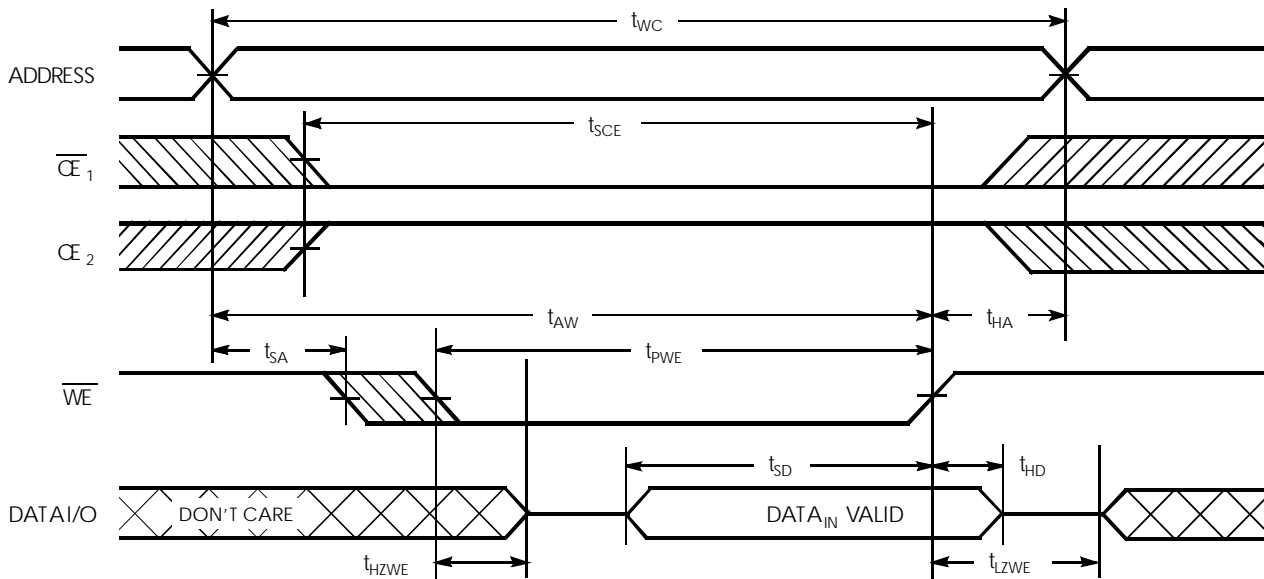
16. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.
17. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
18. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

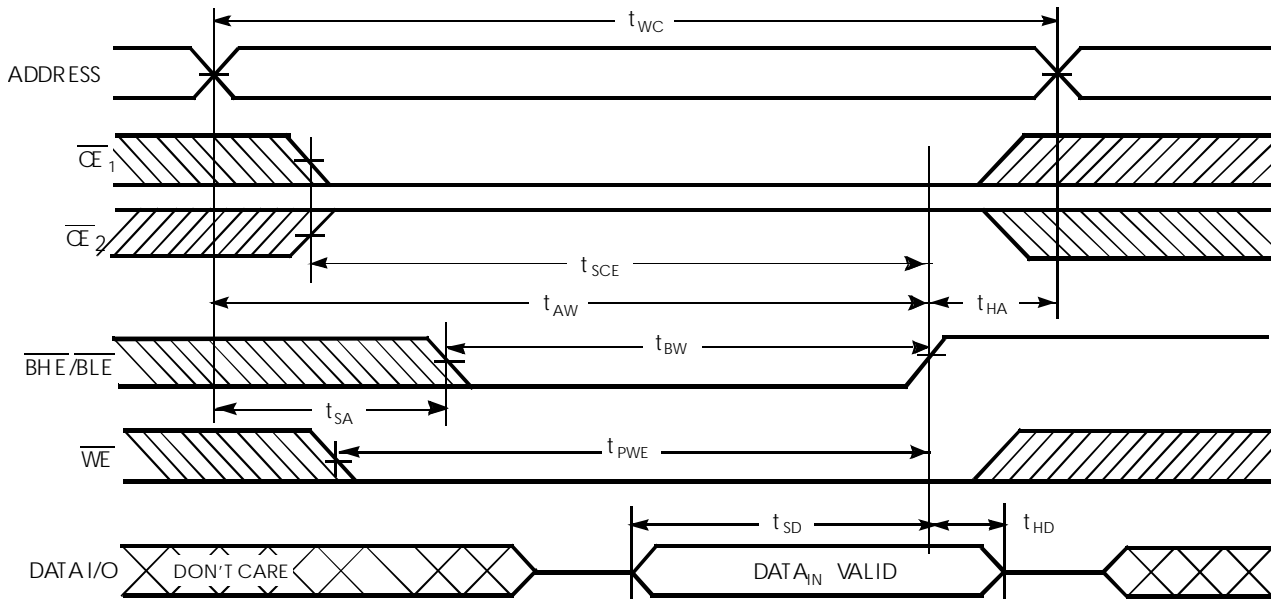
Switching Waveforms (continued)

Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [13, 17, 18, 19]



Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [18, 19]

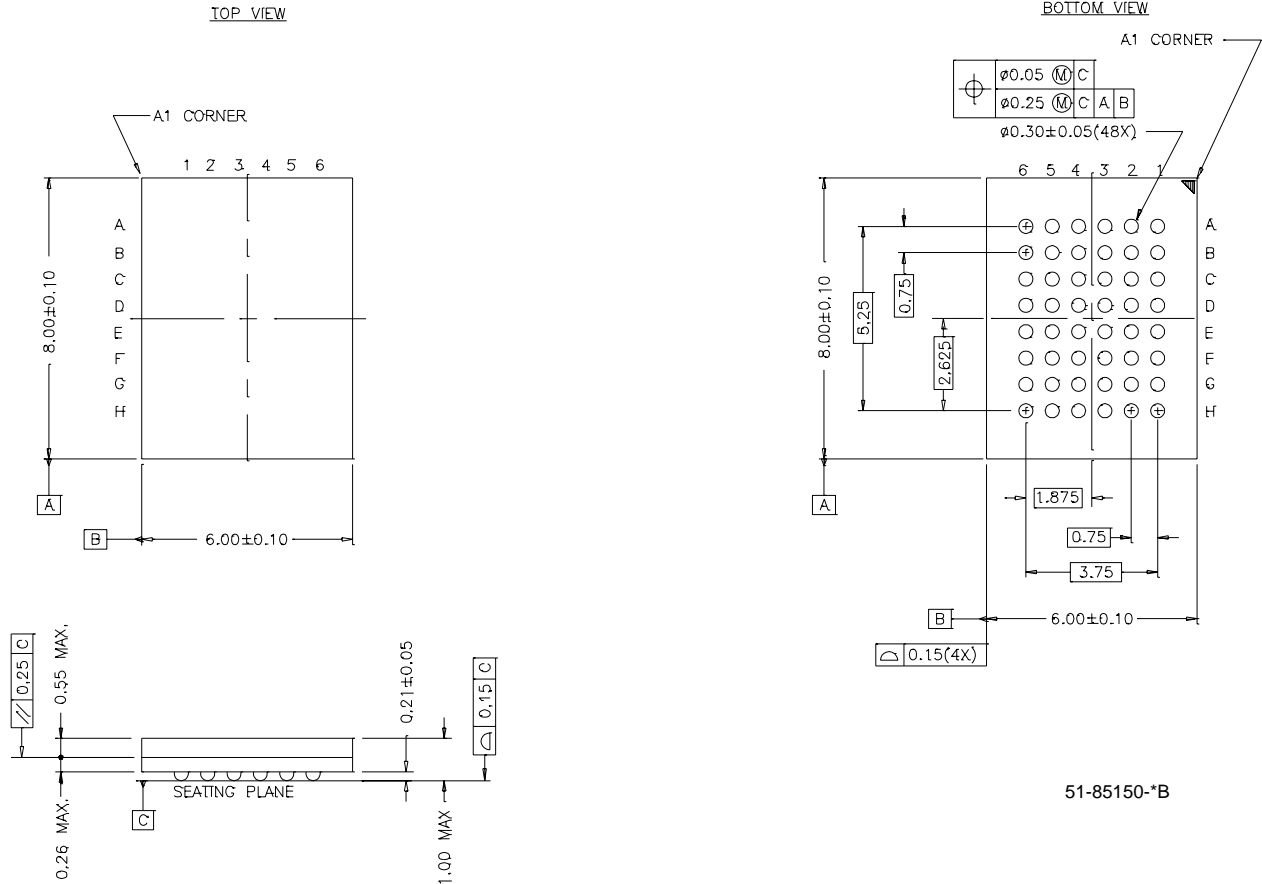


Switching Waveforms (continued)
Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)^[19]

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62157DV20L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
55	CY62157DV20LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
70	CY62157DV20L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62157DV20LL-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagram

48-Lead VFBGA (6 x 8 x 1 mm) BV48A



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Document History Page

Document Title: CY62157DV20 MoBL2™ 512K x 16 Static RAM				
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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	115250	05/29/02	MGN	New Data Sheet
*A	124693	03/18/03	DPM	Preliminary to Final Added Footnote 1 Added LL Bin to lccdr value = 3 uA max Filled in TBD values
*B	124693	03/19/03	Dcon	Minor Change: Fixed incorrect footer on page 1 & 9.