16-Mbit (1M x 16 / 2M x 8) Static RAM

Features

- TSOP I package configurable as 1M x 16 or as 2M x 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 2.20V–3.60V
- Ultra low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra low active power
  - Typical active current: 2.2 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball BGA and 48-pin TSOP I packages

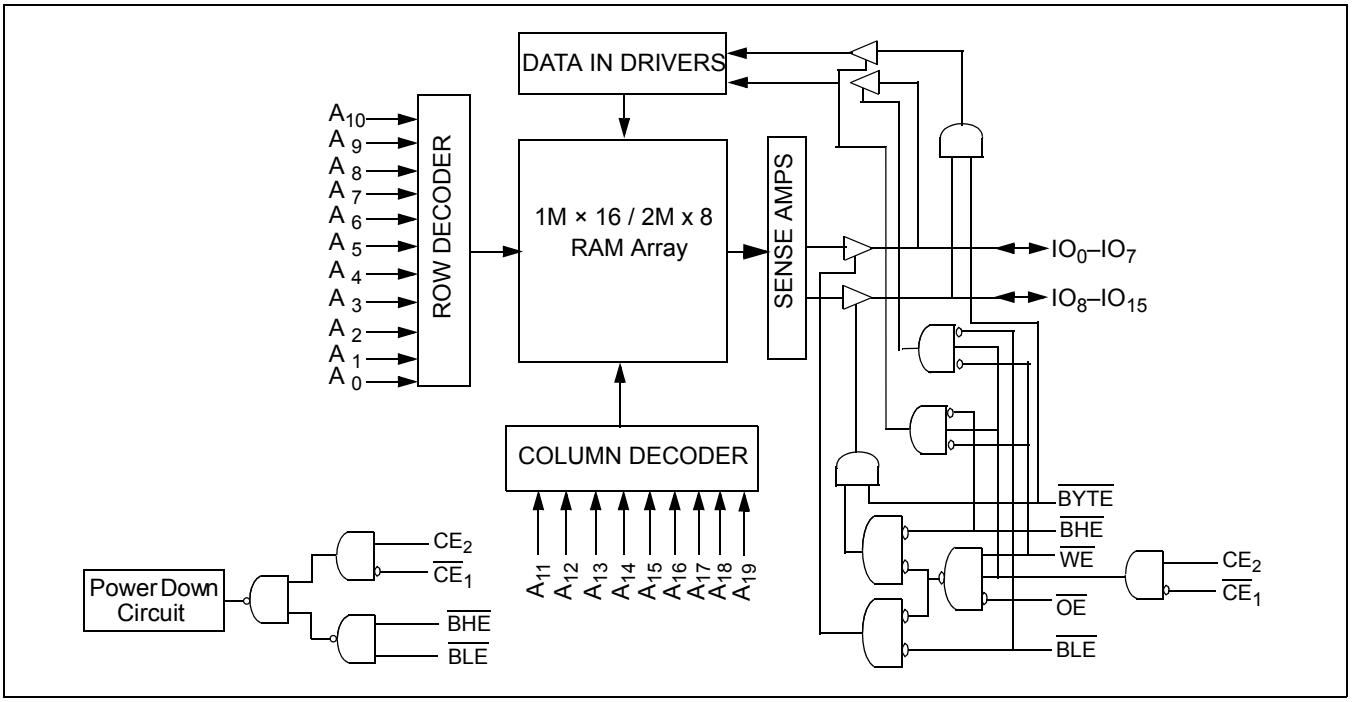
Functional Description[1]

The CY62167EV30 is a high performance CMOS static RAM organized as 1M words by 16 bits / 2M words by 8 bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (IO_0 through IO_{15}) are placed in a high-impedance state when: the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7) is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on IO_8 to IO_{15}. See the "Truth Table" on page 10 for a complete description of read and write modes.

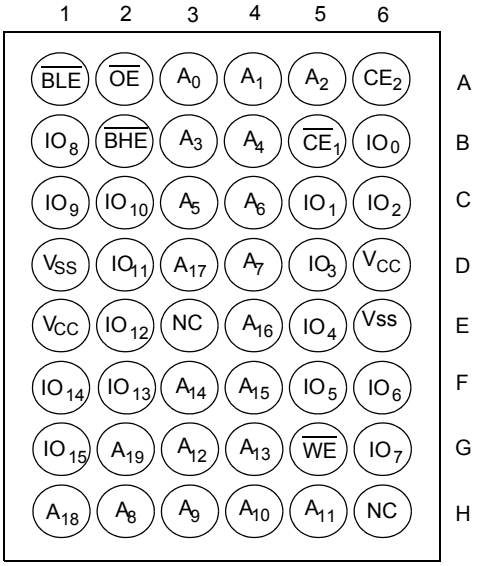
Logic Block Diagram



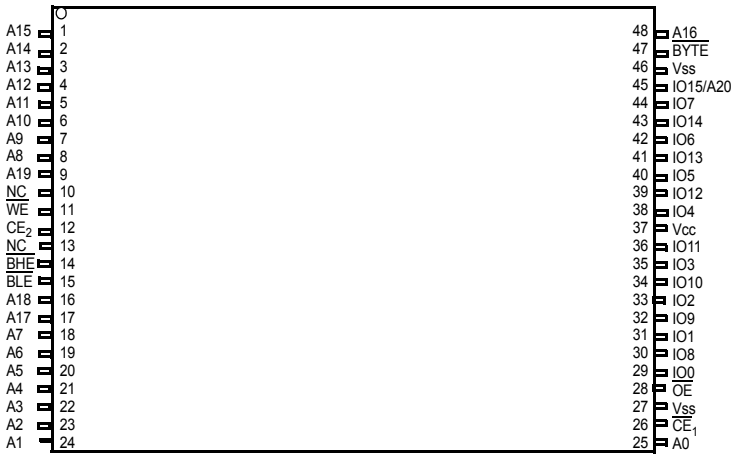
Note
1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Pin Configuration[2, 3, 4]

48-Ball FBGA Top View



48-Pin TSOP I Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[5]	Max		Typ[5]	Max	Typ[5]	Max	Typ[5]	Max
CY62167EV30LL	2.20	3.0	3.60	45	2.2	4.0	25	30	1.5	12

Notes

2. NC pins are not connected on the die.
3. The BYTE pin in the 48-TSOPI package has to be tied to V_{CC} to use the device as a 1M X 16 SRAM. The 48-TSOPI package can also be used as a 2M X 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M x 8 configuration, Pin 45 is A20, while BHE, BLE and IO_8 to IO_{14} pins are not used.
4. Ball H6 for the FBGA package can be used to upgrade to a 32M density.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(typ)$, $T_A = 25°C$.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.3V to 3.9V (V_{CC}(max) + 0.3V

DC Voltage Applied to Outputs in High Z State[6, 7] ..... –0.3V to 3.9V (V_{CC}(max) + 0.3V

DC Input Voltage[6, 7] ..... –0.3V to 3.9V (V_{CC}(max) + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)

Latch up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[8]
CY62167EV30LL	Industrial	–40°C to +85°C	2.2V to 3.6V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ[5]	Max	
V_{OH}	Output HIGH Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0			V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4			V
V_{OL}	Output LOW Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA			0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1mA			0.4	V
V_{IH}	Input HIGH Voltage	$2.2 \le V_{CC} \le 2.7$		1.8		V_{CC} + 0.3V	V
		$2.7 \le V_{CC} \le 3.6$		2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	$2.2 \le V_{CC} \le 2.7$		–0.3		0.6	V
		$2.7 \le V_{CC} \le 3.6$	For FBGA package	–0.3		0.8	V
			For TSOP I package	–0.3		0.7[9]	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1		+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = V_{CC}$(max) I_{OUT} = 0 mA CMOS levels		25	30	mA
		f = 1 MHz			2.2	4.0	mA
I_{SB1}	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$ or $CE_2 \le 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$, $V_{IN} \le 0.2V$, f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V_{CC} = 3.60V			1.5	12	µA
I_{SB2}[10]	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$ or $CE_2 \le 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0, V_{CC} = 3.60V			1.5	12	µA

Capacitance[11]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

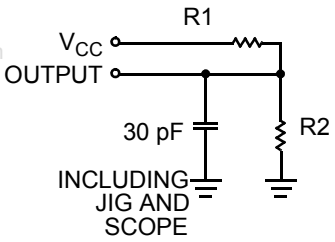
Notes

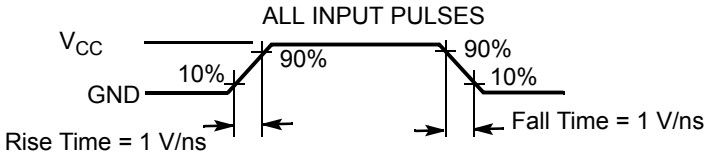
6. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
7. V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.
8. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
9. Under DC conditions the device meets a V_{IL} of 0.8V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7V. This is applicable to TSOP I package only.
10. Only chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance[11]

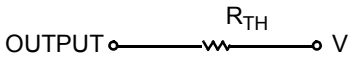
Parameter	Description	Test Conditions	BGA	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	60	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		16	4.3	°C/W

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



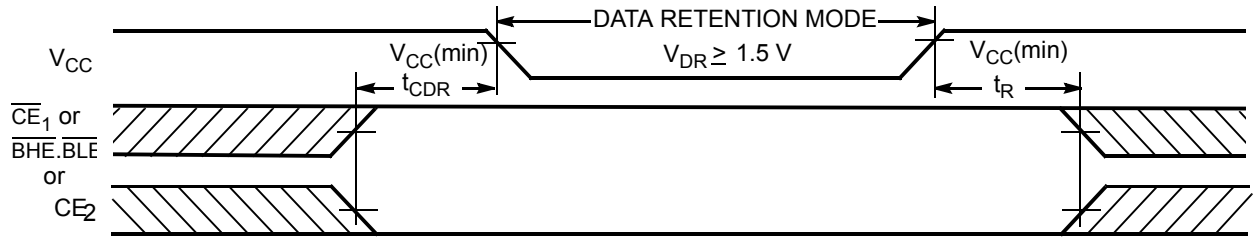
Parameters	2.2V to 2.7V	2.7V to 3.6V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[5]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}[10]	Data Retention Current	V_{CC} = 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			10	µA
t_{CDR}[11]	Chip Deselect to Data Retention Time		0			ns
t_R[12]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform[13]



Notes

12. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 µs or stable at V_{CC}(min) ≥ 100 µs.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range[14, 15]

Parameter	Description	45 ns		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[16]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16, 17]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[16]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[16, 17]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power Down		45	ns
t_{DBE}	BLE / BHE LOW to Data Valid		45	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[16]	10		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z[16, 17]		18	ns
WRITE CYCLE[18]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[16, 17]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[16]	10		ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{CC}(typ)/2, input pulse levels of 0 to V_{CC}(typ), and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 4.
15. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 1 shows address transition controlled read cycle waveforms.[19, 20]

Figure 1. Read Cycle No. 1

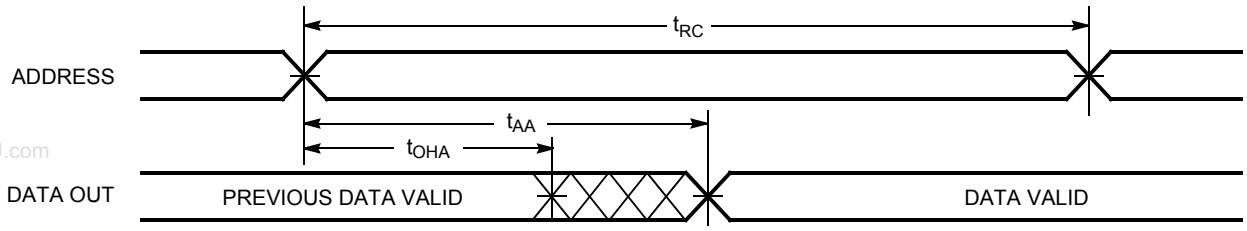
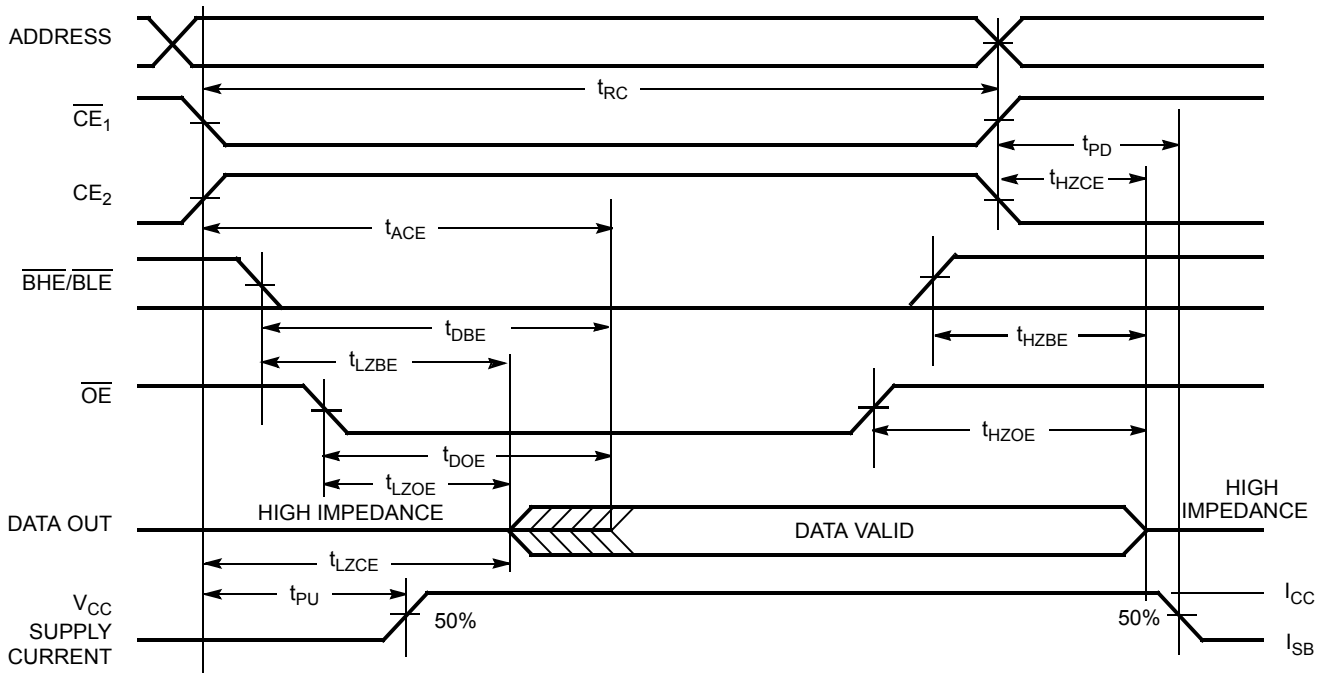


Figure 2 shows $\overline{OE}$ controlled read cycle waveforms.[20, 21]

Figure 2. Read Cycle No. 2

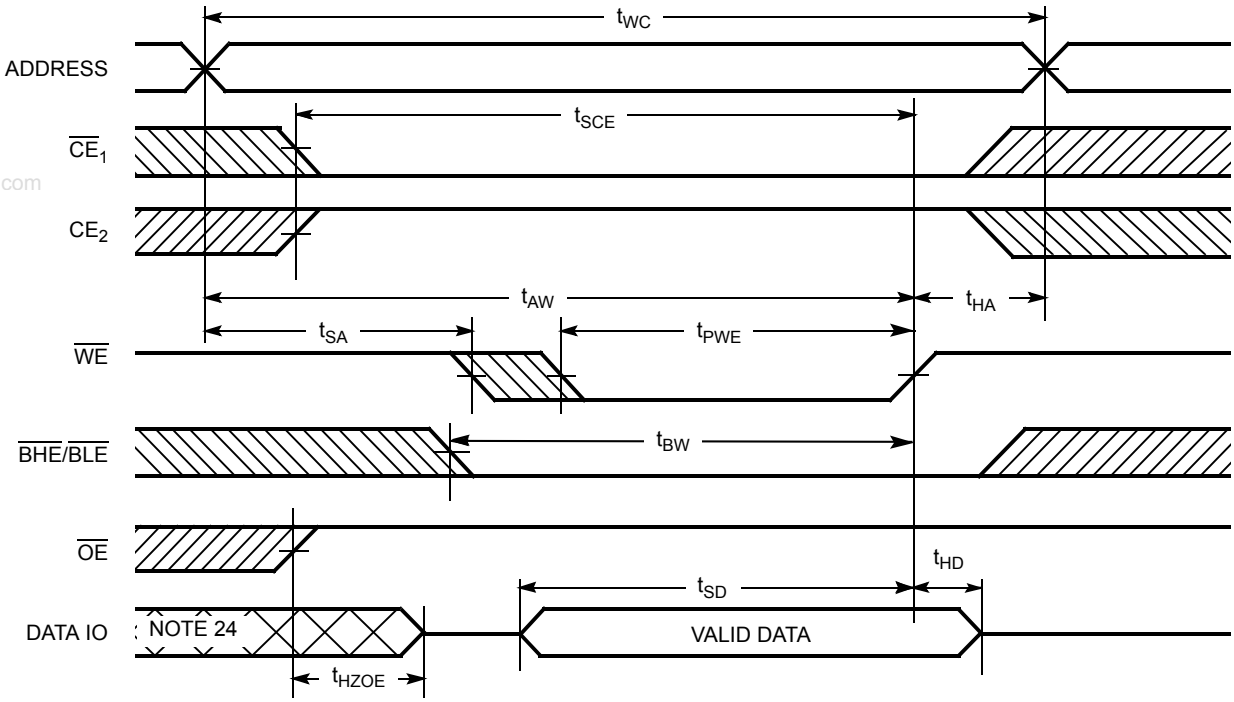


Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 3 shows $\overline{WE}$ controlled write cycle waveforms.[18, 22, 23]

Figure 3. Write Cycle No. 1



Notes
22. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
23. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
24. During this period the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 4 shows $\overline{CE}_1$ or CE_2 controlled write cycle waveforms.[18, 22, 23]

Figure 4. Write Cycle No. 2

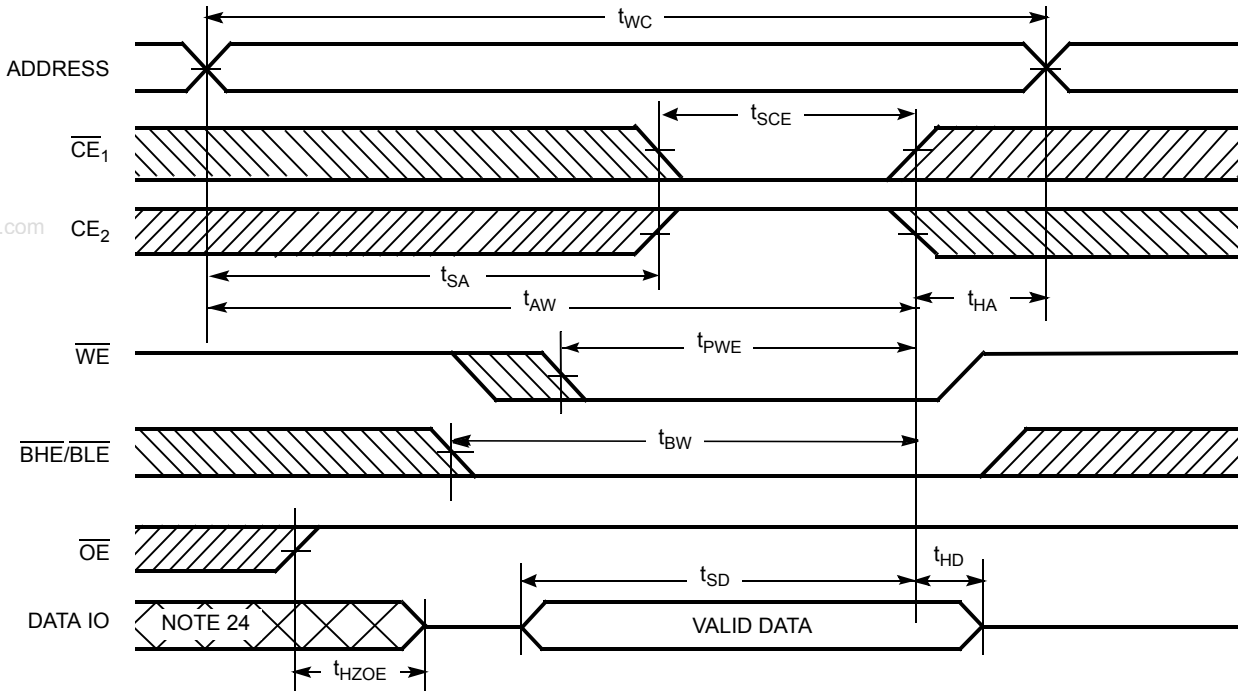
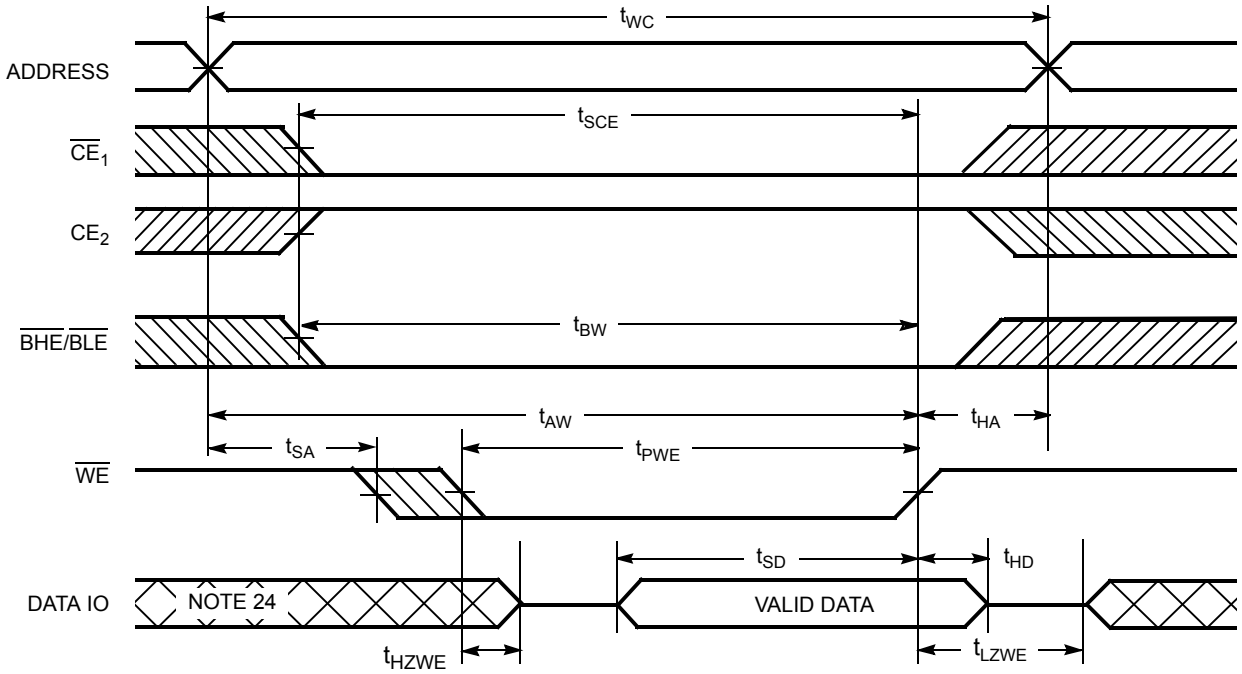


Figure 5 shows $\overline{WE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.[23]

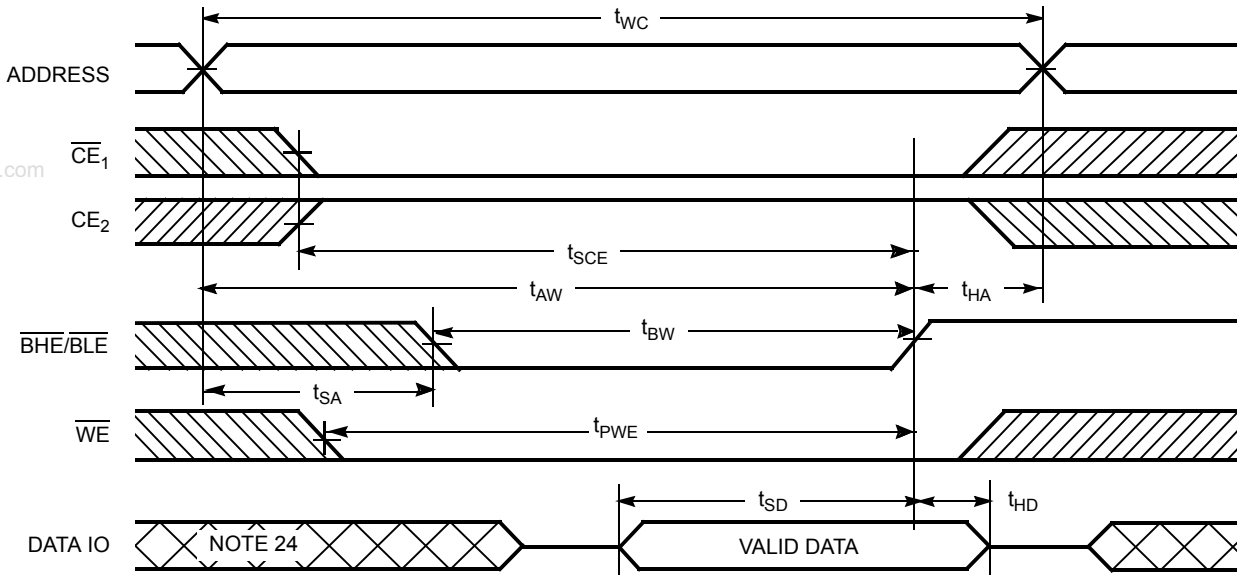
Figure 5. Write Cycle No. 3



Switching Waveforms (continued)

Figure 6 shows $\overline{BHE}/\overline{BLE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.[23]

Figure 6. Write Cycle No. 4



Truth Table

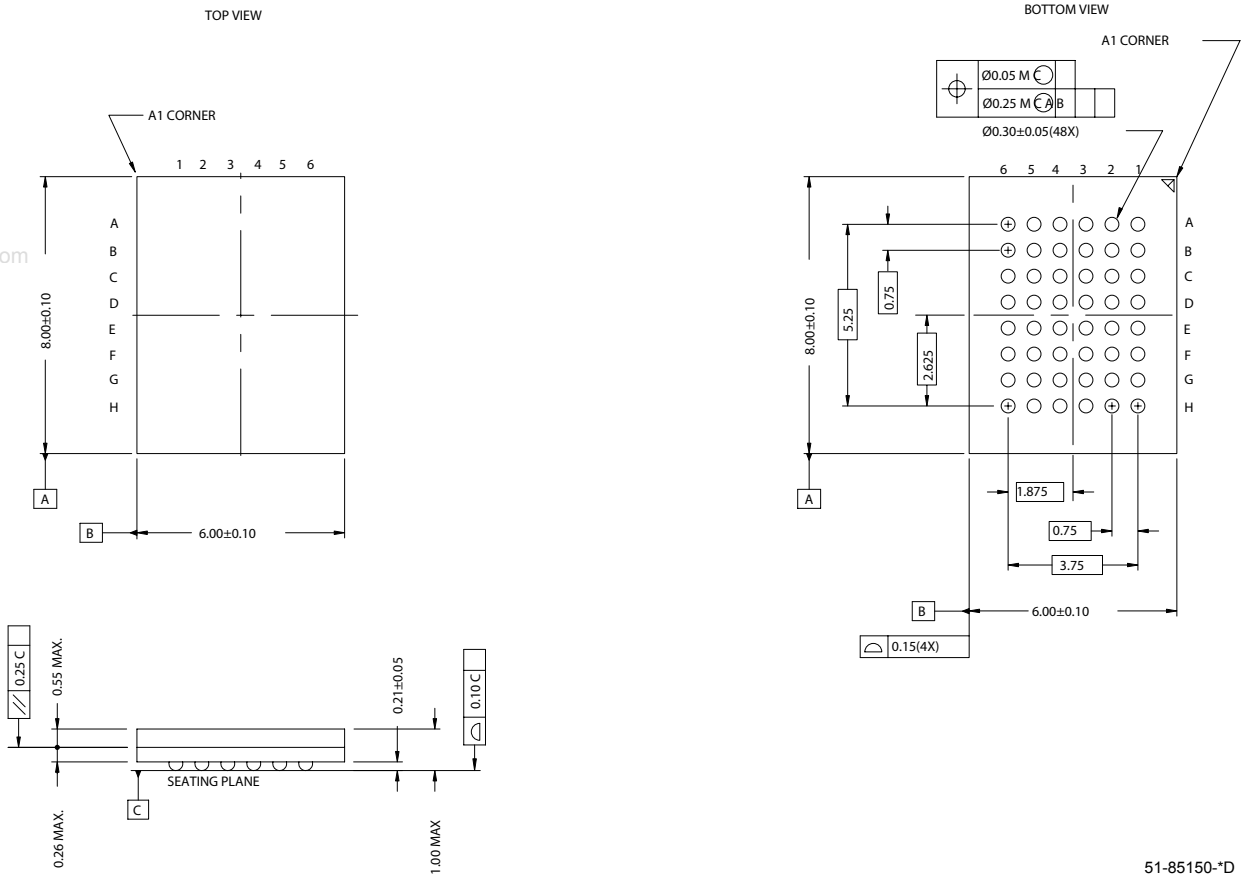
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (IO_0–IO_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (IO_0–IO_7); High Z (IO_8–IO_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (IO_0–IO_7); Data Out (IO_8–IO_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (IO_0–IO_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (IO_0–IO_7); High Z (IO_8–IO_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (IO_0–IO_7); Data In (IO_8–IO_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167EV30LL-45BVXI	51-85150	48-ball Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62167EV30LL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	

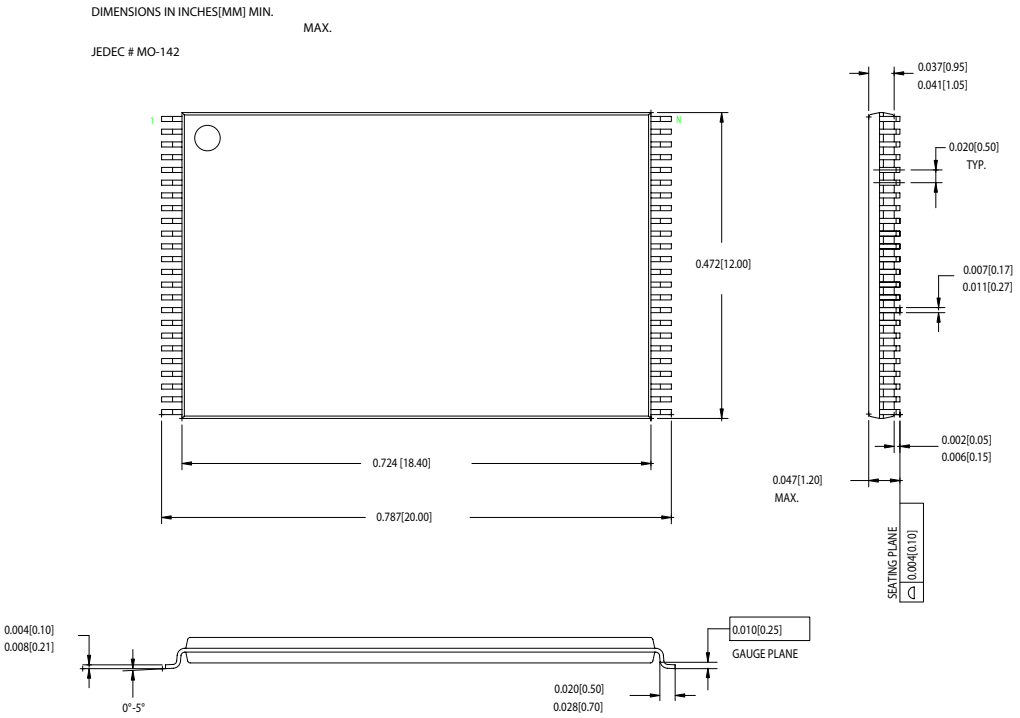
Package Diagrams

Figure 7. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



Package Diagrams (continued)

Figure 8. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



51-85183-*A

Document History Page

Document Title: CY62167EV30 MoBL® 16-Mbit (1M x 16 / 2M x 8) Static RAM Document Number: 38-05446				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	202600	01/23/04	AJU	New Data Sheet
*A	463674	See ECN	NXR	Converted from Advance Information to Preliminary Removed 'L' bin and 35 ns speed bin from product offering Modified Data sheet to include x8 configurability. Changed ball E3 in FBGA pinout from DNU to NC Changed the $I_{SB2(Typ)}$ value from 1.3 μA to 1.5 μA Changed the $I_{CC(Max)}$ value from 40 mA to 25 mA Changed Vcc stabilization time in footnote #9 from 100 μs to 200 μs Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics (t_R) from 100 μs to t_{RC} ns Changed t_{OHA}, t_{LZCE}, t_{LZBE}, and t_{LZWE} from 6 ns to 10 ns Changed t_{LZOE} from 3 ns to 5 ns. Changed t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE}, t_{AW}, and t_{BW} from 40 ns to 35 ns Changed t_{PE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Updated 48 ball FBGA Package Information. Updated the Ordering Information table
*B	469169	See ECN	NSI	Minor Change: Moved to external web
*C	1130323	See ECN	VKN	Converted from preliminary to final Changed I_{CC} max spec from 2.8 mA to 4.0 mA for f=1MHz Changed I_{CC} typ spec from 22 mA to 25 mA for f=f_{max} Changed I_{CC} max spec from 25 mA to 30 mA for f=f_{max} Added V_{IL} spec for TSOP I package and footnote# 9 Added footnote# 10 related to I_{SB2} and I_{CCDR} Changed I_{SB1} and I_{SB2} spec from 8.5 μA to 12 μA Changed I_{CCDR} spec from 8 μA to 10 μA Added footnote# 15 related to AC timing parameters