CY62187EV30 MoBL®

64-Mbit (4 M × 16) Static RAM

Features

- Very high speed
  - 55 ns
- Wide voltage range
  - 2.2 V to 3.7 V
- Ultra low standby power
  - Typical standby current: 8 µA
  - Maximum standby current: 48 µA
- Ultra low active power
  - Typical active current: 7.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball FBGA package

Functional Description

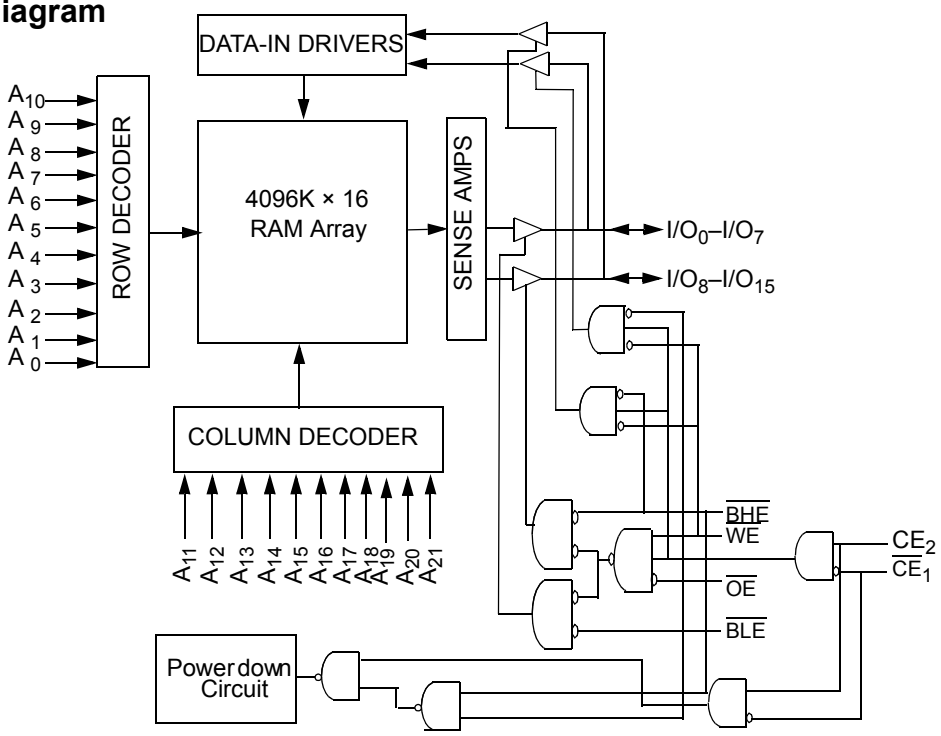
The CY62187EV30 is a high performance CMOS static RAM organized as 4 M words by 16-bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{21}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{21}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 9 for a complete description of read and write modes.

For a complete list of related documentation, click here.

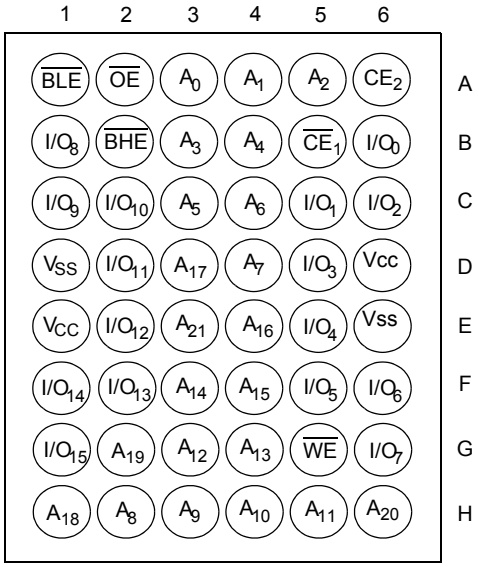
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball FBGA pinout



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ[1]	Max		Typ[1]	Max	Typ[1]	Max	Typ[1]	Max
CY62187EV30LL	2.2	3.0	3.7	55	7.5	9	45	55	8	48

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC Voltage Applied to Outputs in High Z State [2, 3] ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC Input Voltage [2, 3] ..... –0.3 V to $V_{CC\ (max)}$ + 0.3 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[4]
CY62187EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ [5]	Max	
V_{OH}	Output HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OH} = –0.1 mA	2.0	–	–	V
		2.7 V ≤ V_{CC} ≤ 3.7 V	I_{OH} = –1.0 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OL} = 0.1 mA	–	–	0.4	V
		2.7 V ≤ V_{CC} ≤ 3.7 V	I_{OL} = 2.1 mA	–	–	0.4	V
V_{IH}	Input HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		2.7 V ≤ V_{CC} ≤ 3.7 V		2.2	–	V_{CC} + 0.3 V	V
V_{IL}	Input LOW voltage	2.2 V≤ V_{CC} ≤ 2.7 V		–0.3	–	0.6	V
		2.7 V ≤ V_{CC} ≤ 3.7 V		–0.3	–	0.8[6]	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{Max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	45	55	mA
		f = 1 MHz		–	7.5	9	mA
I_{SB2} [7]	Automatic CE power down current — CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.7 V		–	8	48	µA

Notes

2. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
4. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
6. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions input LOW Voltage applied to the device must not be higher than 0.7 V.
7. Chip enables ($\overline{CE_1}$ and CE_2), Address Pins A_{20}, A_{21} and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	25	pF
C_{OUT}	Output capacitance		35	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	FBGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	42.35	°C/W
θ_{JC}	Thermal resistance (junction to case)		6.25	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

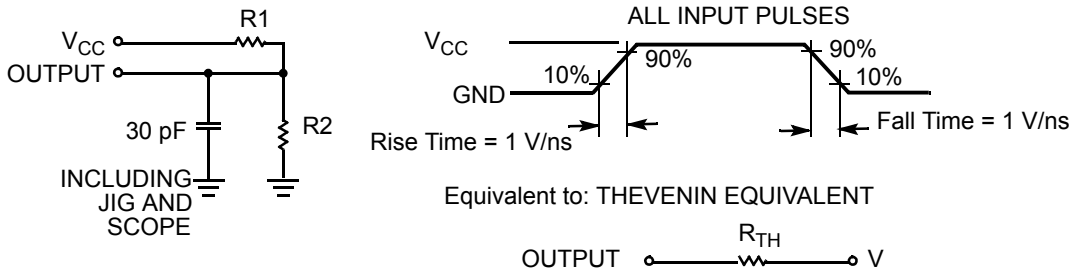


Table 1. AC Test Loads

Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

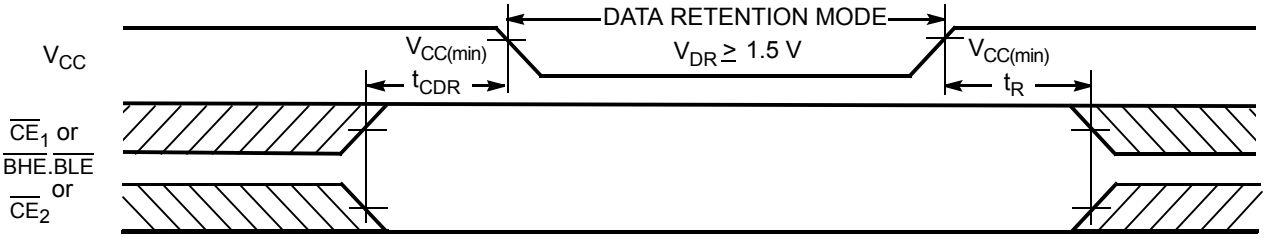
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} [10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	48	µA
t_{CDR} [11]	Chip deselect to data retention time		0	–	–	ns
t_R [12]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform [13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE_1}$ and CE_2), Address Pins A_{20}, A_{21} and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip is deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	6	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[16, 17]	–	20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z[16]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to high Z[16, 17]	–	20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down	–	55	ns
t_{DBE}	BLE/BHE LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z [16]	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z [16, 17]	–	20	ns
Write Cycle[18, 19]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	45	–	ns
t_{AW}	Address setup to write end	45	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	45	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[16, 17]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH}, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 6.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
18. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [20, 21]

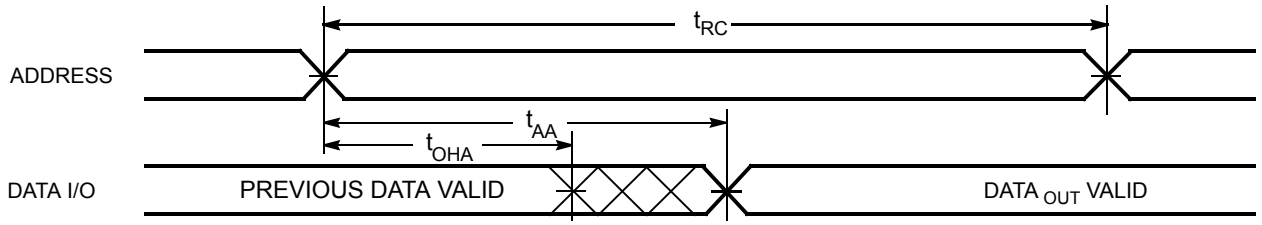
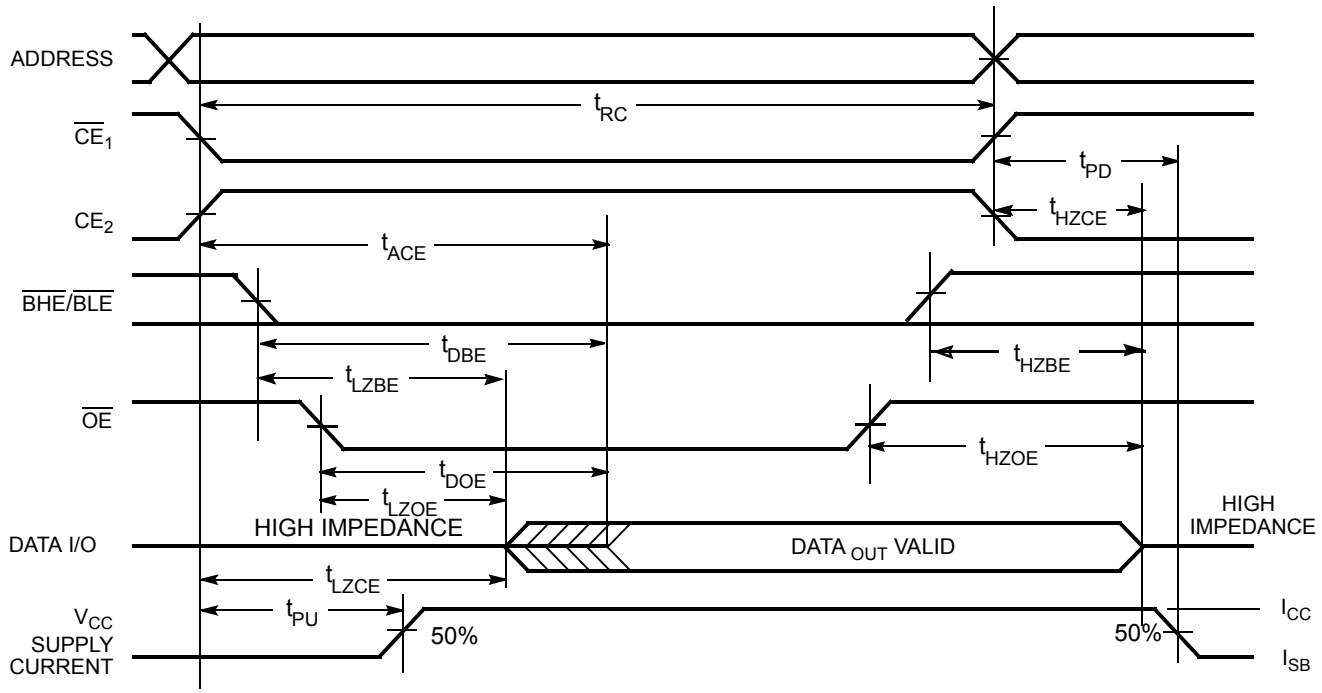


Figure 5. Read Cycle 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms *(continued)*

Figure 6. Write Cycle 1 ($\overline{WE}$ Controlled) [23, 24, 25, 26]

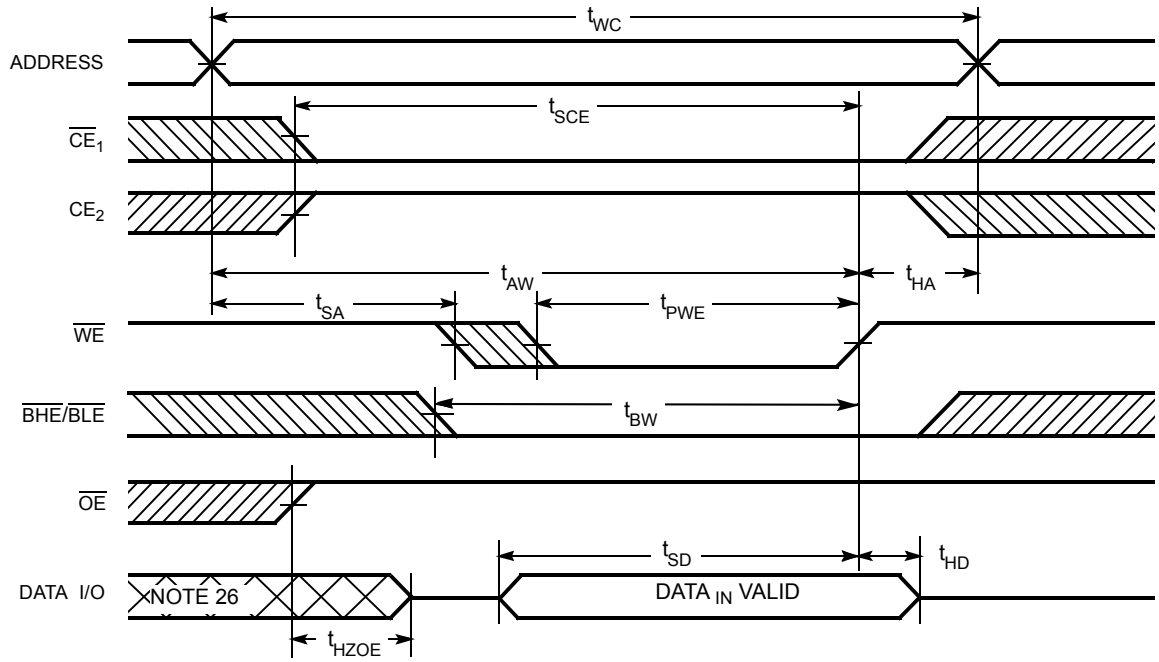
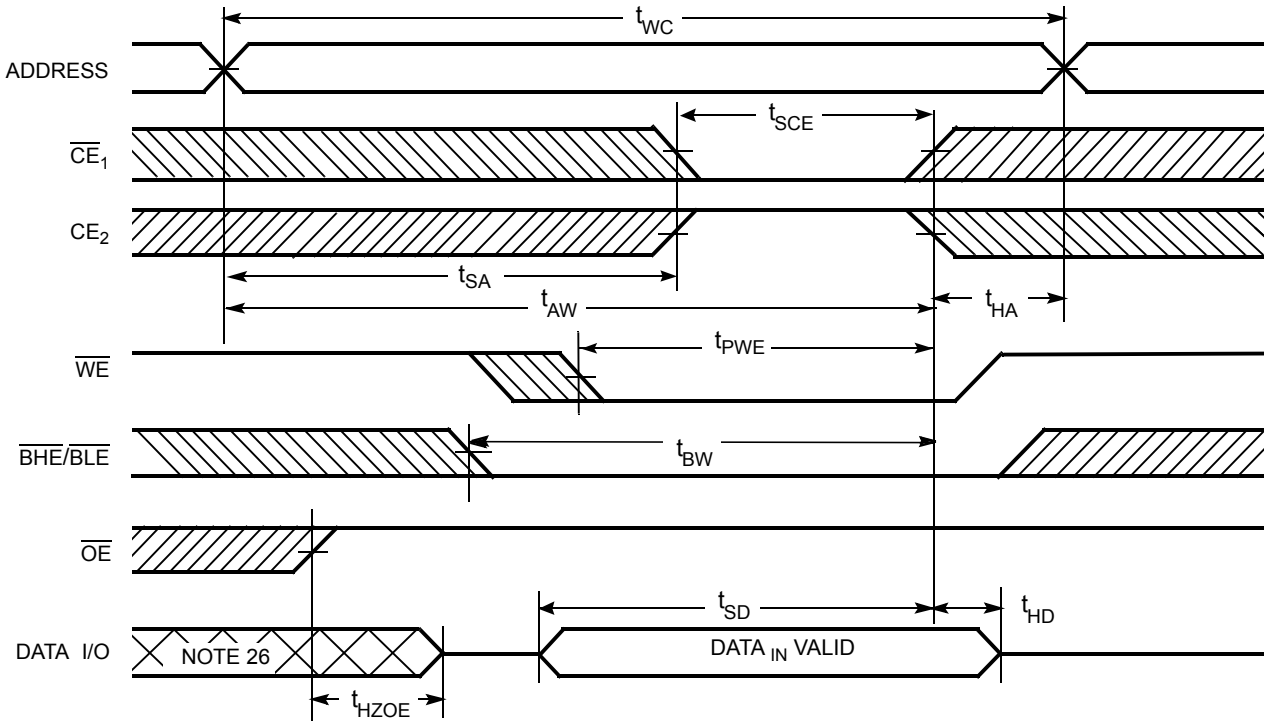


Figure 7. Write Cycle 2 ($\overline{CE}_1$ or CE_2 Controlled) [23, 24, 25, 26]



Notes

23. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
25. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
26. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms *(continued)*

Figure 8. Write Cycle 3 (WE Controlled, OE LOW) [27, 28, 29]

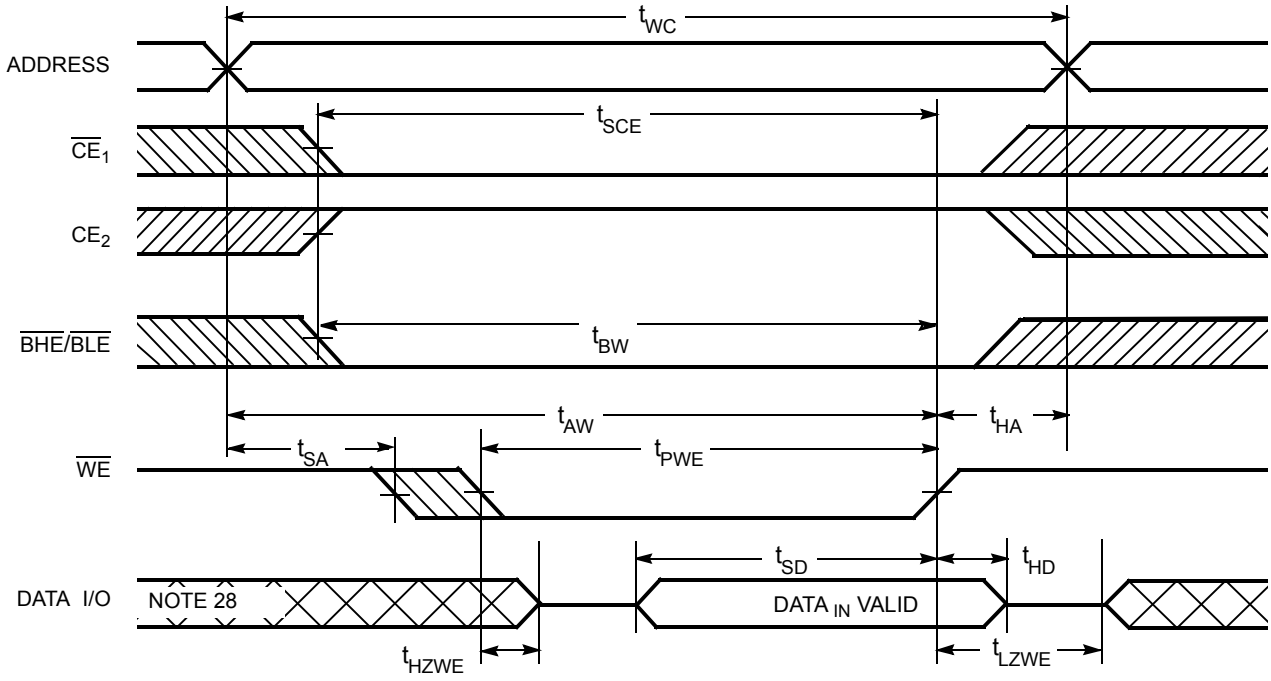
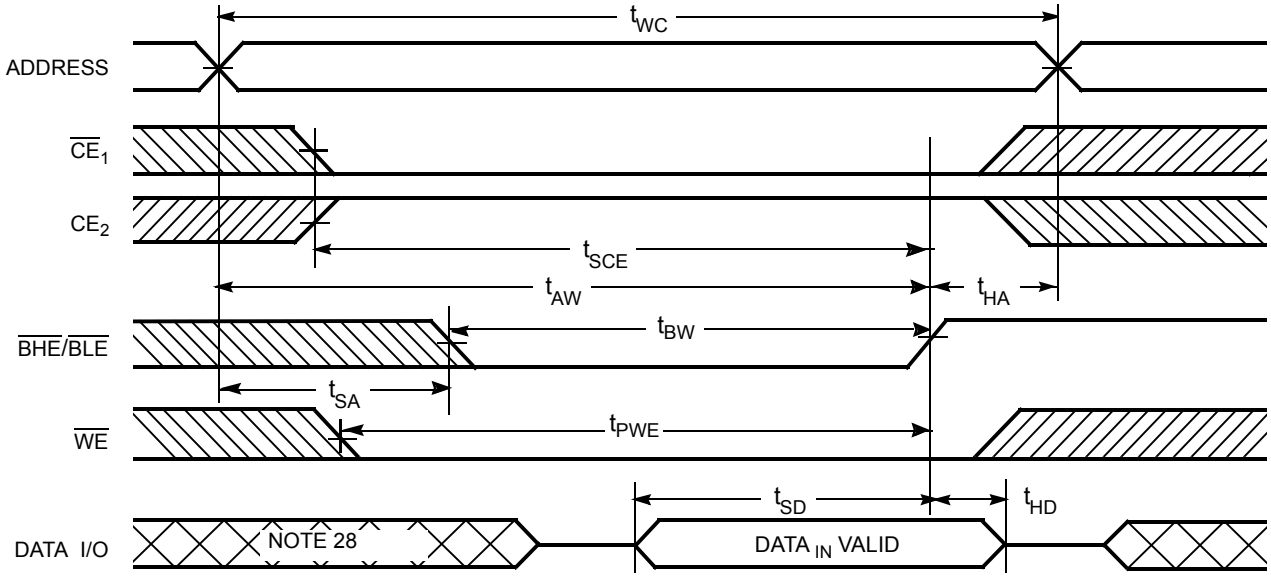


Figure 9. Write Cycle 4 (BHE/BLE Controlled, OE LOW) [27, 28]



Notes
27. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. During this period the I/Os are in output state and input signals should not be applied.
29. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

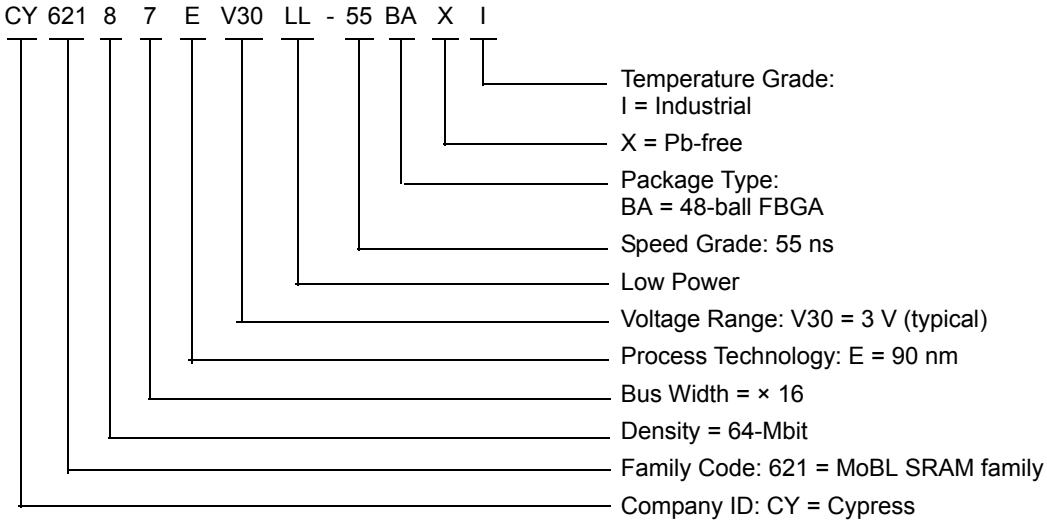
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X[30]	X	X	X[30]	X[30]	High Z	Deselect/Power Down	Standby (I_{SB})
X[30]	L	X	X	X[30]	X[30]	High Z	Deselect/Power Down	Standby (I_{SB})
X[30]	X[30]	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (I/O_8–I/O_{15}); Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (I/O_8–I/O_{15}); Data In (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

Note
30. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

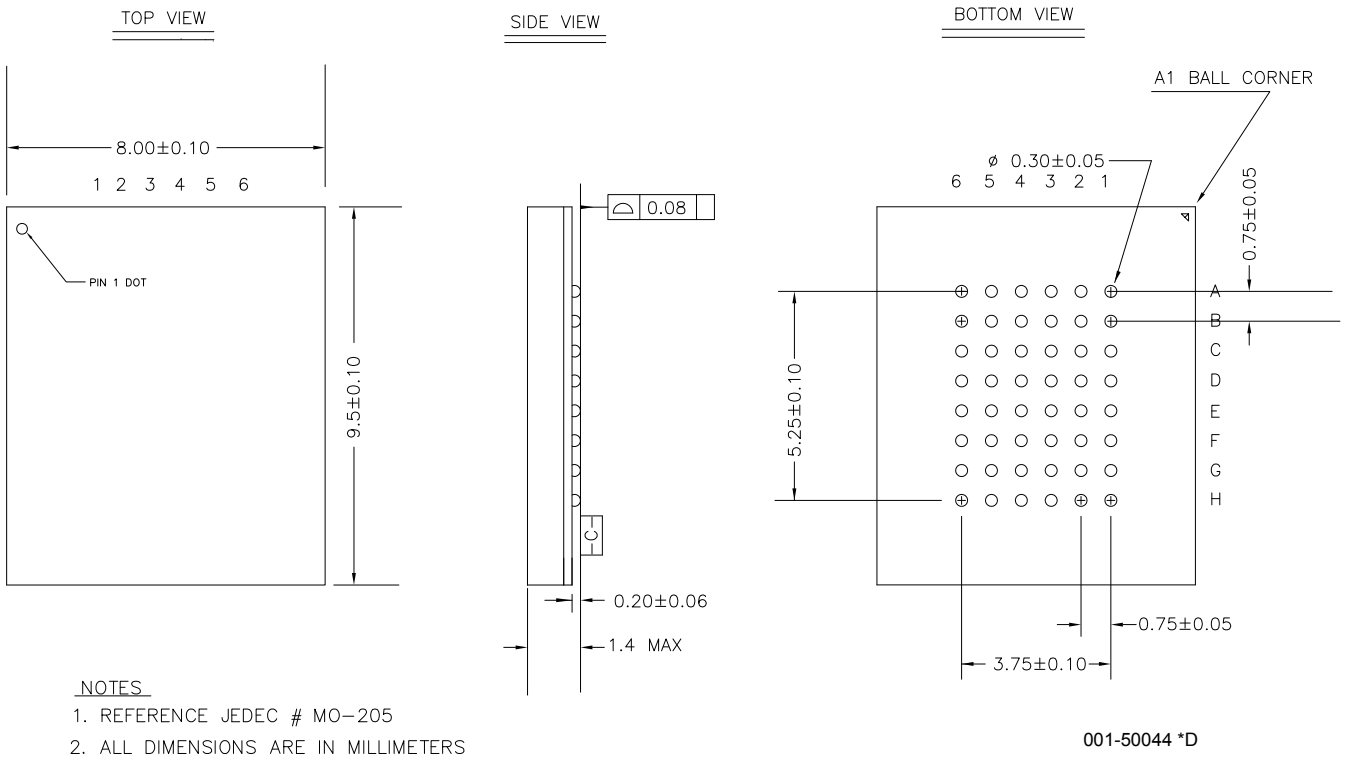
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62187EV30LL-55BAXI	001-50044	48-ball FBGA (8 × 9.5 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball FBGA (8 × 9.5 × 1.4 mm) BK48L Package Outline, 001-50044



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohms
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62187EV30 MoBL®, 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2595932	VKN / PYRS	10/24/08	New data sheet.
*A	2644442	VKN / PYRS	01/23/09	Updated Package Diagram.
*B	2672650	VKN / PYRS	03/12/09	Added 55 ns speed bin related information in all instances across the document. Updated Product Portfolio: Changed maximum value in V_{CC} range from 3.6 V to 3.7 V. Changed typical value of "Operating I_{CC}" from 2.5 mA to 3.5 mA at f = 1 MHz corresponding to 70 ns speed bin. Changed maximum value of "Operating I_{CC}" from 4 mA to 6 mA at f = 1 MHz corresponding to 70 ns speed bin. Changed typical value of "Operating I_{CC}" form 33 mA to 28 mA at f = f_{MAX} corresponding to 70 ns speed bin. Changed maximum value of "Operating I_{CC}" from 40 mA to 45 mA at f = f_{MAX} corresponding to 70 ns speed bin. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 33 mA to 28 mA at f = f_{MAX} corresponding to 70 ns speed bin. Changed maximum value of I_{CC} parameter from 40 mA to 45 mA at f = f_{MAX} corresponding to 70 ns speed bin. Changed typical value of I_{CC} parameter from 2.5 mA to 3.5 mA at f = 1 MHz corresponding to 70 ns speed bin. Changed maximum value of I_{CC} parameter from 4 mA to 6 mA at f = 1 MHz corresponding to 70 ns speed bin. Updated Note 7. Updated Switching Characteristics: Changed minimum value of t_{PWE} parameter from 45 ns to 50 ns corresponding to 70 ns speed bin. Changed minimum value of t_{SD} parameter from 30 ns to 35 ns corresponding to 70 ns speed bin. Updated Package Diagram: Changed 48-ball FBGA package dimensions from "8 × 9.5 × 1.6 mm" to "8 × 9.5 × 1.4 mm". spec 001-50044 – Changed revision from ** to *A.
*C	2737164	VKN / AESA	07/13/09	Changed status from Preliminary to Final. Updated Product Portfolio: Changed typical value of "Operating I_{CC}" from 3.5 mA to 4 mA at f = 1 MHz corresponding to 55 ns and 70 ns speed bins. Changed typical value of "Operating I_{CC}" from 35 mA to 45 mA at f = f_{max} corresponding to 55 ns speed bin. Changed typical value of "Operating I_{CC}" from 28 mA to 35 mA at f = f_{max} corresponding to 70 ns speed bin.

Document History Page *(continued)*

Document Title: CY62187EV30 MoBL®, 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C (cont.)	2737164	VKN / AESA	07/13/09	Updated Electrical Characteristics: Updated details in "Test Conditions" column of V_{OH}, V_{OL}, V_{IH}, V_{IL} parameters (Included V_{CC} range). Changed maximum value of V_{IL} parameter from 0.8 V to 0.7 V corresponding to Test Condition "V_{CC} = 2.7 V to 3.7 V". Changed typical value of I_{CC} parameter from 35 mA to 45 mA at f = f_{max} corresponding to 55 ns speed bin. Changed typical value of I_{CC} parameter from 28 mA to 35 mA at f = f_{max} corresponding to 70 ns speed bin. Changed typical value of I_{CC} parameter from 3.5 mA to 4 mA at f = 1 MHz corresponding to 55 ns and 70 ns speed bins. Updated Capacitance: Changed maximum value of C_{IN} parameter from 20 pF to 25 pF. Changed maximum value of C_{OUT} parameter from 20 pF to 35 pF. Updated Thermal Resistance: Replaced TBD with values for 48-ball FBGA package. Updated AC Test Loads and Waveforms: Updated Table 1: Included V_{CC} range for V_{TH} parameter. Updated Switching Characteristics: Changed minimum value of t_{LZBE} parameter from 5 ns to 10 ns. Updated Truth Table: Added Note 30 and referred the same note in "X" in "$\overline{CE}_1$" and "CE_2" columns.
*D	2765892	VKN	09/18/09	Removed 70 ns speed bin related information in all instances across the document. Updated Product Portfolio: Changed maximum value of "Operating I_{CC}" from 6 mA to 9 mA at f = 1 MHz corresponding to 55 ns speed bin. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 4 mA to 7.5 mA at f = 1 MHz corresponding to 55 ns speed bin. Changed maximum value of I_{CC} parameter from 6 mA to 9 mA at f = 1 MHz corresponding to 55 ns speed bin.
*E	3177000	AJU	02/18/2011	Updated Features: Changed value of "Typical Active Current" from 4 mA to 7.5 mA. Updated Pin Configuration: Fixed typo in Figure 1 (Renamed "48-Ball VFBGA" as "48-ball FBGA"). Updated Product Portfolio: Changed typical value of "Operating I_{CC}" from 4 mA to 7.5 mA at f = 1 MHz corresponding to 55 ns speed bin. Updated Electrical Characteristics: Updated details in "Test Conditions" column of I_{SB2} parameter (Included $\overline{BHE}$ and $\overline{BLE}$ to reflect Byte power down feature). Updated AC Test Loads and Waveforms: Updated Table 1. Updated Data Retention Characteristics: Updated details in "Test Conditions" column of I_{CCDR} parameter (Included $\overline{BHE}$ and $\overline{BLE}$ to reflect Byte power down feature). Changed minimum value of t_R parameter from t_{RC} to 55 ns. Added Ordering Code Definitions under Ordering Information. Updated Package Diagram. Added Acronyms and Units of Measure. Changed all instances of IO to I/O. Updated to new template.

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*F	3282088	RAME	06/14/2011	Updated Functional Description: Removed the note “For best practice recommendations, refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com website” and its reference. Updated Electrical Characteristics: Changed maximum value of V_{IL} parameter corresponding to Test Condition “2.7 V ≤ V_{CC} ≤ 3.7 V” from 0.7 V to 0.8 V. Added Note 6 and referred the same note in maximum value of V_{IL} parameter. Updated to new template.
*G	3785005	TAVA	10/18/2012	Minor text edits. Updated Package Diagram: spec 001-50044 – Changed revision from *C to *D.
*H	4101127	VINI	08/21/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in “Parameter” column. Updated to new template. Completing Sunset Review.
*I	4114808	NILE	09/12/2013	Updated Electrical Characteristics: Updated Note 7. Updated Data Retention Characteristics: Updated Note 10.
*J	4576478	NILE	11/21/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 29 and referred the same note in Figure 8.
*K	4990839	VINI	10/27/2015	Updated Thermal Resistance: Replaced “2-layer” with “four-layer” in “Test Conditions” column. Changed value of θ_{JA} parameter corresponding to FBGA package from 59.06 °C/W to 42.35 °C/W. Changed value of θ_{JC} parameter corresponding to FBGA package from 14.08 °C/W to 6.25 °C/W. Updated to new template. Completing Sunset Review.
*L	5962070	AESATMP8	11/09/2017	Updated logo and Copyright.

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