

128K x 8 Static RAM

Features

- High speed
 - $t_{AA} = 10, 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with \overline{CE} and \overline{OE} options
- Functionally equivalent to CY7C1019

Functional Description

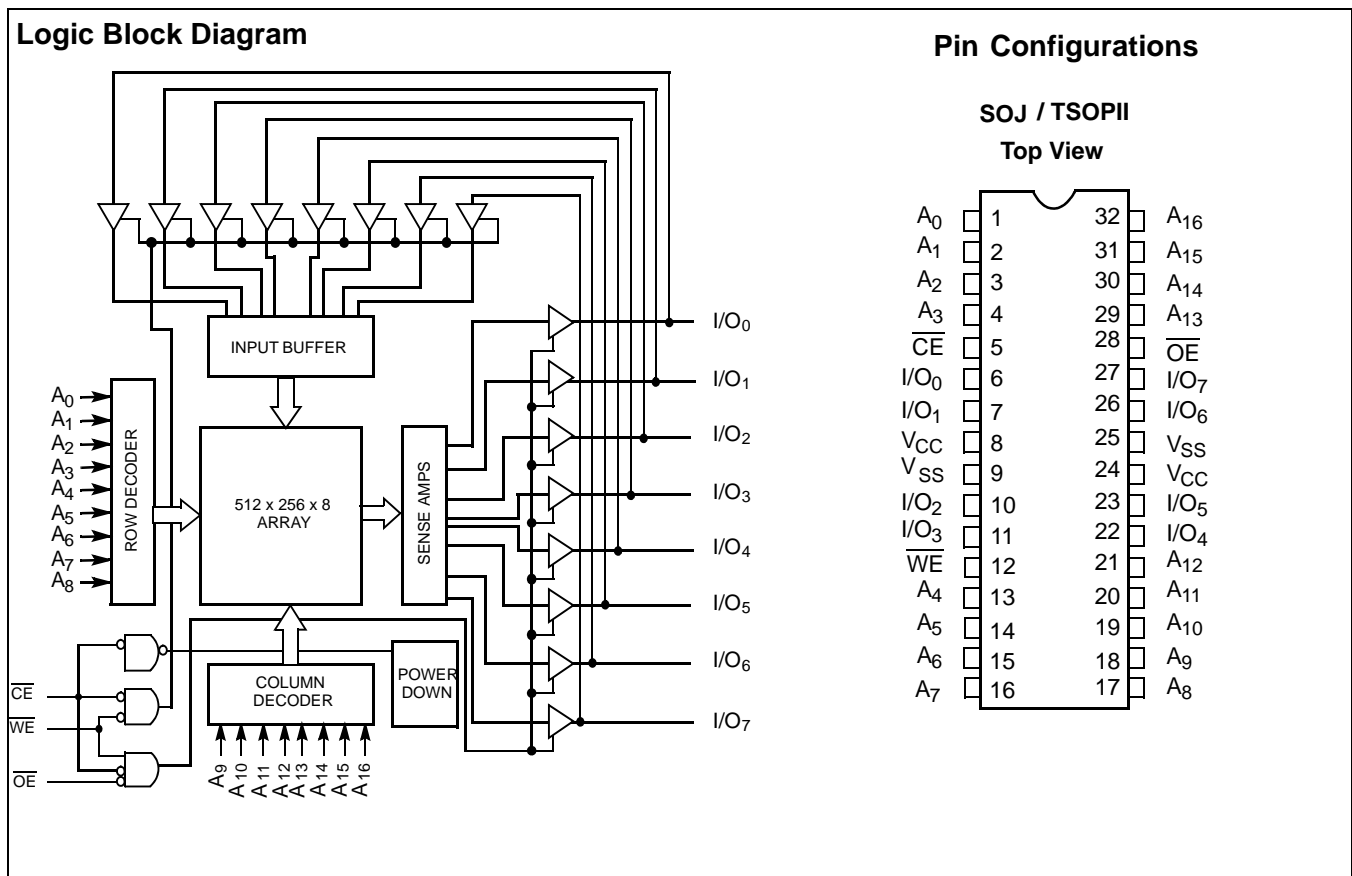
The CY7C1019B/10191B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1019B/10191B is available in standard 32-pin TSOP Type II and 400-mil-wide SOJ packages. Customers should use part number CY7C10191B when ordering parts with 10 ns t_{AA} , and CY7C1019B when ordering 12 and 15 ns t_{AA} .



Selection Guide

	7C10191B-10	7C1019B-12	7C1019B-15	Unit
Maximum Access Time	10	12	15	ns
Maximum Operating Current	150	140	130	mA
Maximum Standby Current	10	10	10	mA
	L	–	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[1] –0.5V to V_{CC} + 0.5V

DC Input Voltage^[1]..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C10191B-10		7C1019B-12		7C1019B-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = – 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	–1	+1	–1	+1	–1	+1	µA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	–5	+5	–5	+5	–5	+5	µA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		150		140		130	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		40		40	mA
			L	20		20		20	
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} – 0.3V, V _{IN} ≥ V _{CC} – 0.3V, or V _{IN} ≤ 0.3V, f = 0		10		10		10	mA
			L	–		1		1	

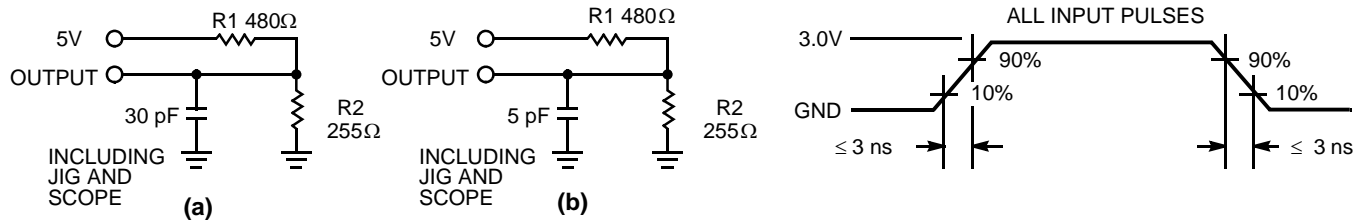
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	6	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V		

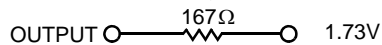
Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the “Instant On” case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics^[4] Over the Operating Range

Parameter	Description	7C10191B-10		7C1019B-12		7C1019B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		10		12		15	ns
Write Cycle^[7, 8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	8		9		10		ns
t_{AW}	Address Set-Up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[5, 6]		5		6		7	ns

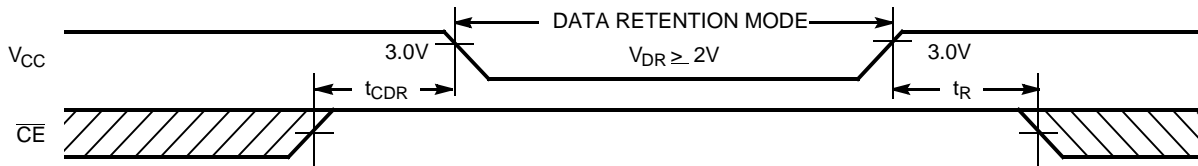
Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range (L Version Only)

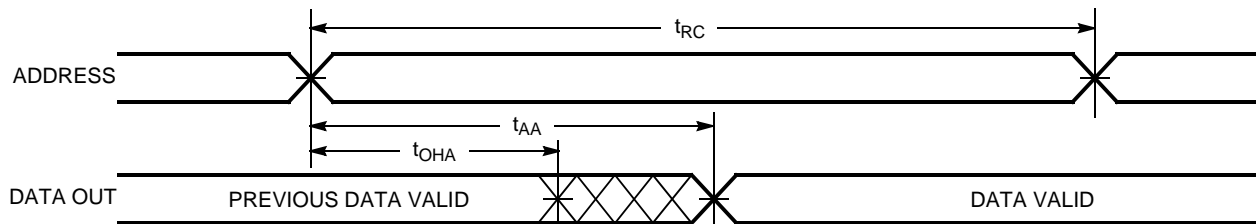
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed $V_{CC} + 0.5V$ $V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current			300	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		200		μs

Data Retention Waveform

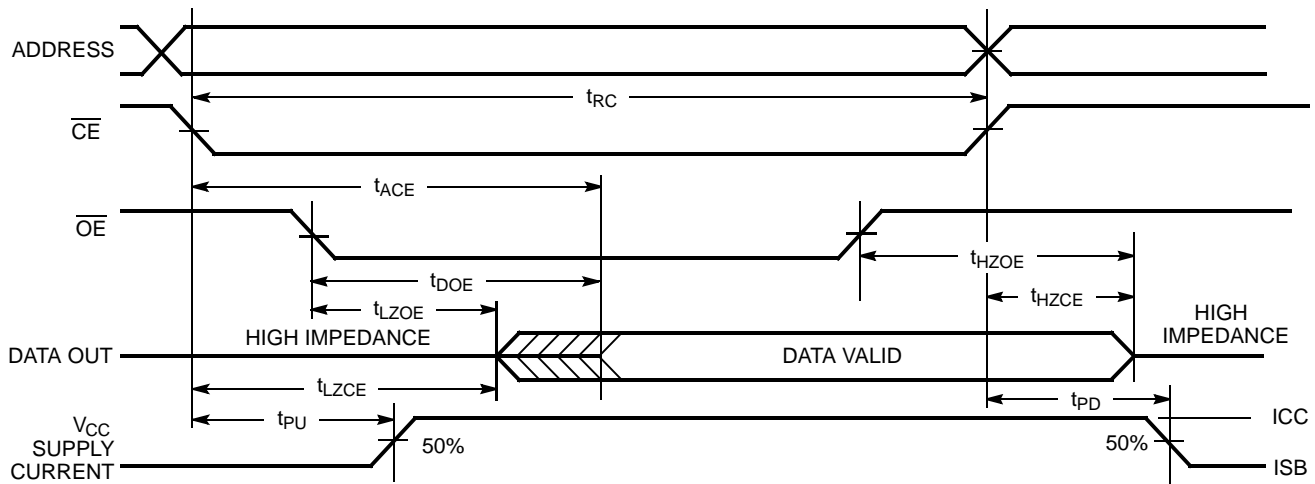


Switching Waveforms

Read Cycle No. 1 ^[9, 10]



Read Cycle No. 2 (OE Controlled) ^[10, 11]

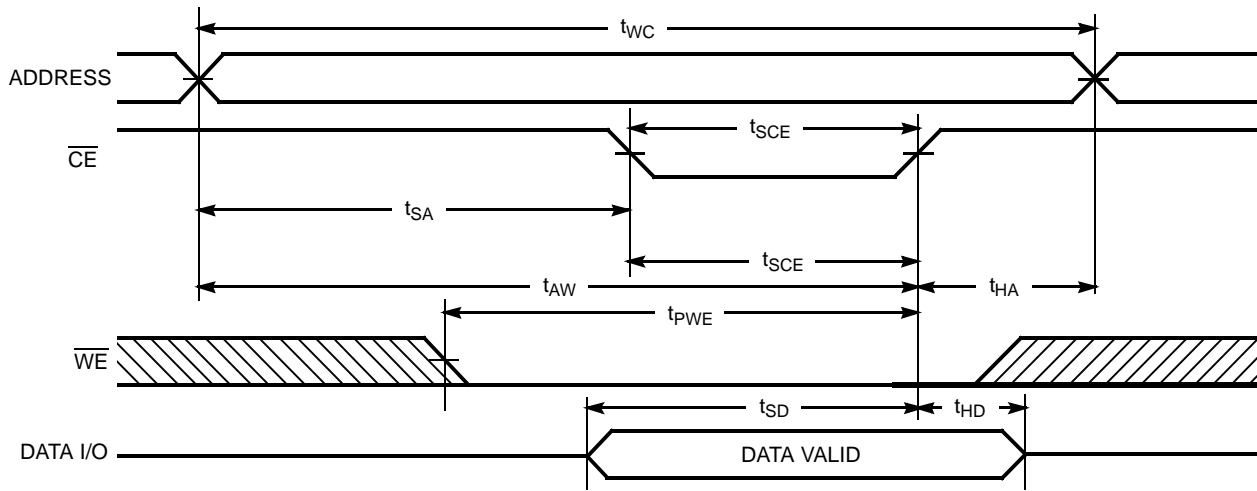


Notes:

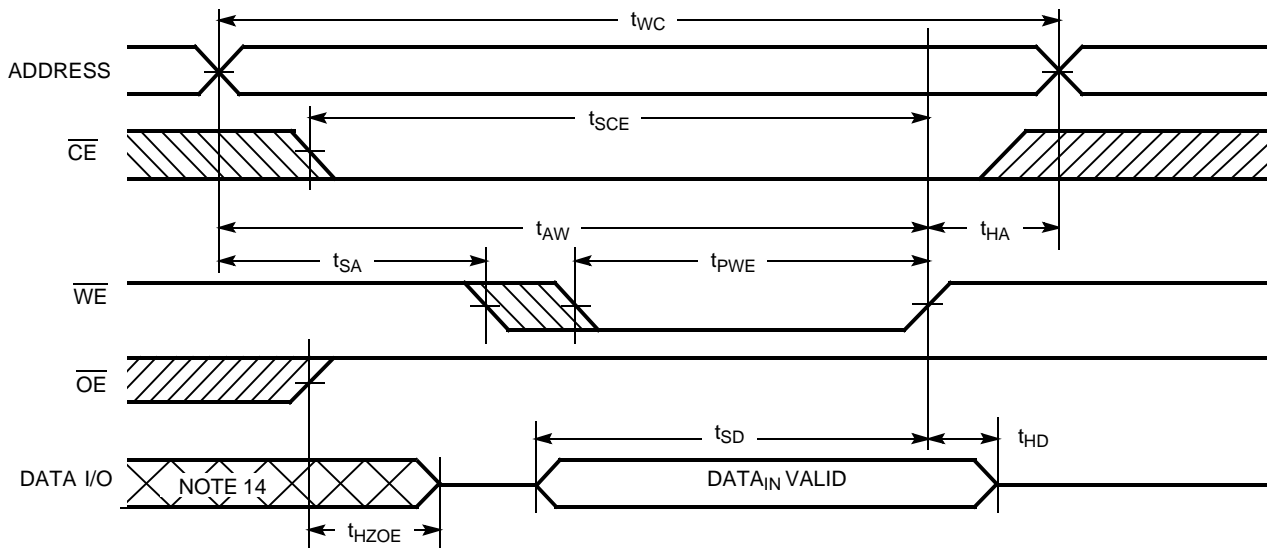
- 9. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- 10. WE is HIGH for read cycle.
- 11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (CE Controlled)^[12, 13]



Write Cycle No. 2 (WE Controlled, OE HIGH During Write)^[12, 13]

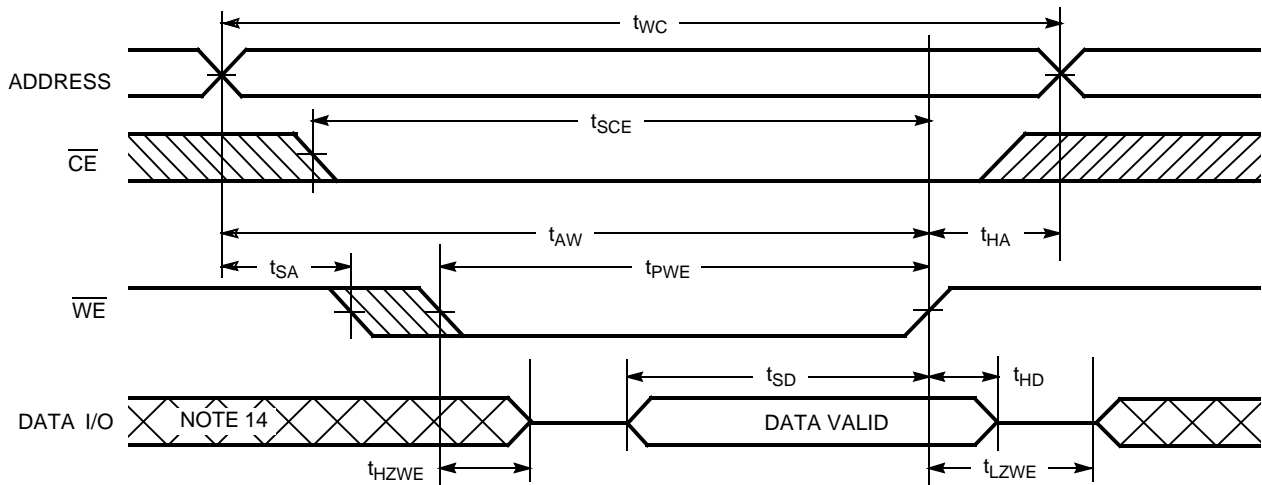


Notes:

- 12. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 13. If \overline{CE} goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
- 14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[13]



Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I _{SB})
X	X	X	High Z	Power-Down	Standby (I _{SB})
L	L	H	Data Out	Read	Active (I _{CC})
L	X	L	Data In	Write	Active (I _{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

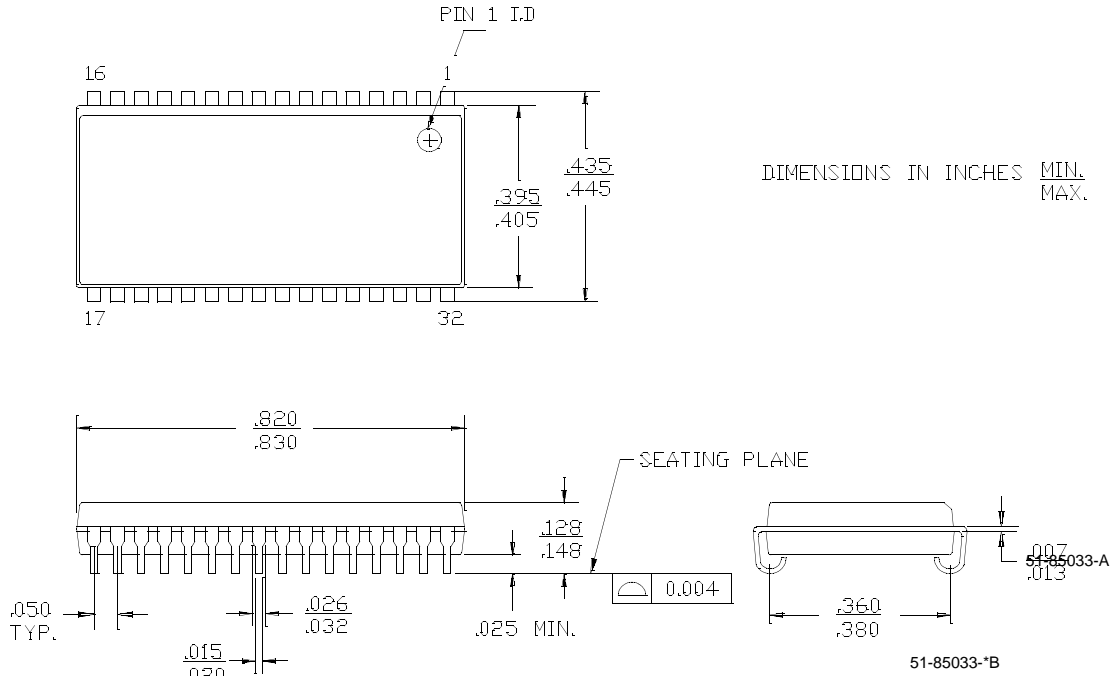
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1019B-12VC	V33	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019B-12ZC	ZS32	32-Lead TSOP Type II	
	CY7C1019B-12ZXC	ZS32	32-Lead TSOP Type II (Pb -Free)	
15	CY7C1019B-15VC	V33	32-Lead 400-Mil Molded SOJ	Commercial
	CY7C1019B-15VI	V33	32-Lead 400-Mil Molded SOJ	Industrial
	CY7C1019B-15ZC	ZS32	32-Lead TSOP Type II	Commercial
	CY7C1019B-15ZXC	ZS32	32-Lead TSOP Type II (Pb -Free)	
	CY7C1019B-15ZI	ZS32	32-Lead TSOP Type II	Industrial

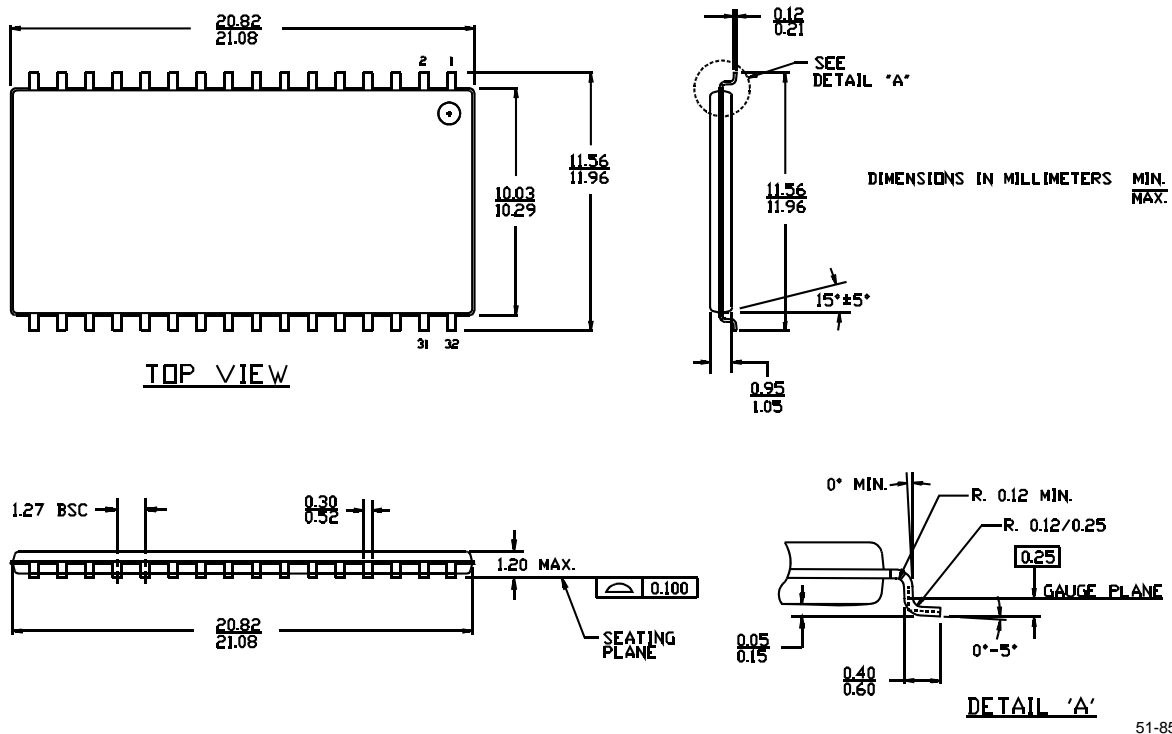
Please contact local sales representative regarding availability of parts

Package Diagrams

32-Lead (400-mil) Molded SOJ V33



32-Lead TSOP II ZS32



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Document History Page

Document Title: CY7C1019B/CY7C10191B 128K x 8 Static RAM				
Document Number: 38-05026				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109949	09/25/01	SZV	Change from Spec number: 38-01115 to 38-05026
*A	116170	08/14/02	HGK	1. SOJ (400-mil) package outline replacing incorrect SOJ package 2. Pin for pin compatible with CY7C1019 3. Industrial packages added to Ordering Information
*B	397875	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Updated the Ordering Information Table on page # 6.