CY7C1049G
CY7C1049GE

4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns
- Embedded ECC for single-bit error correction[1]
- Low active and standby currents
  - Active current: I_{CC} = 38 mA typical
  - Standby current: I_{SB2} = 6 mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Pb-free 36-pin SOJ and 44-pin TSOP II packages

Functional Description

CY7C1049G and CY7C1049GE are high-performance CMOS fast static RAM devices with embedded ECC. Both devices are offered in single and dual chip-enable options and in multiple pin configurations. The CY7C1049GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

Data writes are performed by asserting the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW, while providing the data on I/O_0 through I/O_7 and address on A_0 through A_{18} pins.

Data reads are performed by asserting the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_7).

All I/Os (I/O_0 through I/O_7) are placed in a high-impedance state during the following events:

- The device is deselected ($\overline{CE}$ HIGH)
- The control signal $\overline{OE}$ is de-asserted

On the CY7C1049GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH)[1]. See the Truth Table on page 14 for a complete description of read and write modes.

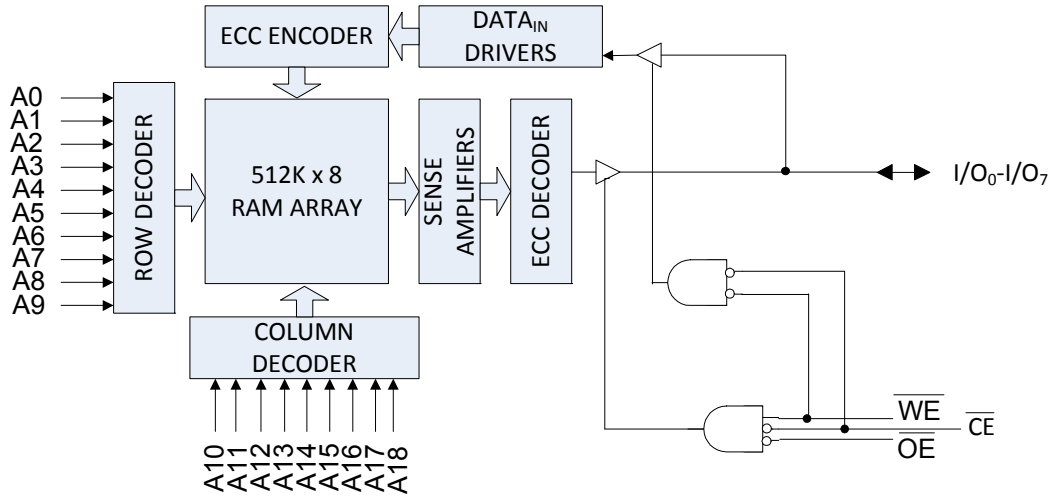
The logic block diagram is on page 2.

Product Portfolio

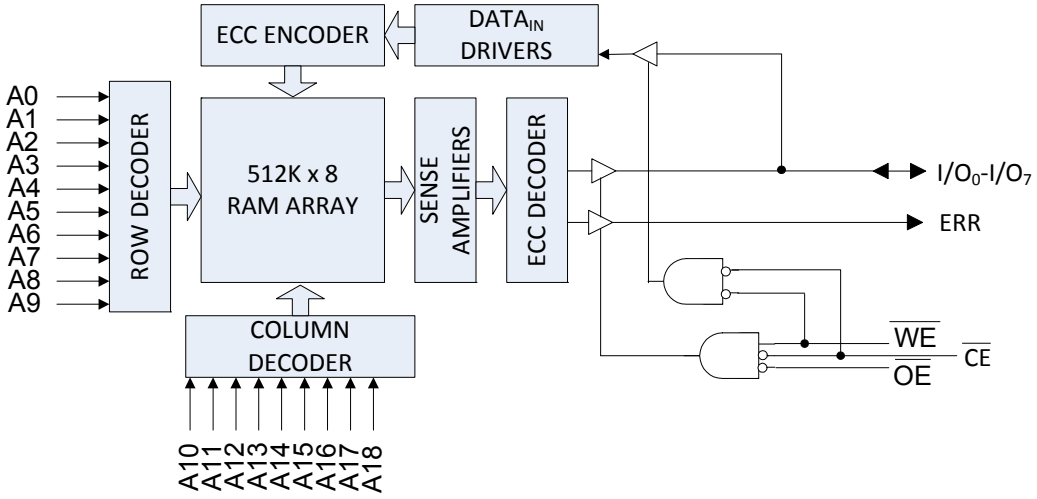
Product[2]	Features and Options (see Pin Configurations on page 4)	Range	V_{CC} Range (V)	Speed (ns) 10/15	Power Dissipation			
					Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
					Typ[3]	Max	Typ[3]	Max
CY7C1049G(E)18	Single or Dual Chip Enables	Industrial	1.65 V–2.2 V	15	–	40	6	8
CY7C1049G(E)30	Optional ERR pins		2.2 V–3.6 V	10	38	45		
CY7C1049G(E)			4.5 V–5.5 V	10	38	45		

Notes
1. This device does not support automatic write-back on error detection.
2. The ERR pin is available only for devices which have ERR option “E” in the ordering code. Refer Ordering Information on page 15 for details.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1049G



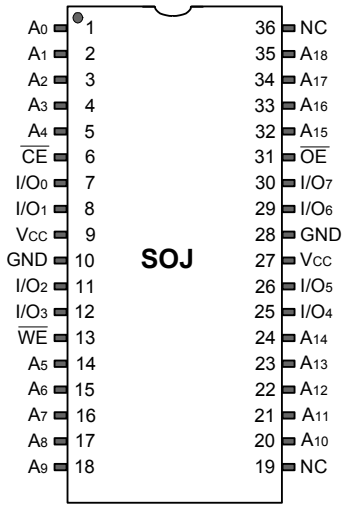
Logic Block Diagram – CY7C1049GE



Contents

Pin Configurations

Figure 1. 36-pin SOJ pinout, Single Chip Enable without ERR - CY7C1049G [4]



Note
4. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 2. 44-pin TSOP II pinout, Single Chip Enable without ERR - CY7C1049G [5]

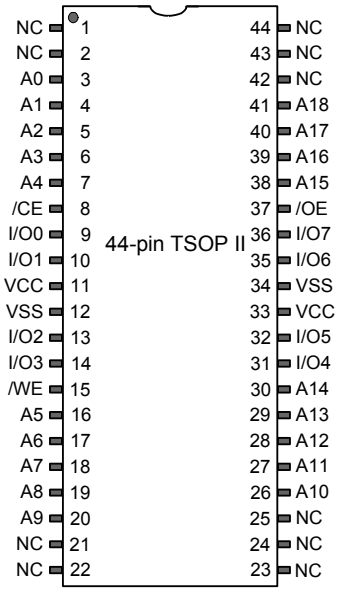
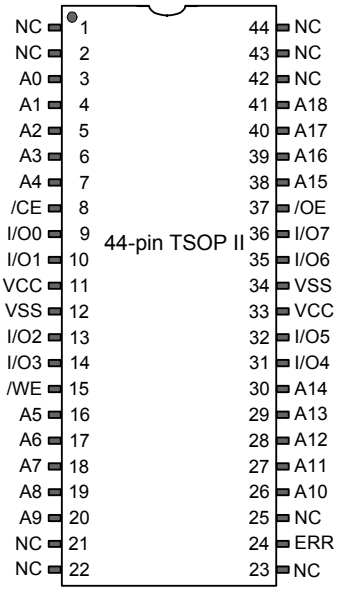


Figure 3. 44-pin TSOP II pinout, Single Chip Enable with ERR - CY7C1049GE [5, 6]



Notes
5. NC pins are not connected internally to the die.
6. ERR is an output pin.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [7] ..... –0.5 to V_{CC} + 0.5 V

DC voltage applied to outputs in HI-Z State [7] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [7] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (in LOW state) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		10 ns / 15 ns			Unit
					Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2	–	–	
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1mA		V_{CC} – 0.5[9]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2[7]	V
		2.2 V to 2.7 V	–		2	–	V_{CC} + 0.3[7]	
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3[7]	
		4.5 V to 5.5 V	–		2	–	V_{CC} + 0.5[7]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	–		–0.2[7]	–	0.4	V
		2.2 V to 2.7 V	–		–0.3[7]	–	0.6	
		2.7 V to 3.6 V	–		–0.3[7]	–	0.8	
		4.5 V to 5.5 V	–		–0.5[7]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	Operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	38	45	mA
				f = 66.7 MHz	–	–	40	
I_{SB1}	Automatic CE power-down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	15	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	6	8	mA

Notes

7. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V – 2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2V – 3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V – 5.5 V), T_A = 25 °C.
9. This parameter is guaranteed by design and not tested.

Capacitance

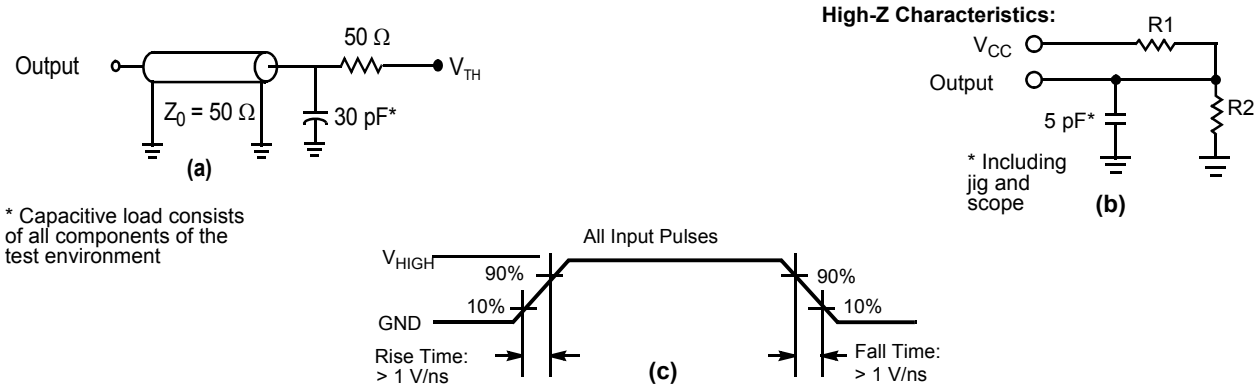
Parameter [10]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	68.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		31.48	15.97	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [11]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full-device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ and a 100-µs wait time after V_{CC} stabilization.

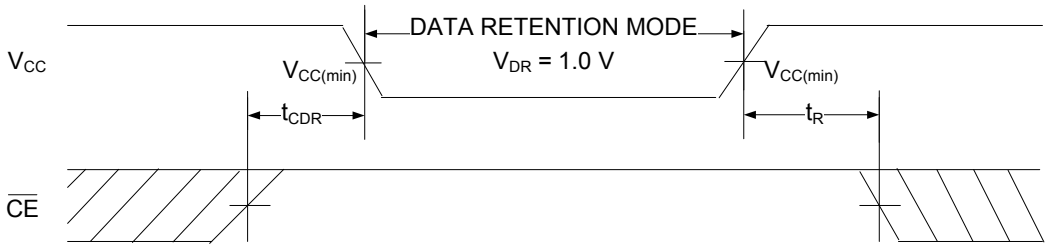
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.2 V, $\overline{CE} \geq V_{CC} - 0.2$ V[13], $V_{IN} \geq V_{CC} - 0.2$ V, or $V_{IN} \leq 0.2$ V	–	8	mA
t_{CDR}[12]	Chip deselect to data retention time		0	–	ns
t_R[12, 13]	Operation recovery time	$V_{CC} \geq 2.2$ V	10	–	ns
		$V_{CC} < 2.2$ V	15	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform[13]



Notes
12. These parameters are guaranteed by design.
13. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC\ (min)} \geq 100$ µs.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [14]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	15	–	ns
t_{AA}	Address to data / ERR valid	–	10	–	15	ns
t_{OHA}	Data / ERR hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data / ERR valid	–	10	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data / ERR valid	–	4.5	–	8	ns
t_{LZOE}	$\overline{OE}$ LOW to low impedance[15]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z[15]	–	5	–	8	ns
t_{LZCE}	$\overline{CE}$ LOW to low impedance[15]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to HI-Z[15]	–	5	–	8	ns
t_{PU}	$\overline{CE}$ LOW to power-up[16, 17]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down[16, 17]	–	10	–	15	ns
Write Cycle [17, 18]						
t_{WC}	Write cycle time	10	–	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	12	–	ns
t_{AW}	Address setup to write end	7	–	12	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	12	–	ns
t_{SD}	Data setup to write end	5	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low impedance[15]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z[15]	–	5	–	8	ns

Notes

14. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 4 on page 7, unless specified otherwise.
15. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 4 on page 7. Transition is measured ±200 mV from steady state voltage.
16. These parameters are guaranteed by design and are not tested.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle pulse width in Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{DS} and t_{HZWE}.

Switching Waveforms

Figure 6. Read Cycle No. 1 of CY7C1049G (Address Transition Controlled) [19, 20]

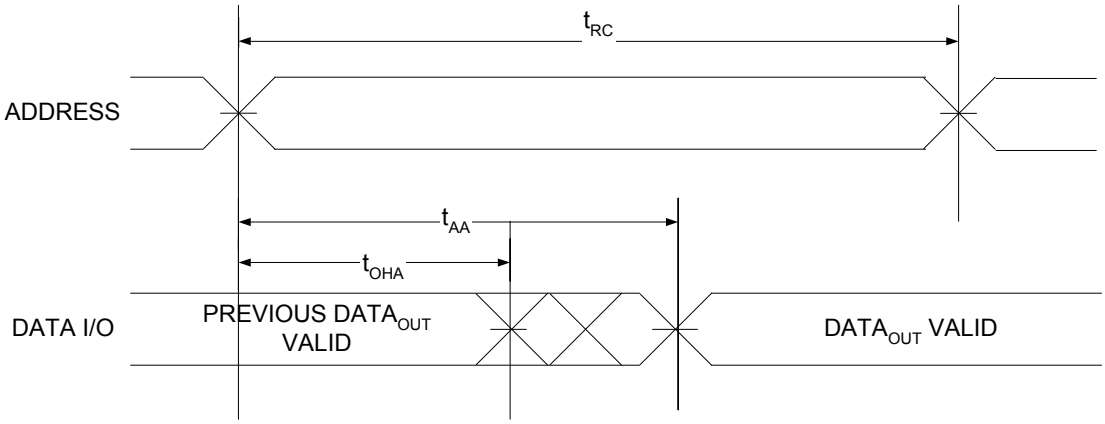
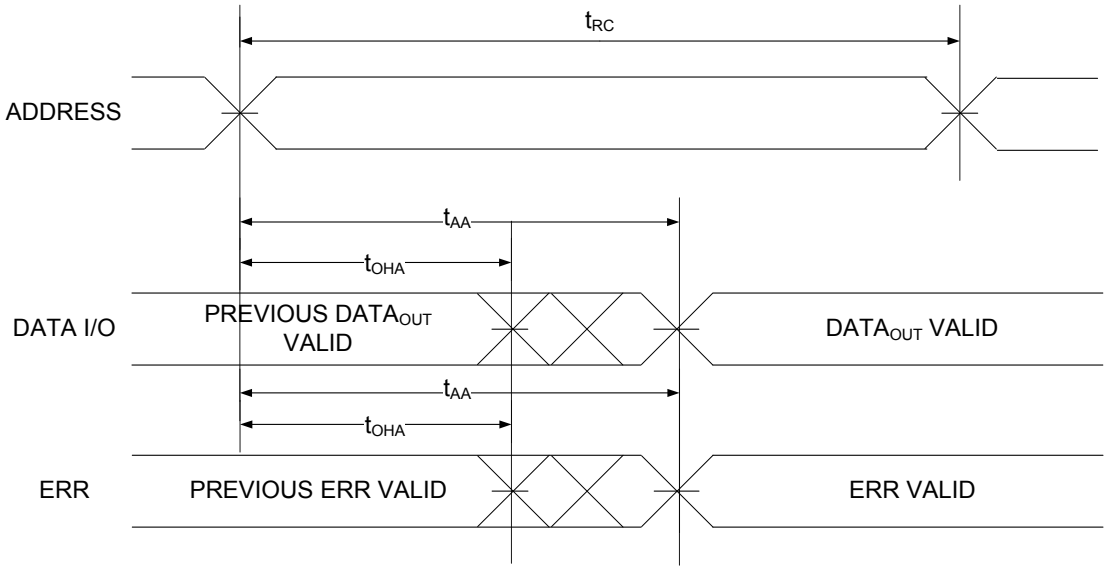


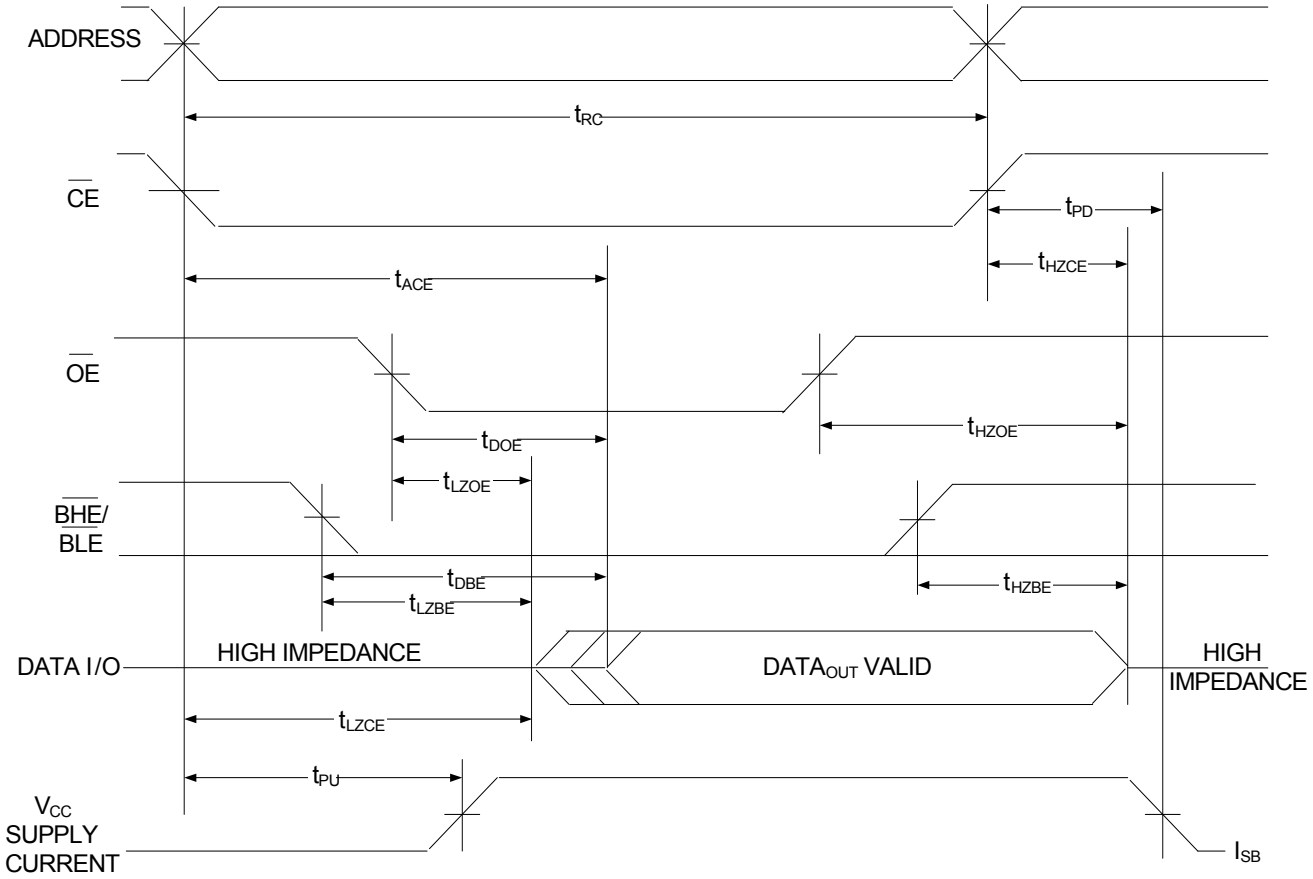
Figure 7. Read Cycle No. 1 of CY7C1049GE (Address Transition Controlled) [19, 20]



Notes
19. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
20. $\overline{WE}$ is HIGH for the read cycle.

Switching Waveforms (continued)

Figure 8. Read Cycle No. 2 (OE Controlled) [21, 22]



Notes
21. WE is HIGH for the read cycle.
22. Address valid prior to or coincident with CE LOW transition.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 1 ($\overline{CE}$ Controlled) [23, 24]

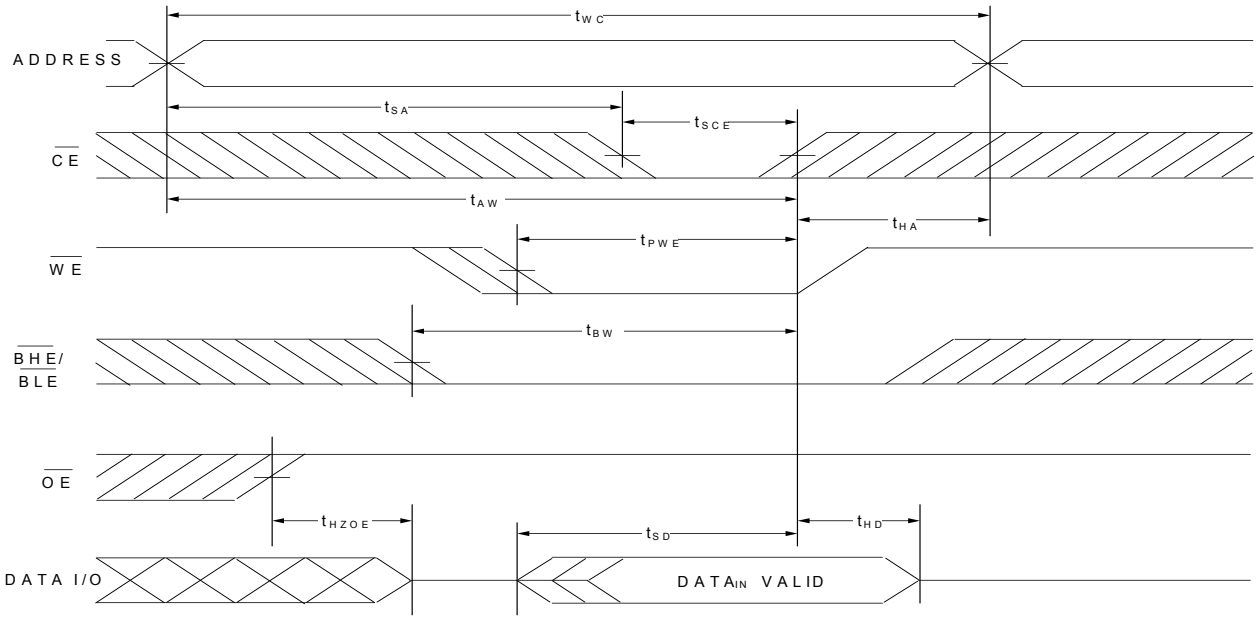
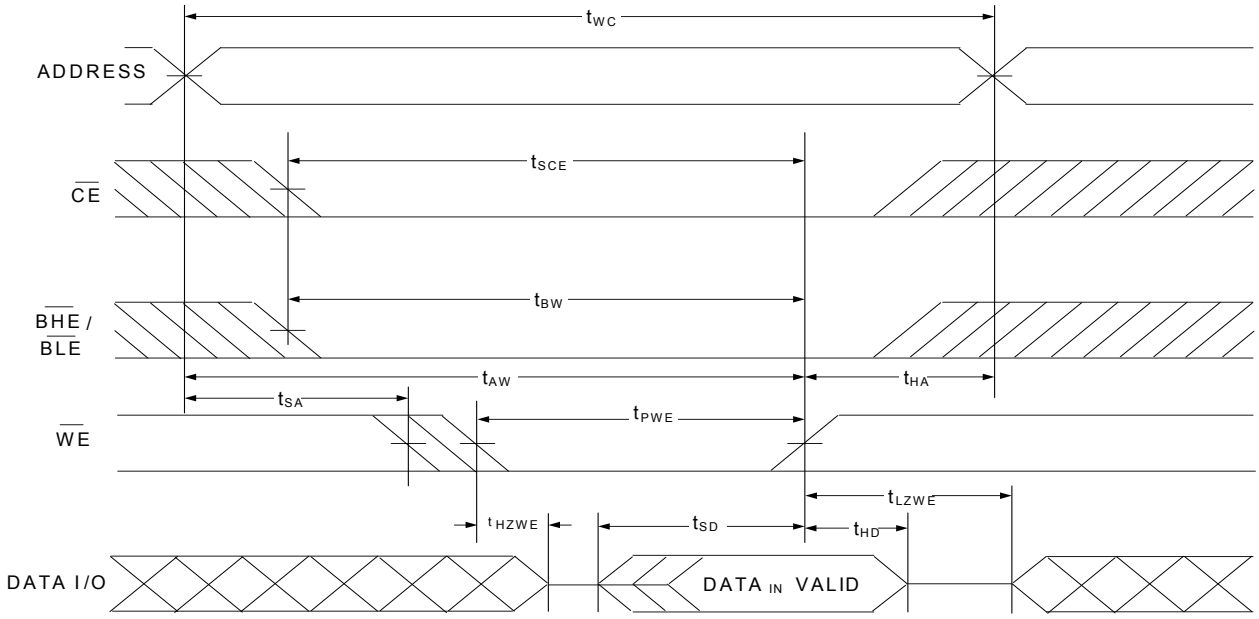


Figure 10. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [23, 24, 25]

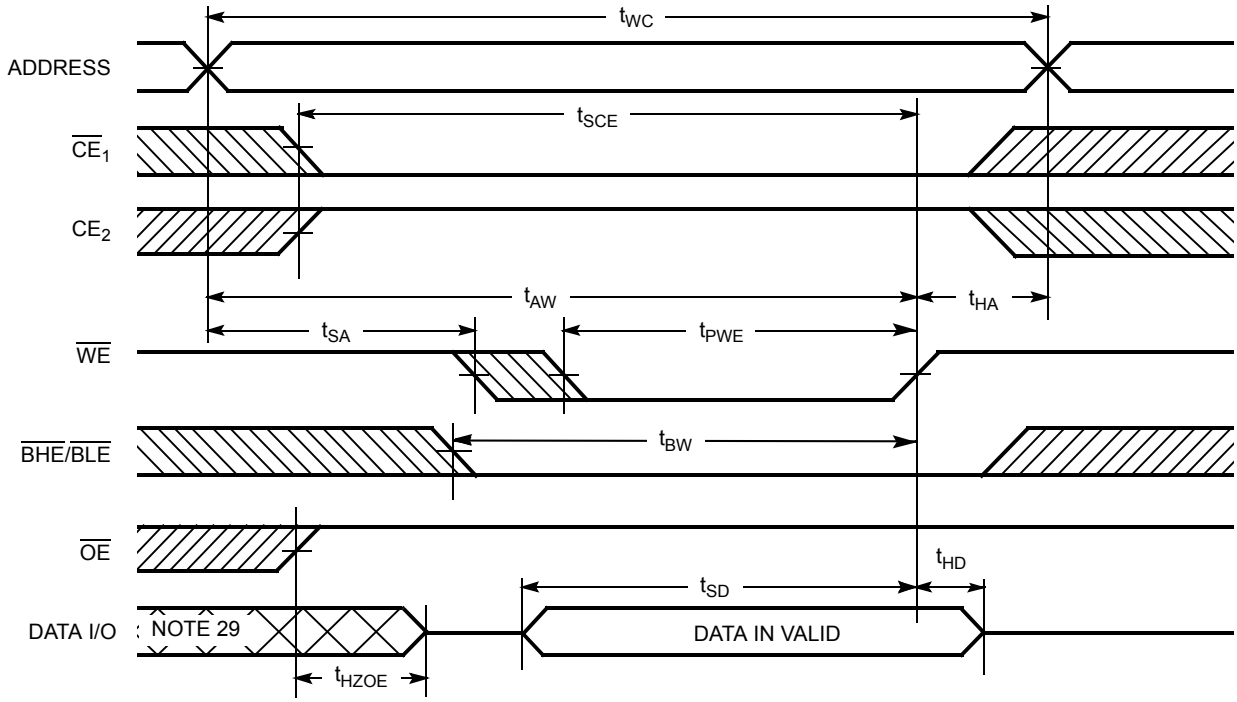


Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}.
25. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 3 ($\overline{WE}$ Controlled) [26, 27, 28]



Notes

26. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
27. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}.
28. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
29. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X[30]	X[30]	HI-Z	Power down	Standby (I_{SB})
L	L	H	Data out	Read all bits	Active (I_{CC})
L	X	L	Data in	Write all bits	Active (I_{CC})
L	H	H	HI-Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7C1049GE

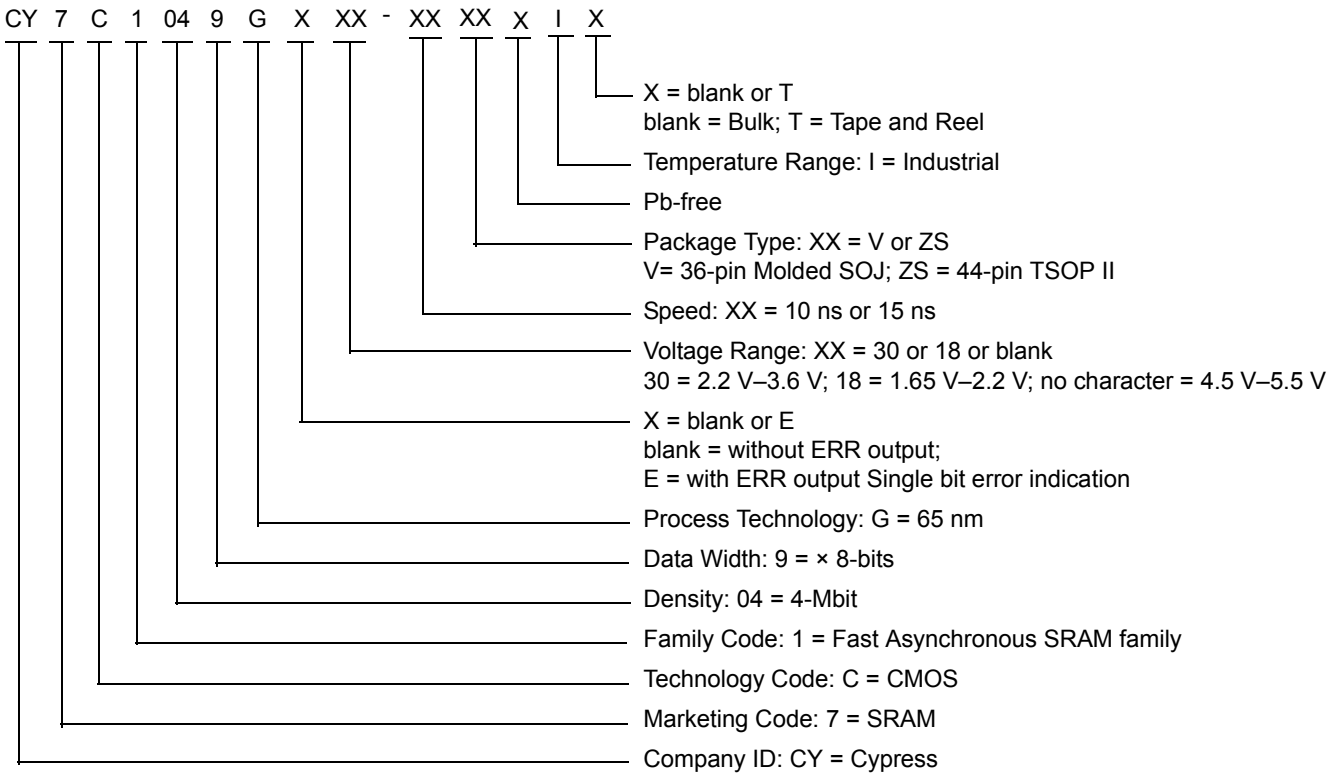
Output [31]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
HI-Z	Device deselected or outputs disabled or Write operation.

Notes
30. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
31. ERR pin is an output pin. It should be left floating when not used.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1049G30-10VXI	51-85090	36-pin Molded SOJ	Industrial
		CY7C1049G30-10VXIT	51-85090	36-pin Molded SOJ, Tape and Reel	
		CY7C1049GE30-10ZSXI	51-85087	44-pin TSOP II, ERR output	
		CY7C1049GE30-10ZSXIT	51-85087	44-pin TSOP II, ERR output, Tape and Reel	
		CY7C1049G30-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1049G30-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
15	1.65 V–2.2 V	CY7C1049G18-15ZSXI	51-85087	44-pin TSOP II	
		CY7C1049G18-15ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
10	4.5 V–5.5 V	CY7C1049G-10VXI	51-85090	36-pin Molded SOJ	
		CY7C1049G-10VXIT	51-85090	36-pin Molded SOJ, Tape and Reel	
		CY7C1049G-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1049G-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	

Ordering Code Definitions



Package Diagrams

Figure 12. 44-pin TSOP II Package Outline, 51-85087

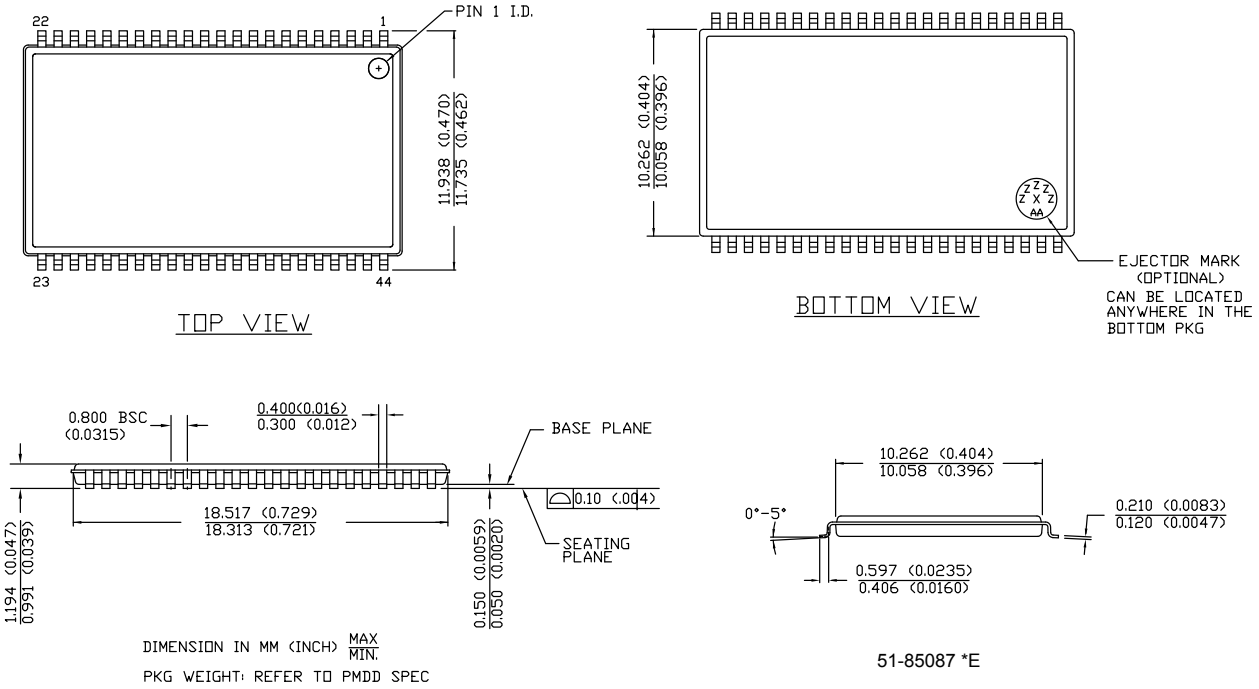
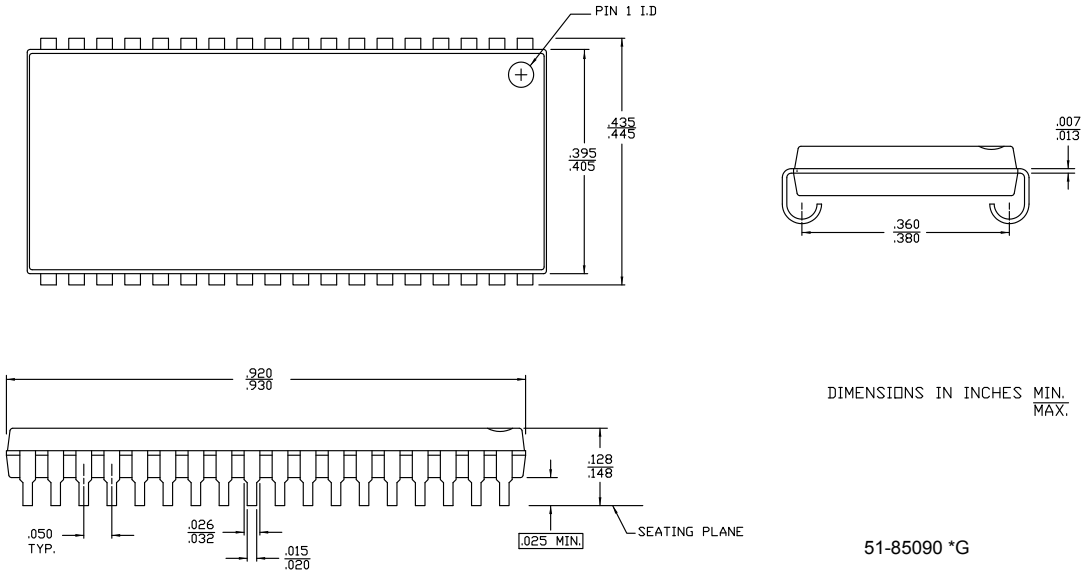


Figure 13. 36L SOJ V36.4 (Molded) Package Outline, 51-85090



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1049G/CY7C1049GE, 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95412				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4685774	VINI	03/13/2015	New data sheet.
*A	4831087	NILE	07/10/2015	Updated Package Diagrams: Added spec 51-85090 *G (Figure 13). Removed spec 51-85082 *E. Removed spec 51-85150 *H.
*B	4968879	NILE	10/16/2015	Fixed typo in bookmarks.
*C	5020573	VINI	11/25/2015	Changed status from Preliminary to Final. Updated Pin Configurations: Removed figure “36-pin SOJ Single Chip Enable with ERR CY7C1049GE”. Updated Ordering Information: Updated part numbers.
*D	5429076	NILE	09/07/2016	Updated Maximum Ratings: Updated Note 7 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V_{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V_{OH} parameter. Changed minimum value of V_{IH} parameter from 2.2 V to 2 V corresponding to Operating Range “4.5 V to 5.5 V”. Updated Ordering Information: Updated part numbers. Updated to new template.

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