



CYPRESS

PRELIMINARY

CY7C1049

## 512K x 8 Static RAM

### Features

- **High speed**
  - $t_{AA} = 15 \text{ ns}$
- **Low active power**
  - 1210 mW (max.)
- **Low CMOS standby power (Commercial L version)**
  - 2.75 mW (max.)
- **2.0V Data Retention (400  $\mu\text{W}$  at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**

### Functional Description

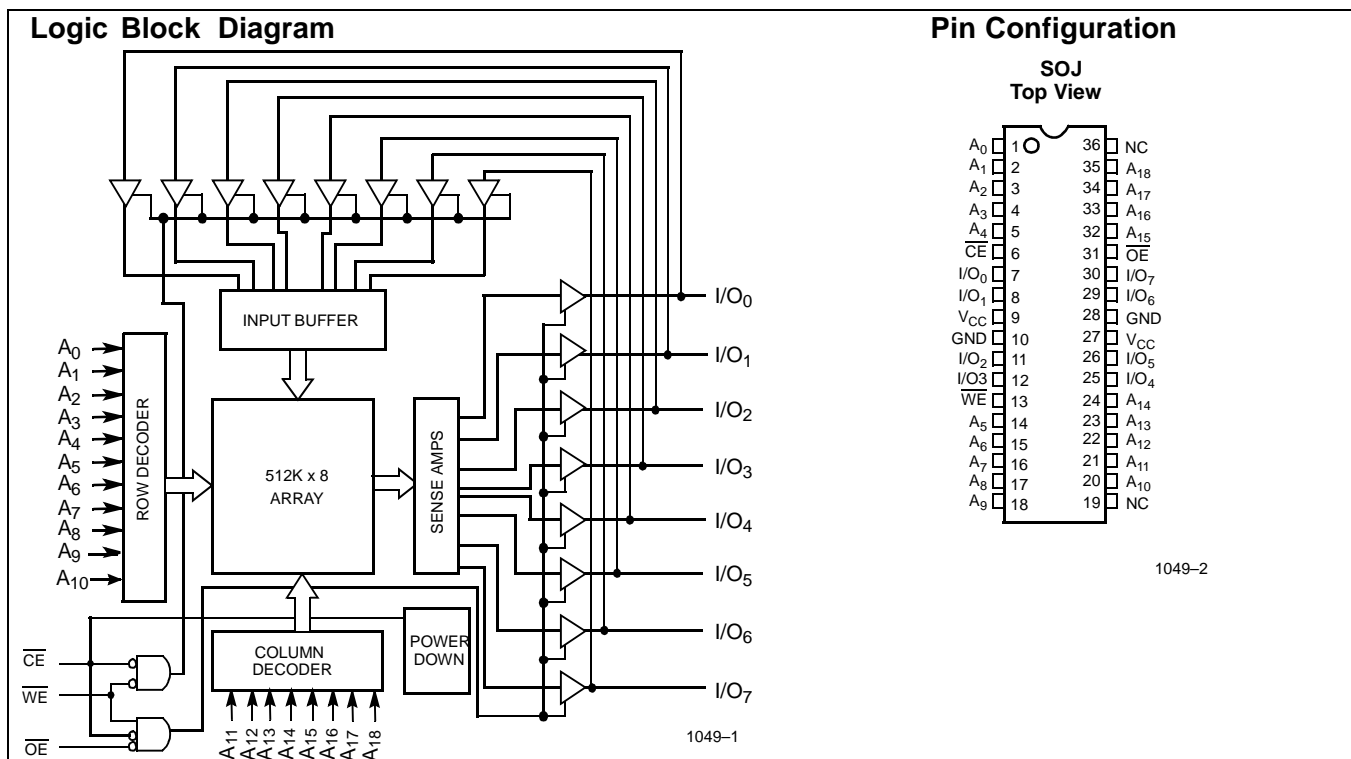
The CY7C1049 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion

is provided by an active LOW chip enable ( $\overline{\text{CE}}$ ), an active LOW output enable ( $\overline{\text{OE}}$ ), and three-state drivers. Writing to the device is accomplished by taking chip enable ( $\overline{\text{CE}}$ ) and write enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ).

Reading from the device is accomplished by taking chip enable ( $\overline{\text{CE}}$ ) and output enable ( $\overline{\text{OE}}$ ) LOW while forcing write enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1049 is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.



### Selection Guide

		7C1049-12	7C1049-15	7C1049-17	7C1049-20	7C1049-25
Maximum Access Time (ns)		12	15	17	20	25
Maximum Operating Current (mA)		240	220	195	185	180
Maximum CMOS Standby Current (mA)	Com'l	8	8	8	8	8
	Com'l L	0.5	0.5	0.5	0.5	0.5
	Ind'l	9	9	9	9	9
	Military				10	10

Shaded areas contain advance information.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

## Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	-40°C to +85°C	
Military	-55°C to +125°C	

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1049-12		7C1049-15		7C1049-17		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.3	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}$ $f = f_{MAX} = 1/t_{RC}$		240		220		195	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		40		40		40	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f=0$	Com'l			8		8	mA
			Com'l L			0.5		0.5	mA
			Ind'l			9		9	mA
			Military			10		10	mA

Shaded areas contain advance information.

### Notes:

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.

**Electrical Characteristics** Over the Operating Range (continued)

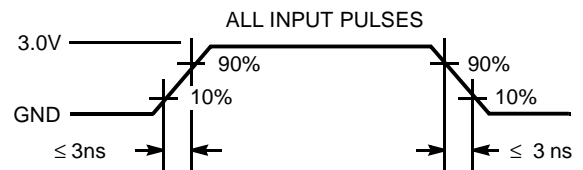
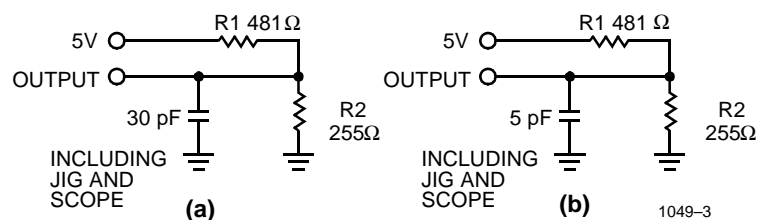
Parameter	Description	Test Conditions		7C1049-20		7C1049-25		Unit	
				Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = −4.0 mA		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA			0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage			2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>			−0.3	0.8	−0.3	0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		−1	+1	−1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled		−1	+1	−1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max. f = f <sub>MAX</sub> = 1/t <sub>RC</sub>			185		180	mA	
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>			40		40	mA	
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> − 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V, or V <sub>IN</sub> ≤ 0.3V, f=0	Com'l		8		8	mA	
			Com'l	L	0.5		0.5	mA	
			Ind'l			9		9	mA
			Military			10		10	mA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 5.0\text{V}$	8	pF
$C_{OUT}$	I/O Capacitance		8	pF

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


1049-4

Equivalent to: THÉVENIN EQUIVALENT

OUTPUT  $\text{---} \frac{167\Omega}{\text{---}} \text{---} 1.73\text{V}$

**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	7C1049-12		7C1049-15		7C1049-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t <sub>RC</sub>	Read Cycle Time	12		15		17		ns
t <sub>AA</sub>	Address to Data Valid		12		15		17	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
WRITE CYCLE <sup>[7,8]</sup>								
t <sub>WC</sub>	Write Cycle Time	12		15		17		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	10		12		12		ns
t <sub>AW</sub>	Address Set-Up to Write End	10		12		12		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	10		12		12		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		8		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		6		7		8	ns

Shaded areas contain advance information.

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics<sup>[4]</sup>** Over the Operating Range (continued)

Parameter	Description	7C1049-20		7C1049-25		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t <sub>RC</sub>	Read Cycle Time	20		25		ns
t <sub>AA</sub>	Address to Data Valid		20		25	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		20		25	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		8		10	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		8		10	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		8		10	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		20		25	ns
WRITE CYCLE <sup>[7]</sup>						
t <sub>WC</sub>	Write Cycle Time	20		25		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	13		15		ns
t <sub>AW</sub>	Address Set-Up to Write End	13		15		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	13		15		ns
t <sub>SD</sub>	Data Set-Up to Write End	9		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		8		10	ns

**Data Retention Characteristics** Over the Operating Range

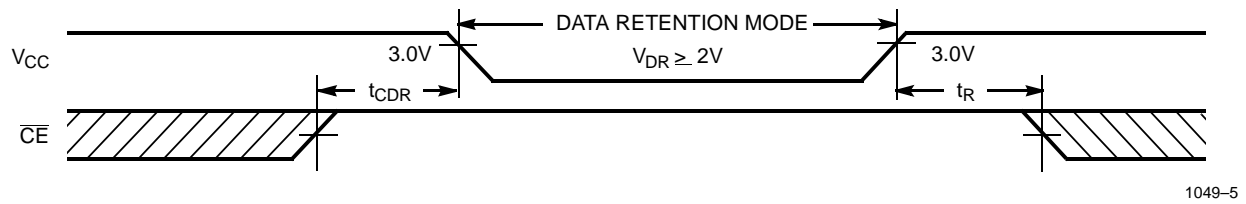
Parameter	Description			Conditions <sup>[10]</sup>	Min.	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention				2.0		V
I <sub>CCDR</sub>	Data Retention Current	Com'l	L	V <sub>CC</sub> = V <sub>DR</sub> = 3.0V, CE ≥ V <sub>CC</sub> − 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V or V <sub>IN</sub> ≤ 0.3V		200	μA
		Ind'l				1	mA
		Military				2	mA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time				0		ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time				t <sub>RC</sub>		ns

**Notes:**

9.  $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 ns and slower speeds.

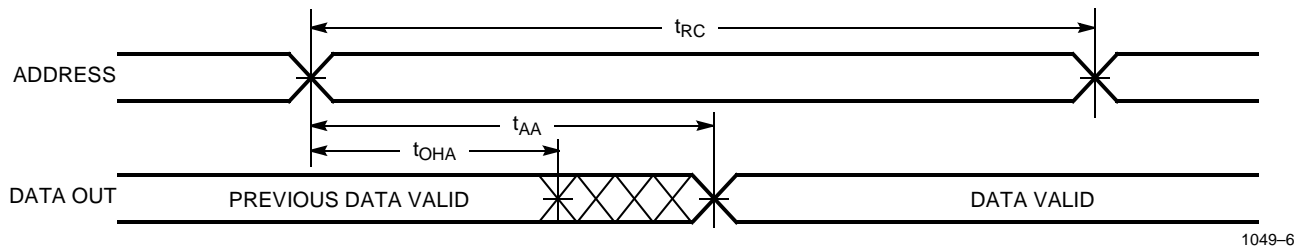
10. No input may exceed  $V_{CC} + 0.5V$ .

## Data Retention Waveform

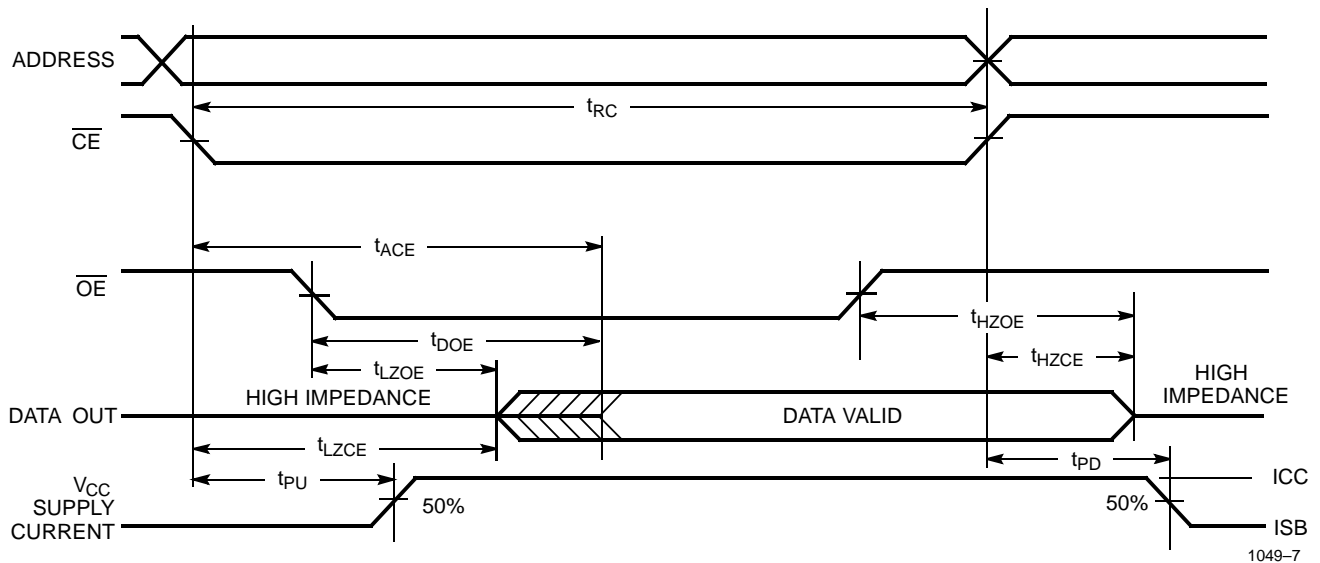


## Switching Waveforms

### Read Cycle No. 1<sup>[11, 12]</sup>

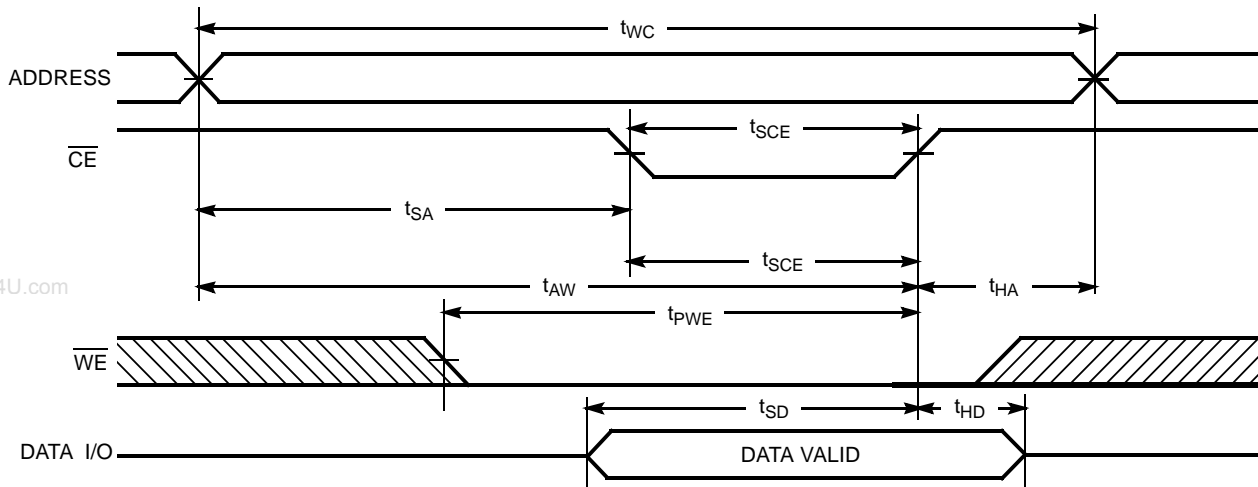


### Read Cycle No. 2 (OE Controlled)<sup>[12, 13]</sup>

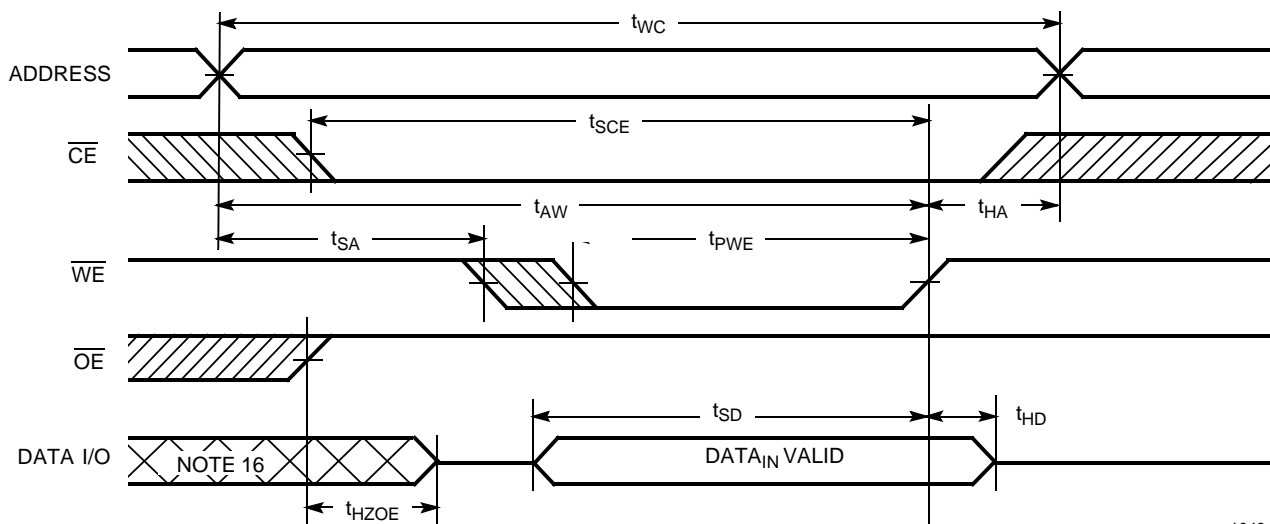


#### Notes:

11. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[14, 15]</sup>**


1049-8

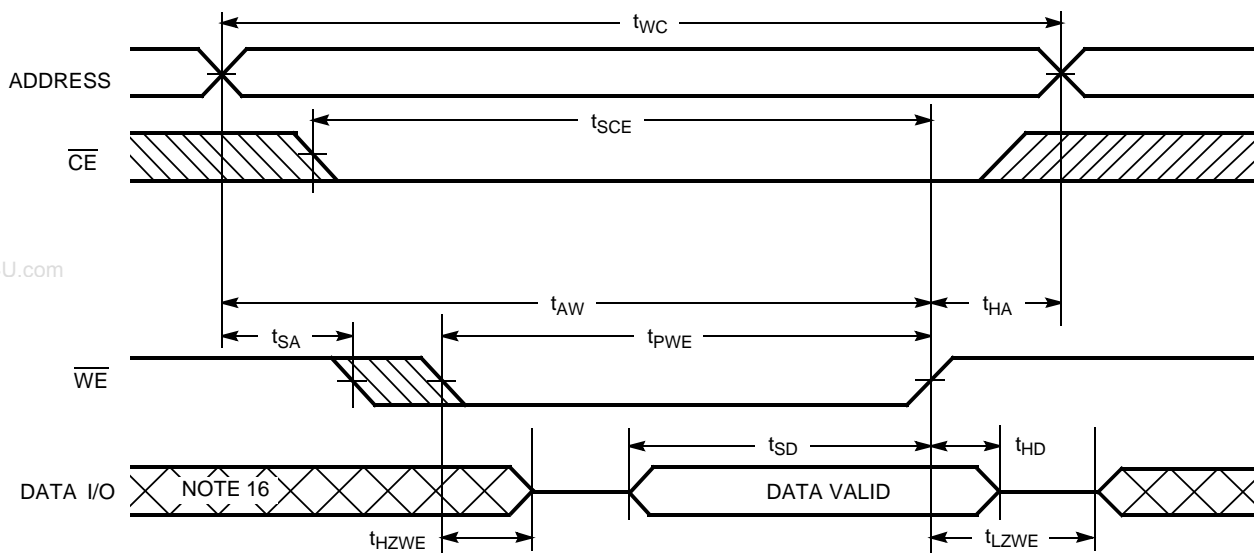
**Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write)<sup>[14, 15]</sup>**


1049-9

**Notes:**

14. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[15]</sup>**


1049-10

**Ordering Information**

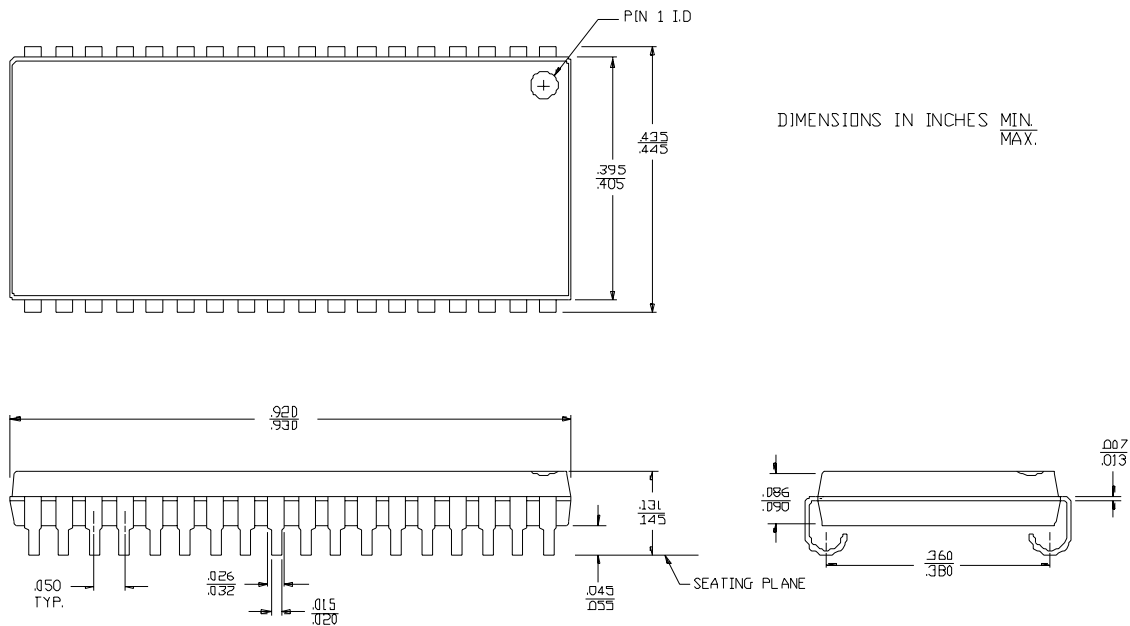
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1049-15VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-15VC	V36	36-Lead (400-Mil) Molded SOJ	
17	CY7C1049-17VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-17VC	V36	36-Lead (400-Mil) Molded SOJ	
20	CY7C1049-20VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-20VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-20VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049L-20VI	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-20VM	V36	36-Lead (400-Mil) Molded SOJ	Military
	CY7C1049L-20VM	V36	36-Lead (400-Mil) Molded SOJ	
25	CY7C1049-25VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-25VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-25VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049L-25VI	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-25VM	V36	36-Lead (400-Mil) Molded SOJ	Military
	CY7C1049L-25VM	V36	36-Lead (400-Mil) Molded SOJ	

Shaded areas contain advance information.



## Package Diagram

### 36-Lead (400-Mil) Molded SOJ V36





**PRELIMINARY**

**CY7C1049**

**Document Title: CY7C1049 512K x 8 Static RAM**  
**Document Number: 38-05063**

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107256	09/10/01	SZV	Change from Spec number: 38-00563 to 38-05063