

## Features

- Pin- and function-compatible with CY7C106B/CY7C1006B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
  - $I_{SB2} = 3.0 \text{ mA}$
- 2.0 V Data Retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- CY7C106D available in Pb-free 28-pin 400-Mil wide Molded SOJ package. CY7C1006D available in Pb-free 28-pin 300-Mil wide Molded SOJ package

## Functional Description

The CY7C106D [1] and CY7C1006D [1] are high-performance CMOS static RAMs organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and tri-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when the devices are deselected. The four input and output pins (IO<sub>0</sub> through IO<sub>3</sub>) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- When the write operation is active ( $\overline{CE}$  and  $\overline{WE}$  LOW)

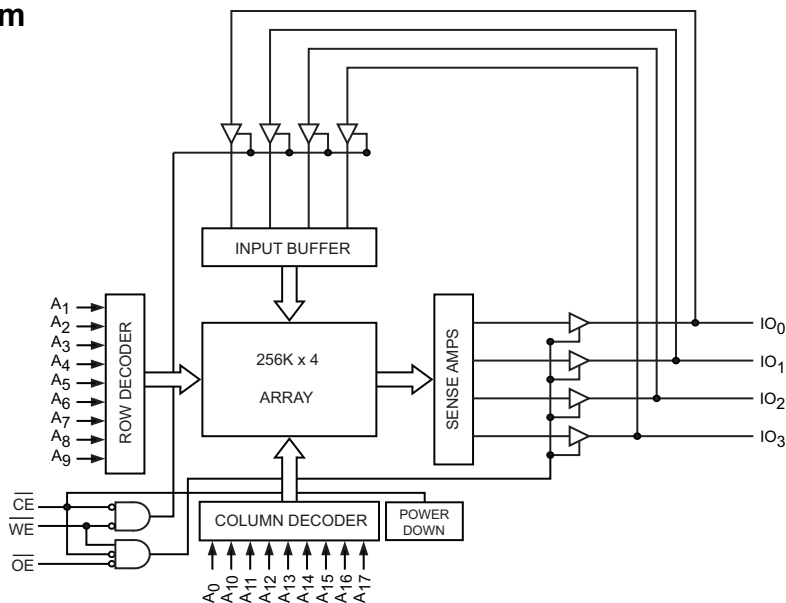
Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the four IO pins (IO<sub>0</sub> through IO<sub>3</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the four IO pins.

Both CY7C106D and CY7C1006D devices are suitable for interfacing with processors that have TTL I/P levels. They are not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

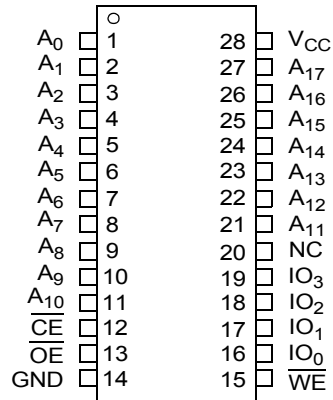
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configurations

Figure 1. 28-pin SOJ pinout (Top View) <sup>[2]</sup>



## Selection Guide

| Description               | CY7C106D-10<br>CY7C1006D-10 | Unit |
|---------------------------|-----------------------------|------|
| Maximum Access Time       | 10                          | ns   |
| Maximum Operating Current | 80                          | mA   |
| Maximum Standby Current   | 3                           | mA   |

**Note**

2. NC pins are not connected on the die.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

|   |                                   |
|---|-----------------------------------|
| Storage Temperature .....                                   | -65 °C to +150 °C                 |
| Ambient Temperature with Power Applied .....                | -55 °C to +125 °C                 |
| Supply Voltage on V <sub>CC</sub> Relative to GND [3] ..... | -0.5 V to +6.0 V                  |
| DC Voltage Applied to Outputs in High Z State [3] .....     | -0.5 V to V <sub>CC</sub> + 0.5 V |

|   |                                   |
|---|-----------------------------------|
| DC Input Voltage [3] .....                                    | -0.5 V to V <sub>CC</sub> + 0.5 V |
| Current into Outputs (LOW) .....                              | 20 mA                             |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... | > 2001 V                          |
| Latch-up Current .....  | > 200 mA                          |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> | Speed |
|------------|---------------------|-----------------|-------|
| Industrial | -40 °C to +85 °C    | 5 V ± 0.5 V     | 10 ns |

## Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                   | Test Conditions  | 7C106D-10<br>7C1006D-10 |                       | Unit |    |
|------------------|---|--|-------------------------|-----------------------|------|----|
|                  |   |  | Min                     | Max                   |      |    |
| V <sub>OH</sub>  | Output HIGH Voltage                           | I <sub>OH</sub> = -4.0 mA  | 2.4                     | -                     | V    |    |
|                  |   | I <sub>OH</sub> = -0.1 mA  | -                       | 3.4 [4]               |      |    |
| V <sub>OL</sub>  | Output LOW Voltage                            | I <sub>OL</sub> = 8.0 mA   | -                       | 0.4                   | V    |    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |  | 2.2                     | V <sub>CC</sub> + 0.5 | V    |    |
| V <sub>IL</sub>  | Input LOW Voltage [3]                         |  | -0.5                    | 0.8                   | V    |    |
| I <sub>IX</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -1                      | +1                    | μA   |    |
| I <sub>OZ</sub>  | Output Leakage Current                        | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled   | -1                      | +1                    | μA   |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA,<br>f = f <sub>max</sub> = 1/t <sub>RC</sub>  | 100 MHz                 | -                     | 80   | mA |
|                  |   |  | 83 MHz                  | -                     | 72   | mA |
|                  |   |  | 66 MHz                  | -                     | 58   | mA |
|                  |   |  | 40 MHz                  | -                     | 37   | mA |
| I <sub>SB1</sub> | Automatic CE Power-Down Current — TTL Inputs  | Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ ,<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub> | -                       | 10                    | mA   |    |
| I <sub>SB2</sub> | Automatic CE Power-Down Current — CMOS Inputs | Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3$ V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0            | -                       | 3                     | mA   |    |

### Note

- V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.
- Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V<sub>IH</sub> of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.

## Capacitance

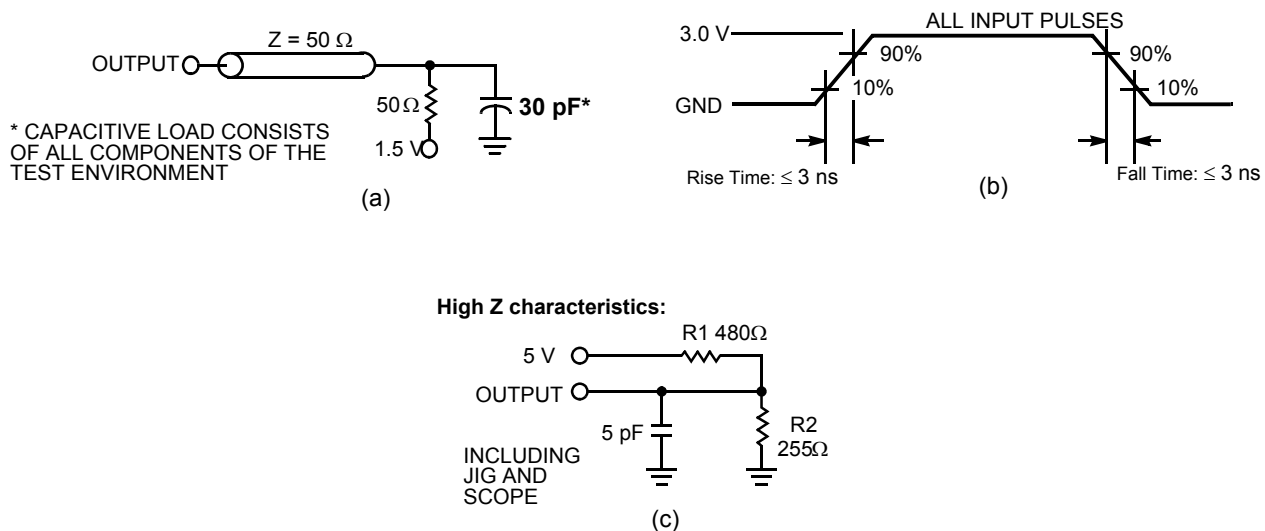
| Parameter <sup>[5]</sup>    | Description        | Test Conditions  | Max | Unit |
|-----------------------------|--------------------|--|-----|------|
| C <sub>IN</sub> : Addresses | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V | 7   | pF   |
| C <sub>IN</sub> : Controls  |                    |  | 10  | pF   |
| C <sub>OUT</sub>            | Output capacitance |  | 10  | pF   |

## Thermal Resistance

| Parameter <sup>[5]</sup> | Description                              | Test Conditions   | 300-Mil Wide SOJ | 400-Mil Wide SOJ | Unit |
|--------------------------|--|---|------------------|------------------|------|
| Θ <sub>JA</sub>          | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 59.16            | 58.76            | °C/W |
| Θ <sub>JC</sub>          | Thermal resistance (junction to case)    |   | 40.84            | 40.54            | °C/W |

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[6]</sup>



### Notes

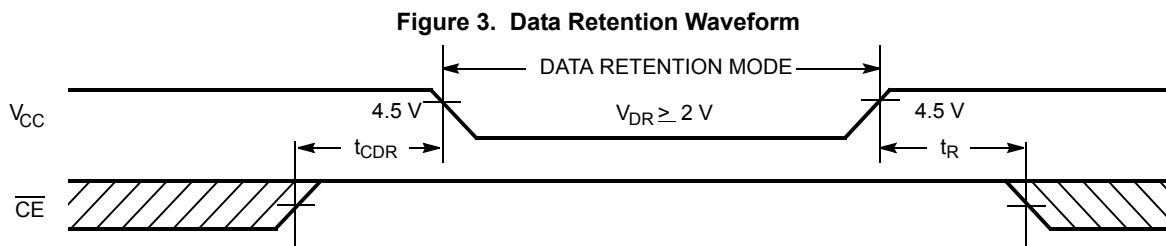
- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in part (a) of Figure 2. High Z characteristics are tested for all speeds using the test load shown in part (c) of Figure 2.

## Data Retention Characteristics

Over the Operating Range

| Parameter       | Description                          | Conditions   | Min      | Max | Unit |
|-----------------|--------------------------------------|--|----------|-----|------|
| $V_{DR}$        | $V_{CC}$ for Data Retention          |  | 2.0      | –   | V    |
| $I_{CCDR}$      | Data Retention Current               | $V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | –        | 3   | mA   |
| $t_{CDR}^{[7]}$ | Chip Deselect to Data Retention Time |  | 0        | –   | ns   |
| $t_R^{[8,9]}$   | Operation Recovery Time              |  | $t_{RC}$ | –   | ns   |

## Data Retention Waveform



### Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .
9.  $t_r \leq 3\text{ ns}$  for all speeds.

## Switching Characteristics

Over the Operating Range

| Parameter <sup>[10]</sup>              | Description  | 7C106D-10<br>7C1006D-10 |     | Unit    |
|--|--|-------------------------|-----|---------|
|  |  | Min                     | Max |         |
| <b>Read Cycle</b>                      |  |                         |     |         |
| $t_{power}^{[11]}$                     | $V_{CC}$ (typical) to the first access             | 100                     | –   | $\mu$ s |
| $t_{RC}$                               | Read Cycle Time                                    | 10                      | –   | ns      |
| $t_{AA}$                               | Address to Data Valid                              | –                       | 10  | ns      |
| $t_{OHA}$                              | Data Hold from Address Change                      | 3                       | –   | ns      |
| $t_{ACE}$                              | $\overline{CE}$ LOW to Data Valid                  | –                       | 10  | ns      |
| $t_{DOE}$                              | $\overline{OE}$ LOW to Data Valid                  | –                       | 5   | ns      |
| $t_{LZOE}$                             | $\overline{OE}$ LOW to Low Z                       | 0                       | –   | ns      |
| $t_{HZOE}$                             | $\overline{OE}$ HIGH to High Z <sup>[12, 13]</sup> | –                       | 5   | ns      |
| $t_{LZCE}$                             | $\overline{CE}$ LOW to Low Z <sup>[13]</sup>       | 3                       | –   | ns      |
| $t_{HZCE}$                             | $\overline{CE}$ HIGH to High Z <sup>[12, 13]</sup> | –                       | 5   | ns      |
| $t_{PU}^{[14]}$                        | $\overline{CE}$ LOW to Power-Up                    | 0                       | –   | ns      |
| $t_{PD}^{[14]}$                        | $\overline{CE}$ HIGH to Power-Down                 | –                       | 10  | ns      |
| <b>Write Cycle <sup>[15, 16]</sup></b> |  |                         |     |         |
| $t_{WC}$                               | Write Cycle Time                                   | 10                      | –   | ns      |
| $t_{SCE}$                              | $\overline{CE}$ LOW to Write End                   | 7                       | –   | ns      |
| $t_{AW}$                               | Address Set-Up to Write End                        | 7                       | –   | ns      |
| $t_{HA}$                               | Address Hold from Write End                        | 0                       | –   | ns      |
| $t_{SA}$                               | Address Set-Up to Write Start                      | 0                       | –   | ns      |
| $t_{PWE}$                              | $\overline{WE}$ Pulse Width                        | 7                       | –   | ns      |
| $t_{SD}$                               | Data Set-Up to Write End                           | 6                       | –   | ns      |
| $t_{HD}$                               | Data Hold from Write End                           | 0                       | –   | ns      |
| $t_{LZWE}$                             | $\overline{WE}$ HIGH to Low Z <sup>[13]</sup>      | 3                       | –   | ns      |
| $t_{HZWE}$                             | $\overline{WE}$ LOW to High Z <sup>[12, 13]</sup>  | –                       | 5   | ns      |

### Notes

10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
11.  $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
13. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
14. This parameter is guaranteed by design and is not tested.
15. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
16. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

Figure 4. Read Cycle No.1 (Address Transition Controlled) [17, 18]

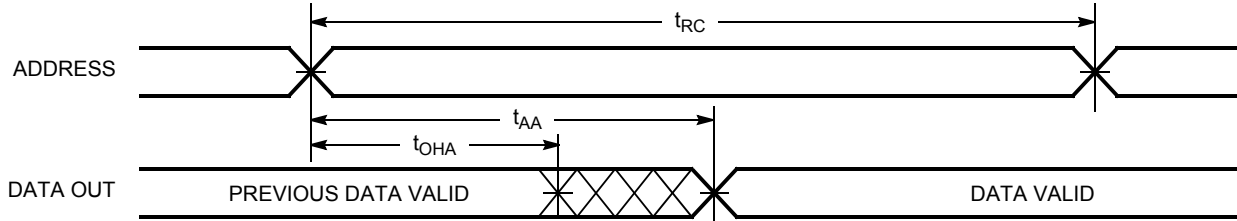
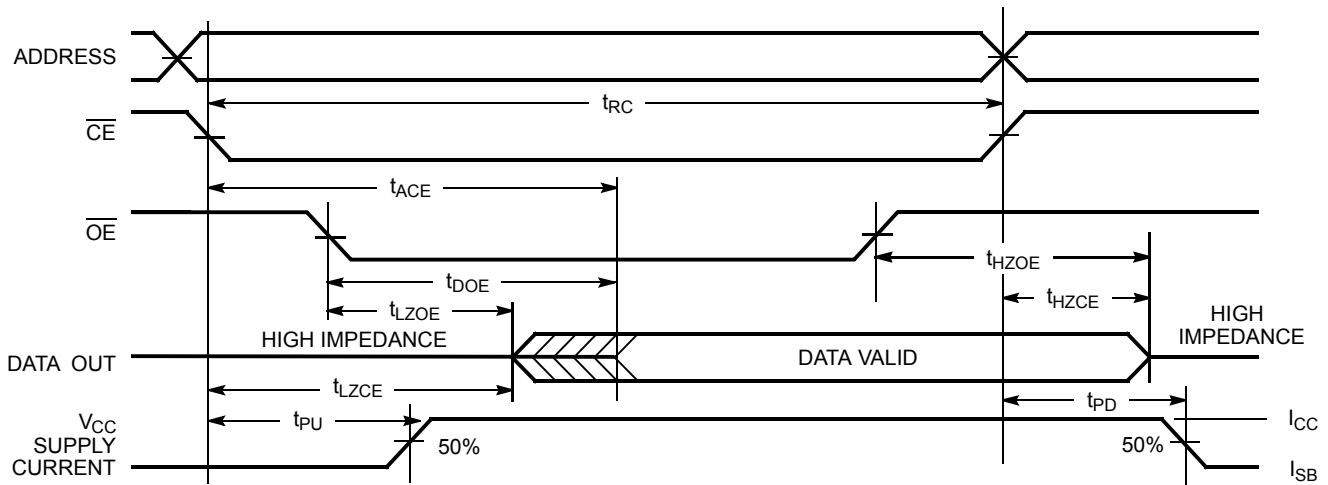


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [18, 19]



### Notes

17. Device is continuously selected,  $\overline{OE}$  and  $\overline{CE} = V_{IL}$ .
18.  $\overline{WE}$  is HIGH for read cycle.
19. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{CE}$  Controlled) [20, 21]

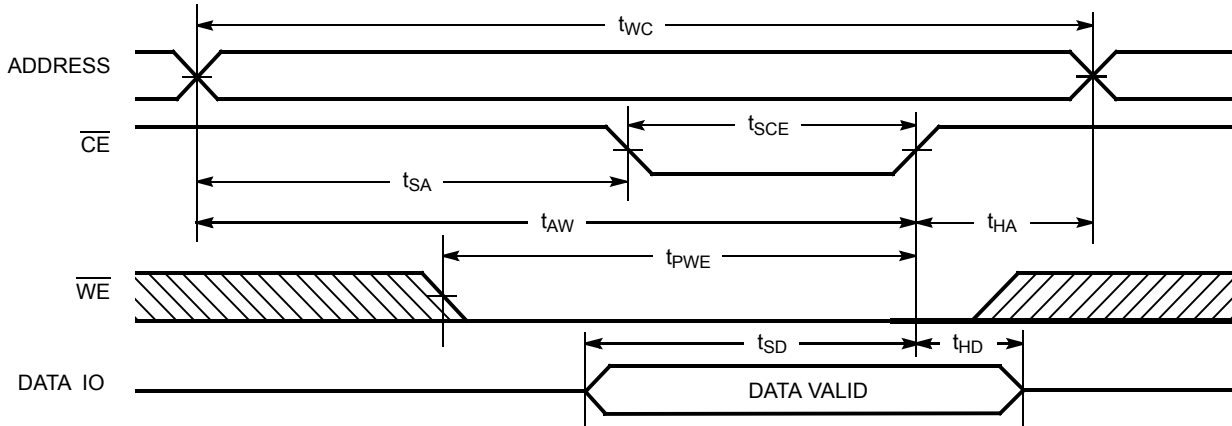
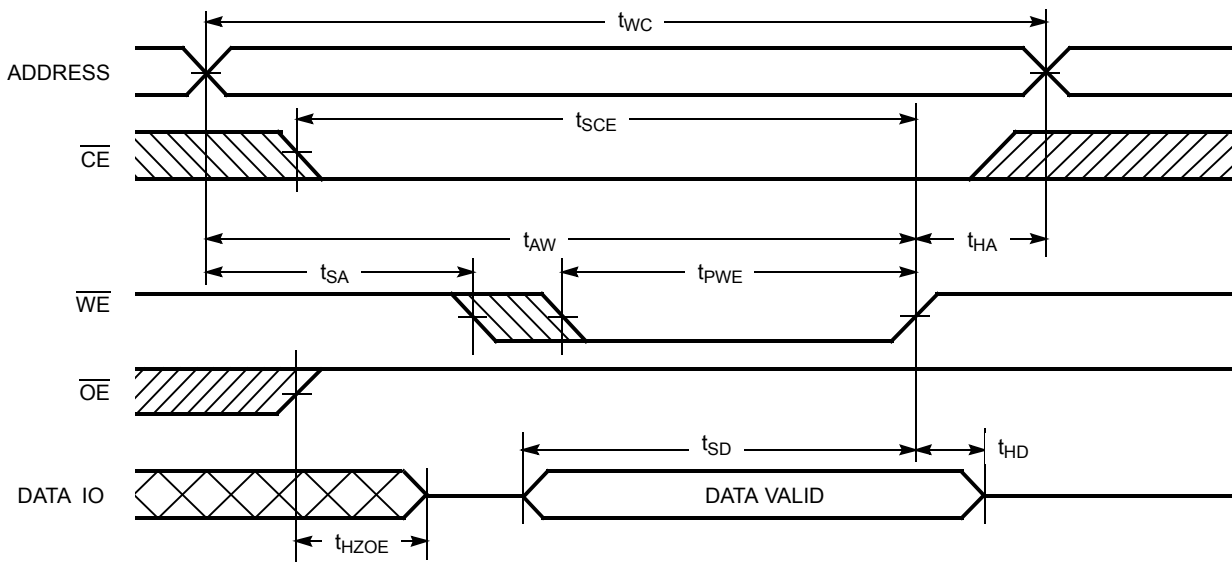


Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [20, 21]

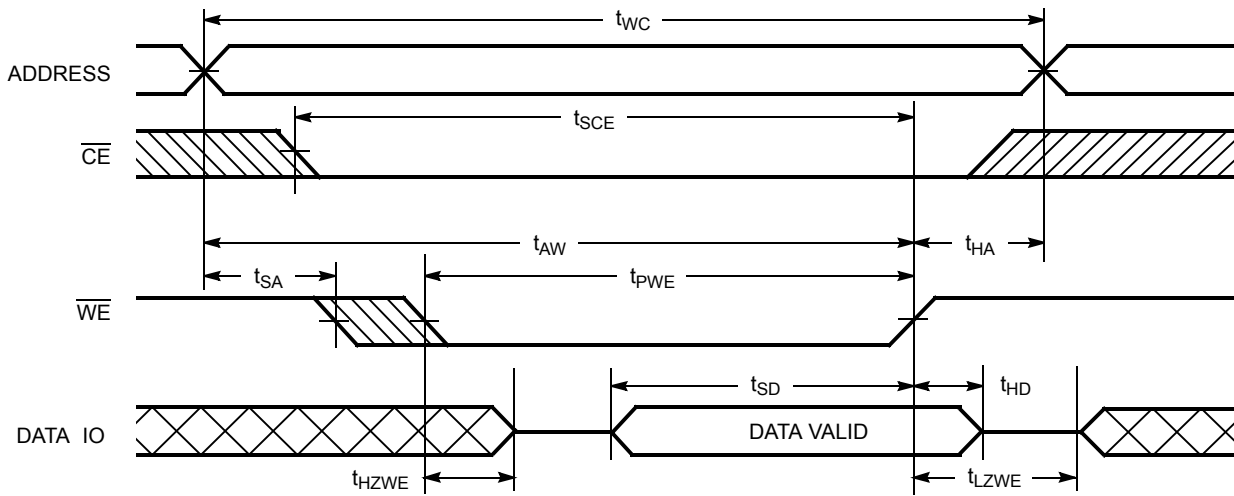


Notes

- 20. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 21. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [22, 23]



Notes

- 22. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 23. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .

### Truth Table

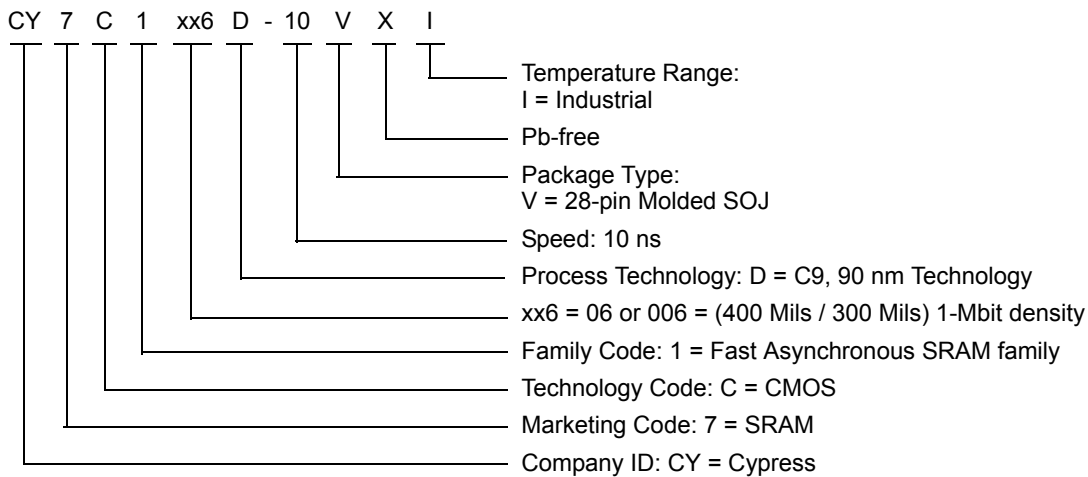
| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Input/Output | Mode                       | Power                |
|-----------------|-----------------|-----------------|--------------|----------------------------|----------------------|
| H               | X               | X               | High Z       | Power-Down                 | Standby ( $I_{SB}$ ) |
| L               | L               | H               | Data Out     | Read                       | Active ( $I_{CC}$ )  |
| L               | X               | L               | Data In      | Write                      | Active ( $I_{CC}$ )  |
| L               | H               | H               | High Z       | Selected, Outputs Disabled | Active ( $I_{CC}$ )  |

### Ordering Information

| Speed (ns) | Ordering Code  | Package Diagram | Package Type                  | Operating Range |
|------------|----------------|-----------------|-------------------------------|-----------------|
| 10         | CY7C106D-10VXI | 51-85032        | 28-pin SOJ (400 Mils) Pb-free | Industrial      |

Please contact your local Cypress sales representative for availability of these parts.

### Ordering Code Definitions

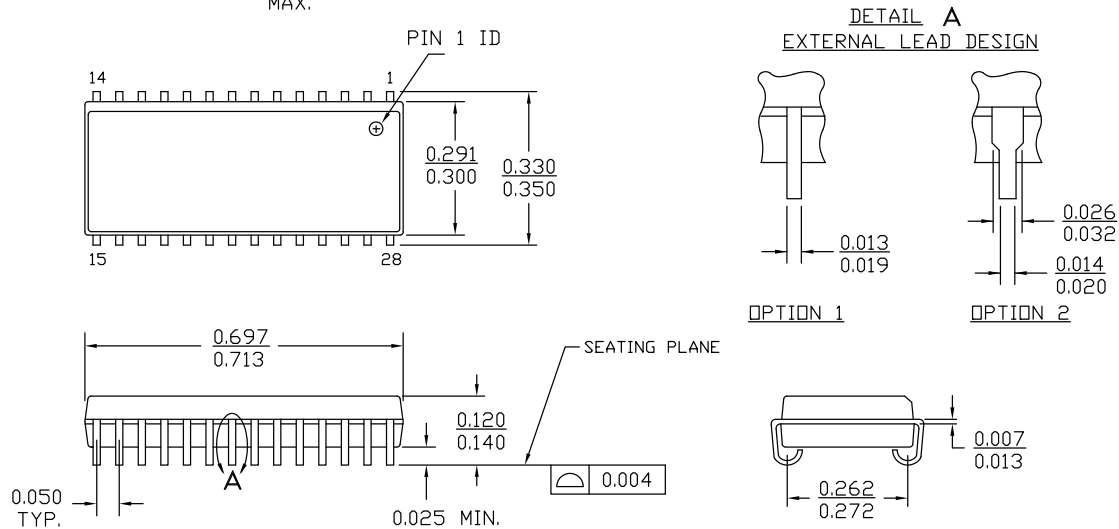


## Package Diagrams

**Figure 9. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031**

NOTE :

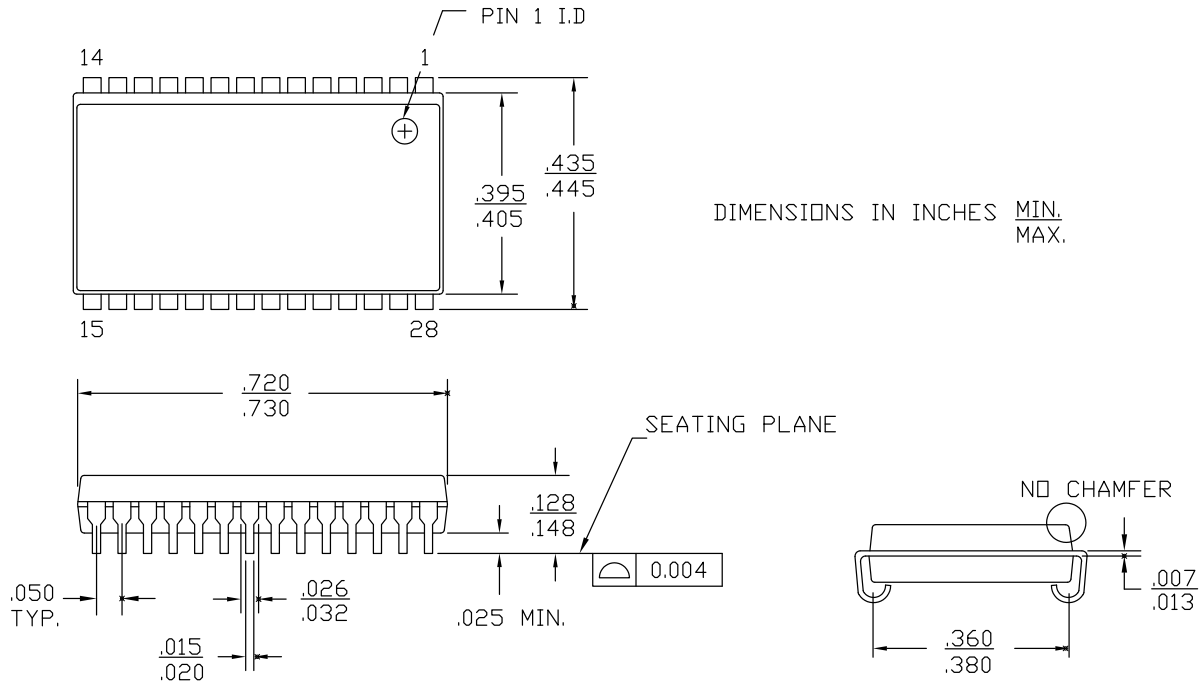
1. JEDEC STD REF MD088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.



51-85031 \*E

**Package Diagrams** (continued)

**Figure 10. 28-pin (400 Mils) V28.4 (Molded SOJ V28) Package Outline, 51-85032**



NOTES :

1. PACKAGE WEIGHT : 1.24g
2. JEDEC REFERENCE : MS-027

51-85032 \*F

## Acronyms

| Acronym         | Description                             |
|-----------------|---|
| $\overline{CE}$ | Chip Enable                             |
| CMOS            | Complementary Metal-Oxide Semiconductor |
| I/O             | Input/Output                            |
| $\overline{OE}$ | Output Enable                           |
| SOJ             | Small Outline J-lead                    |
| SRAM            | Static Random Access Memory             |
| TTL             | Transistor-Transistor Logic             |
| $\overline{WE}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol      | Unit of Measure |
|-------------|-----------------|
| $^{\circ}C$ | degree Celsius  |
| MHz         | megahertz       |
| $\mu A$     | microampere     |
| $\mu s$     | microsecond     |
| mA          | milliampere     |
| ns          | nanosecond      |
| $\Omega$    | ohm             |
| %           | percent         |
| pF          | picofarad       |
| V           | volt            |
| W           | watt            |

## Document History Page

| Document Title: CY7C106D/CY7C1006D, 1-Mbit (256 K × 4) Static RAM |         |            |                 |   |
|---|---------|------------|-----------------|---|
| Document Number: 38-05459   |         |            |                 |   |
| Rev.  | ECN No. | Issue Date | Orig. of Change | Description of Change   |
| **  | 201560  | See ECN    | SWI             | Advance information data sheet for C9 IPP   |
| *A  | 233693  | See ECN    | RKF             | I <sub>CC</sub> , I <sub>SB1</sub> , I <sub>SB2</sub> Specs are modified as per EROS (Spec # 01-2165)<br>Pb-free offering in the 'ordering information'   |
| *B  | 262950  | See ECN    | RKF             | Added T <sub>power</sub> Spec in Switching Characteristics table<br>Shaded 'Ordering Information'   |
| *C  | See ECN | See ECN    | RKF             | Reduced Speed bins to -10 and -12 ns  |
| *D  | 560995  | See ECN    | VKN             | Converted from Preliminary to Final<br>Removed Commercial Operating range<br>Removed 12 ns speed bin<br>Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz<br>Updated Thermal Resistance table<br>Updated Ordering Information table<br>Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #3  |
| *E  | 802877  | See ECN    | VKN             | Changed I <sub>CC</sub> spec from 60 mA to 80 mA for 100 MHz, 55 mA to 72 mA for 83 MHz, 45 mA to 58 mA for 66 MHz, 30 mA to 37 mA for 40 MHz   |
| *F  | 2898399 | 03/24/2010 | AJU             | Updated <a href="#">Package Diagrams</a> .  |
| *G  | 3104943 | 12/08/2010 | AJU             | Added <a href="#">Ordering Code Definitions</a> .   |
| *H  | 3244490 | 04/29/2011 | PRAS            | Updated <a href="#">Package Diagrams</a> .<br>Added <a href="#">Acronyms and Units of Measure</a> .<br>Updated in new template.   |
| *I  | 4033580 | 06/19/2013 | MEMJ            | Updated <a href="#">Functional Description</a> .<br>Updated <a href="#">Electrical Characteristics</a> :<br>Added one more Test Condition "I <sub>OH</sub> = -0.1 mA" for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition.<br>Added Note 4 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition "I <sub>OH</sub> = -0.1 mA".<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85031 – Changed revision from *D to *E. |
| *J  | 4385788 | 05/21/2014 | MEMJ            | Updated <a href="#">Package Diagrams</a> :<br>spec 51-85032 – Changed revision from *E to *F.<br>Completing Sunset.Review.  |
| *K  | 4579569 | 11/26/2014 | MEMJ            | Added related documentation hyperlink in page 1.<br>Removed the prune part number CY7C1006D-10VXI in <a href="#">Ordering Information</a> .   |

## Sales, Solutions and Legal Information

### Worldwide Sales and Design Support

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