CY7C109D
CY7C1009D

1-Mbit (128 K × 8) Static RAM

Features

- Pin- and function-compatible with CY7C109B/CY7C1009B
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 80 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 3 mA
- 2.0 V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ options
- CY7C109D available in Pb-free 32-pin 400-Mil wide Molded SOJ and 32-pin TSOP I packages. CY7C1009D available in Pb-free 32-pin 300-Mil wide Molded SOJ package

Functional Description

The CY7C109D/CY7C1009D [1] is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers.The eight input and output pins (I/O_0 through I/O_7) are placed in a high-impedance state when:

- Deselected ($\overline{CE}_1$ HIGH or CE_2 LOW),
- Outputs are disabled ($\overline{OE}$ HIGH),
- When the write operation is active ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW)

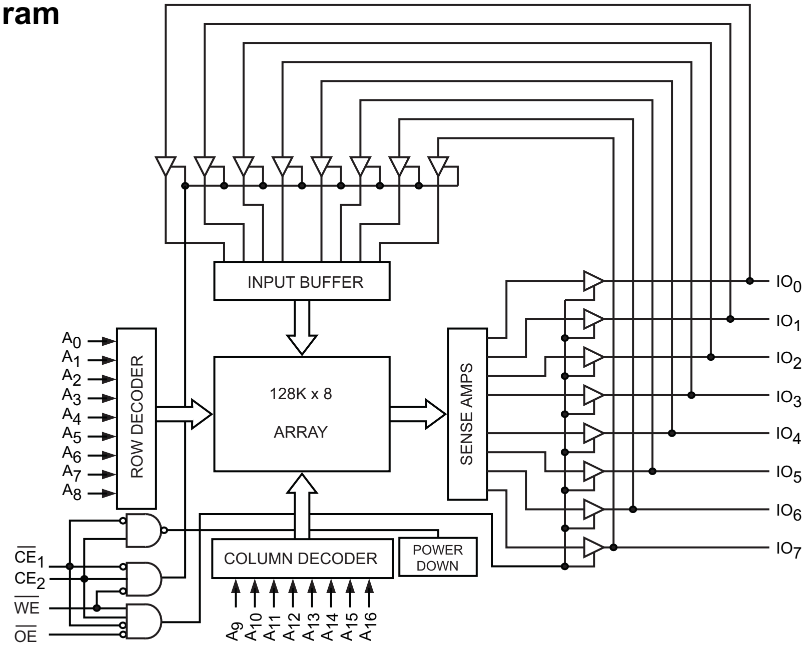
Write to the device by taking Chip Enable One ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Read from the device by taking Chip Enable One ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

The CY7C109D/CY7C1009D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

Logic Block Diagram



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Note

1. For guidelines on SRAM system design, please refer to the ‘System Design Guidelines’ Cypress application note, available on the internet at www.cypress.com.

Pin Configurations

Figure 1. 32-pin TSOP I pinout

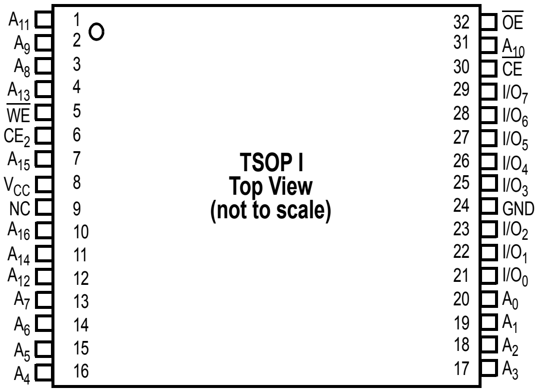
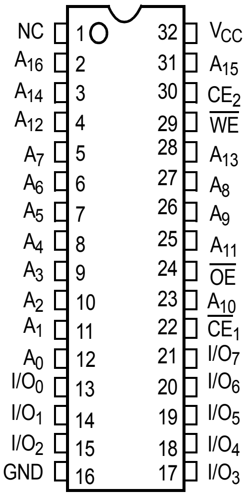


Figure 2. 32-pin SOJ pinout (Top View) [2]



Selection Guide

Description	CY7C109D-10 CY7C1009D-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	3	mA

Note

2. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage on
V_{CC} to Relative GND [3] ....–0.5 V to +6.0 V

DC Voltage Applied to Outputs
in High-Z State [3] ....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage [3] ....–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ....> 2001 V

Latch-up Current ....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		7C109D-10 7C1009D-10		Unit
				Min	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA		2.4	–	V
		I_{OH} = –0.1mA		–	3.4 [4]	
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage [3]			–0.5	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{max} = $1/t_{RC}$	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{max}		–	10	mA
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}_1 \geq V_{CC}$ – 0.3 V, or $CE_2 \leq$ 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0		–	3	mA

Note

[3] V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 1 V for pulse durations of less than 5 ns.

[4] Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.

Capacitance

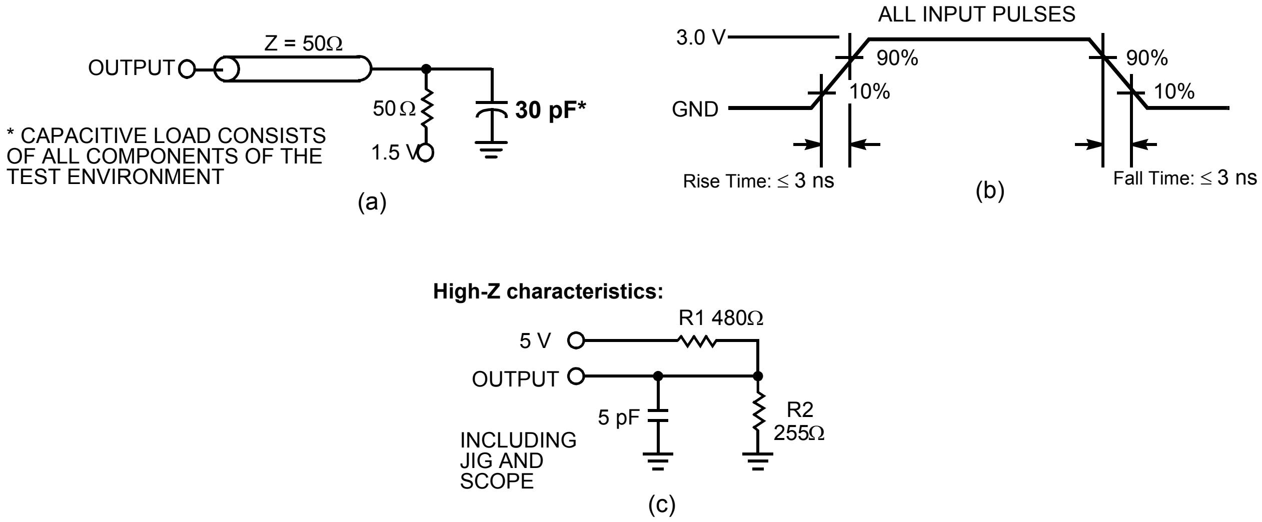
Parameter [5]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.61	56.29	50.72	°C/W
Θ_{JC}	Thermal resistance (junction to case)		40.53	38.14	16.21	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [6]



Notes

5. Tested initially and after any design or process changes that may affect these parameters.
6. AC characteristics (except High-Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

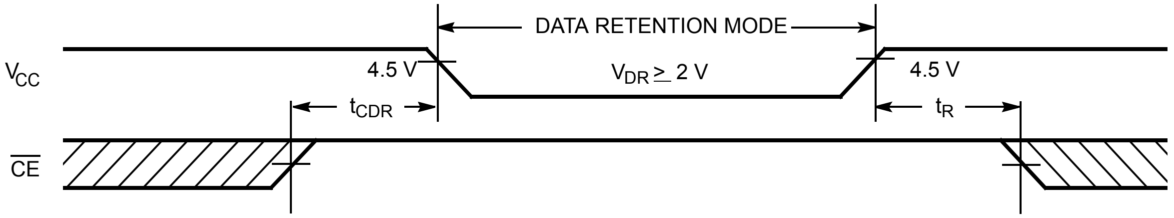
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE}_1 \geq V_{CC} - 0.3$ V or $CE_2 \leq 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	2.0	–	V
I_{CCDR}	Data Retention Current		–	3	mA
t_{CDR} [7]	Chip Deselect to Data Retention Time		0	–	ns
t_R [8]	Operation Recovery Time		t_{RC}	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

Switching Characteristics

Over the Operating Range

Parameter [9]	Description	7C109D-10 7C1009D-10		Unit
		Min	Max	
Read Cycle				
t_{power} [10]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read Cycle Time	10	–	ns
t_{AA}	Address to Data Valid	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [11, 12]	–	5	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z [12]	3	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z [11, 12]	–	5	ns
t_{PU} [13]	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0	–	ns
t_{PD} [13]	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down	–	10	ns
Write Cycle [14, 15]				
t_{WC}	Write Cycle Time	10	–	ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	7	–	ns
t_{AW}	Address Set-Up to Write End	7	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-Up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	–	ns
t_{SD}	Data Set-Up to Write End	6	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [12]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [11, 12]	–	5	ns

Notes

[9] Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

[10] t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.

[11] t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 3 on page 5. Transition is measured when the outputs enter a high impedance state.

[12] At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

[13] This parameter is guaranteed by design and is not tested.

[14] The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

[15] The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

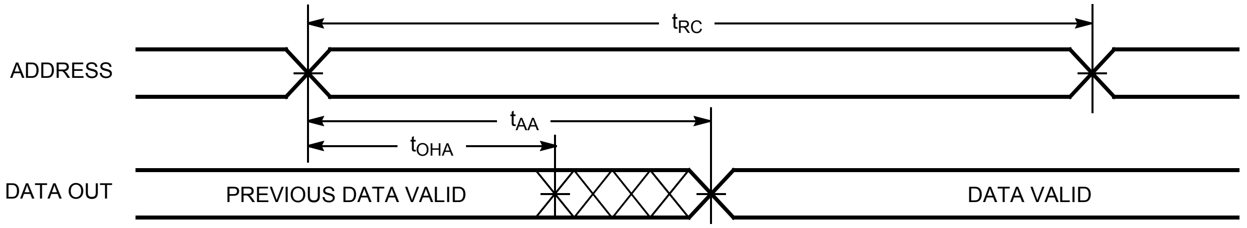


Figure 5. Read Cycle No. 1 (Address Transition Controlled) [16, 17]

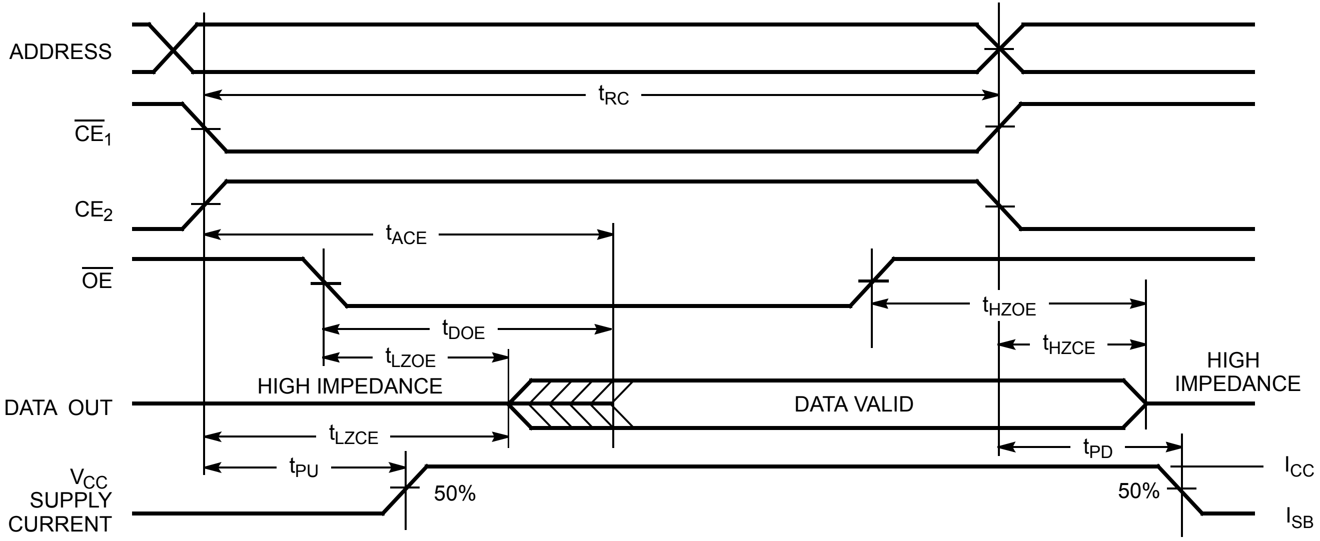


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [17, 18]

Notes

16. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled) [19, 20]

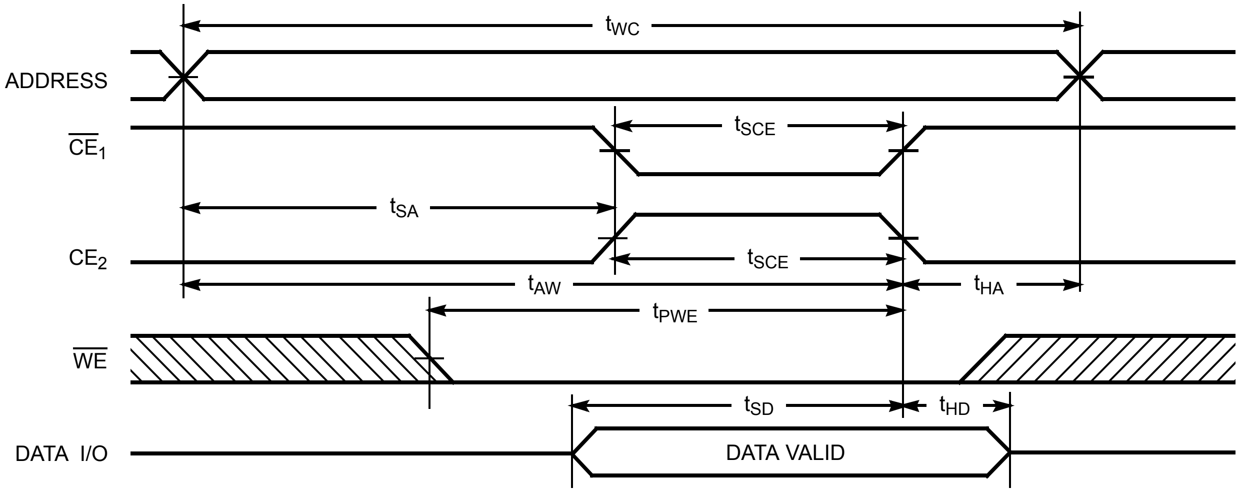
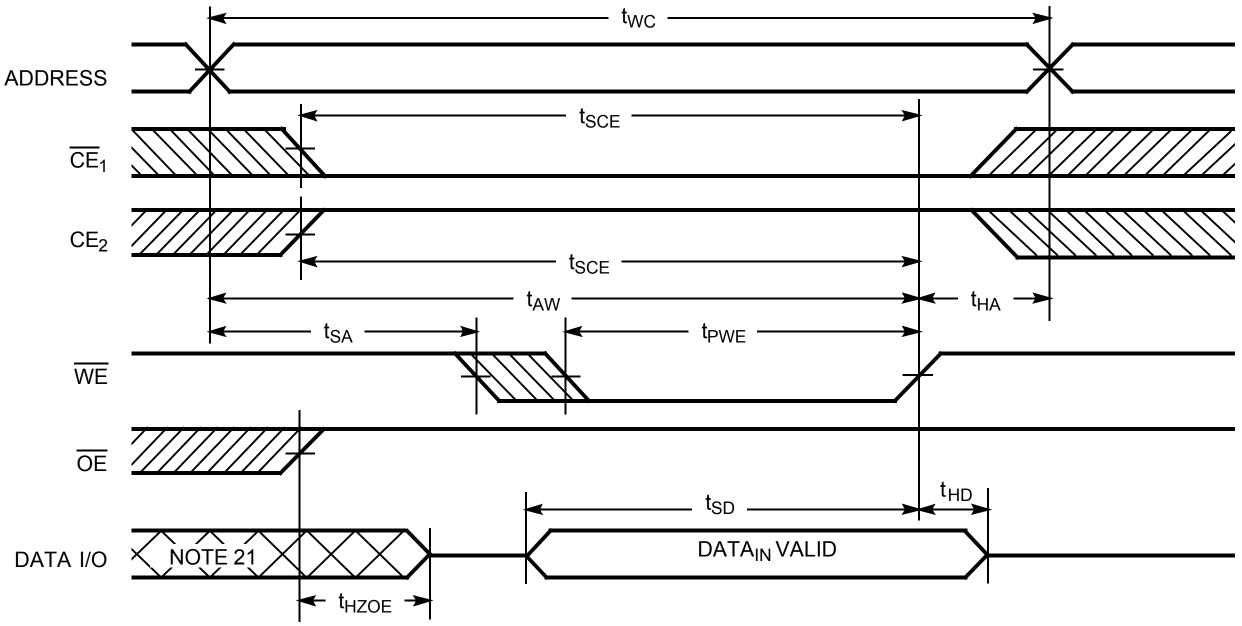


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [19, 20]



Notes

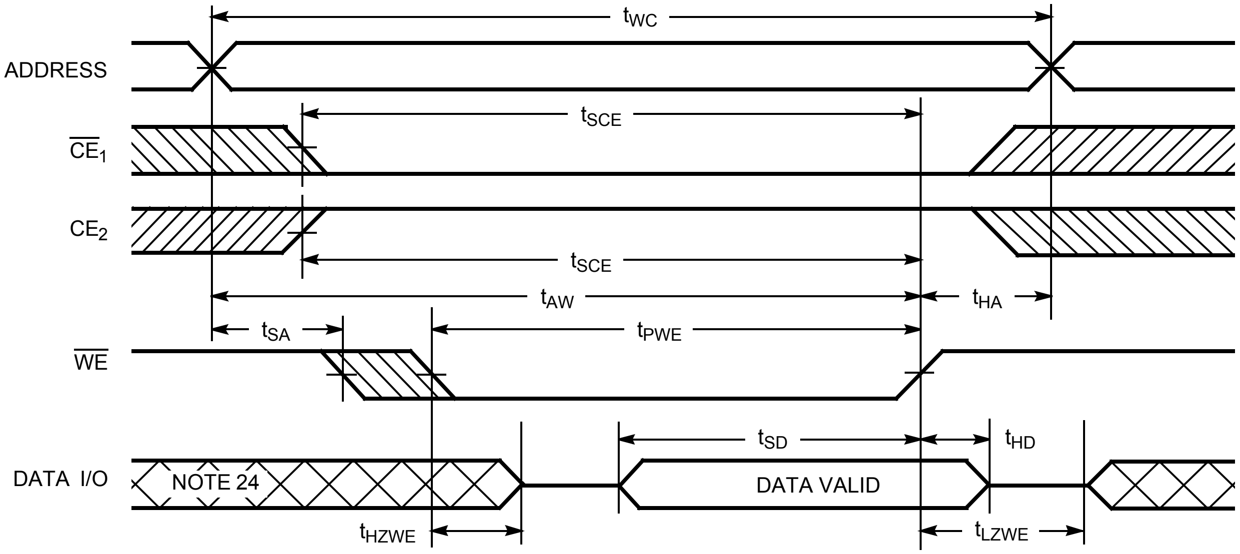
[19] Data I/O is high impedance if $\overline{OE} = V_{IH}$.

[20] If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

[21] During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [22, 23]



Notes

22. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
23. If $\overline{\text{CE}}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
24. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

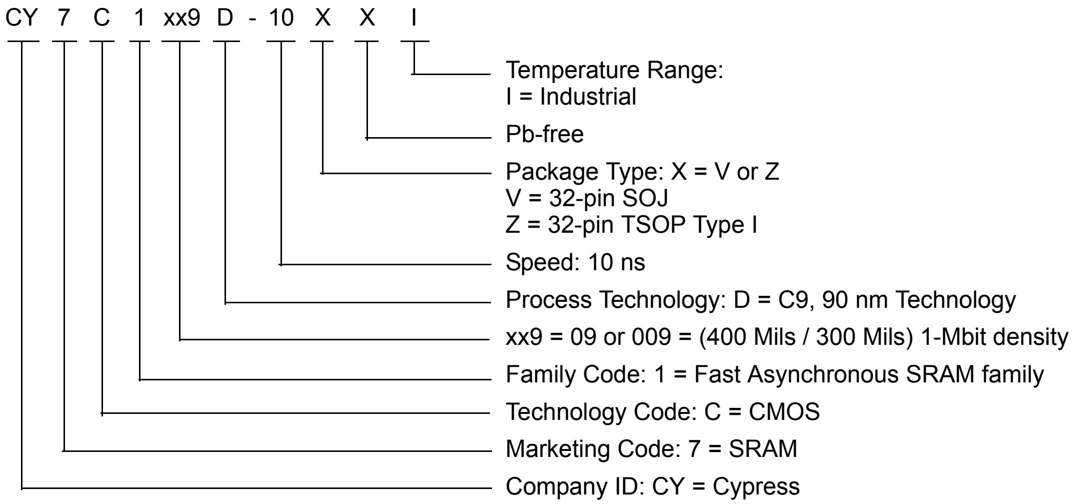
$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I_{SB})
X	L	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C109D-10VXI	51-85033	32-pin SOJ (400 Mils) Pb-free	Industrial
	CY7C109D-10ZXI	51-85056	32-pin TSOP (Type I) Pb-free	
	CY7C1009D-10VXI	51-85041	32-pin SOJ (300 Mils) Pb-free	

Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Temperature Range:
I = Industrial

Pb-free

Package Type: X = V or Z
V = 32-pin SOJ
Z = 32-pin TSOP Type I

Speed: 10 ns

Process Technology: D = C9, 90 nm Technology

xx9 = 09 or 009 = (400 Mils / 300 Mils) 1-Mbit density

Family Code: 1 = Fast Asynchronous SRAM family

Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

Package Diagrams

Figure 10. 32-pin SOJ (300 Mils) V32.3 (Catalog 32.3 Molded SOJ) Package Outline, 51-85041

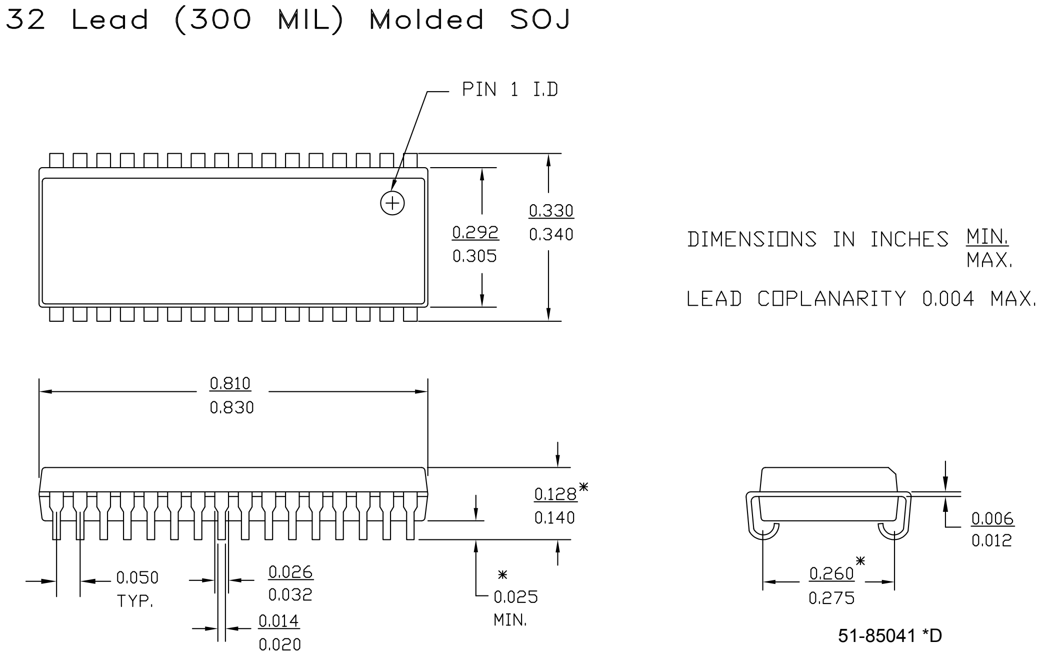
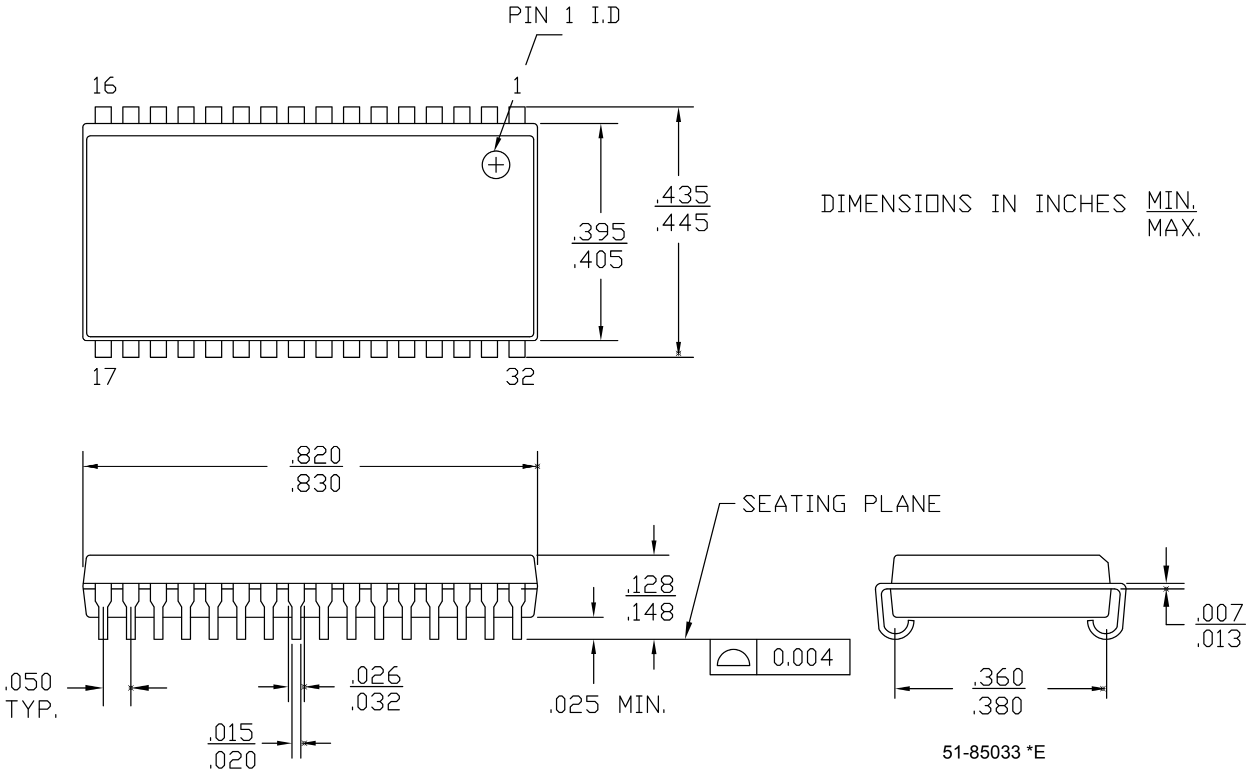
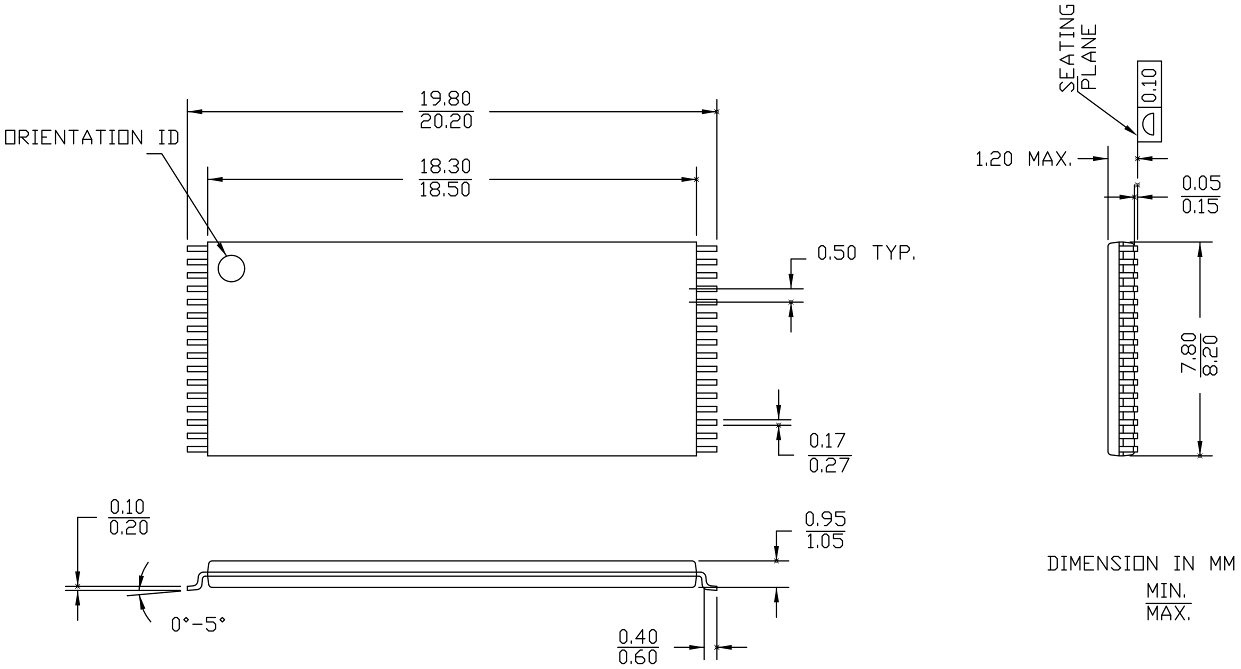


Figure 11. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033



Package Diagrams (continued)

Figure 12. 32-pin TSOP I (8 × 20 × 1.0 mm) Z32R Package Outline, 51-85056



51-85056 *G

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C109D/CY7C1009D, 1-Mbit (128 K × 8) Static RAM **Document Number: 38-05468**				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics Table Shaded Ordering Information
*C	See ECN	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I_{CC} values for the frequencies 83MHz, 66MHz and 40MHz Changed Overshoot spec from V_{CC}+2 V to V_{CC}+1 V in footnote #3 Updated Thermal Resistance table Updated Ordering Information Table
*E	802877	See ECN	VKN	Changed I_{CC} spec from 60 mA to 80 mA for 100 MHz, 55 mA to 72 mA for 83 MHz, 45 mA to 58 mA for 66 MHz, 30 mA to 37 mA for 40 MHz
*F	3104943	12/08/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.
*G	3220123	04/08/2011	PRAS	Updated package diagrams: 51-85033 to *D 51-85056 to *F Added Acronyms and Units of measure. Updated template and styles as per current Cypress standards.
*H	4041855	06/27/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition “I_{OH} = –0.1 mA” for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 4 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition “I_{OH} = –0.1 mA”. Updated Package Diagrams: spec 51-85041 – Changed revision from *B to *C. Updated in new template.
*I	4386284	05/21/2014	MEMJ	Updated Package Diagrams: spec 51-85033 – Changed revision from *D to *E. spec 51-85056 – Changed revision from *F to *G. Completing Sunset Review.
*J	4578447	01/16/2015	MEMJ	Added related documentation hyperlink in page 1. Updated Figure 10 in Package Diagrams (spec 51-85041 *C to *D).

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