CY7C1371S

18-Mbit (512K × 36) Flow-Through SRAM with NoBL™ Architecture

Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133-MHz bus operations with zero wait states
- Data is transferred on every clock
- Pin-compatible and functionally equivalent to ZBT™ devices
- Internally self-timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte Write capability
- 3.3 V/2.5 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self-timed writes
- Asynchronous Output Enable
- Available in JEDEC-standard Pb-free 100-pin TQFP, and non Pb-free 119-ball BGA
- Three chip enables for simple depth expansion
- Automatic Power down feature available using ZZ mode or CE deselect
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- Burst Capability – linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1371S is a 3.3 V, 512K × 36 Synchronous flow through Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations with no wait state insertion. The CY7C1371S is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write-Read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

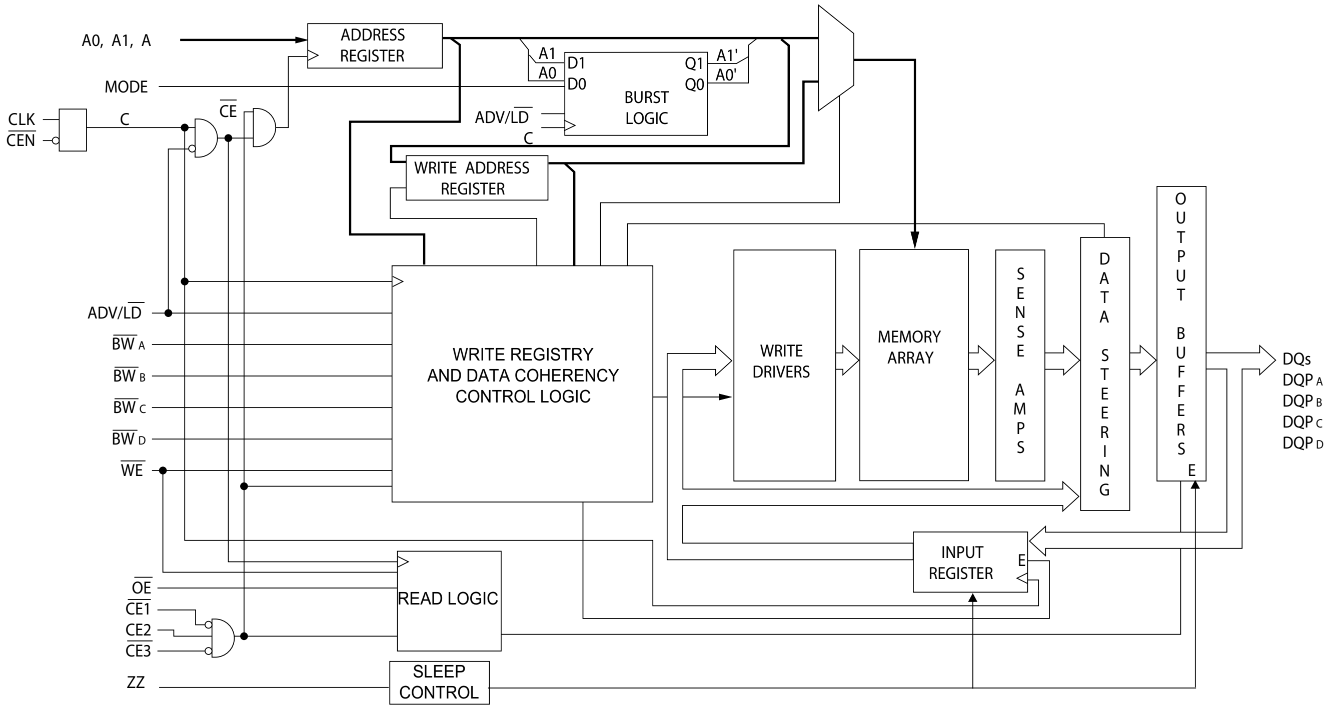
Write operations are controlled by the two or four Byte Write Select ($\overline{BW_X}$) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	210	mA
Maximum CMOS Standby Current	70	mA

Logic Block Diagram – CY7C1371S



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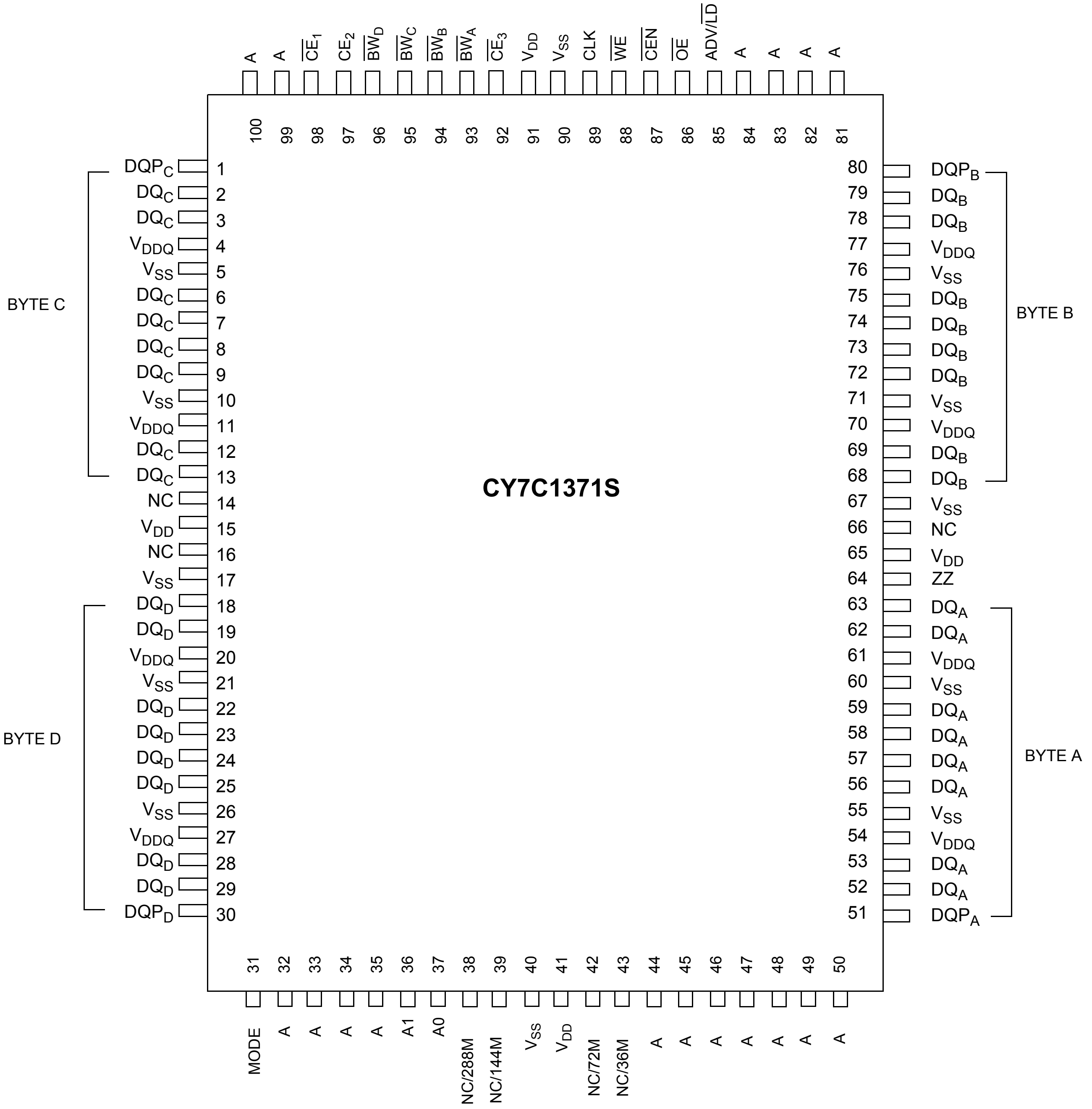
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Pin Configurations (continued)

Figure 2. 119-ball BGA (14 × 22 × 2.4 mm) pinout

CY7C1371S (512K × 36)

	1	**2**	**3**	**4**	**5**	**6**	**7**
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC/576M	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE}_3$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	A	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{WE}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. While deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and $DQP_{[A:D]}$ are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to DQ_s.
MODE	Input Strap Pin	**Mode Input. Selects the Burst Order of the Device**. When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**.
TDO	JTAG serial output Synchronous	**Serial Data Out to the JTAG Circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being used, this pin must be left unconnected. This pin is not available on TQFP packages.

Pin Definitions (continued)

Name	I/O	Description
TDI	JTAG serial input Synchronous	**Serial Data In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial Data In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock Input to the JTAG Circuitry**. If the JTAG feature is not being used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die. NC/(36M, 72M, 144M, 288M, 576M, 1G) are address expansion pins and are not internally connected to the die.

Functional Overview

The CY7C1371S is a synchronous flow through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{\text{CEN}}$). If $\overline{\text{CEN}}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{\text{CEN}}$. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{\text{CE}}_1$, CE_2, $\overline{\text{CE}}_3$) active at the rising edge of the clock. If Clock Enable ($\overline{\text{CEN}}$) is active LOW and ADV/$\overline{\text{LD}}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{\text{WE}}$). $\overline{\text{BW}}_X$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{\text{WE}}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{\text{CE}}_1$, CE_2, $\overline{\text{CE}}_3$) and an asynchronous Output Enable ($\overline{\text{OE}}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{\text{LD}}$ must be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{\text{CEN}}$ is asserted LOW
- $\overline{\text{CE}}_1$, CE_2, and $\overline{\text{CE}}_3$ are ALL asserted active
- The Write Enable input signal $\overline{\text{WE}}$ is deasserted HIGH
- ADV/$\overline{\text{LD}}$ is asserted LOW.

The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{\text{OE}}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{\text{OE}}$ and the internal control logic. $\overline{\text{OE}}$ must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1371S has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{\text{LD}}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A_0 and A_1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{\text{LD}}$ increments the internal burst counter regardless of the state of chip enable inputs or $\overline{\text{WE}}$. $\overline{\text{WE}}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{\text{CEN}}$ is asserted LOW, (2) $\overline{\text{CE}}_1$, CE_2, and $\overline{\text{CE}}_3$ are ALL asserted active, and (3) the write signal $\overline{\text{WE}}$ is asserted LOW. The address presented to the address bus is loaded into the Address Register. The write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{\text{OE}}$ input signal. This allows the external logic to present the data on DQs and DQP_X.

On the next clock rise the data presented to DQs and DQP_X (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by $\overline{\text{BW}}_X$ signals. The CY7C1371S provides byte write capability that is described in the truth table. Asserting the Write Enable input ($\overline{\text{WE}}$) with the selected Byte Write Select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1371S is a common I/O device, data must not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and DQP_X are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1371S has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in the Single Write Access section. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the Chip Enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}_X$ inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	80	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1371S follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{\text{CE}}_1$	CE_2	$\overline{\text{CE}}_3$	ZZ	ADV/$\overline{\text{LD}}$	$\overline{\text{WE}}$	$\overline{\text{BW}}_X$	$\overline{\text{OE}}$	$\overline{\text{CEN}}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L–>H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L–>H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L–>H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L–>H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L–>H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L–>H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L–>H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L–>H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L–>H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L–>H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L–>H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L–>H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L–>H	–
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Partial Truth Table for Read/Write

Function (CY7C1371S) [1, 2, 8]	$\overline{\text{WE}}$	$\overline{\text{BW}}_A$	$\overline{\text{BW}}_B$	$\overline{\text{BW}}_C$	$\overline{\text{BW}}_D$
Read	H	X	X	X	X
Write No bytes written	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write Byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write Byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write Byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Notes

1. X = "Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{\text{BW}}_X$ = 0 signifies at least one Byte Write Select is active, $\overline{\text{BW}}_X$ = Valid signifies that the desired byte write selects are asserted, see truth table for details.
2. Write is defined by $\overline{\text{BW}}_X$, and $\overline{\text{WE}}$. See truth table for Read/Write.
3. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
4. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{\text{OE}}$ signal. $\overline{\text{OE}}$ is asynchronous and is not sampled with the clock.
5. $\overline{\text{CEN}}$ = H, inserts wait states.
6. Device powers up deselected and the IOs in a tri-state condition, regardless of $\overline{\text{OE}}$.
7. $\overline{\text{OE}}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = Tri-state when $\overline{\text{OE}}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{\text{OE}}$ is active.
8. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{\text{BW}}_X$ is valid Appropriate write is based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1371S incorporates a serial boundary scan test access port (TAP).This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1371S contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device is up in a reset state which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram on page 12. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Identification Codes on page 16). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and scans data into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 13. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This shifts data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 16.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Identification Codes on page 16. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller is moved into the Update-IR state.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the shift-DR controller state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO balls and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is supplied a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

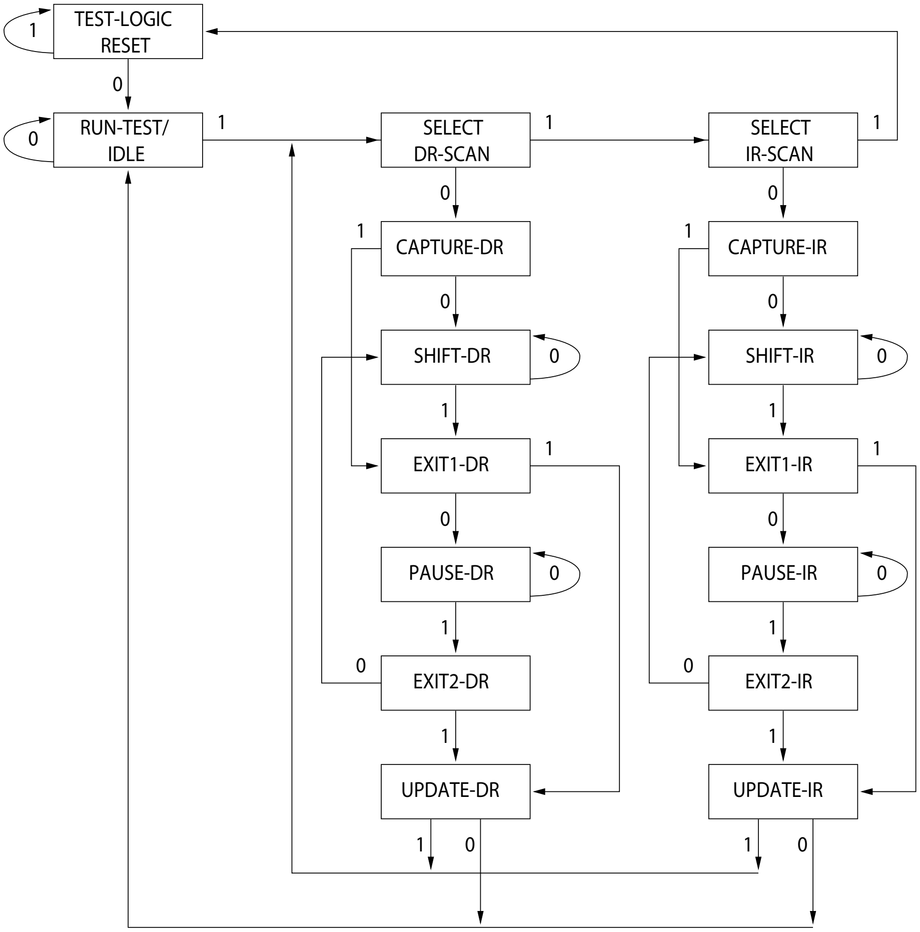
The boundary scan register has a special bit located at bit #85 (for 119-ball BGA package). When this scan cell, called the "extest output bus tri-state," is latched into the preload register during the "Update-DR" state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR," the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

Reserved

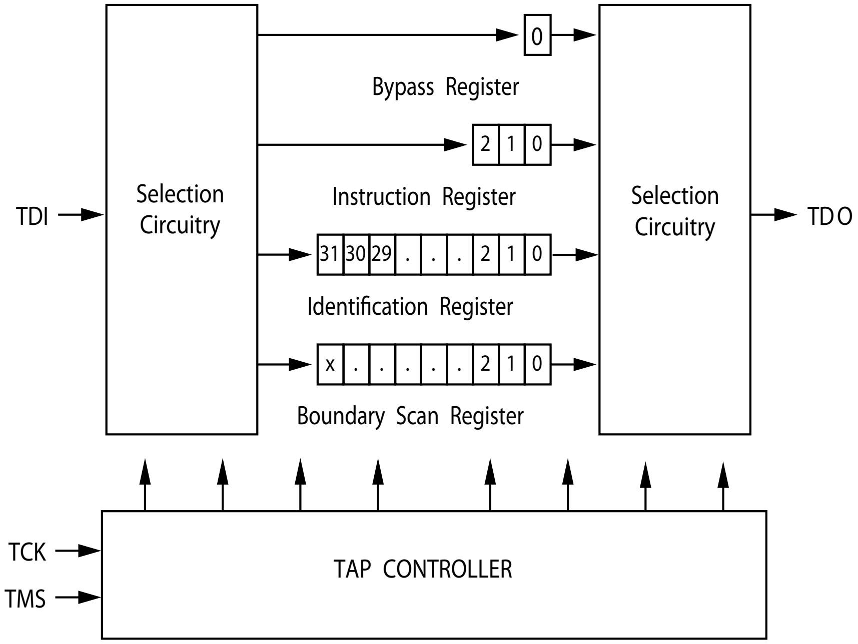
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



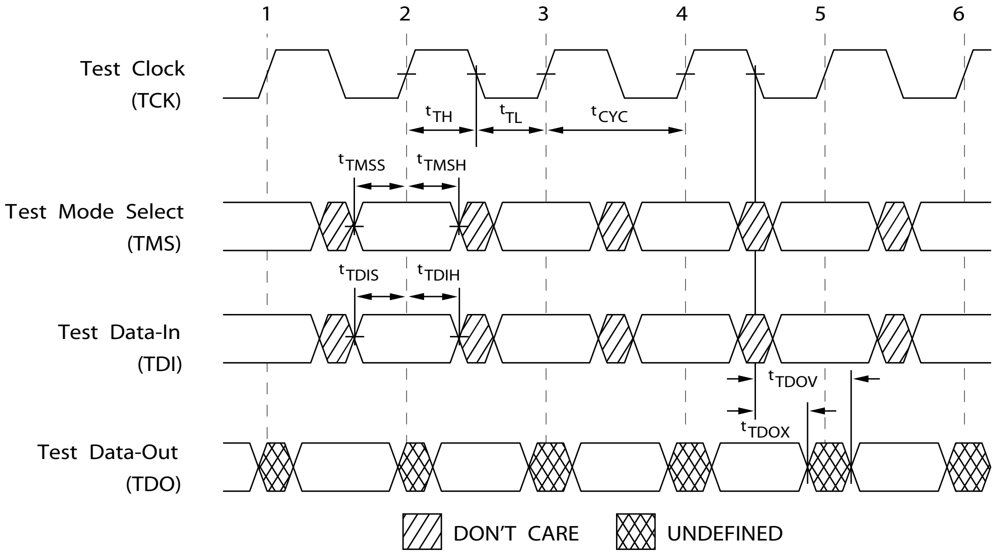
The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing

Figure 3. TAP Timing



TAP AC Switching Characteristics

Over the Operating Range

Parameter [9, 10]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH time	20	–	ns
t_{TL}	TCK Clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

Notes

[9] t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.

[10] Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

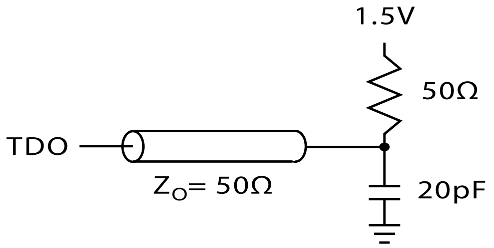
3.3 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 3.3 V
Input rise and fall times ....1 ns
Input timing reference levels .... 1.5 V
Output reference levels .... 1.5 V
Test load termination supply voltage .... 1.5 V

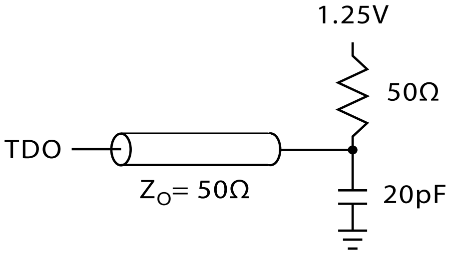
2.5 V TAP AC Test Conditions

Input pulse level .... V_{SS} to 2.5 V
Input rise and fall time ....1 ns
Input timing reference levels .... .1.25 V
Output reference levels .... 1.25 V
Test load termination supply voltage .... 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter [11]	Description	Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	V_{DDQ} = 3.3 V	2.4	–	V
		I_{OH} = –1.0 mA	V_{DDQ} = 2.5 V	2.0	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
		I_{OL} = 1.0 mA	V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3 V	–0.5	0.7	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input Load Current	GND $\leq V_{IN} \leq V_{DDQ}$		–5	5	µA

Note

[11] All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1371S (512K × 36)	Description
Revision Number (31:29)	000	Describes the version number
Device Depth (28:24)	01011	Reserved for internal use
Device Width (23:18)	001001	Defines memory type and architecture
Cypress Device ID (17:12)	100101	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary Scan Order (119-ball BGA package)	85

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Boundary Scan Order

119-ball BGA [12, 13]

Bit #	Ball ID
1	H4
2	T4
3	T5
4	T6
5	R5
6	L5
7	R6
8	U6
9	R7
10	T7
11	P6
12	N7
13	M6
14	L7
15	K6
16	P7
17	N6
18	L6
19	K7
20	J5
21	H6
22	G7
23	F6
24	E7
25	D7
26	H7
27	G6
28	E6
29	D6
30	C7
31	B7
32	C6
33	A6
34	C5
35	B5
36	G5
37	B6
38	D4
39	B4
40	F4
41	M4
42	A5
43	K4
44	E4
45	G4
46	A4
47	G3
48	C3
49	B2
50	B3
51	A3
52	C2
53	A2
54	B1
55	C1
56	D2
57	E1
58	F2
59	G1
60	H2
61	D1
62	E2
63	G2
64	H1
65	J3
66	2K
67	L1
68	M2
69	N1
70	P1
71	K1
72	L2
73	N2
74	P2
75	R3
76	T1
77	R1
78	T2
79	L3
80	R2
81	T3
82	L4
83	N4
84	P4
85	Internal

Notes

[12] Balls which are NC (No Connect) are pre-set LOW.

[13] Bit# 85 is pre-set HIGH.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to $+V_{DD}$

DC Voltage Applied to Outputs in Tri-State ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [14, 15]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [14]	for 3.3 V I/O		2.0	V_{DD} + 0.3	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage [14]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	$GND \leq V_I \leq V_{DDQ}$		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{DD} [16]	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{CYC}$	7.5 ns cycle, 133 MHz	–	210	mA
I_{SB1}	Automatic CE Power down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$, inputs switching	7.5 ns cycle, 133 MHz	–	140	mA
I_{SB2}	Automatic CE Power down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DD} - 0.3$ V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	70	mA
I_{SB3}	Automatic CE Power down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, $f = f_{MAX}$, inputs switching	7.5 ns cycle, 133 MHz	–	130	mA
I_{SB4}	Automatic CE Power down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	80	mA

Notes

14. Overshoot: $V_{IH(AC)} < V_{DD}$ +1.5V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)} > -2V$ (Pulse width less than $t_{CYC}/2$).
15. $T_{Power\ up}$: Assumes a linear ramp from 0V to $V_{DD(min.)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
16. The operation current is calculated with 50% read cycle and 50% write cycle.

Capacitance

Parameter [17]	Description	Test Conditions	100-pin TQFP Package	119-ball BGA Package	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	8	pF
C_{CLK}	Clock input capacitance		5	8	pF
C_{IO}	Input/Output capacitance		5	8	pF

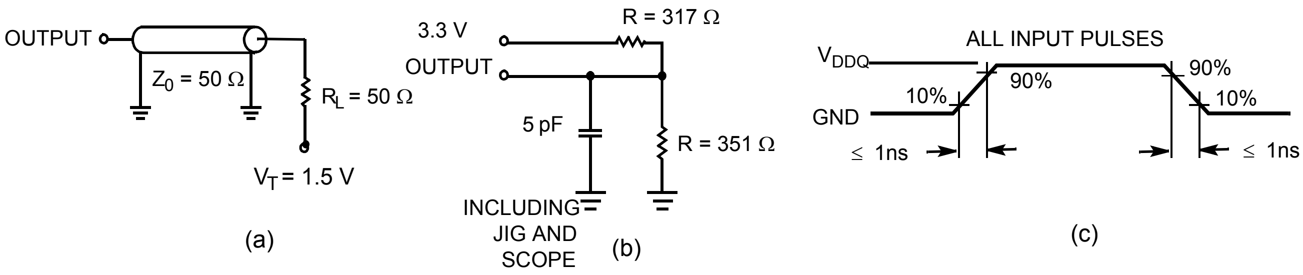
Thermal Resistance

Parameter [17]	Description	Test Conditions	100-pin TQFP Package	119-ball BGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	28.66	23.8	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.08	6.2	°C/W

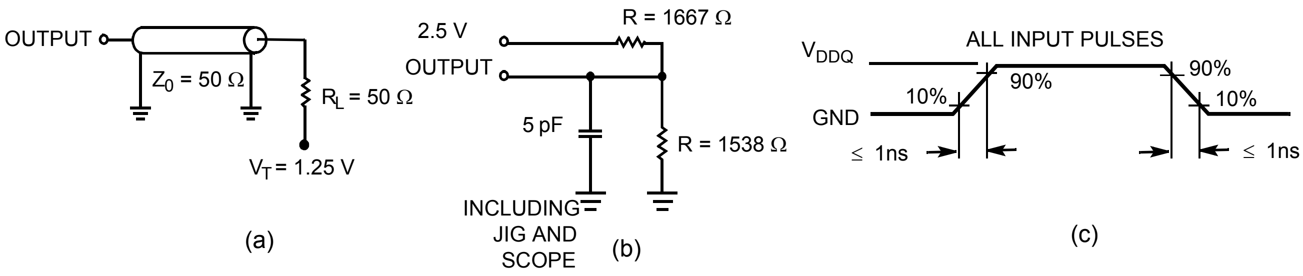
AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Note

17. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [18, 19]	Description	133 MHz		Unit
		Min	Max	
t_{POWER}[20]		1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	7.5	–	ns
t_{CH}	Clock HIGH	2.1	–	ns
t_{CL}	Clock LOW	2.1	–	ns
Output Times				
t_{CDV}	Data Output Valid After CLK Rise	–	6.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0	–	ns
t_{CLZ}	Clock to Low Z [21, 22, 23]	2.0	–	ns
t_{CHZ}	Clock to High Z [21, 22, 23]	–	4.0	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.2	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [21, 22, 23]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [21, 22, 23]	–	4.0	ns
Setup Times				
t_{AS}	Address Setup Before CLK Rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ Setup Before CLK Rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ Setup Before CLK Rise	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.5	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ Hold After CLK Rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW_X}$ Hold After CLK Rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5	–	ns

Notes

18. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
19. Test conditions shown in (a) of Figure 4 on page 19 unless otherwise noted.
20. This part has a voltage regulator internally; t_{POWER} is the time that the power is supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
21. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 4 on page 19. Transition is measured ±200 mV from steady-state voltage.
22. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
23. This parameter is sampled and not 100% tested.

Switching Waveforms

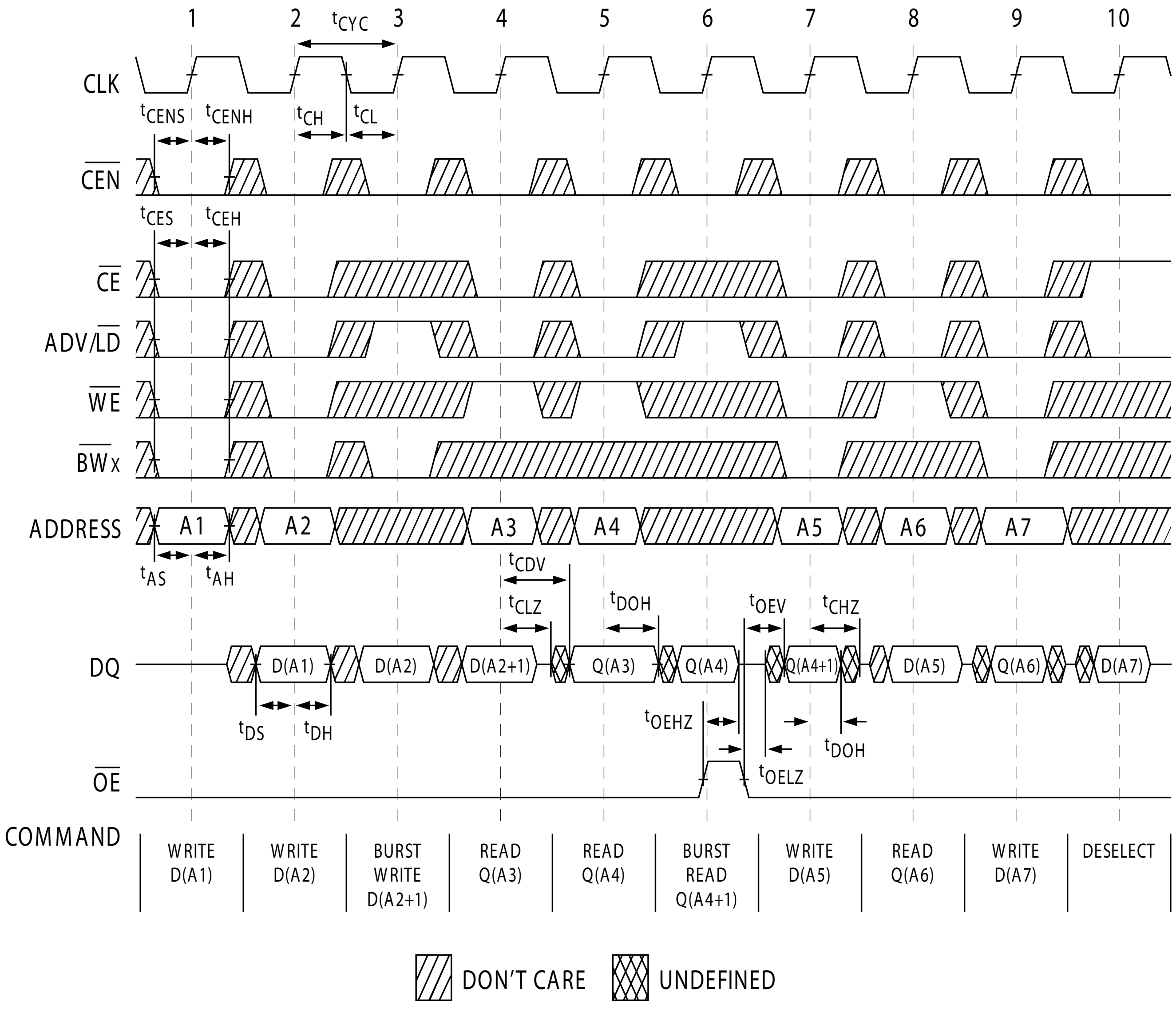


Figure 5. Read/Write Waveforms [24, 25, 26]

Notes

[24] For this waveform ZZ is tied LOW.

[25] When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

[26] Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

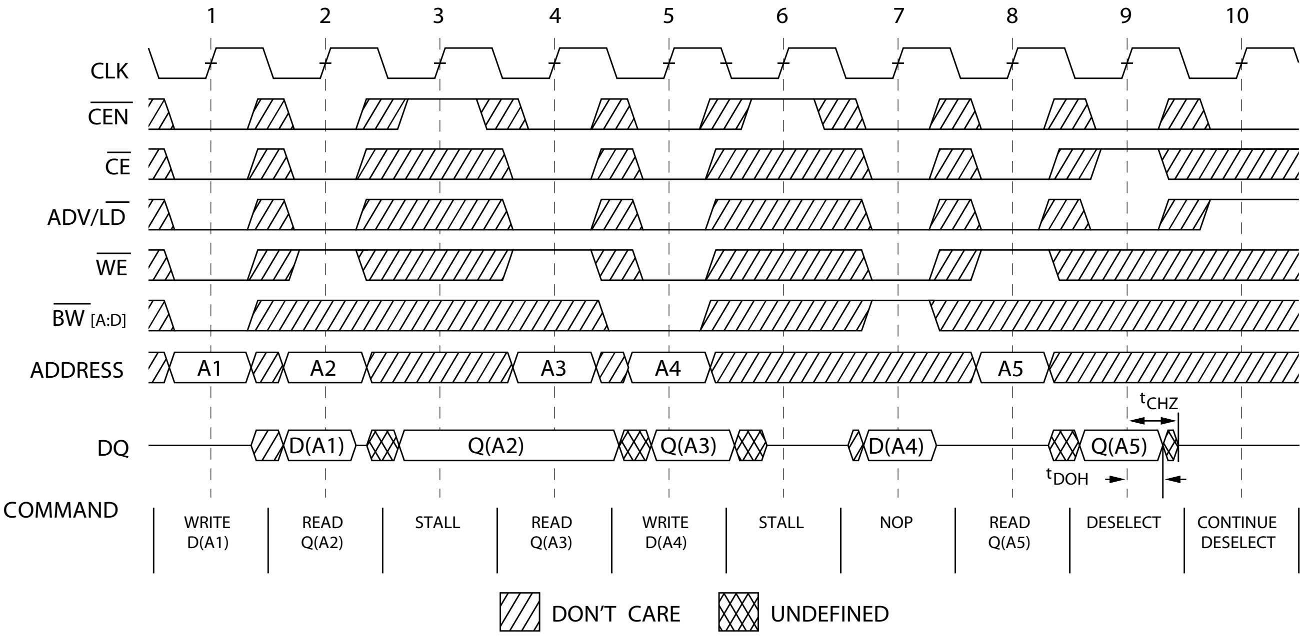


Figure 6. NOP, STALL AND DESELECT Cycles [27, 28, 29]

Notes

[27] For this waveform ZZ is tied LOW.

[28] When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

[29] The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

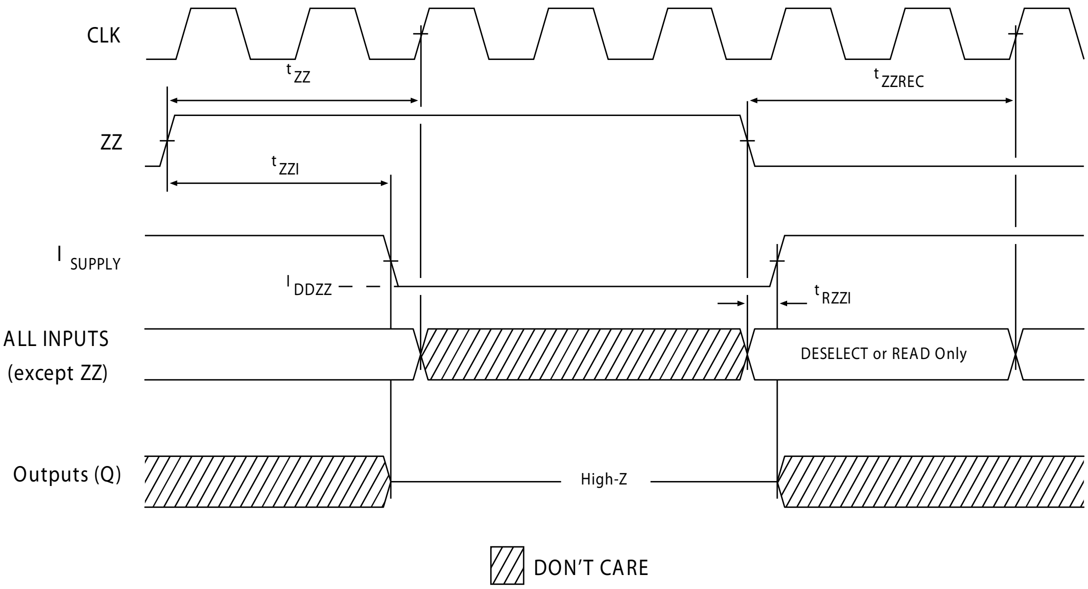


Figure 7. ZZ Mode Timing [30, 31]

Notes

30. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
31. DQs are in high Z when exiting ZZ sleep mode.

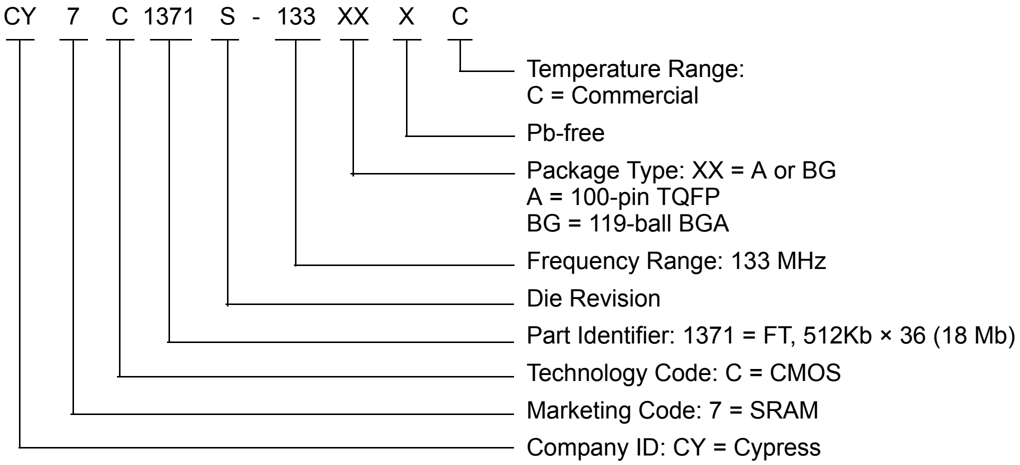
Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available.For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

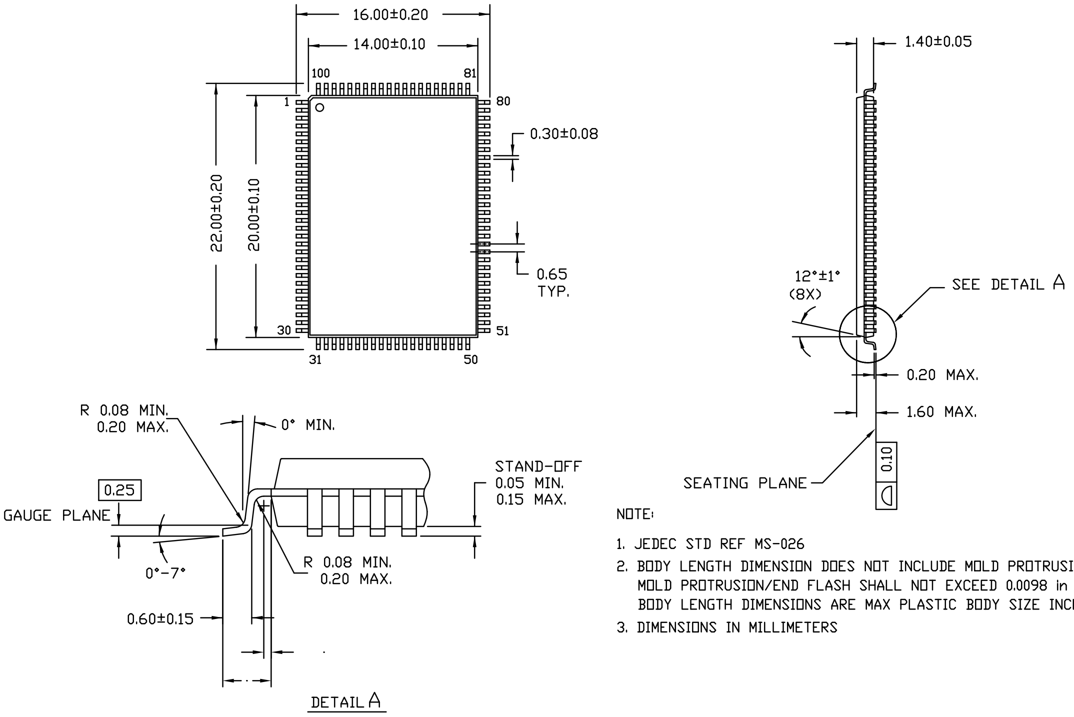
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1371S-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1371S-133BGC	51-85115	119-ball BGA (14 × 22 × 2.4 mm)	

Ordering Code Definitions



Package Diagrams

Figure 8. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



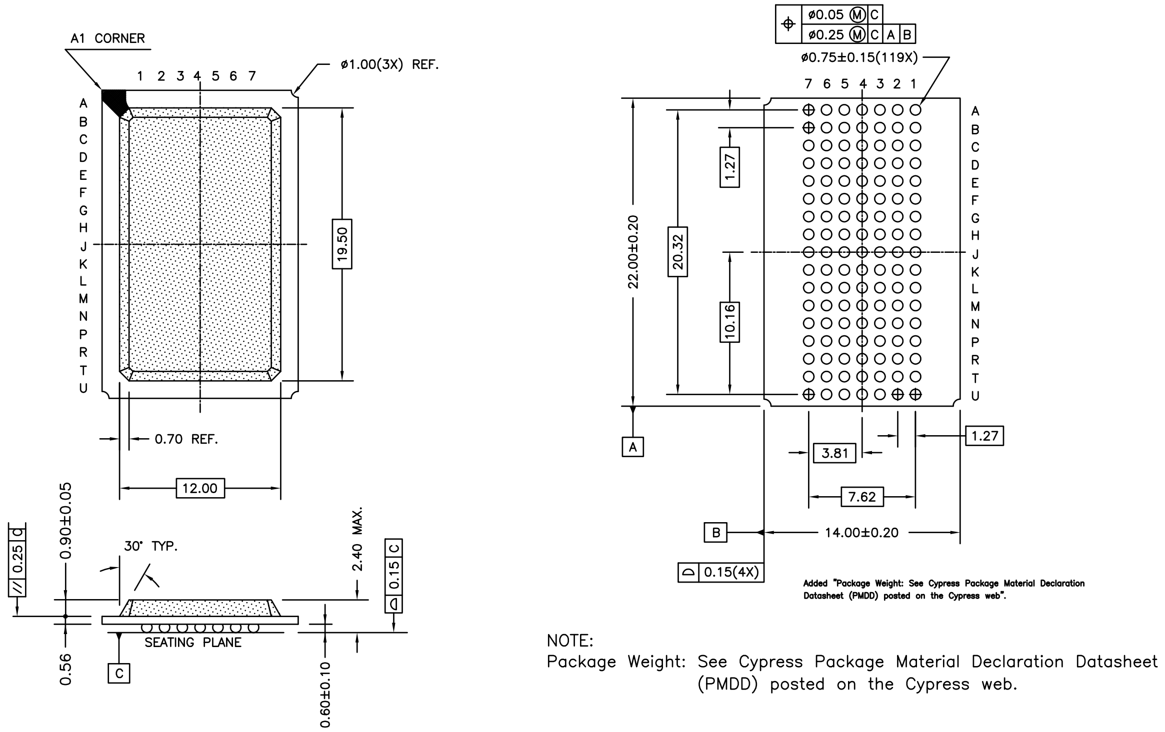
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E

Package Diagrams (continued)

Figure 9. 119-ball BGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Acronym	Description
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data-In
TDO	Test Data-Out
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1371S, 18-Mbit (512K × 36) Flow-Through SRAM with NoBL™ Architecture
Document Number: 001-43826

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	1898286	See ECN	VKN / AESA	New data sheet.
*A	2082246	See ECN	JASM	Changed status from Preliminary to Final.
*B	2897885	03/23/10	NJY	Updated Ordering Information (Removed inactive parts). Updated Package Diagrams.
*C	3203729	03/23/2011	NJY	Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Updated to new template.
*D	3571224	04/03/2012	PRIT	Updated Features (Removed 165-ball FBGA package and Pb-free 119-ball BGA related information). Updated Functional Description (Removed CY7C1373S related information, removed the Note For best practices or recommendations, please refer to the Cypress application note AN1064, SRAM System Design Guidelines on www.cypress.com.” and its reference). Updated Selection Guide (Removed 100 MHz frequency related information). Removed Logic Block Diagram – CY7C1373S. Updated Pin Configurations (Removed CY7C1373S related information, and 165-ball FBGA package related information). Updated Functional Overview (Removed CY7C1373S related information). Updated Truth Table (Removed CY7C1373S related information). Removed Partial Truth Table for Read/Write (Corresponding to CY7C1373S). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1373S related information). Updated Identification Register Definitions (Removed CY7C1373S related information). Updated Scan Register Sizes (Removed 165-ball FBGA package related information and removed Bit Size (× 18) column). Removed Boundary Scan Order (Corresponding to 165-ball FBGA package). Updated Operating Range (Removed Industrial Temperature range). Updated Electrical Characteristics (Removed 100 MHz frequency related information). Updated Capacitance (Removed 165-ball FBGA package related information). Updated Thermal Resistance (Removed 165-ball FBGA package related information). Updated Switching Characteristics (Removed 100 MHz frequency related information). Updated Package Diagrams (Removed 165-ball FBGA package related information). Replaced all instances of IO with I/O across the document.
*E	3978170	04/22/2013	PRIT	Updated Package Diagrams: spec 51-85115 – Changed revision from *C to *D. Completing Sunset Review.
*F	5181234	03/18/2016	PRIT	Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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