CY7C1371DV25
CY7C1373DV25

18-Mbit (512K x 36/1M x 18) Flow-Through SRAM with NoBL™ Architecture

Features

- **No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles**
- **Can support up to 133-MHz bus operations with zero wait states**
  - **— Data is transferred on every clock**
- **Pin compatible and functionally equivalent to ZBT™ devices**
- **Internally self-timed output buffer control to eliminate the need to use $\overline{\text{OE}}$**
- **Registered inputs for flow-through operation**
- **Byte Write capability**
- **2.5V core power supply (V_{DD})**
- **2.5V I/O power supply (V_{DDQ})**
- **Fast clock-to-output times**
  - **— 6.5 ns (for 133-MHz device)**
- **Clock Enable ($\overline{\text{CEN}}$) pin to enable clock and suspend operation**
- **Synchronous self-timed writes**
- **Asynchronous Output Enable**
- **Available in JEDEC-standard lead-free 100-Pin TQFP, lead-free and non-lead-free 119-Ball BGA and 165- Ball FBGA package.**
- **Three chip enables for simple depth expansion**
- **Automatic Power-down feature available using ZZ mode or CE deselect**
- **IEEE 1149.1 JTAG-Compatible Boundary Scan**
- **Burst Capability—linear or interleaved burst order**
- **Low standby power**

Functional Description[1]

The CY7C1371DV25/CY7C1373DV25 is a 2.5V, 512K x 36/1M x 18 Synchronous Flow-through Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1371DV25/CY7C1373DV25 is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent Write-Read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{\text{CEN}}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by the two or four Byte Write Select ($\overline{\text{BW}}_X$) and a Write Enable ($\overline{\text{WE}}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{\text{CE}}_1$, CE_2, $\overline{\text{CE}}_3$) and an asynchronous Output Enable ($\overline{\text{OE}}$) provide for easy bank selection and output tri-state control. In order to avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

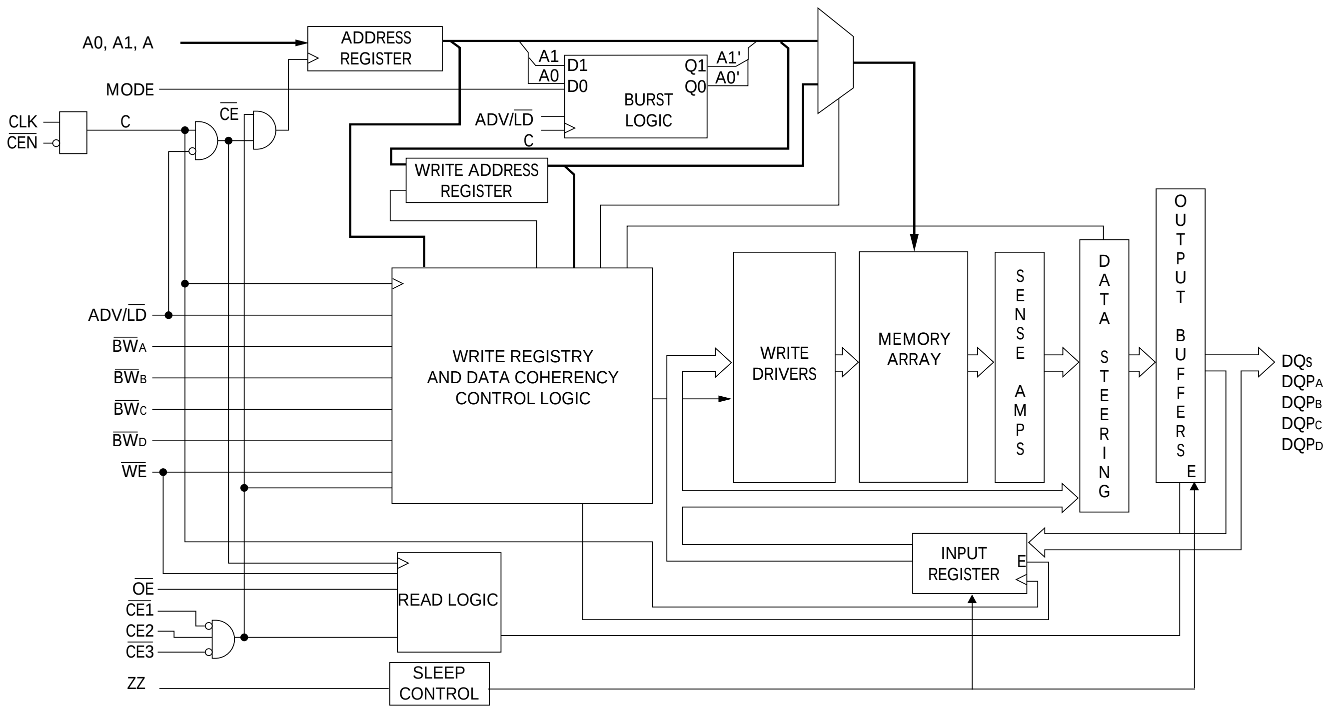
Selection Guide

	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	210	175	mA
Maximum CMOS Standby Current	70	70	mA

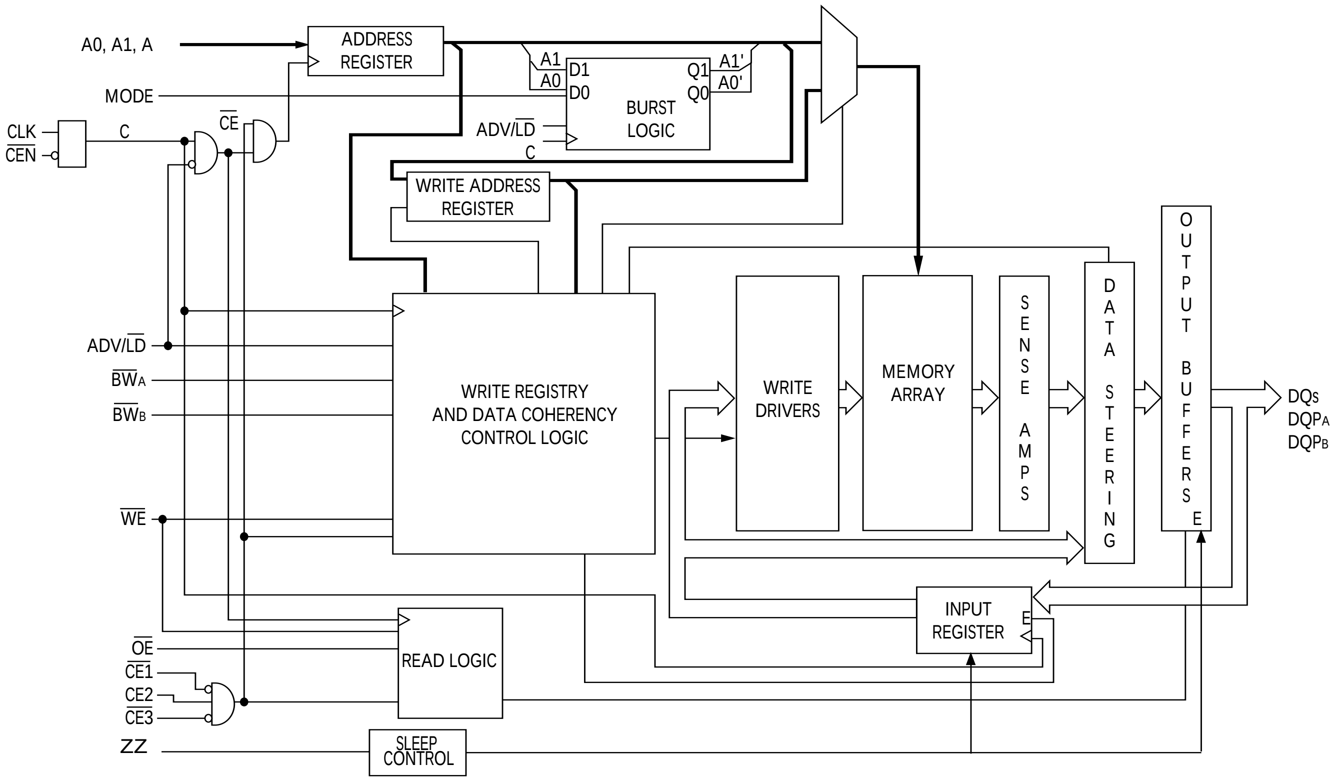
Notes:

1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Logic Block Diagram – CY7C1371DV25 (512K x 36)

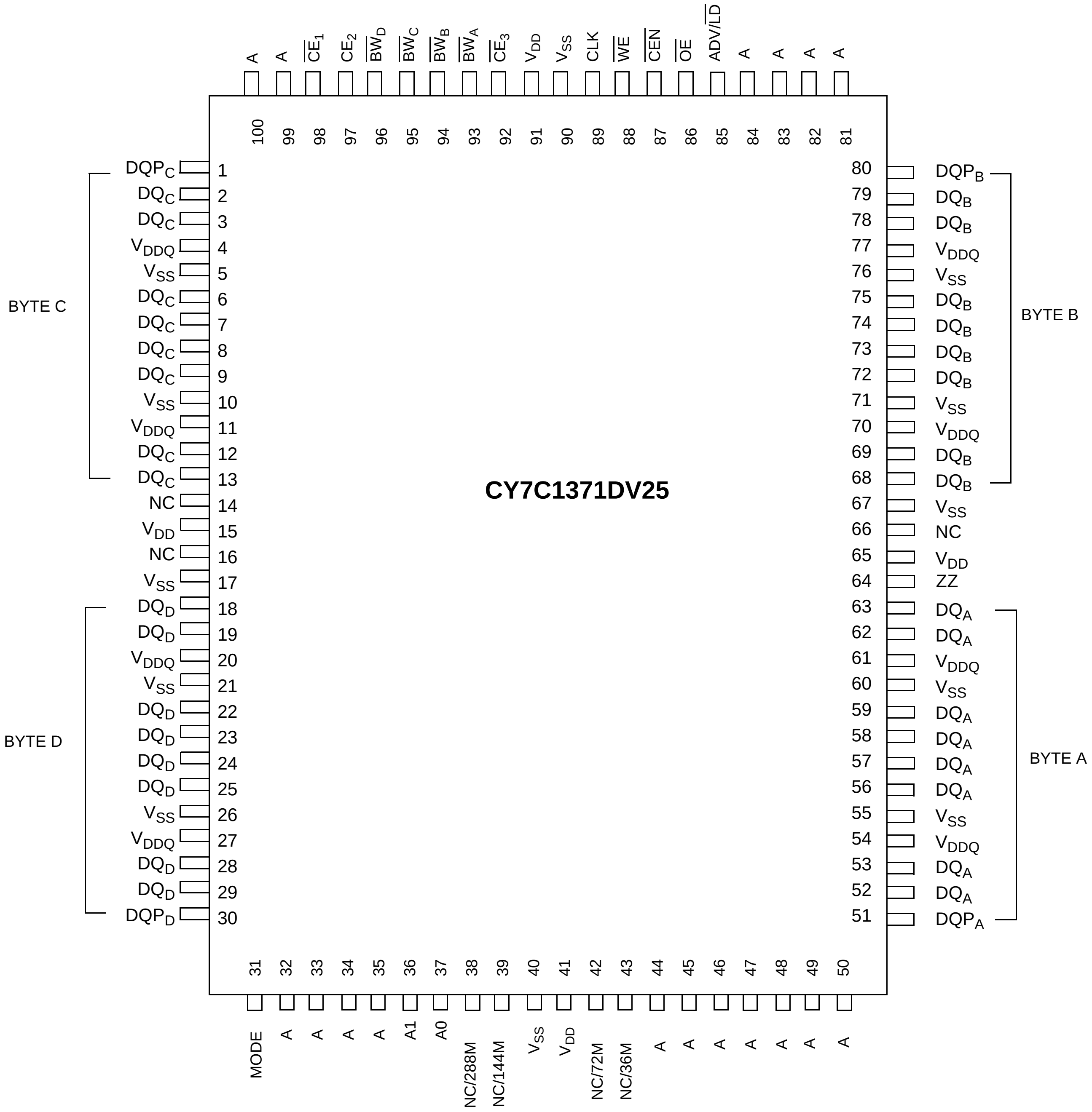


Logic Block Diagram – CY7C1373DV25 (1M x 18)



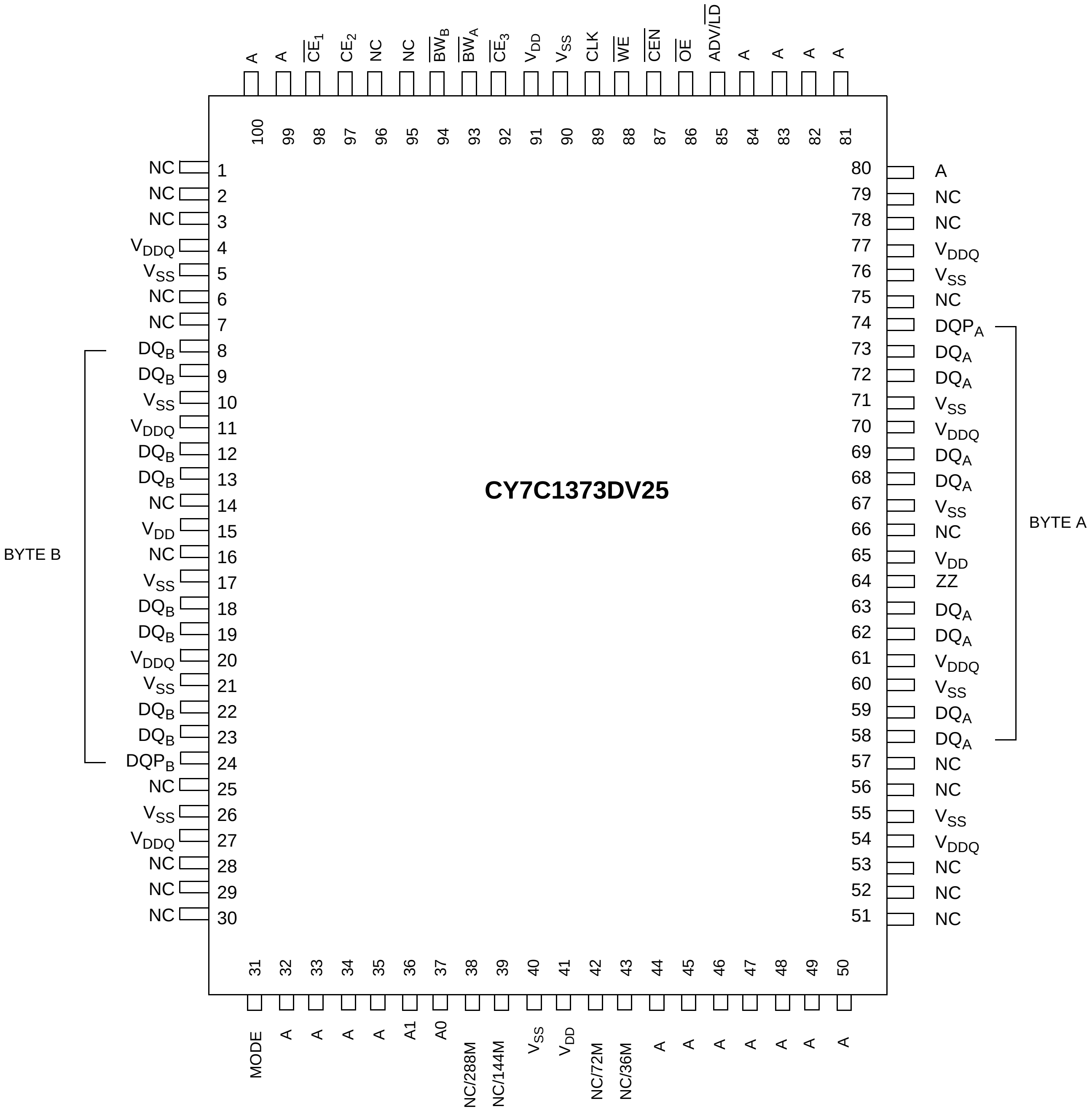
Pin Configurations

100-pin TQFP Pinout



Pin Configurations (continued)

100-Pin TQFP Pinout



Pin Configurations (continued)

119-Ball BGA Pinout

CY7C1371DV25 (512K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC/576M	CE_2	A	$ADV/\overline{LD}$	A	$\overline{CE}_3$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	A	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{WE}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1373DV25 (1M x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC/576M	CE_2	A	$ADV/\overline{LD}$	A	$\overline{CE}_3$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{BW}_B$	A	NC	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CLK	V_{SS}	NC	DQ_A
L	DQ_B	NC	NC	NC	$\overline{BW}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC/72M	A	A	NC/36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-Ball FBGA Pinout

CY7C1371DV25 (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1373DV25 (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC/1G	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input- Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_A$, $\overline{BW}_B$ $\overline{BW}_C$, $\overline{BW}_D$	Input- Synchronous	**Byte Write Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input- Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input- Synchronous	**Advance/Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input- Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input- Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2, and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input- Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input- Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input- Asynchronous	**Output Enable, asynchronous input, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	Input- Synchronous	**Clock Enable Input, active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	Input- Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ_S	I/O- Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_S and $DQP_{[A:D]}$ are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O- Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_S.
MODE	Input Strap Pin	**Mode Input. Selects the burst order of the device.** When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.

Pin Definitions (continued)

Name	I/O	Description
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V_{DD} through a pull-up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No Connects**. Not internally connected to the die. 36 Mbit, 72 Mbit, 144 Mbit, 288 Mbit, 576 Mbit and 1 Gbit are address expansion pins and are not internally connected to the die.

Functional Overview

The CY7C1371DV25/CY7C1373DV25 is a synchronous flow-through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise (t$_{CDV}$) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three Chip Enables (CE$_1$, CE$_2$, CE$_3$) active at the rising edge of the clock. If Clock Enable (CEN) is active LOW and ADV/LD is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the Write Enable (WE). BW$_X$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable (WE). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables (CE$_1$, CE$_2$, CE$_3$) and an asynchronous Output Enable (OE) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/LD should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE$_1$, CE$_2$, and CE$_3$ are ALL asserted active, (3) the Write Enable input signal WE is deasserted HIGH, and (4) ADV/LD is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided OE is active LOW. After the first clock of the read access, the output buffers are controlled by OE and the internal control logic. OE must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output will be tri-stated immediately.

Burst Read Accesses

The CY7C1371DV25/CY7C1373DV25 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/LD must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap around when incremented sufficiently. A HIGH input on ADV/LD will increment the internal burst counter regardless of the state of chip enable inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE$_1$, CE$_2$, and CE$_3$ are ALL asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address bus is loaded into the Address Register. The write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the OE input signal. This allows the external logic to present the data on DQs and DQP$_X$.

On the next clock rise the data presented to DQs and DQP$_X$ (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (Read/Write/Deselect) can be initiated on this cycle.

The data written during the Write operation is controlled by BW$_X$ signals. The CY7C1371DV25/CY7C1373DV25 provides byte write capability that is described in the truth table. Asserting the Write Enable input (WE) with the selected Byte Write Select input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1371DV25/CY7C1373DV25 is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable (OE) can be deasserted HIGH before presenting data to the DQs and DQP$_X$ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs and DQP$_X$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1371DV25/CY7C1373DV25 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/LD is driven HIGH on the subsequent clock rise, the Chip Enables (CE$_1$, CE$_2$, and CE$_3$) and WE inputs are ignored and the burst counter is incremented. The correct BW$_X$ inputs must be driven in each cycle of the burst write, in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE$_1$, CE$_2$, and CE$_3$, must remain inactive for the duration of t$_{ZZREC}$ after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		80	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$ADV/\overline{LD}$	$\overline{WE}$	$\overline{BW}_X$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Notes:

[2] X = “Don't Care.” H = Logic HIGH, L = Logic LOW. $\overline{BW}_X$ = 0 signifies at least one Byte Write Select is active, $\overline{BW}_X$ = Valid signifies that the desired byte write selects are asserted, see truth table for details.

[3] Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See truth table for Read/Write.

[4] When a write cycle is detected, all I/Os are tri-stated, even during byte writes.

[5] The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

[6] $\overline{CEN}$ = H, inserts wait states.

[7] Device will power-up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.

[8] $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = Tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{OE}$ is active.

Partial Truth Table for Read/Write[2, 3, 9]

Function (CY7C1371DV25)	$\overline{\mathrm{WE}}$	$\overline{\mathrm{BW}}_A$	$\overline{\mathrm{BW}}_B$	$\overline{\mathrm{BW}}_C$	$\overline{\mathrm{BW}}_D$
Read	H	X	X	X	X
Write No bytes written	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write Byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write Byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write Byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Partial Truth Table for Read/Write[2, 3, 9]

Function (CY7C1373DV25)	$\overline{\mathrm{WE}}$	$\overline{\mathrm{BW}}_A$	$\overline{\mathrm{BW}}_B$
Read	H	X	X
Write - No bytes written	L	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H
Write Byte B – (DQ_B and DQP_B)	L	H	L
Write All Bytes	L	L	L

Note:

9. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{\mathrm{BW}}_X$ is valid. Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

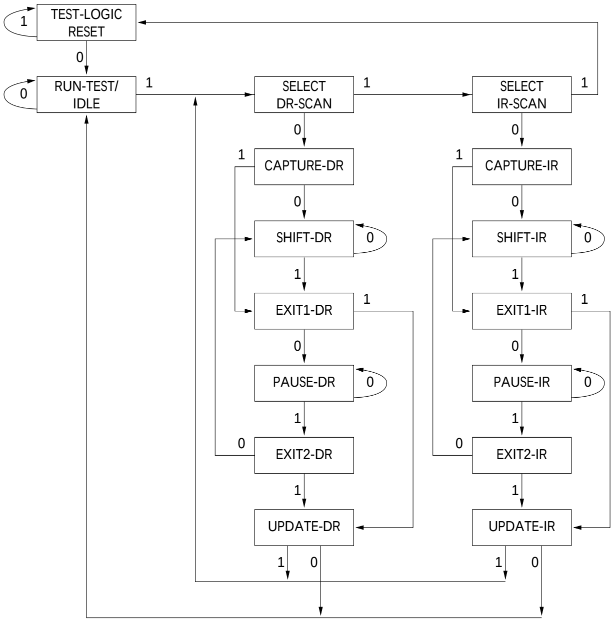
The CY7C1371DV25/CY7C1373DV25 incorporates a serial boundary scan test access port (TAP).This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels.

The CY7C1371DV25/CY7C1373DV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

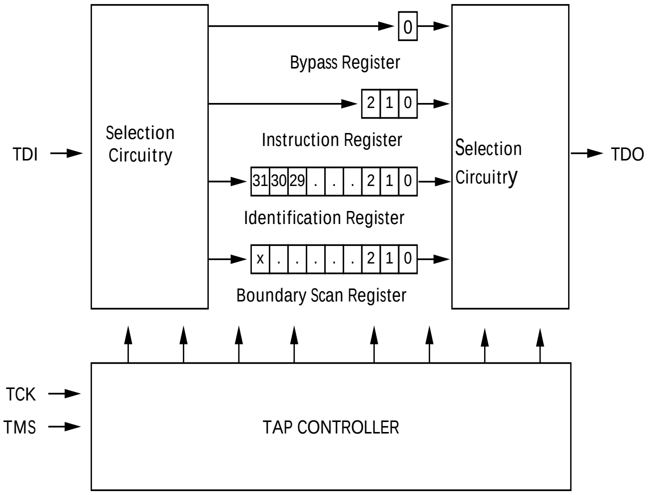
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see figure. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

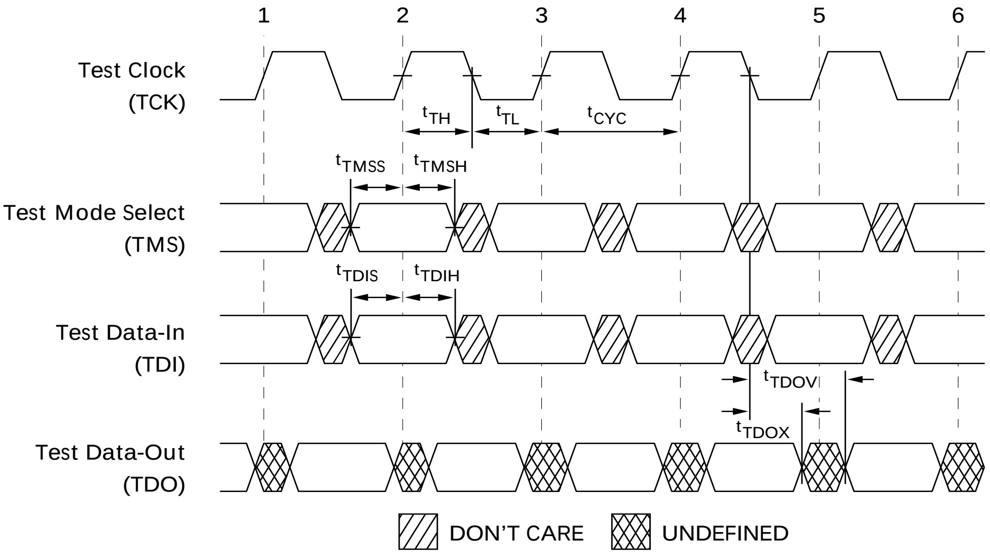
The boundary scan register has a special bit located at bit #85 (for 119-BGA package) or bit #89 (for 165-fBGA package). When this scan cell, called the “extest output bus tri-state,” is latched into the preload register during the “Update-DR” state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR,” the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics Over the Operating Range[10, 11]

Parameter	Description	Min.	Max.	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	5		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	5		ns
t_{CS}	Capture Set-up to TCK Rise	5		
Hold Times				
t_{TMSH}	TMS hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes:

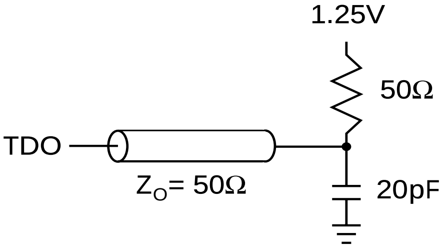
[10] t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.

[11] Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

2.5V TAP AC Test Conditions

Input pulse levels	V_{SS} to 2.5V
Input rise and fall time	1 ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V

2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < TA < +70°C; VDD = 2.5V ±0.125V unless otherwise noted)[12]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA, V_{DDQ} = 2.5V		2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA, V_{DDQ} = 2.5V			0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Identification Register Definitions

Instruction Field	CY7C1371DV25 (512Kx36)	CY7C1373DV25 (1Mx18)	Description
Revision Number (31:29)	000	000	Describes the version number
Device Depth (28:24)[13]	01011	01011	Reserved for internal use
Device Width (23:18)	001001	001001	Defines memory type and architecture
Cypress Device ID (17:12)	100101	010101	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	85	85
Boundary Scan Order (165-ball FBGA package)	89	89

Notes:

[12] All voltages referenced to V_{SS} (GND).

[13] Bit #24 is “1” in the Register Definitions for both 2.5v and 3.3v versions of this device.

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

119-Ball BGA Boundary Scan Order [14, 15]

Bit #	Ball ID
1	H4
2	T4
3	T5
4	T6
5	R5
6	L5
7	R6
8	U6
9	R7
10	T7
11	P6
12	N7
13	M6
14	L7
15	K6
16	P7
17	N6
18	L6
19	K7
20	J5
21	H6
22	G7
23	F6
24	E7
25	D7
26	H7
27	G6
28	E6
29	D6
30	C7
31	B7
32	C6
33	A6
34	C5
35	B5
36	G5
37	B6
38	D4
39	B4
40	F4
41	M4
42	A5
43	K4
44	E4
45	G4
46	A4
47	G3
48	C3
49	B2
50	B3
51	A3
52	C2
53	A2
54	B1
55	C1
56	D2
57	E1
58	F2
59	G1
60	H2
61	D1
62	E2
63	G2
64	H1
65	J3
66	2K
67	L1
68	M2
69	N1
70	P1
71	K1
72	L2
73	N2
74	P2
75	R3
76	T1
77	R1
78	T2
79	L3
80	R2
81	T3
82	L4
83	N4
84	P4
85	Internal

Notes:

[14] Balls which are NC (No Connect) are pre-set LOW.

[15] Bit# 85 is pre-set HIGH.

165-Ball BGA Boundary Scan Order [14, 16]

Bit #	Ball ID
1	N6
2	N7
3	N10
4	P11
5	P8
6	R8
7	R9
8	P9
9	P10
10	R10
11	R11
12	H11
13	N11
14	M11
15	L11
16	K11
17	J11
18	M10
19	L10
20	K10
21	J10
22	H9
23	H10
24	G11
25	F11
26	E11
27	D11
28	G10
29	F10
30	E10
31	D10
32	C11
33	A11
34	B11
35	A10
36	B10
37	A9
38	B9
39	C10
40	A8
41	B8
42	A7
43	B7
44	B6
45	A6
46	B5
47	A5
48	A4
49	B4
50	B3
51	A3
52	A2
53	B2
54	C2
55	B1
56	A1
57	C1
58	D1
59	E1
60	F1
61	G1
62	D2
63	E2
64	F2
65	G2
66	H1
67	H3
68	J1
69	K1
70	L1
71	M1
72	J2
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Note:

16. Bit# 89 is pre-set HIGH.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND........ –0.5V to +3.6V

Supply Voltage on V_{DDQ} Relative to GND ...... –0.5V to +V_{DD}

DC Voltage Applied to Outputs
in Tri-State.. –0.5V to V_{DDQ} + 0.5V

DC Input Voltage .... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage.. >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}/V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range[17, 18]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage	for 2.5V I/O		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	for 2.5V I/O, $I_{OH} = -1.0$ mA		2.0		V
V_{OL}	Output LOW Voltage	for 2.5V I/O, $I_{OL} = 1.0$ mA			0.4	V
V_{IH}	Input HIGH Voltage[17]	for 2.5V I/O		1.7	$V_{DD} + 0.3V$	V
V_{IL}	Input LOW Voltage[17]	for 2.5V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DD,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz		210	mA
			10-ns cycle, 100 MHz		175	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz		140	mA
			10-ns cycle, 100 MHz		120	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DD} – 0.3V, f = 0, inputs static	All speeds		70	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX}, inputs switching	7.5-ns cycle, 133 MHz		130	mA
			10-ns cycle, 100 MHz		110	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All Speeds		80	mA

Notes:

[17] Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).

[18] $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Capacitance[19]

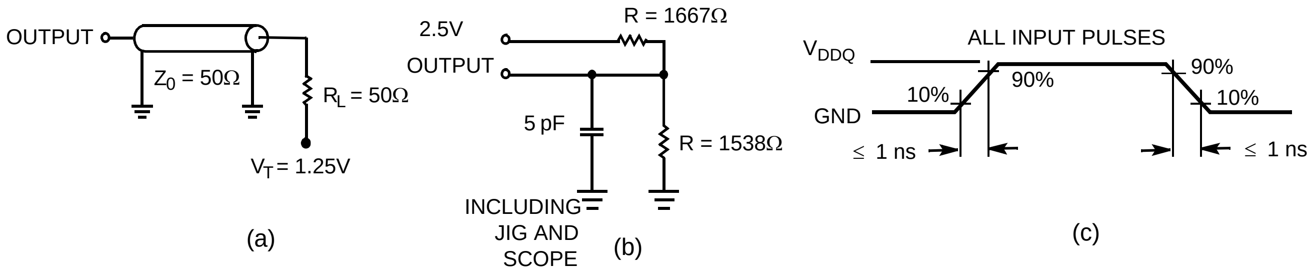
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 2.5V V_{DDQ} = 2.5V	5	8	9	pF
C_{CLK}	Clock Input Capacitance		5	8	9	pF
$C_{I/O}$	Input/Output Capacitance		5	8	9	pF

Thermal Resistance[19]

Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	28.66	23.8	20.7	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		4.08	6.2	4.0	°C/W

AC Test Loads and Waveforms

2.5V I/O Test Load



Note:

19. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics Over the Operating Range[24, 25]

Parameter	Description	133 MHz		100 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{POWER}[20]		1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	2.1		2.5		ns
t_{CL}	Clock LOW	2.1		2.5		ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise		6.5		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		ns
t_{CLZ}	Clock to Low-Z[21, 22, 23]	2.0		2.0		ns
t_{CHZ}	Clock to High-Z[21, 22, 23]		4.0		5.0	ns
t_{OEV}	$\overline{\text{OE}}$ LOW to Output Valid		3.2		3.8	ns
t_{OELZ}	$\overline{\text{OE}}$ LOW to Output Low-Z[21, 22, 23]	0		0		ns
t_{OEHZ}	$\overline{\text{OE}}$ HIGH to Output High-Z[21, 22, 23]		4.0		5.0	ns
Set-up Times						
t_{AS}	Address Set-up Before CLK Rise	1.5		1.5		ns
t_{ALS}	ADV/$\overline{\text{LD}}$ Set-up Before CLK Rise	1.5		1.5		ns
t_{WES}	$\overline{\text{WE}}$, $\overline{\text{BW}}_X$ Set-up Before CLK Rise	1.5		1.5		ns
t_{CENS}	$\overline{\text{CEN}}$ Set-up Before CLK Rise	1.5		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.5		1.5		ns
t_{CES}	Chip Enable Set-Up Before CLK Rise	1.5		1.5		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{ALH}	ADV/$\overline{\text{LD}}$ Hold After CLK Rise	0.5		0.5		ns
t_{WEH}	$\overline{\text{WE}}$, $\overline{\text{BW}}_X$ Hold After CLK Rise	0.5		0.5		ns
t_{CENH}	$\overline{\text{CEN}}$ Hold After CLK Rise	0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		ns

Notes:

[20] This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially, before a read or write operation can be initiated.

[21] t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.

[22] At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.

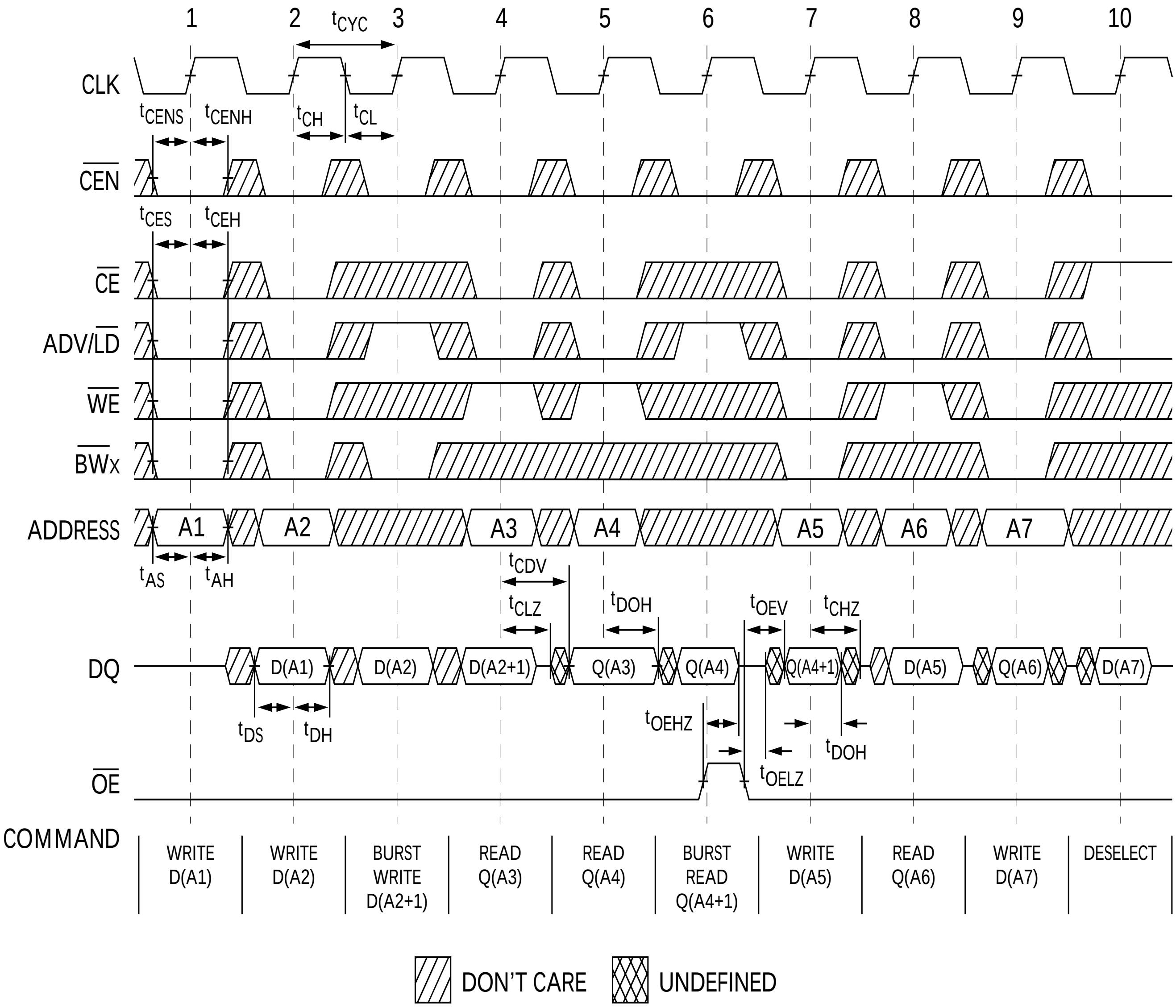
[23] This parameter is sampled and not 100% tested.

[24] Timing reference level is 1.25V when V_{DDQ} = 2.5V.

[25] Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Waveforms

Read/Write Waveforms[26, 27, 28]

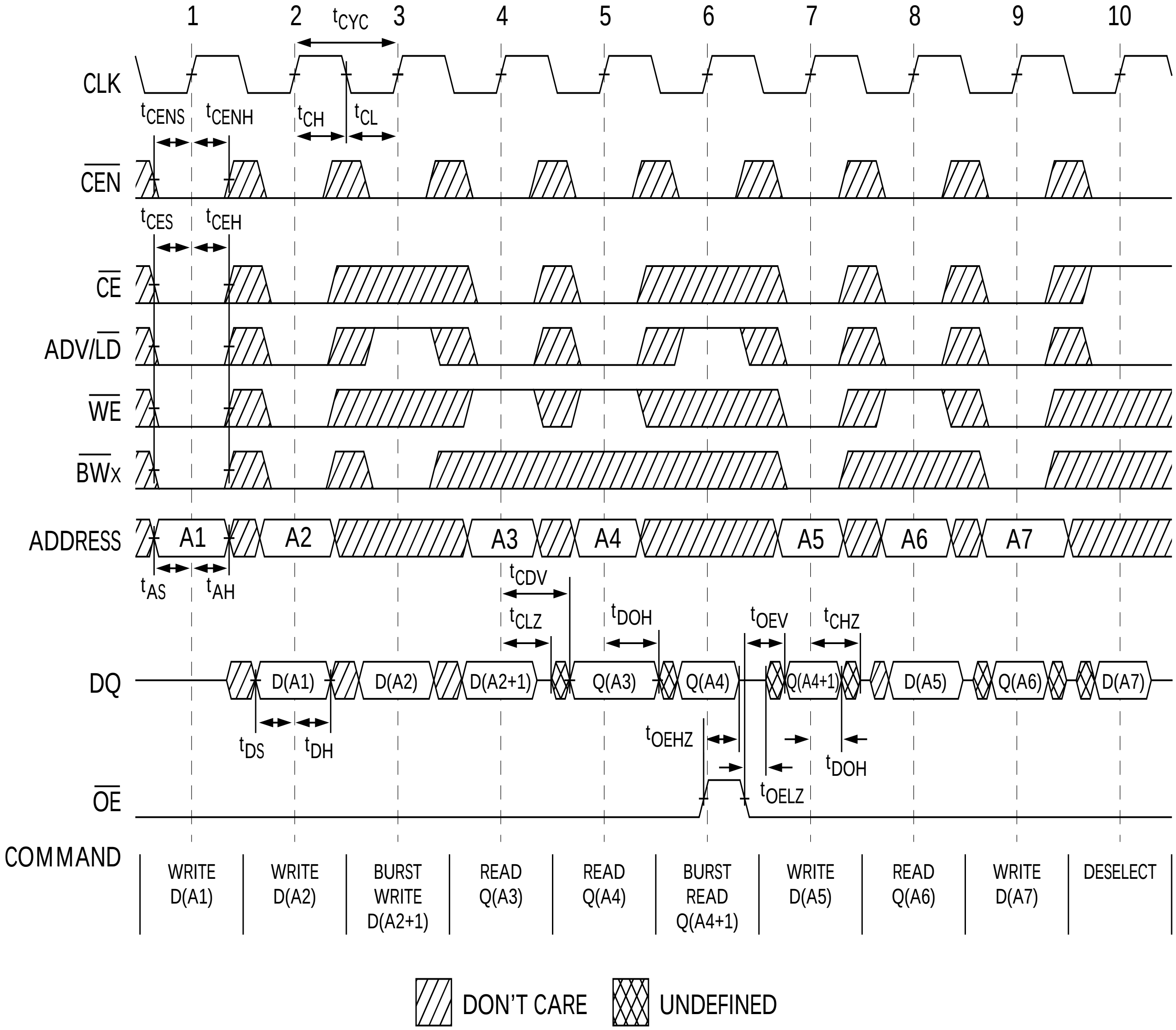


Notes:

26. For this waveform ZZ is tied LOW.
27. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
28. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

NOP, STALL AND DESELECT Cycles[26, 27, 29]

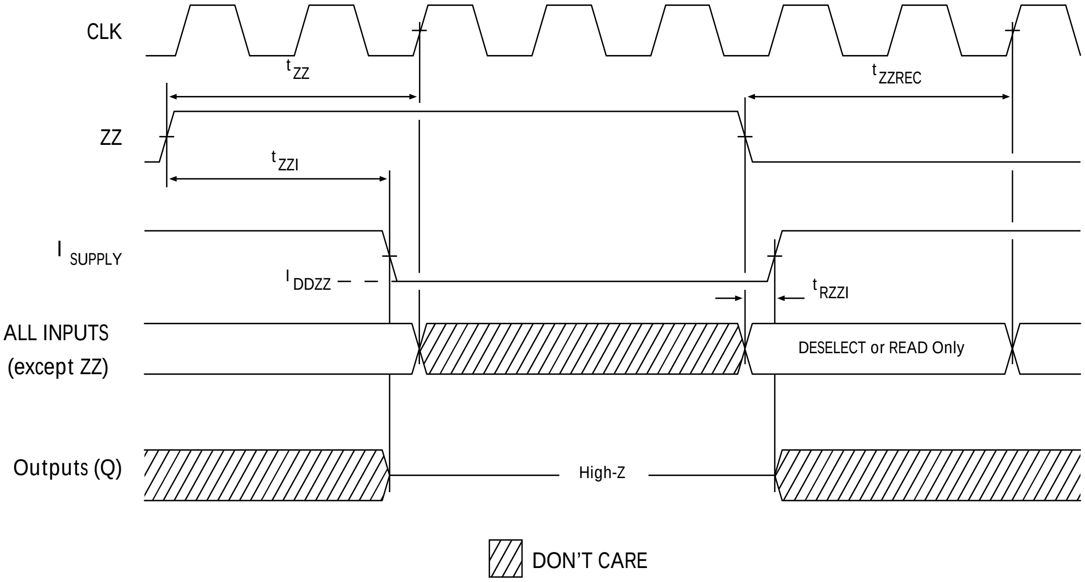


Note:

29. The Ignore Clock Edge or Stall cycle (Clock 3) illustrates $\overline{\text{CEN}}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

ZZ Mode Timing[30, 31]



Notes:

30. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
31. DQs are in high-Z when exiting ZZ sleep mode.

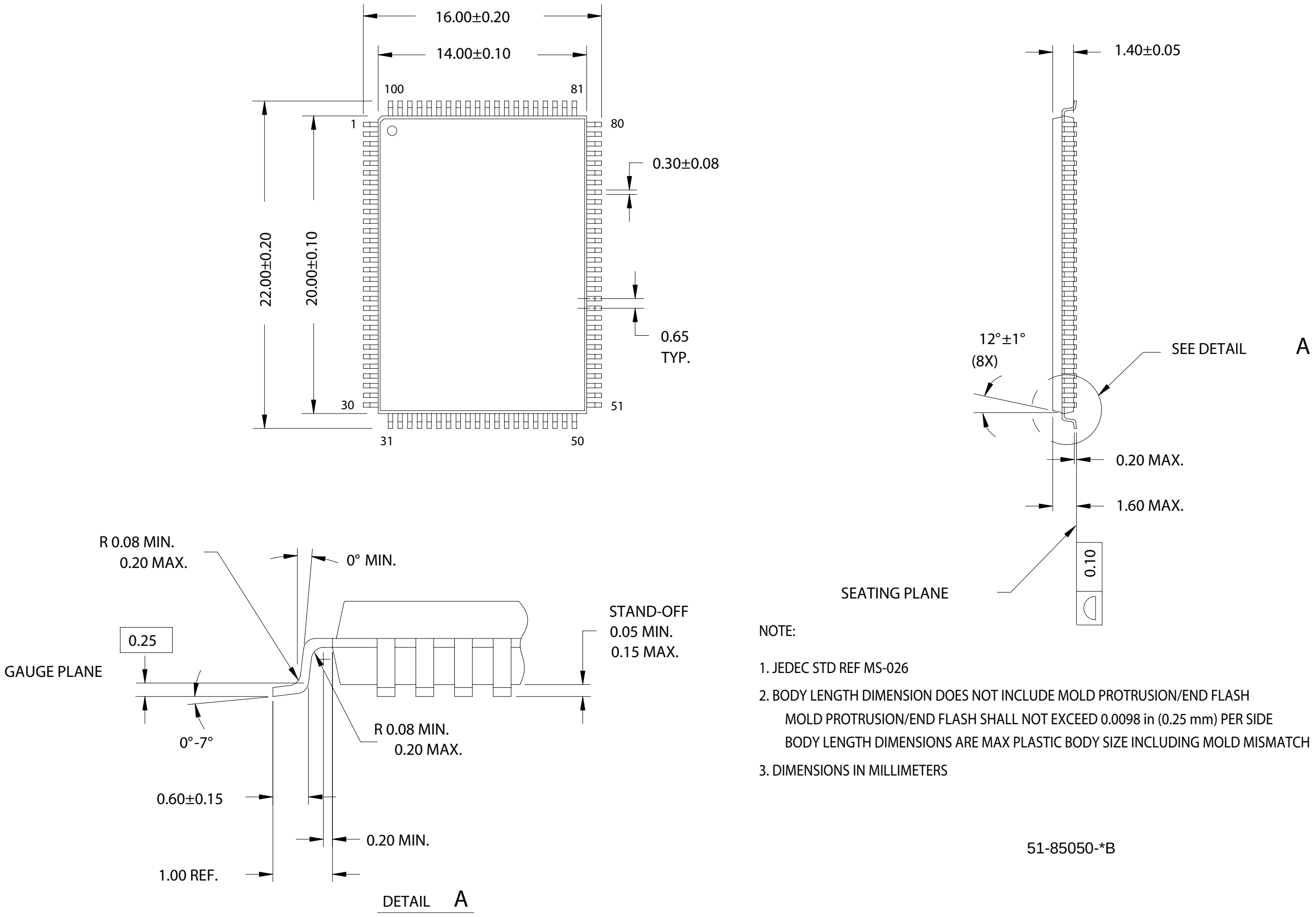
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1371DV25-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Commercial
	CY7C1373DV25-133AXC			
	CY7C1371DV25-133BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1373DV25-133BGC			
	CY7C1371DV25-133BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free	
	CY7C1373DV25-133BGXC			
	CY7C1371DV25-133BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1373DV25-133BZC			
	CY7C1371DV25-133BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	
	CY7C1373DV25-133BZXC			
	CY7C1371DV25-133AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Industrial
	CY7C1373DV25-133AXI			
	CY7C1371DV25-133BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1373DV25-133BGI			
	CY7C1371DV25-133BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free	
	CY7C1373DV25-133BGXI			
	CY7C1371DV25-133BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1373DV25-133BZI			
	CY7C1371DV25-133BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	
	CY7C1373DV25-133BZXI			
100	CY7C1371DV25-100AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Commercial
	CY7C1373DV25-100AXC			
	CY7C1371DV25-100BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1373DV25-100BGC			
	CY7C1371DV25-100BGXC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free	
	CY7C1373DV25-100BGXC			
	CY7C1371DV25-100BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1373DV25-100BZC			
	CY7C1371DV25-100BZXC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	
	CY7C1373DV25-100BZXC			
	CY7C1371DV25-100AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Industrial
	CY7C1373DV25-100AXI			
	CY7C1371DV25-100BGI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1373DV25-100BGI			
	CY7C1371DV25-100BGXI	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm) Lead-Free	
	CY7C1373DV25-100BGXI			
	CY7C1371DV25-100BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1373DV25-100BZI			
	CY7C1371DV25-100BZXI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm) Lead-Free	
	CY7C1373DV25-100BZXI			

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) (51-85050)



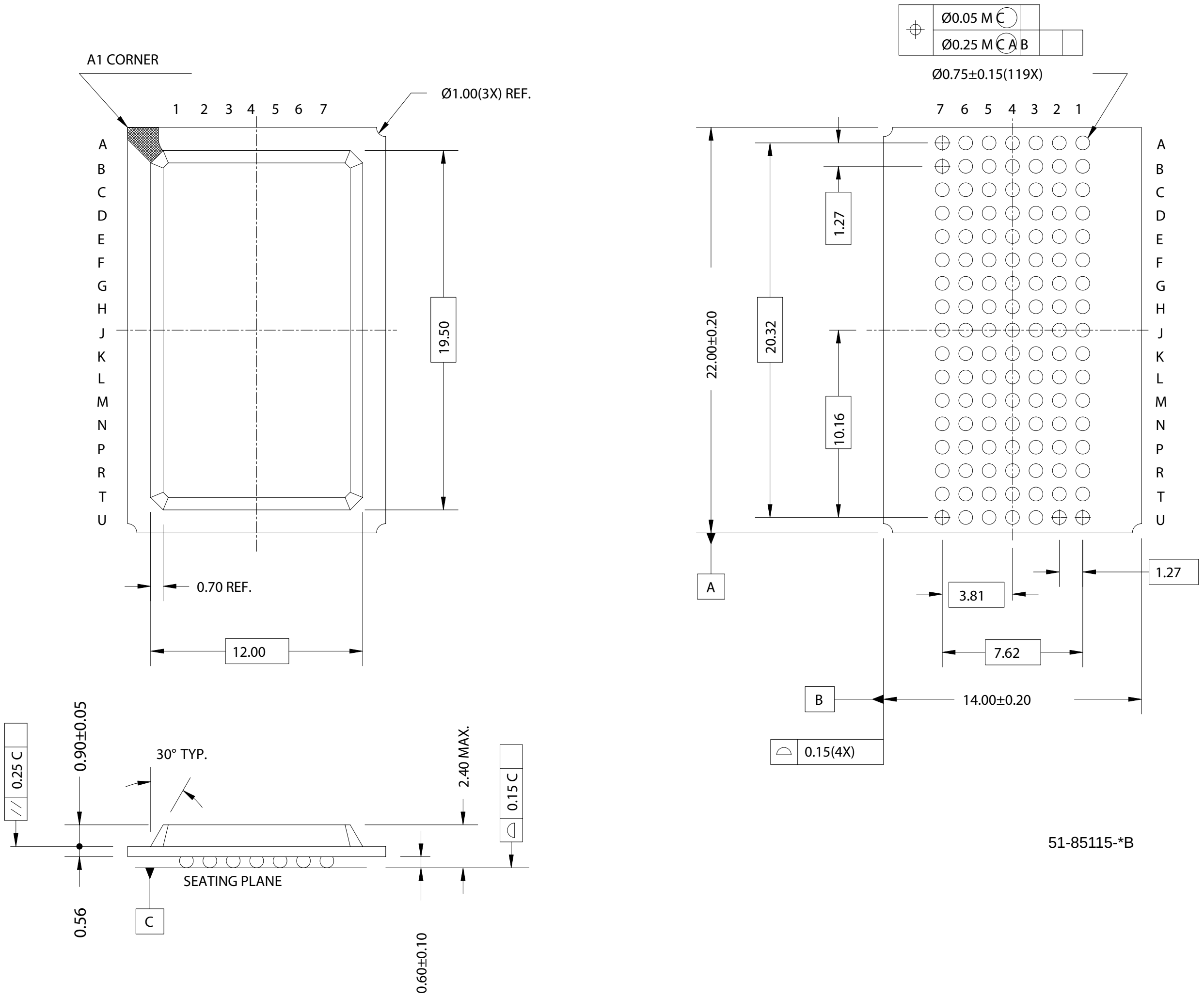
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

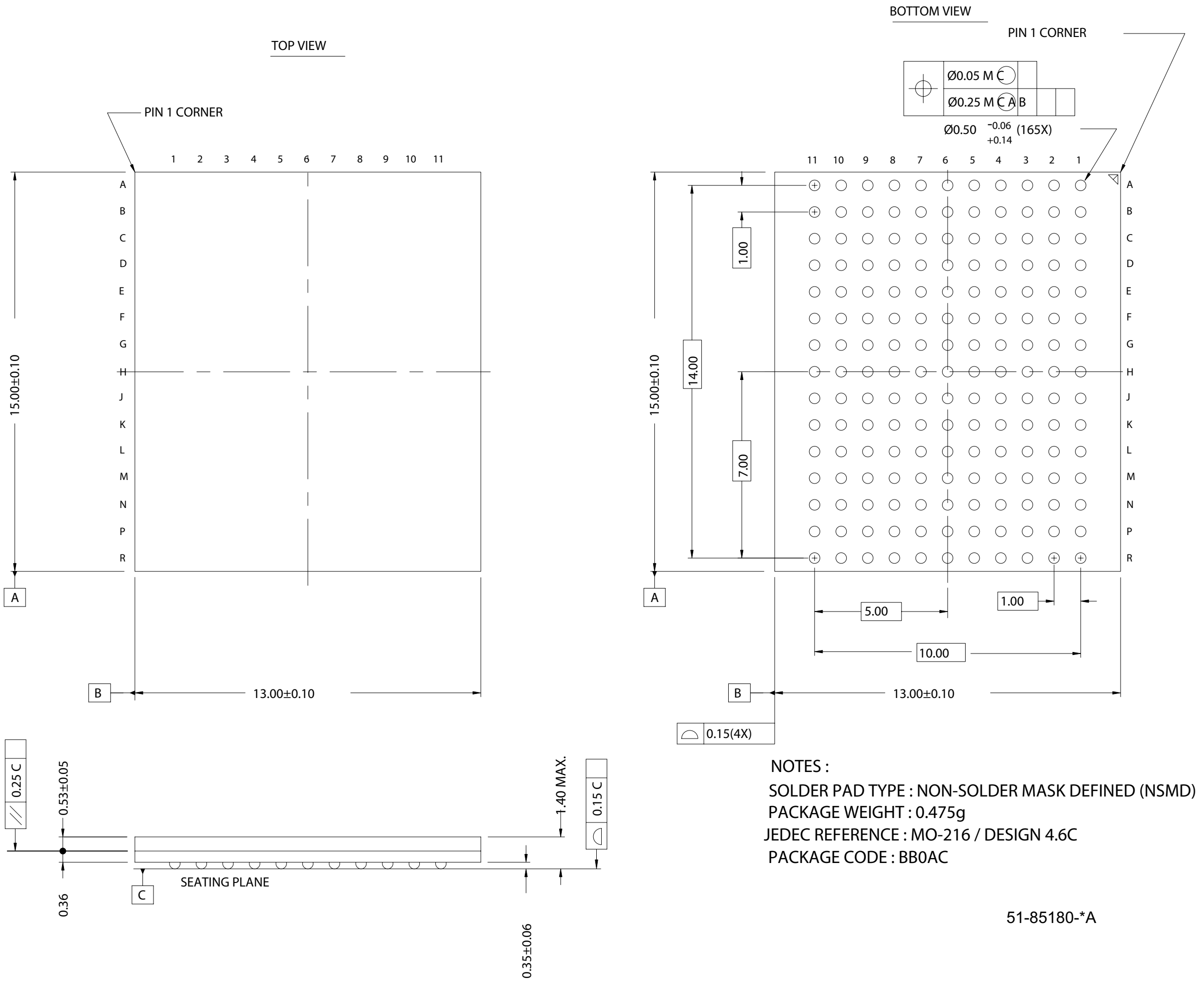
Package Diagrams (continued)

119-Ball BGA (14 x 22 x 2.4 mm) (51-85115)



Package Diagrams (continued)

165-Ball FBGA (13 x 15 x 1.4 mm) (51-85180)



NOTES :

SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)
PACKAGE WEIGHT : 0.475g
JEDEC REFERENCE : MO-216 / DESIGN 4.6C
PACKAGE CODE : BB0AC

51-85180-*A

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Document History Page

Document Title: CY7C1371DV25/CY7C1373DV25 18-Mbit (512K x 36/1M x 18) Flow-Through SRAM with NoBL™ Architecture
Document Number: 38-05557

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	254513	See ECN	RKF	New data sheet
*A	288531	See ECN	SYT	Edited description under “IEEE 1149.1 Serial Boundary Scan (JTAG)” for non-compliance with 1149.1 Removed 117 Mhz Speed Bin Added lead-free information for 100-Pin TQFP, 119 BGA and 165 FBGA package Added comment of ‘Lead-free BG packages availability’ below the Ordering Information
*B	326078	See ECN	PCI	Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added description on EXTEST Output Bus Tri-State Changed description on the Tap Instruction Set Overview and Extest Changed Θ_{JA} and Θ_{JC} for TQFP Package from 31 and 6 °C/W to 28.66 and 4.08 °C/W respectively Changed Θ_{JA} and Θ_{JC} for BGA Package from 45 and 7 °C/W to 23.8 and 6.2 °C/W respectively Changed Θ_{JA} and Θ_{JC} for FBGA Package from 46 and 3 °C/W to 20.7 and 4.0 °C/W respectively Modified $V_{OL,}$ V_{OH} test conditions Removed comment of ‘Lead-free BG packages availability’ below the Ordering Information Updated Ordering Information Table
*C	416321	See ECN	NXR	Converted From Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Corrected typo in Partial Truth Table for Read/Write of CY7C1373DV25 on page #11 Changed the description of I_X from Input Load Current to Input Leakage Current on page# 20 Changed the Ix current values of MODE on page # 20 from -5 μA and 30 μA to -30 μA and 5 μA Changed the Ix current values of ZZ on page # 20 from -30 μA and 5 μA to -5 μA and 30 μA Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$on page # 20 Replaced Package Name column with Package Diagram in the Ordering Information table Updated Ordering Information Table
*D	475677	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND. Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.