CY7C1441AV25
CY7C1447AV25

36-Mbit (1M × 36/512K × 72) Flow-Through SRAM

Features

- Supports 133 MHz bus operations
- 1M × 36/512K × 72 common I/O
- 2.5 V core power supply
- 2.5 V I/O power supply
- Fast clock-to-output times
  - 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed write
- Asynchronous output enable
- CY7C1441AV25 available in Pb-free 165-ball FBGA package. CY7C1447AV25 available in non Pb-free 209-ball FBGA package.
- JTAG boundary scan for FBGA package
- ZZ sleep mode option

Functional Description

The CY7C1441AV25/CY7C1447AV25 are 2.5 V, 1M × 36/512K × 72 Synchronous Flow-Through SRAMs, designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable ($\overline{CE_1}$), depth expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables ($\overline{BW_x}$ and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1441AV25/CY7C1447AV25 allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence and a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the Address Advancement ($\overline{ADV}$) input.

Addresses and chip enables are registered at rising edge of clock when either $\overline{ADSP}$ or $\overline{ADSC}$ are active. Subsequent burst addresses can be internally generated as controlled by the $\overline{ADV}$.

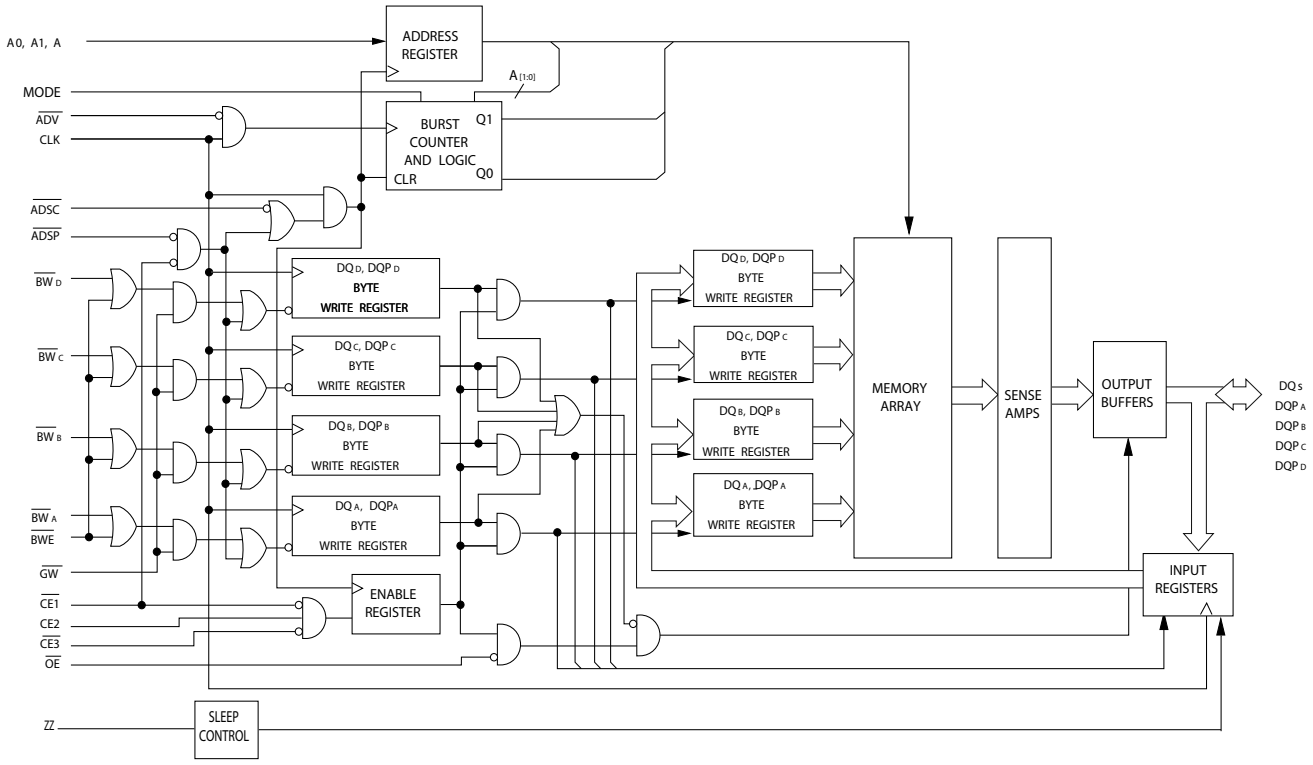
The CY7C1441AV25/CY7C1447AV25 operates from a +2.5 V core power supply while all outputs may operate with either a +2.5 V supply. All inputs and outputs are JEDEC-standard JESD8-5 compatible.

For a complete list of related documentation, click here.

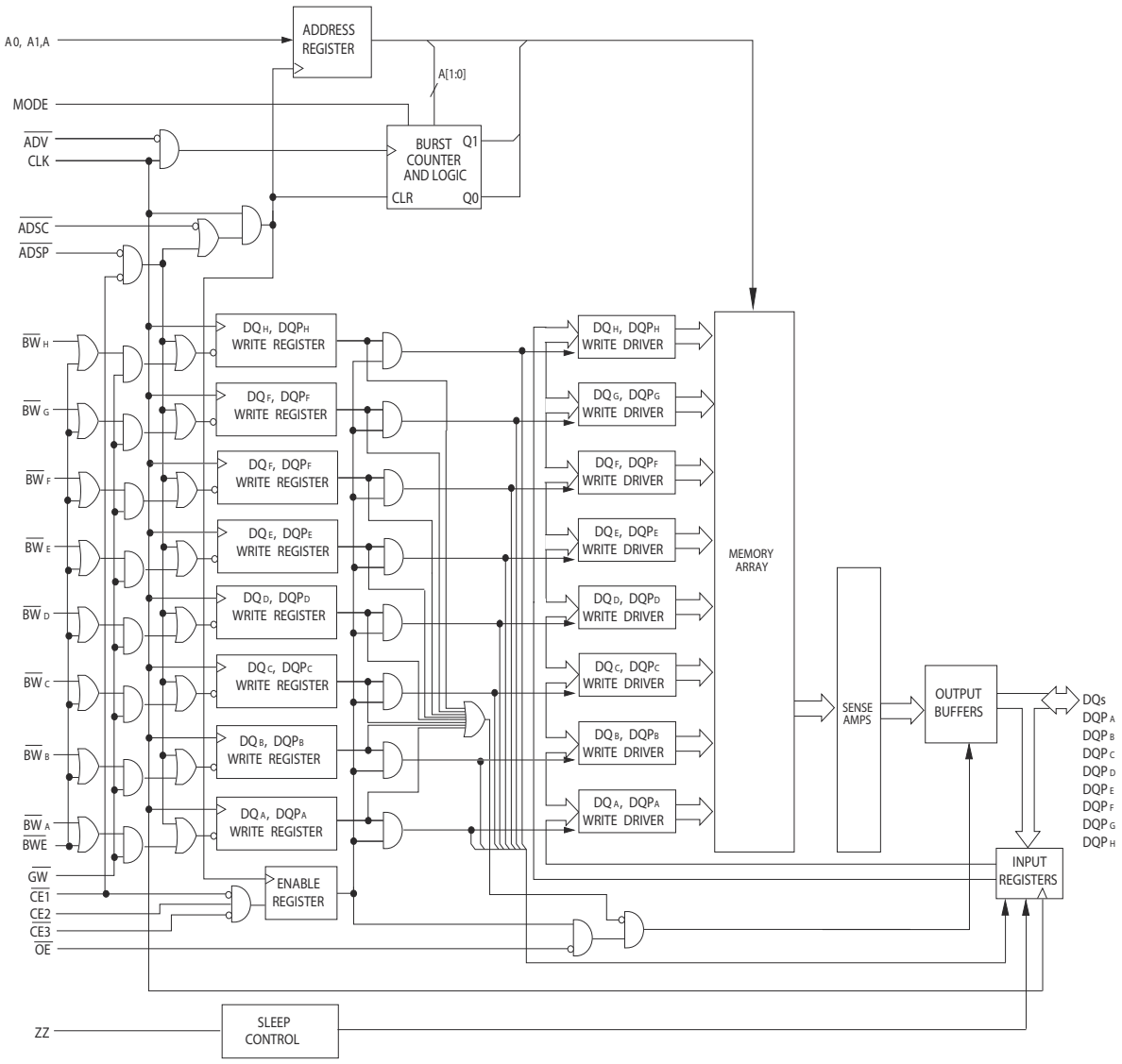
Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	270	mA
Maximum CMOS Standby Current	120	mA

Logic Block Diagram – CY7C1441AV25



Logic Block Diagram – CY7C1447AV25



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Pin Configurations

Figure 1. 165-ball FBGA (15 × 17 × 1.4 mm) pinout

CY7C1441AV25 (1M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Configurations (continued)

Figure 2. 209-ball FBGA (14 × 22 × 1.76 mm) pinout

CY7C1447AV25 (512K × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQ_G	DQ_G	A	CE_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{CE}_3$	A	DQ_B	DQ_B
B	DQ_G	DQ_G	$\overline{BWS}_C$	$\overline{BWS}_G$	NC/288M	$\overline{BW}$	A	$\overline{BWS}_B$	$\overline{BWS}_F$	DQ_B	DQ_B
C	DQ_G	DQ_G	$\overline{BWS}_H$	$\overline{BWS}_D$	NC/144M	$\overline{CE}_1$	NC/576M	$\overline{BWS}_E$	$\overline{BWS}_A$	DQ_B	DQ_B
D	DQ_G	DQ_G	V_{SS}	NC	NC/1G	$\overline{OE}$	$\overline{GW}$	NC	V_{SS}	DQ_B	DQ_B
E	DQP_G	DQP_C	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_F	DQP_B
F	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
G	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
H	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
J	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
K	NC	NC	CLK	NC	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	NC
L	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
M	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
N	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
P	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
R	DQP_D	DQP_H	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_A	DQP_E
T	DQ_D	DQ_D	V_{SS}	NC	NC	MODE	NC	NC	V_{SS}	DQ_E	DQ_E
U	DQ_D	DQ_D	NC/72M	A	A	A	A	A	A	DQ_E	DQ_E
V	DQ_D	DQ_D	A	A	A	A1	A	A	A	DQ_E	DQ_E
W	DQ_D	DQ_D	TMS	TDI	A	A0	A	TDO	TCK	DQ_E	DQ_E

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs.** Used to select one of the address locations. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$, $\overline{BW}_E$, $\overline{BW}_F$, $\overline{BW}_G$, $\overline{BW}_H$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input Signal.** Sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor.** Sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller.** Sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	**ZZ Sleep Input, Active HIGH**. When asserted HIGH places the device in a non time-critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQs	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQPX are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_x is controlled by $\overline{BW}_X$ correspondingly.
MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull up.

Pin Definitions (continued)

Name	I/O	Description
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for I/O Circuitry**.
V_{SS}	Ground	**Ground for the Core of the Device**.
V_{SSQ}	I/O Ground	**Ground for I/O Circuitry**.
TDO	JTAG Serial Output Synchronous	**Serial Data-Out to the JTAG Circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not utilized, this pin should be left unconnected.
TDI	JTAG Serial Input Synchronous	**Serial Data-In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not utilized, this pin can be left floating or connected to V_{DD} through a pull up resistor.
TMS	JTAG Serial Input Synchronous	**Serial Data-In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not utilized, this pin can be disconnected or connected to V_{DD}.
TCK	JTAG-Clock	**Clock Input to the JTAG Circuitry**. If the JTAG feature is not utilized, this pin must be connected to V_{SS}.
NC	–	**No Connects**. Not internally connected to the die.
NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No Connects**. Not internally connected to the die. NC/72M, NC/144M, NC/288M, NC/576M, and NC/1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1441AV25/CY7C1447AV25 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either ADSP or ADSC. Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW_X}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter or control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data is available as the data outputs a maximum to t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) are ignored during this first clock cycle. If the write inputs are asserted active (see Truth Table on page 10 for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. All I/Os are tri-stated during a byte write. Because this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated when a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted

HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter or control logic and delivered to the memory core. The information presented to DQ_S is written into the specified address location. Byte writes are allowed. All I/Os are tri-stated when a write is detected, even a byte write. Because this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated when a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1441AV25/CY7C1447AV25 provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. When in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2$ V	–	100	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1441AV25/CY7C1447AV25 follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	X	X	X	L	H	L	X	X	X	L–H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
1. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more Byte Write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1441AV25 follows. [6, 7]

Function (CY7C1441AV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ_A, DQP_A)	H	L	H	H	H	L
Write Byte B(DQ_B, DQP_B)	H	L	H	H	L	H
Write Bytes A, B (DQ_A, DQ_B, DQP_A, DQP_B)	H	L	H	H	L	L
Write Byte C (DQ_C, DQP_C)	H	L	H	L	H	H
Write Bytes C, A (DQ_C, DQ_A, DQP_C, DQP_A)	H	L	H	L	H	L
Write Bytes C, B (DQ_C, DQ_B, DQP_C, DQP_B)	H	L	H	L	L	H
Write Bytes C, B, A (DQ_C, DQ_B, DQ_A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write Byte D (DQ_D, DQP_D)	H	L	L	H	H	H
Write Bytes D, A (DQ_D, DQ_A, DQP_D, DQP_A)	H	L	L	H	H	L
Write Bytes D, B (DQ_D, DQ_A, DQP_D, DQP_A)	H	L	L	H	L	H
Write Bytes D, B, A (DQ_D, DQ_B, DQ_A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write Bytes D, B (DQ_D, DQ_B, DQP_D, DQP_B)	H	L	L	L	H	H
Write Bytes D, B, A (DQ_D, DQ_C, DQ_A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write Bytes D, C, A (DQ_D, DQ_B, DQ_A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1447AV25 follows. [6, 8]

Function (CY7C1447AV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_x}$
Read	H	H	X
Read	H	L	All $\overline{BW}$ = H
Write Byte x – (DQ_x and DQP_x)	H	L	L
Write All Bytes	H	L	All $\overline{BW}$ = L
Write All Bytes	L	X	X

Notes
6. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
7. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write is done based on which byte write is active.
8. $\overline{BW}$x represents any byte write signal $\overline{BW_X}$.To enable any byte write $\overline{BW_X}$, a logic LOW signal should be applied at clock rise. Any number of bye writes can be enabled at the same time for any given write.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1441AV25/CY7C1447AV25 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 2.5 V I/O logic level.

The CY7C1441AV25/CY7C1447AV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. On power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This ball can be left unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Tap Controller State Diagram on page 14. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data out from the registers. The output is active depending on the current state of the TAP state machine (see Identification Codes on page 18). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram on page 15. On power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to allow fault isolation of the board level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that is placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state. It is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions are used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 18.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register.All combinations are listed in the Identification Codes on page 18. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute

the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register on power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

When the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

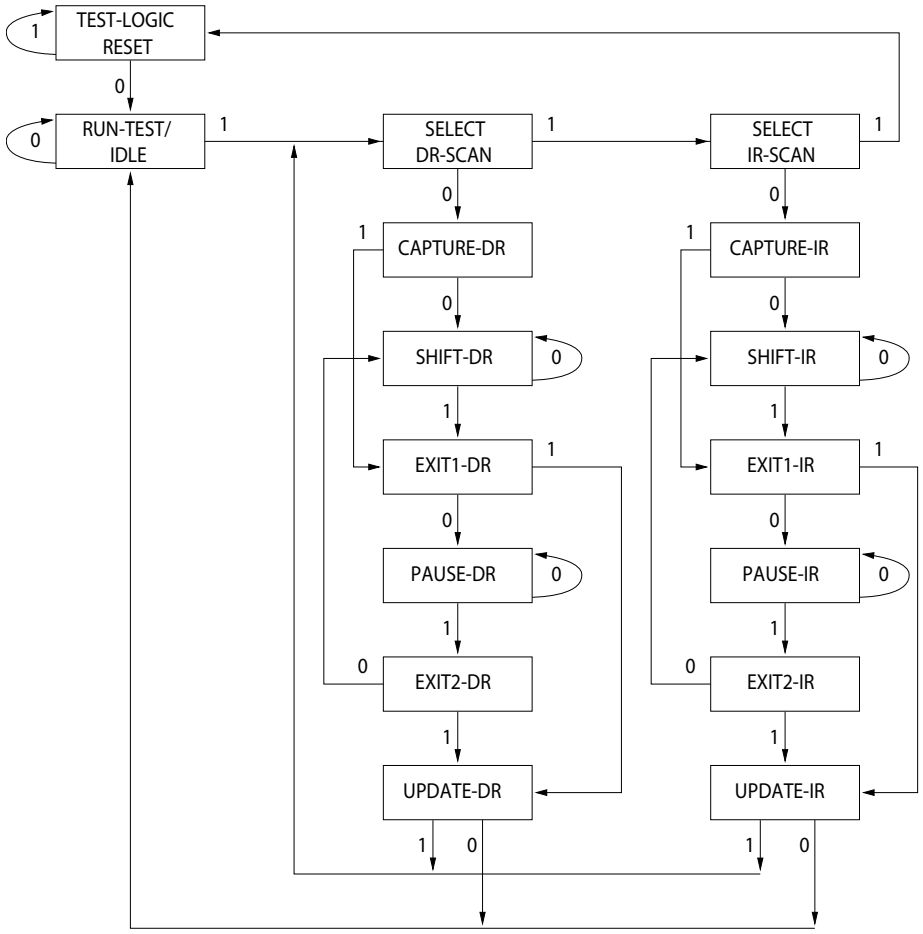
The boundary scan register has a special bit located at bit #138 (for 209-ball FBGA package). When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

This bit can be set by entering the SAMPLE/PRELOAD, or EXTEST command and then shifting the desired bit into that cell during the Shift-DR state. During Update-DR, the value loaded into that shift register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up and also when the TAP controller is in the Test-Logic-Reset” state.

Reserved

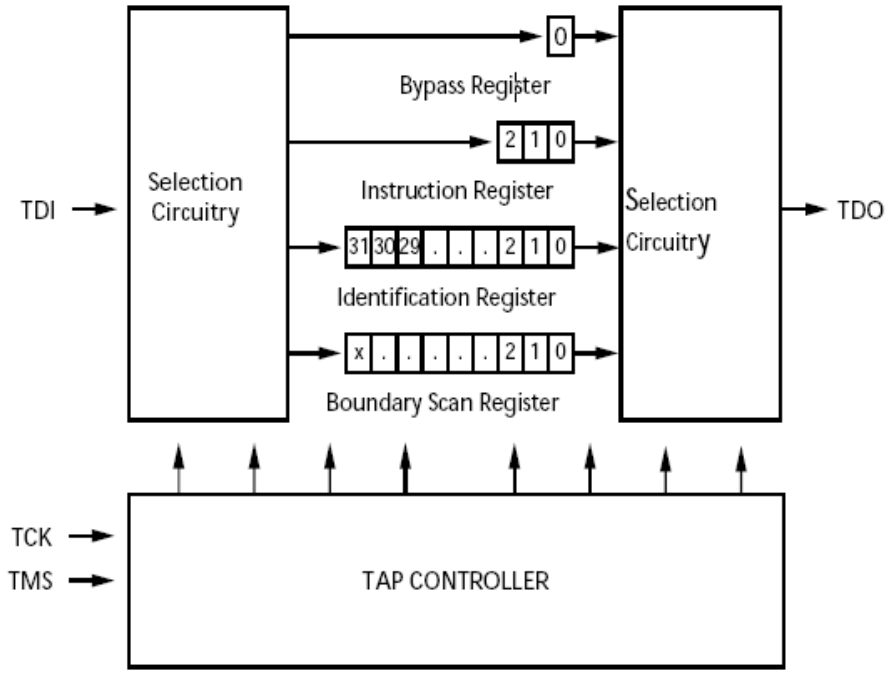
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



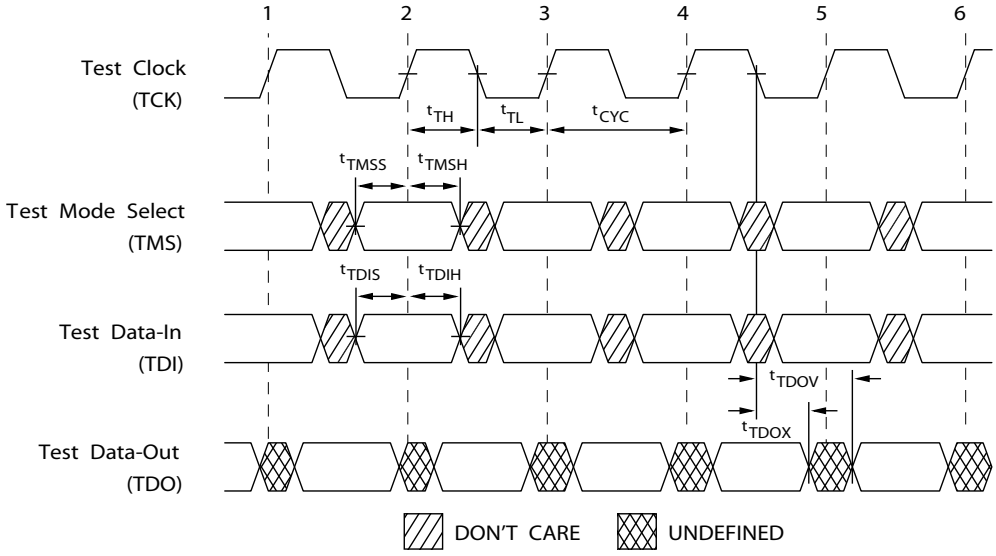
The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing

Figure 3. TAP Timing



TAP AC Switching Characteristics

Over the Operating Range

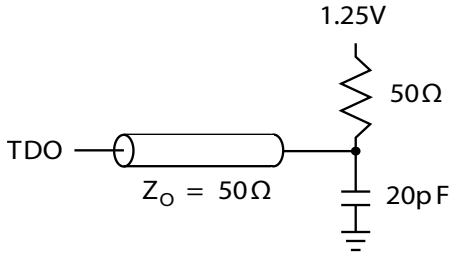
Parameter [9, 10]	Parameter	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH time	20	–	ns
t_{TL}	TCK Clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture SetUp to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

Notes
9. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
10. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

2.5 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 2.5 V ± 0.125 V unless otherwise noted)

Parameter [11]	Description	Description	Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{DDQ} = 2.5 V	2.0	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 1.0 mA	V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
11. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	Bit Configuration CY7C1441AV25 (1M × 36)	Bit Configuration CY7C1447AV25 (512K × 72)	Description
Revision Number (31:29)	000	000	Describes the version number.
Device Depth (28:24)	01011	01011	Reserved for internal use.
Architecture and Memory Type (23:18)	000001	000001	Defines memory type and architecture.
Bus Width and Density (17:12)	100111	110111	Defines width and density.
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)	Bit Size (× 72)
Instruction Bypass	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (165-ball FBGA package)	89	–
Boundary Scan Order (209-ball FBGA package)	–	138

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Boundary Scan Order

165-ball FBGA [12, 13]

CY7C1441AV25 (1M × 36)

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	N6	26	E11	51	A3	76	N1
2	N7	27	D11	52	A2	77	N2
3	N10	28	G10	53	B2	78	P1
4	P11	29	F10	54	C2	79	R1
5	P8	30	E10	55	B1	80	R2
6	R8	31	D10	56	A1	81	P3
7	R9	32	C11	57	C1	82	R3
8	P9	33	A11	58	D1	83	P2
9	P10	34	B11	59	E1	84	R4
10	R10	35	A10	60	F1	85	P4
11	R11	36	B10	61	G1	86	N5
12	H11	37	A9	62	D2	87	P6
13	N11	38	B9	63	E2	88	R6
14	M11	39	C10	64	F2	89	Internal
15	L11	40	A8	65	G2		
16	K11	41	B8	66	H1		
17	J11	42	A7	67	H3		
18	M10	43	B7	68	J1		
19	L10	44	B6	69	K1		
20	K10	45	A6	70	L1		
21	J10	46	B5	71	M1		
22	H9	47	A5	72	J2		
23	H10	48	A4	73	K2		
24	G11	49	B4	74	L2		
25	F11	50	B3	75	M2		

Notes
12. Balls which are NC (No Connect) are preset LOW.
13. Bit# 89 is preset HIGH.

Boundary Scan Order

209-ball FBGA [14, 15]

CY7C1447AV25 (512K × 72)

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	W6	36	F6	71	H6	106	K3
2	V6	37	K8	72	C6	107	K4
3	U6	38	K9	73	B6	108	K6
4	W7	39	K10	74	A6	109	K2
5	V7	40	J11	75	A5	110	L2
6	U7	41	J10	76	B5	111	L1
7	T7	42	H11	77	C5	112	M2
8	V8	43	H10	78	D5	113	M1
9	U8	44	G11	79	D4	114	N2
10	T8	45	G10	80	C4	115	N1
11	V9	46	F11	81	A4	116	P2
12	U9	47	F10	82	B4	117	P1
13	P6	48	E10	83	C3	118	R2
14	W11	49	E11	84	B3	119	R1
15	W10	50	D11	85	A3	120	T2
16	V11	51	D10	86	A2	121	T1
17	V10	52	C11	87	A1	122	U2
18	U11	53	C10	88	B2	123	U1
19	U10	54	B11	89	B1	124	V2
20	T11	55	B10	90	C2	125	V1
21	T10	56	A11	91	C1	126	W2
22	R11	57	A10	92	D2	127	W1
23	R10	58	C9	93	D1	128	T6
24	P11	59	B9	94	E1	129	U3
25	P10	60	A9	95	E2	130	V3
26	N11	61	D7	96	F2	131	T4
27	N10	62	C8	97	F1	132	T5
28	M11	63	B8	98	G1	133	U4
29	M10	64	A8	99	G2	134	V4
30	L11	65	D8	100	H2	135	5W
31	L10	66	C7	101	H1	136	5V
32	K11	67	B7	102	J2	137	5U
33	M6	68	A7	103	J1	138	Internal
34	L6	69	D6	104	K1		
35	J6	70	G6	105	N6		

Notes
14. Balls which are NC (No Connect) are preset LOW.
15. Bit# 138 is preset HIGH.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.3 V to +3.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.3 V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	2.5 V ± 5%	1.7 V to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [16, 17]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage	for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [16]	for 2.5 V I/O		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage [16]	for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5 ns cycle, 133 MHz	–	270	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, Inputs Switching	7.5 ns cycle, 133 MHz	–	150	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, Inputs Static	7.5 ns cycle, 133 MHz	–	120	mA
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{DDQ} – 0.3 V or V_{IN} ≤ 0.3 V, f = f_{MAX}, Inputs Switching	7.5 ns cycle, 133 MHz	–	150	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, Inputs Static	7.5 ns cycle, 133 MHz	–	135	mA

Notes
16. Overshoot: $V_{IH(AC)}$ < V_{DD} +1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
17. $T_{Power-up}$: Assumes a linear ramp from V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

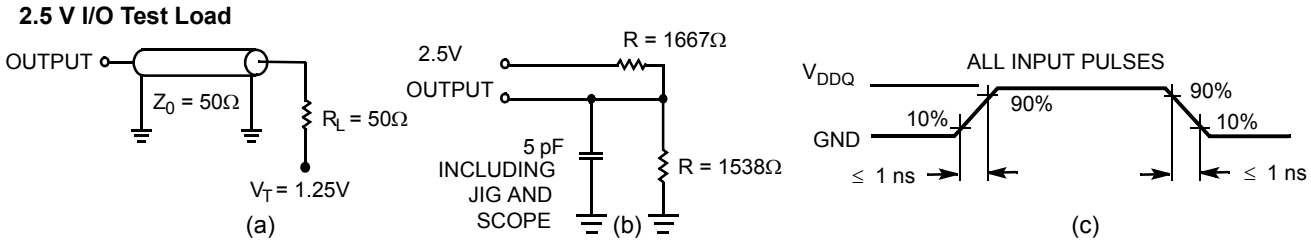
Parameter [18]	Description	Test Conditions	165-ball FBGA Max	209-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 2.5 V, V_{DDQ} = 2.5 V	7	5	pF
C_{CLK}	Clock input capacitance		7	5	pF
$C_{I/O}$	Input/Output capacitance		6	7	pF

Thermal Resistance

Parameter [18]	Description	Test Conditions	165-ball FBGA Package	209-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	20.8	25.31	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.2	4.48	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Note
18. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

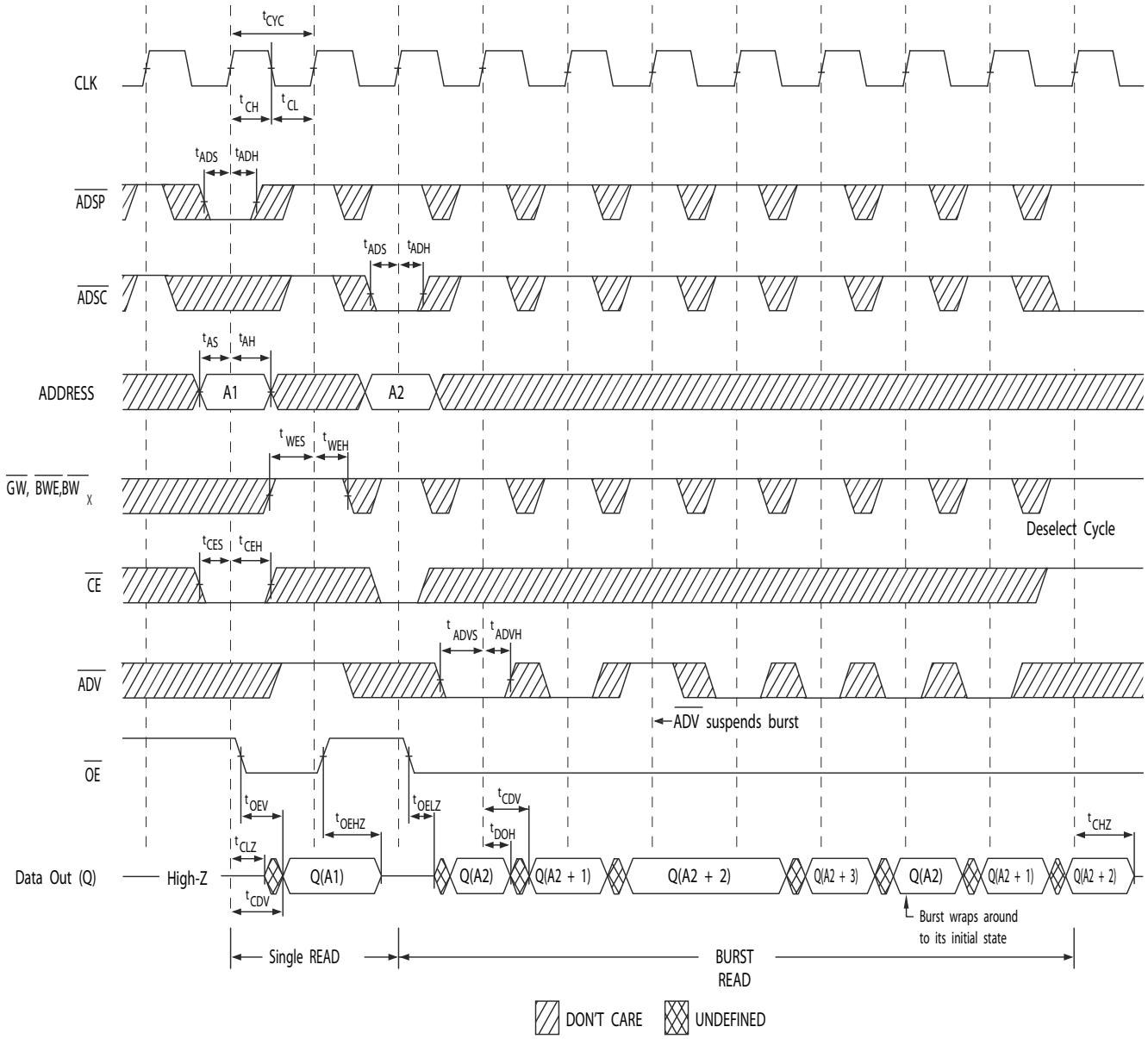
Over the Operating Range

Parameter [19, 20]	Description	-133		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [21]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
t_{CL}	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data output valid after CLK rise	–	6.5	ns
t_{DOH}	Data output hold after CLK rise	2.5	–	ns
t_{CLZ}	Clock to low Z [22, 23, 24]	2.5	–	ns
t_{CHZ}	Clock to high Z [22, 23, 24]	–	3.8	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [22, 23, 24]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [22, 23, 24]	–	3.0	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ setup before CLK rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CES}	Chip enable setup	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes
19. Timing reference level is 1.25 V when V_{DDQ} = 2.5 V.
20. Test conditions shown in (a) of Figure 4 on page 22 unless otherwise noted.
21. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
22. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 4 on page 22. Transition is measured ±200 mV from steady-state voltage.
23. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
24. This parameter is sampled and not 100% tested.

Timing Diagrams

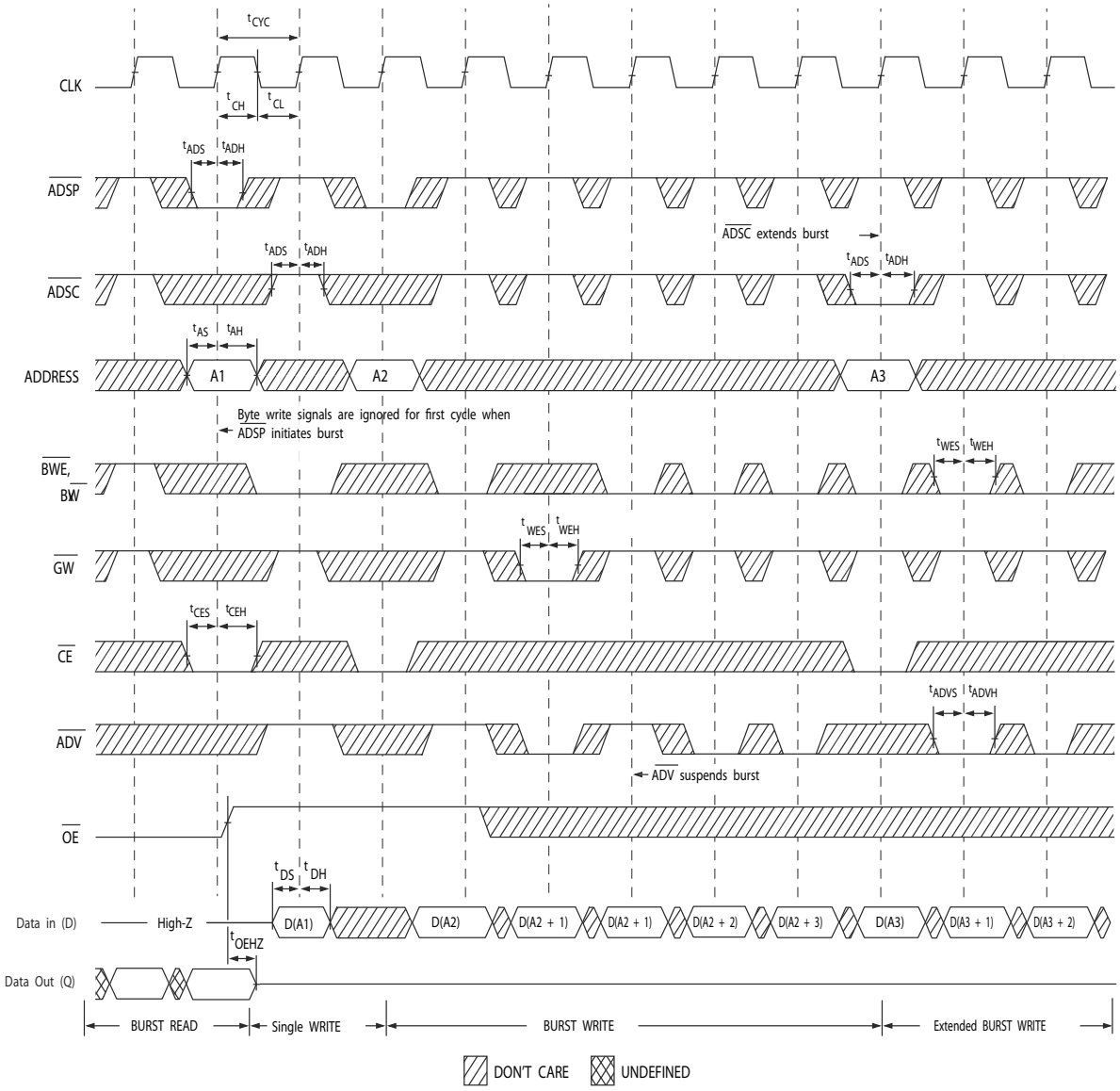
Figure 5. Read Cycle Timing [25]



Note
25. In this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams (continued)

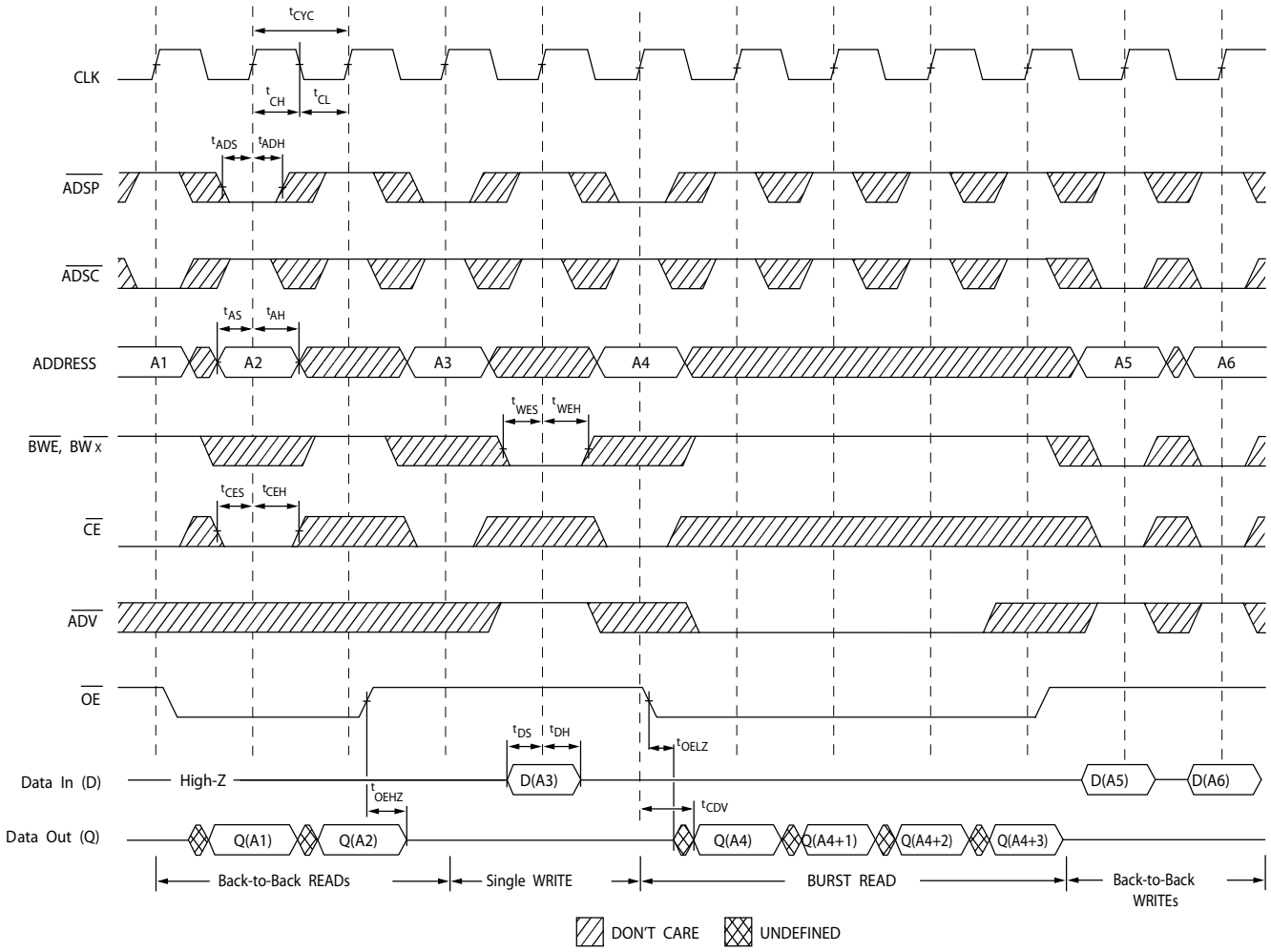
Figure 6. Write Cycle Timing [26, 27]



Notes
26. In this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
27. Full width write is initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

Timing Diagrams (continued)

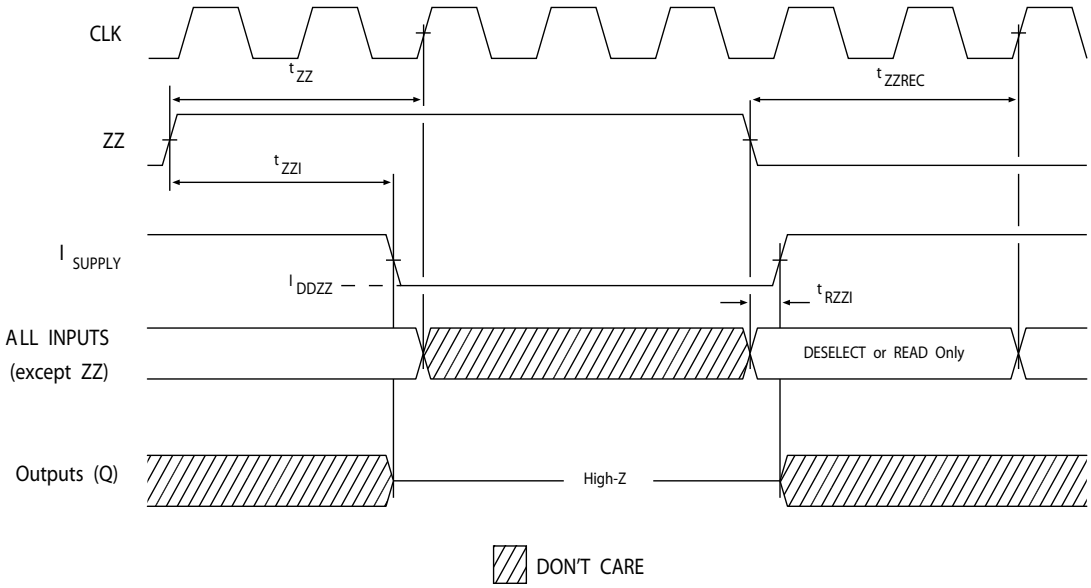
Figure 7. Read/Write Cycle Timing [28, 29, 30]



Notes
28. In this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
29. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
30. $\overline{GW}$ is HIGH.

Timing Diagrams (continued)

Figure 8. ZZ Mode Timing [31, 32]



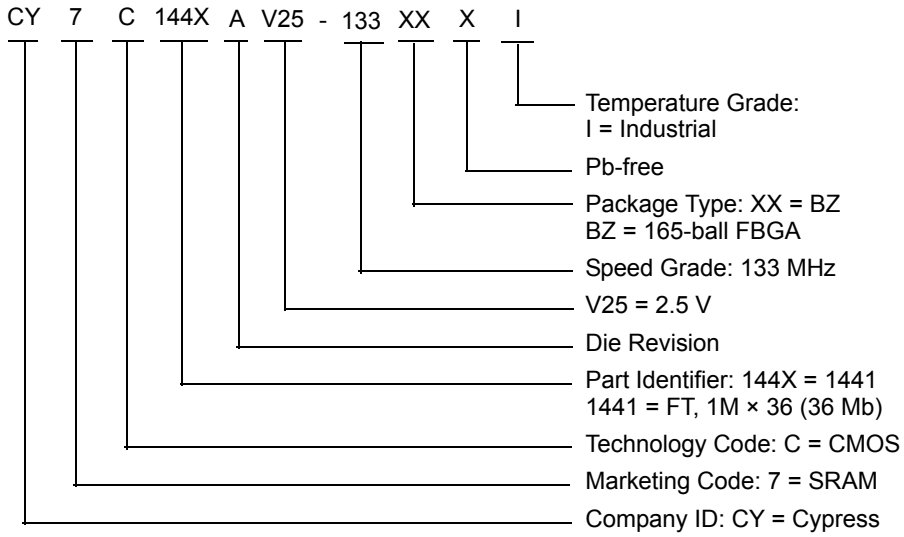
Notes
31. Device must be deselected when entering ZZ mode. See Truth Table on page 10 for all possible signal conditions to deselect the device.
32. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package, and temperature ranges are available. Contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	MPN Status	Package Diagram	Part and Package Type	Operating Range
133	CY7C1441AV25-133BZXI [33]	NRND	51-85195	165-ball FBGA (15 × 17 × 1.4 mm) Pb-free	Industrial

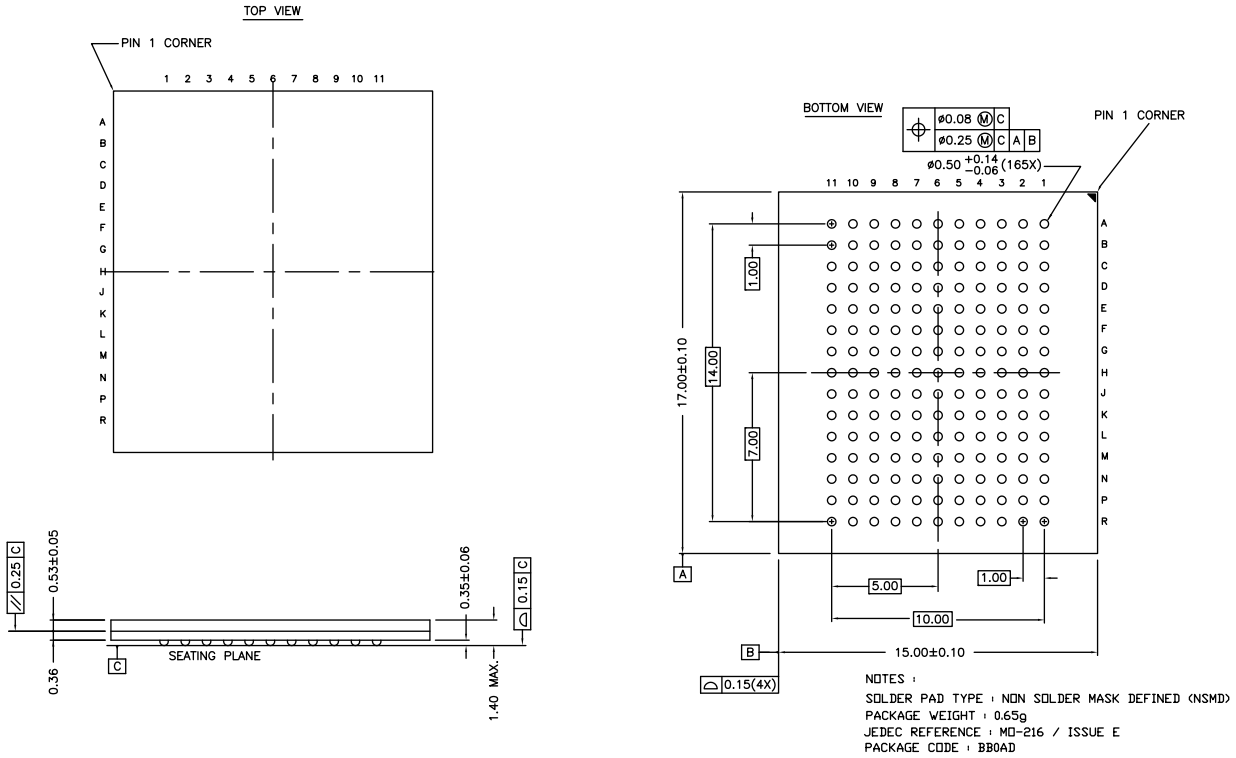
Ordering Code Definitions



Note
33. This MPN is not recommended for new designs.

Package Diagrams

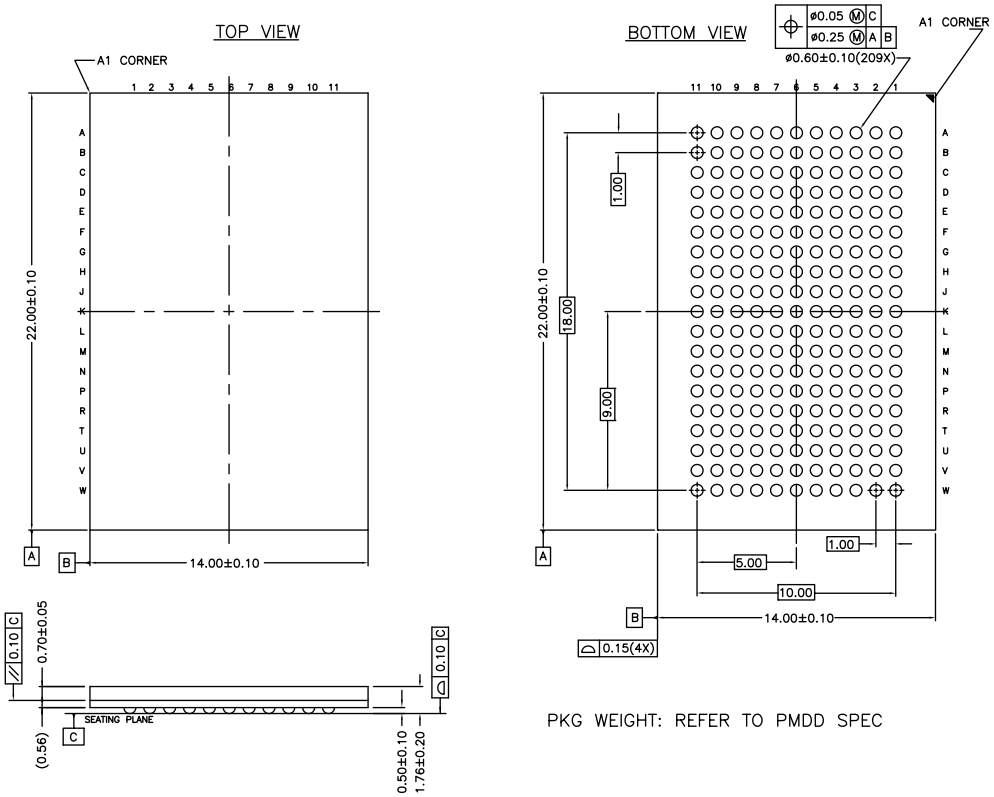
Figure 9. 165-ball FBGA (15 × 17 × 1.40 mm) (0.50 Ball Diameter) Package Outline, 51-85195



51-85195 *D

Package Diagrams (continued)

Figure 10. 209-ball FBGA (14 × 22 × 1.76 mm) BB209A Package Outline, 51-85167



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1441AV25/CY7C1447AV25, 36-Mbit (1M × 36/512K × 72) Flow-Through SRAM Document Number: 001-75380				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	3534404	02/28/2012	GOPA	New data sheet.
*A	3606230	05/02/2012	PRIT / GOPA	Updated Features (Included CY7C1441AV25 related information). Updated Functional Description (Included CY7C1441AV25 related information). Included Logic Block Diagram – CY7C1441AV25. Updated Pin Configurations (Included CY7C1441AV25 related information, included 165-ball FBGA package related information). Updated Functional Overview (Included CY7C1441AV25 related information). Updated Truth Table (Included CY7C1441AV25 related information). Added Partial Truth Table for Read/Write (Corresponding to CY7C1441AV25). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Included CY7C1441AV25 related information). Updated Identification Register Definitions (Included CY7C1441AV25 related information). Updated Scan Register Sizes (Included 165-ball FBGA package related information, added Bit Size (× 36) column). Added Boundary Scan Order (Corresponding to CY7C1441AV25). Updated Capacitance (Included 165-ball FBGA package related information). Updated Thermal Resistance (Included 165-ball FBGA package related information). Updated Ordering Information (Updated part numbers). Updated Package Diagrams (Included 165-ball FBGA package related information (spec 51-85165)).
*B	3925180	03/07/2013	PRIT	Updated Package Diagrams: spec 51-85167 – Changed revision from *B to *C.
*C	4575392	11/20/2014	PRIT	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*D	4675874	03/04/2015	PRIT	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Removed spec 51-85165 *D. Added spec 51-85195 *C. Updated to new template.
*E	4908404	09/04/2015	PRIT	Removed 1.8 V TAP AC Test Conditions. Removed 1.8 V TAP AC Output Load Equivalent. Updated TAP DC Electrical Characteristics and Operating Conditions: Removed details corresponding to Test Condition “VDDQ = 1.8 V” for all parameters. Updated Electrical Characteristics: Removed details corresponding to Test Condition “for 1.8 V I/O” for all parameters. Updated Package Diagrams: spec 51-85195 – Changed revision from *C to *D.
*F	5164560	03/07/2016	PRIT	Added watermark “Not Recommended for New Designs.” across the document. Updated Ordering Information: No change in part numbers. Added a column “MPN Status”. Added Note 33 and referred the same note in “CY7C1441AV25-133BZXI”. Updated to new template. Completing Sunset Review.

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