CY7C1521KV18

72-Mbit DDR II SRAM Four-Word Burst Architecture

Features

- 72-Mbit Density (2M × 36)
- 250 MHz Clock for High Bandwidth
- Four-word Burst for reducing Address Bus Frequency
- Double Data Rate (DDR) Interfaces (data transferred at 500 MHz) at 250 MHz
- Two Input Clocks (K and $\overline{K}$) for precise DDR Timing
    - SRAM uses rising edges only
- Two Input Clocks for Output Data (C and $\overline{C}$) to minimize Clock Skew and Flight Time mismatches
- Echo Clocks (CQ and $\overline{CQ}$) simplify Data Capture in High Speed Systems
- Synchronous Internally Self-timed Writes
- DDR II operates with 1.5 Cycle Read Latency when $\overline{DOFF}$ is asserted HIGH
- Operates similar to DDR-I Device with 1 Cycle Read Latency when $\overline{DOFF}$ is asserted LOW
- 1.8V Core Power Supply with HSTL Inputs and Outputs
- Variable drive HSTL Output Buffers
- Expanded HSTL Output Voltage (1.4 V–V_{DD})
    - Supports both 1.5 V and 1.8 V I/O supply
- Available in 165-ball FBGA Package (13 × 15 × 1.4 mm)
- Offered in Pb-free Packages
- JTAG 1149.1 compatible Test Access Port
- Phase Locked Loop (PLL) for accurate Data Placement

Configurations

CY7C1521KV18 – 2M × 36

Functional Description

The CY7C1521KV18 is 1.8 V Synchronous Pipelined SRAM equipped with DDR II architecture. The DDR II consists of an SRAM core with advanced synchronous peripheral circuitry and a two-bit burst counter. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of C and $\overline{C}$ if provided, or on the rising edge of K and $\overline{K}$ if C/$\overline{C}$ are not provided. For CY7C1521KV18 the burst counter takes in the least two significant bits of the external address and bursts four 36-bit words in the case of CY7C1521KV18, sequentially into or out of the device.

Asynchronous inputs include an output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs, D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need to capture data separately from each individual DDR SRAM in the system design. Output data clocks (C/$\overline{C}$) enable maximum system clocking and data synchronization flexibility.

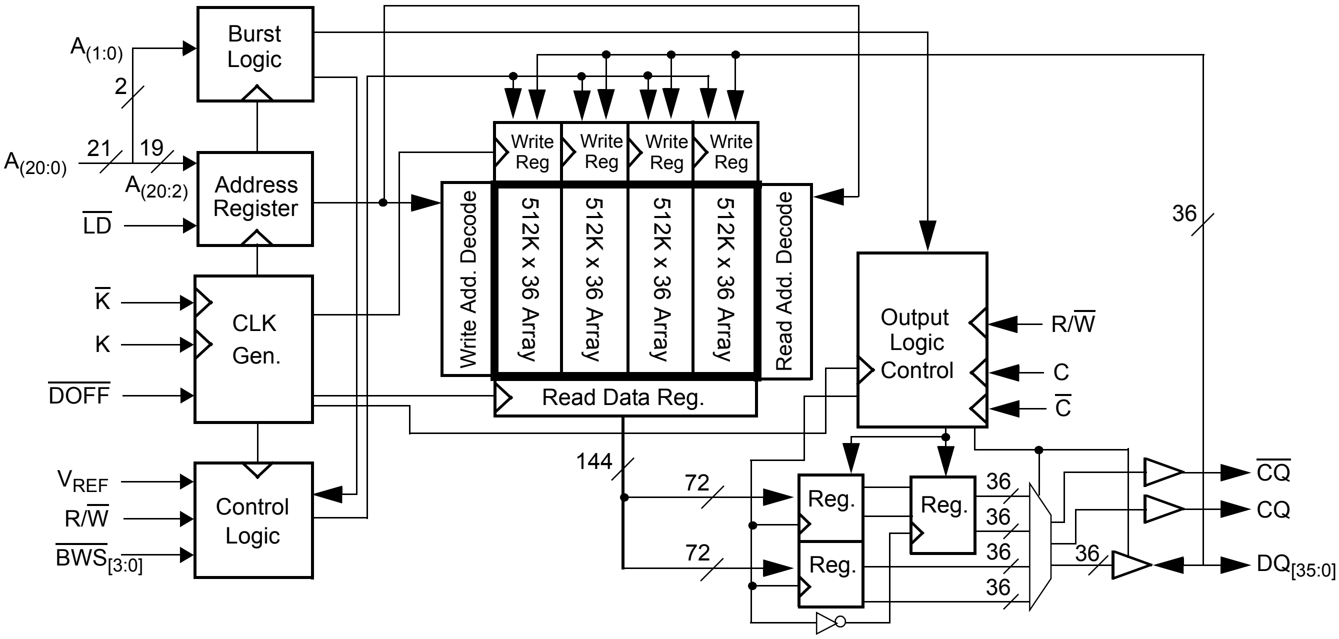
All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ (or K or $\overline{K}$ in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

For a complete list of related documentation, click here.

Selection Guide

Description		250 MHz	Unit
Maximum Operating Frequency		250	MHz
Maximum Operating Current	× 36	420	mA

Logic Block Diagram – CY7C1521KV18



Contents

Pin Configurations

The pin configurations for CY7C1521KV18 follow. [1]

Figure 1. 165-ball FBGA (13 × 15 × 1.4 mm) pinout

CY7C1521KV18 (2M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	R/$\overline{W}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	A	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	A	A0	A1	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	A	A	A	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	A	A	C	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Note

1. NC/144M and NC/288M are not connected to the die and can be tied to any voltage level.

Pin Definitions

Pin Name	I/O	Pin Description
$DQ_{[x:0]}$	Input Output-Synchronous	**Data Input Output Signals**. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during read operations or K and $\overline{K}$ when in single clock mode. When read access is deselected, $Q_{[x:0]}$ are automatically tristated. CY7C1521KV18 – $DQ_{[35:0]}$
$\overline{LD}$	Input-Synchronous	**Synchronous Load**. This input is brought LOW when a bus cycle sequence is defined. This definition includes address and read/write direction. All transactions operate on a burst of 4 data (two clock periods of bus activity).
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, BWS_3	Input-Synchronous	**Byte Write Select 0, 1, 2, and 3 – Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the Write operations. Bytes not written remain unaltered. CY7C1521KV18 – BWS_0 controls $D_{[8:0]}$, BWS_1 controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A, A_0, A1	Input-Synchronous	**Address Inputs**. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2M × 36 (4 arrays each of 512K × 36) for CY7C1521KV18. CY7C1521KV18 – A_0 and A_1 are the inputs to the burst counter. These are incremented internally in a linear fashion. 21address inputs are needed to access the entire memory array.
R/$\overline{W}$	Input-Synchronous	**Synchronous Read/Write Input**. When $\overline{LD}$ is LOW, this input designates the access type (read when R/$\overline{W}$ is HIGH, write when R/$\overline{W}$ is LOW) for the loaded address. R/$\overline{W}$ must meet the setup and hold times around the edge of K.
C	Input Clock	**Positive Input Clock for Output Data.** C is used in conjunction with $\overline{C}$ to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See Application Example on page 8 for more information.
$\overline{C}$	Input Clock	**Negative Input Clock for Output Data**. $\overline{C}$ is used in conjunction with C to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See Application Example on page 8 for more information.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous data being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Output Clock	**CQ Referenced with Respect to C**. This is a free running clock and is synchronized to the input clock for output data (C) of the DDR II. In single clock mode, CQ is generated with respect to K. The timing for the echo clocks is shown in Switching Characteristics on page 22.
$\overline{CQ}$	Output Clock	**$\overline{CQ}$ Referenced with Respect to $\overline{C}$**. This is a free running clock and is synchronized to the input clock for output data ($\overline{C}$) of the DDR II. In single clock mode, $\overline{CQ}$ is generated with respect to $\overline{K}$. The timing for the echo clocks is shown in Switching Characteristics on page 22.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 × RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**PLL Turn Off – Active LOW**. Connecting this pin to ground turns off the PLL inside the device. The timing in the PLL turned off operation is different from that listed in this data sheet. For normal operation, this pin is connected to a pull up through a 10K ohm or less pull up resistor. The device behaves in DDR-I mode when the PLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR-I timing.

Pin Definitions (continued)

Pin Name	I/O	Pin Description
TDO	Output	**TDO Pin for JTAG**.
TCK	Input	**TCK Pin for JTAG**.
TDI	Input	**TDI Pin for JTAG**.
TMS	Input	**TMS Pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

Functional Overview

The CY7C1521KV18 is synchronous pipelined Burst SRAM equipped with a DDR interface, which operates with a read latency of one and half cycles when $\overline{\text{DOFF}}$ pin is tied HIGH. When $\overline{\text{DOFF}}$ pin is set LOW or connected to V_{SS} the device behaves in DDR-I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the rising edge of the output clocks (C/$\overline{C}$, or K/$\overline{K}$ when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (C/$\overline{C}$, or K/$\overline{K}$ when in single-clock mode).

All synchronous control (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS}_{[0:X]}$) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C1521KV18 is described in the following sections.

Read Operations

The CY7C1521KV18 is organized internally as four arrays of 512K × 36. Accesses are completed in a burst of four sequential 36-bit data words. Read operations are initiated by asserting R/$\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the read address register and the least two significant bits of the address are presented to the burst counter. The burst counter increments the address in a linear fashion. Following the next K clock rise, the corresponding 36-bit word of data from this address location is driven onto $Q_{[35:0]}$, using $\overline{C}$ as the output timing reference. On the subsequent rising edge of C the next 36-bit data word from the address location generated by the burst counter is driven onto $Q_{[36:0]}$. This process continues until all four 36-bit data words are driven out onto $Q_{[35:0]}$. The requested data is valid 0.45 ns from the rising edge of the output clock (C or $\overline{C}$, or K and $\overline{K}$ 250 MHz device). To maintain the internal logic, each read access must be allowed to complete. Each read access consists of four 36-bit data words and takes two clock cycles to complete. Therefore, read accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second read request. Read accesses can be initiated on every other K clock rise. Doing so pipelines the data flow such that data is transferred out of the device on every rising edge of the output clocks (C/$\overline{C}$ or K/$\overline{K}$ when in single-clock mode).

The CY7C1521KV18 first completes the pending read transactions, when read access is deselected. Synchronous internal circuitry automatically tristates the output following the next rising edge of the positive output clock (C). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register and the least two significant bits of the address are presented to the burst counter. The burst counter increments the address in a linear fashion. On the following K clock rise the data presented to $D_{[35:0]}$ is latched and stored into the 36-bit write data register, provided $\overline{BWS}_{[3:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$) the information presented to $D_{[35:0]}$ is also stored into the write data register, provided $\overline{BWS}_{[3:0]}$ are both asserted active. This process continues for one more cycle until four 36-bit words (a total of 144 bits) of data are stored in the SRAM. The 144 bits of data are then written into the memory array at the specified location. Therefore, Write accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second write request. Write accesses can be initiated on every other rising edge of the positive input clock (K). Doing so pipelines the data flow such that 36 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When Write access is deselected, the device ignores all inputs after the pending write operations are completed.

Byte Write Operations

Byte write operations are supported by the CY7C1521KV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$ and $\overline{BWS}_3$, which are sampled with each set of 36-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature is used to simplify read/modify/write operations to a byte write operation.

Single Clock Mode

The CY7C1521KV18 is used with a single clock that controls both the input and output registers. In this mode the device recognizes only a single pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, tie C and $\overline{C}$ HIGH at power on. This function is a strap option and not alterable during device operation.

DDR Operation

The CY7C1521KV18 enables high-performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. The CY7C1521KV18 requires a single No Operation (NOP) cycle when transitioning from a read to a write cycle. At higher frequencies, some applications may require a second NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a posted write.

If a read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals can be common between banks as appropriate.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5 × the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with $V_{DDQ} = 1.5$ V. The output impedance is adjusted every 1024 cycles at power up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR II to simplify data capture on high speed systems. Two echo clocks are generated by the DDR II. CQ is referenced with respect to C and $\overline{CQ}$ is referenced with respect to $\overline{C}$. These are free running clocks and are synchronized to the output clock of the DDR II. In the single clock mode, CQ is generated with respect to K and $\overline{CQ}$ is generated with respect to $\overline{K}$. The timing for the echo clocks is shown in Switching Characteristics on page 22.

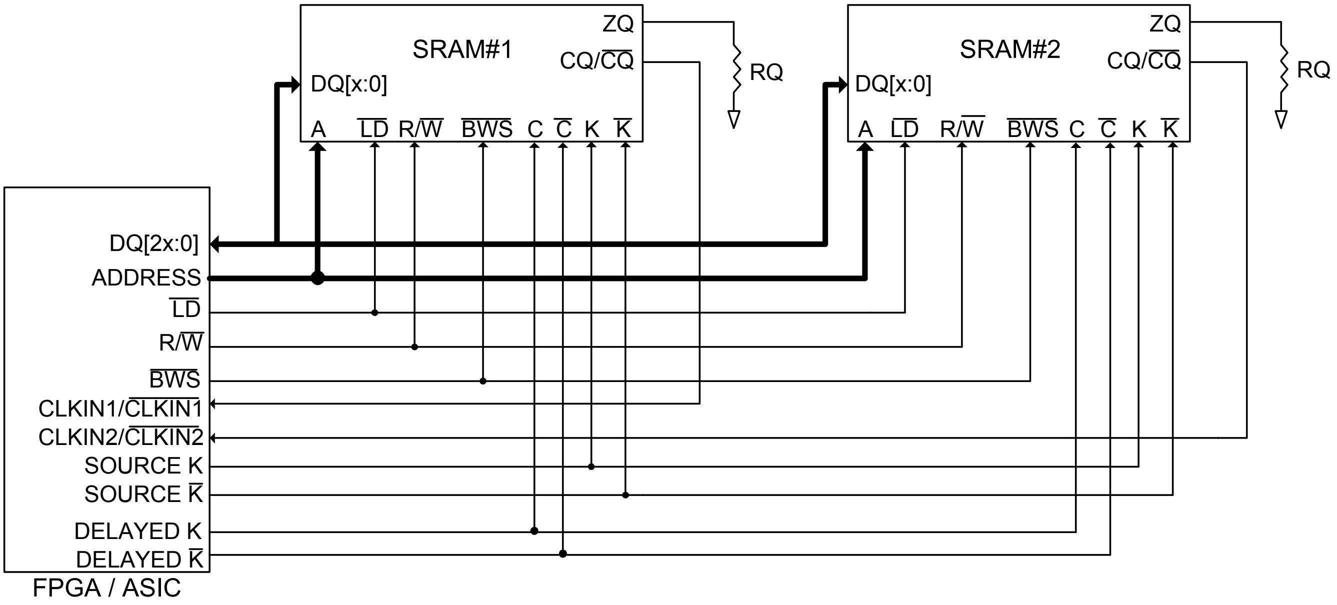
PLL

These chips use a Phase Locked Loop (PLL) that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the $\overline{DOFF}$ is tied HIGH, the PLL is locked after 20 μs of stable clock. The PLL can also be reset by slowing or stopping the input clocks K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock it to the desired frequency. The PLL automatically locks 20 μs after a stable clock is presented. The PLL may be disabled by applying ground to the $\overline{DOFF}$ pin. When the PLL is turned off, the device behaves in DDR-I mode (with one cycle latency and a longer access time).

Application Example

Figure 2 shows two DDR II used in an application.

Figure 2. Application Example (Width Expansion)



Truth Table

The truth table for the CY7C1521KV18 follows. [2, 3, 4, 5, 6, 7]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ	DQ	DQ
Write Cycle: Load address; wait one cycle; input write data on four consecutive K and $\overline{K}$ rising edges.	L–H	L	L	D(A1) at K(t + 1)↑	D(A2) at $\overline{K}$(t + 1)↑	D(A3) at K(t + 2)↑	D(A4) at $\overline{K}$(t + 2)↑
Read Cycle: Load address; wait one and a half cycle; read data on four consecutive $\overline{C}$ and C rising edges.	L–H	L	H	Q(A1) at $\overline{C}$(t + 1)↑	Q(A2) at C(t + 2)↑	Q(A3) at $\overline{C}$(t + 2)↑	Q(A4) at C(t + 3)↑
NOP: No Operation	L–H	H	X	High-Z	High-Z	High-Z	High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

Burst Address Table

(CY7C1521KV18)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X..X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

Notes

2. X = “Don’t Care,” H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
3. Device powers up deselected with the outputs in a tristate condition.
4. On CY7C1521KV18, “A1” represents address location latched by the devices when transaction was initiated and “A2”, “A3”, “A4” represents the addresses sequence in the burst.
5. “t” represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the “t” clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
7. It is recommended that K = $\overline{K}$ and C = $\overline{C}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

Write Cycle Descriptions

The write cycle description table for CY7C1521KV18 follows. [8, 9]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

Notes

[8] X = “Don’t Care,” H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.

[9] Is based on a write cycle that was initiated in accordance with the Truth Table on page 9. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

IEEE 1149.1 Serial Boundary Scan (JTAG)

This SRAM incorporates a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8 V IO logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port

Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 13. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 17). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and is performed when the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions are serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 14. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions are used to capture the contents of the input and output ring.

The Boundary Scan Order on page 18 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and is shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 17.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 17. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #108. When this scan cell, called the "extest output bus tristate," is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

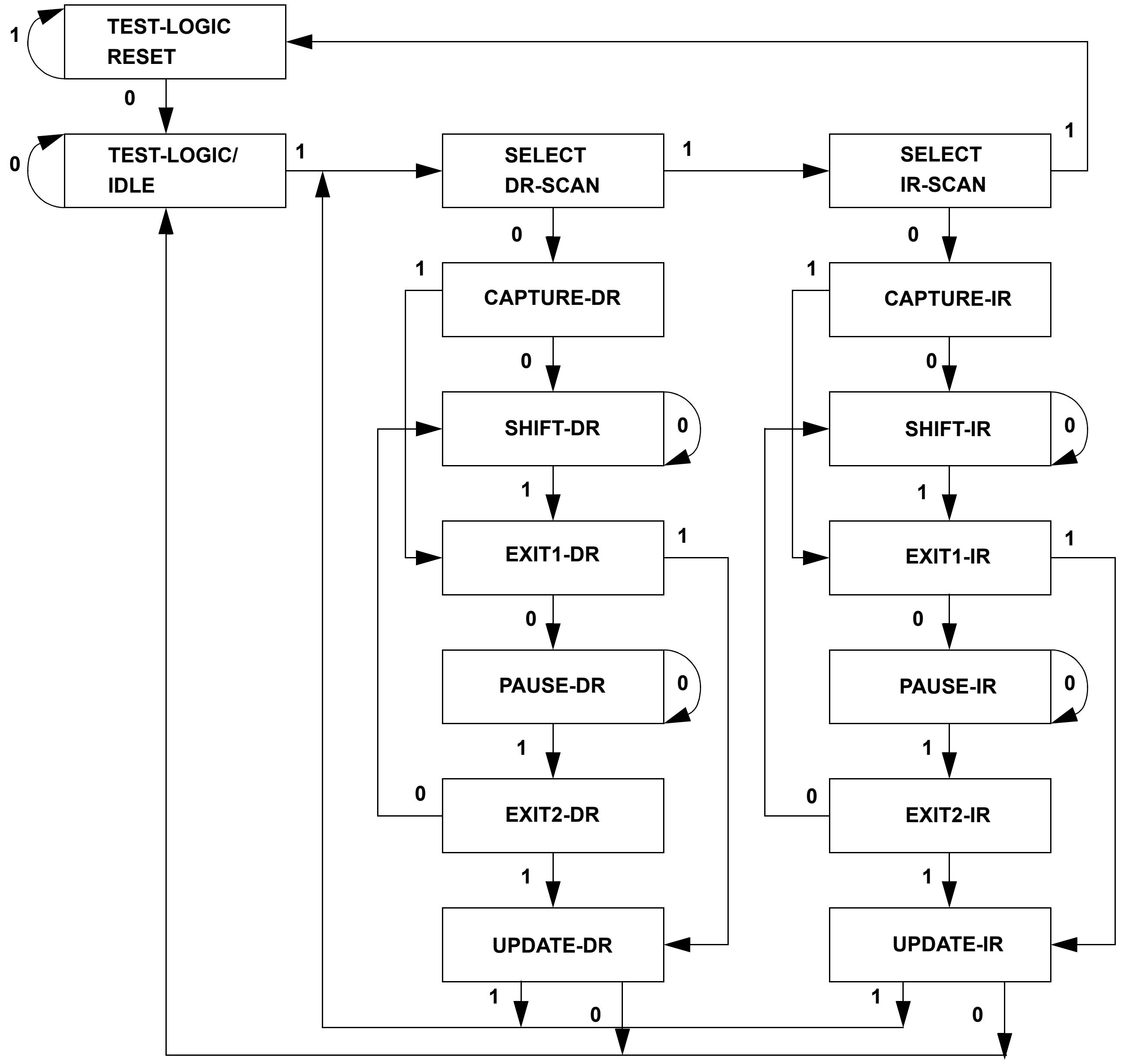
This bit is set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

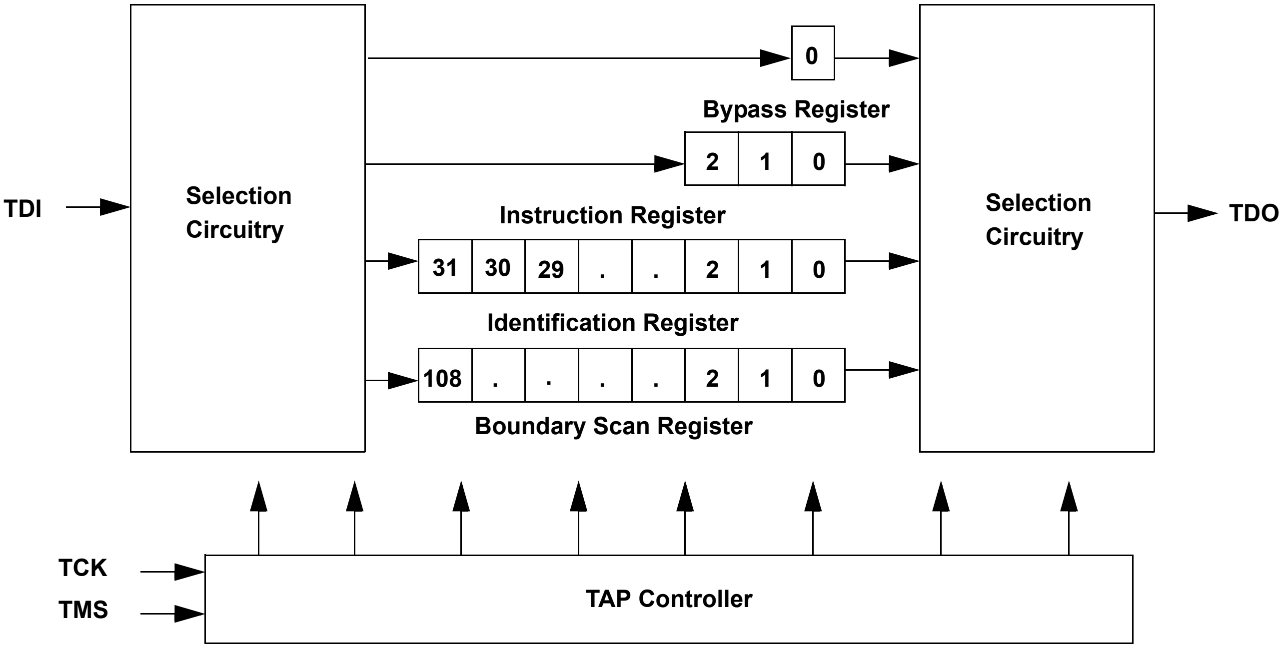
The state diagram for the TAP controller follows. [10]



Note

10. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range

Parameter [11, 12, 13]	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	$I_{OH} = –2.0$ mA	1.4	–	V
V_{OH2}	Output HIGH Voltage	$I_{OH} = –100$ µA	1.6	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA	–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	–	0.2	V
V_{IH}	Input HIGH Voltage		0.65 × V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.35 × V_{DD}	V
I_X	Input and Output Load Current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes

11. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics on page 20.
12. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > –1.5$ V (Pulse width less than $t_{CYC}/2$).
13. All voltage referenced to Ground.

TAP AC Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	Min	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH	20	–	ns
t_{TL}	TCK Clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns

Notes

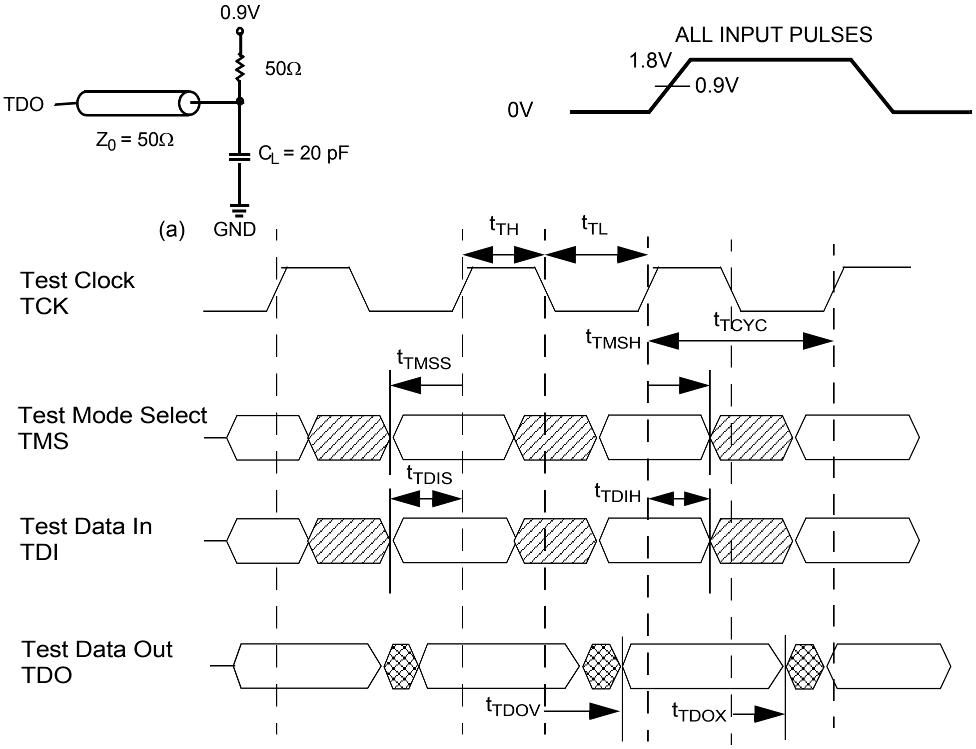
[14] t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.

[15] Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions

Figure 3 shows the TAP timing and test conditions. [16]

Figure 3. TAP Timing and Test Conditions



Note

16. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	Value	Description
	CY7C1521KV18	
Revision Number (31:29)	000	Version number.
Cypress Device ID (28:12)	11010100011100100	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	10A
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	2A
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1H
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R
108	Internal

Power Up Sequence in DDR II SRAM

DDR II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

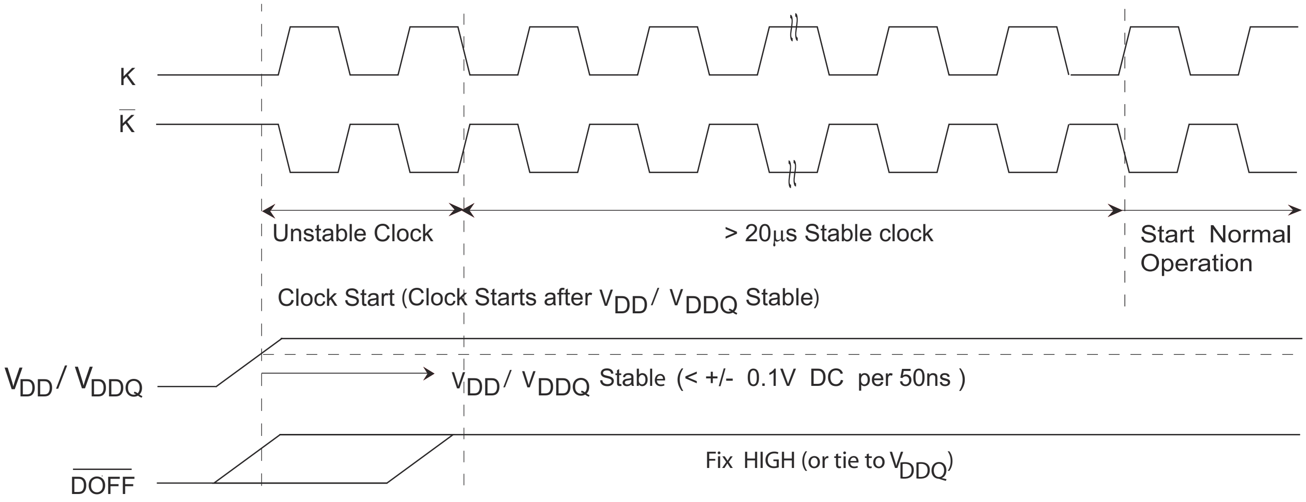
Power Up Sequence

- Apply power and drive $\overline{\text{DOFF}}$ either HIGH or LOW (All other inputs can be HIGH or LOW).
  - Apply V_{DD} before V_{DDQ}.
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - Drive $\overline{\text{DOFF}}$ HIGH.
- Provide stable $\overline{\text{DOFF}}$ (HIGH), power and clock (K, $\overline{\text{K}}$) for 20 μs to lock the PLL.

PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20 μs of stable clock to relock to the desired clock frequency.

Figure 4. Power Up Waveforms



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +2.9 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to $+V_{DD}$

DC Applied to Outputs in High-Z ......–0.5 V to V_{DDQ} + 0.3 V

DC Input Voltage [17] ....–0.5 V to V_{DD} + 0.3 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage (MIL-STD-883, M 3015) .... >2001V

Latch up Current .... >200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD} [18]	V_{DDQ} [18]
Commercial	0 °C to +70 °C	1.8 ± 0.1 V	1.4 V to V_{DD}

Electrical Characteristics

Over the Operating Range

DC Electrical Characteristics

Over the Operating Range

Parameter [19]	Description	Test Conditions			Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage				1.7	1.8	1.9	V
V_{DDQ}	IO Supply Voltage				1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH Voltage	Note 20			$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW Voltage	Note 21			$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH Voltage	$I_{OH} = –0.1$ mA, Nominal Impedance			$V_{DDQ} – 0.2$	–	V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW Voltage	$I_{OL} = 0.1$ mA, Nominal Impedance			V_{SS}	–	0.2	V
V_{IH}	Input HIGH Voltage				$V_{REF} + 0.1$	–	$V_{DDQ} + 0.3$	V
V_{IL}	Input LOW Voltage				–0.3	–	$V_{REF} – 0.1$	V
I_X	Input Leakage Current	GND $\leq V_I \leq V_{DDQ}$			–5	–	5	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{DDQ}$, Output Disabled			–5	–	5	µA
V_{REF}	Input Reference Voltage [22]	Typical Value = 0.75 V			0.68	0.75	0.95	V
I_{DD} [23]	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{CYC}$	250 MHz	(× 36)	–	–	420	mA
I_{SB1}	Automatic Power Down Current	Max V_{DD}, Both Ports Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ $f = f_{MAX} = 1/t_{CYC}$, Inputs Static	250 MHz	(× 36)	–	–	270	mA

AC Electrical Characteristics

Over the Operating Range

Parameter [17]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		$V_{REF} + 0.2$	–	–	V
V_{IL}	Input LOW Voltage		–	–	$V_{REF} – 0.2$	V

Notes

[17] Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > –1.5$ V (Pulse width less than $t_{CYC}/2$).

[18] Power up: assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

[19] All voltage referenced to Ground.

[20] Outputs are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω $\leq$ RQ $\leq$ 350 Ω.

[21] Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω $\leq$ RQ $\leq$ 350 Ω.

[22] V_{REF}(min) = 0.68V or $0.46V_{DDQ}$, whichever is larger, V_{REF}(max) = 0.95V or $0.54V_{DDQ}$, whichever is smaller.

[23] The operation current is calculated with 50% read cycle and 50% write cycle.

Capacitance

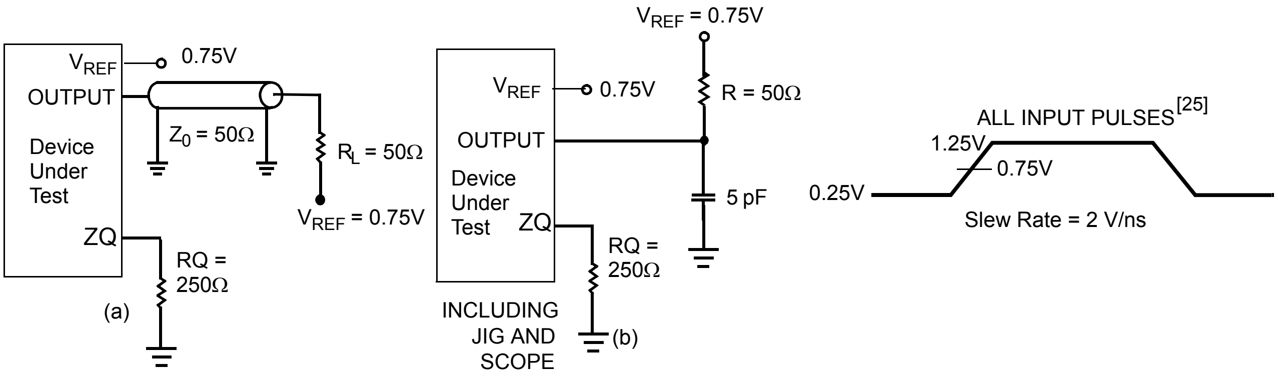
Parameter [24]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V	2	pF
C_O	Output capacitance		3	pF

Thermal Resistance

Parameter [24]	Description	Test Conditions	165-ball FBGA Package	Unit
Θ_{JA} (0 m/s)	Thermal resistance (junction to ambient)	Socketed on a 170 × 220 × 2.35 mm, eight-layer printed circuit board	14.43	°C/W
Θ_{JA} (1 m/s)			13.40	°C/W
Θ_{JA} (3 m/s)			12.66	°C/W
Θ_{JB}	Thermal resistance (junction to board)		11.38	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.30	°C/W

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



Notes

24. Tested initially and after any design or process change that may affect these parameters.
25. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, V_{REF} = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of Figure 5.

Switching Characteristics

Over the Operating Range

Parameters [25, 26]		Description	250 MHz		Unit
Cypress Parameter	**Consortium Parameter**		**Min**	**Max**	
t_{POWER}		V_{DD}(Typical) to the First Access [27]	1	–	ms
t_{CYC}	t_{KHKH}	K Clock and C Clock Cycle Time	4.0	8.4	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	1.6	–	ns
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	1.6	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise and C to $\overline{C}$ Rise (rising edge to rising edge)	1.8	–	ns
t_{KHCH}	t_{KHCH}	K/$\overline{K}$ Clock Rise to C/$\overline{C}$ Clock Rise (rising edge to rising edge)	0.0	1.8	ns
Setup Times					
t_{SA}	t_{AVKH}	Address Setup to K Clock Rise	0.5	–	ns
t_{SC}	t_{IVKH}	Control Setup to K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.5	–	ns
t_{SCDDR}	t_{IVKH}	Double Data Rate Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.35	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ Setup to Clock (K/$\overline{K}$) Rise	0.35	–	ns
Hold Times					
t_{HA}	t_{KHAX}	Address Hold after K Clock Rise	0.5	–	ns
t_{HC}	t_{KHIX}	Control Hold after K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.5	–	ns
t_{HCDDR}	t_{KHIX}	Double Data Rate Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.35	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise	0.35	–	ns

---

Notes

26. When a part with a maximum frequency above 167 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is operated and outputs data with the output timings of that frequency range.
27. This part has an internal voltage regulator; t_{POWER} is the time that the power is supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.

Switching Characteristics (continued)

Over the Operating Range

Parameters [25, 26]		Description	250 MHz		Unit
Cypress Parameter	Consortium Parameter		Min	Max	
Output Times					
t_{CO}	t_{CHQV}	C/$\overline{C}$ Clock Rise (or K/$\overline{K}$ in single clock mode) to Data Valid	–	0.45	ns
t_{DOH}	t_{CHQX}	Data Output Hold after Output C/$\overline{C}$ Clock Rise (Active to Active)	–0.45	–	ns
t_{CCQO}	t_{CHCQV}	C/$\overline{C}$ Clock Rise to Echo Clock Valid	–	0.45	ns
t_{CQOH}	t_{CHCQX}	Echo Clock Hold after C/$\overline{C}$ Clock Rise	–0.45	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid	–	0.30	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.30	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH [28]	1.75	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise (rising edge to rising edge) [28]	1.75	–	ns
t_{CHZ}	t_{CHQZ}	Clock (C/$\overline{C}$) Rise to High-Z (Active to High-Z) [29, 30]	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (C/$\overline{C}$) Rise to Low-Z [29, 30]	–0.45	–	ns
PLL Timing					
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	PLL Lock Time (K, C)	20	–	μs
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to PLL Reset	30	–	ns

---

Notes

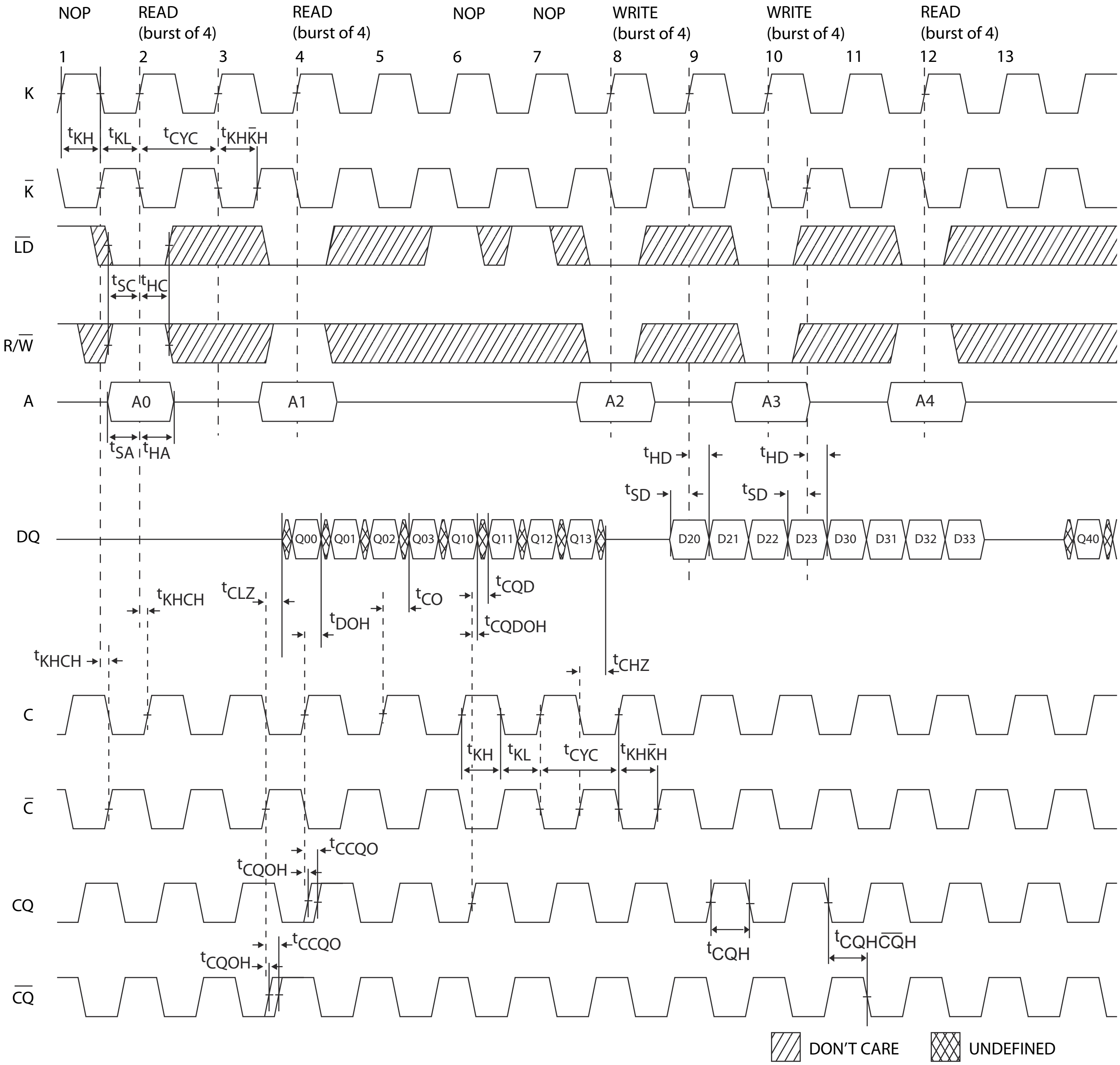
[28] These parameters are extrapolated from the input timing parameters (t_{CYC}/2 - 250 ps, where 250 ps is the internal jitter). These parameters are only guaranteed by design and are not tested in production.

[29] t_{CHZ}, t_{CLZ} are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 21. Transition is measured ±100 mV from steady-state voltage.

[30] At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.

Switching Waveforms

Figure 6. Read/Write/Deselect Sequence [31, 32, 33]



Notes

31. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
32. Outputs are disabled (High-Z) one clock cycle after a NOP.
33. In this example, if address A4 = A3, then data Q40 = D30, Q41 = D31, Q42 = D32, and Q43 = D43. Write data is forwarded immediately as read results. This note applies to the whole diagram.

Ordering Information

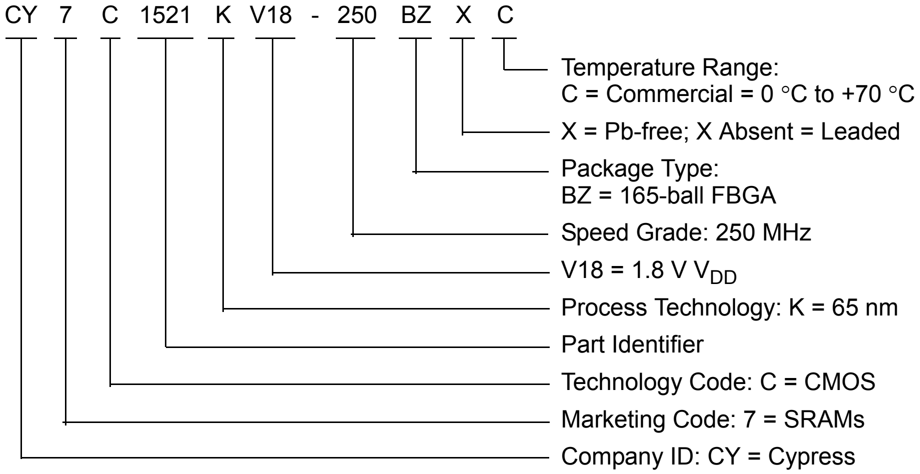
The following table lists all possible speed, package, and temperature range options supported for these devices. Note that some options listed may not be available for order entry. To verify the availability of a specific option, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative for the status of availability of parts.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://app.cypress.com/portal/server.pt?space=CommunityPage&control=SetCommunity&CommunityID=201&PageID=230.

Table 1. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
250	CY7C1521KV18-250BZXC	51-85180	165-Ball FBGA (13 × 15 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions



CY 7 C 1521 K V18 - 250 BZ X C

Temperature Range:
C = Commercial = 0 °C to +70 °C

X = Pb-free; X Absent = Leaded

Package Type:
BZ = 165-ball FBGA

Speed Grade: 250 MHz

V18 = 1.8 V V_{DD}

Process Technology: K = 65 nm

Part Identifier

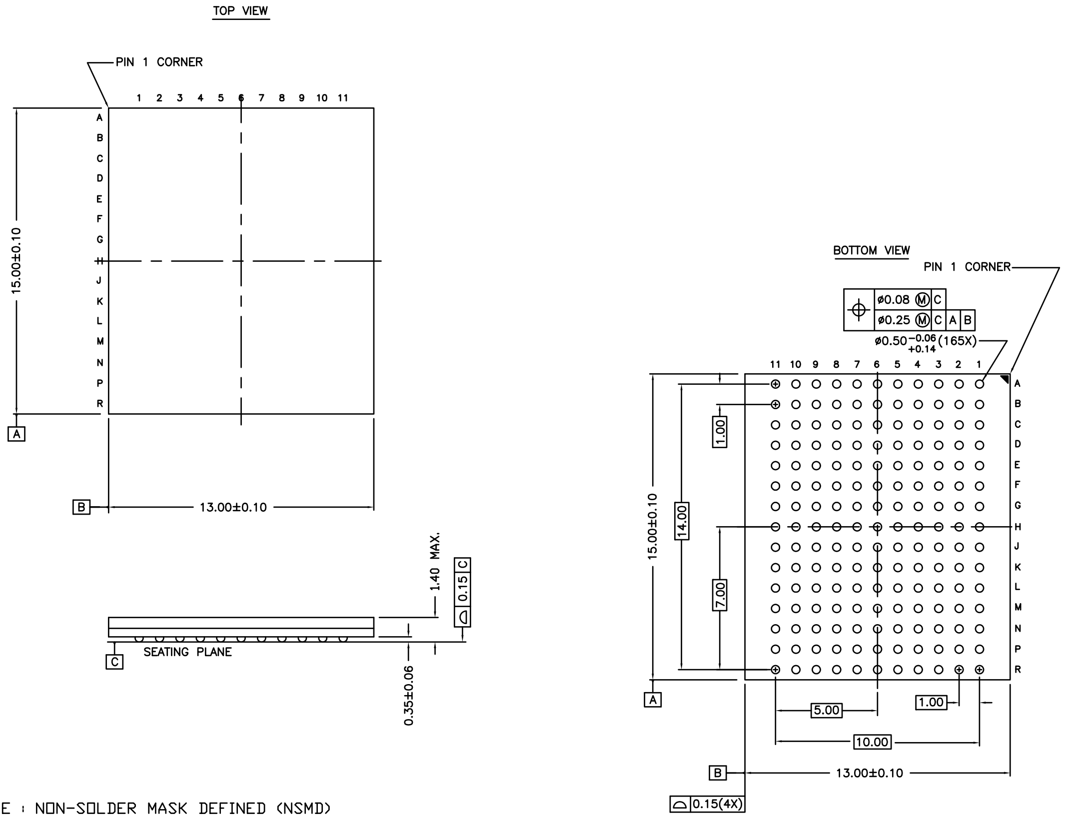
Technology Code: C = CMOS

Marketing Code: 7 = SRAMs

Company ID: CY = Cypress

Package Diagram

Figure 7. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180



NOTES :
SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)
JEDEC REFERENCE : MO-216 / ISSUE E
PACKAGE CODE : BB0AC/BW0AC
PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION
DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.

51-85180 *G

Acronyms

Acronym	Description
DDR	Double Data Rate
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
HSTL	High-Speed Transceiver Logic
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
LMBU	Logical Multiple Bit Upset
LSB	Least Significant Bit
LSBU	Logical Single Bit Upset
MSB	Most Significant Bit
PLL	Phase Locked Loop
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1521KV18, 72-Mbit DDR II SRAM Four-Word Burst Architecture Document Number: 001-00439				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	374703	SYT	See ECN	New data sheet.
*A	1103903	VKN	See ECN	Updated I_{DD} Spec Updated Ordering Information.
*B	1699246	VKN / AESA	See ECN	Changed status from Advance Information to Preliminary.
*C	1939726	VKN / AESA	See ECN	Changed PLL lock time from 1024 cycles to 20 μs Added footnote #19 related to I_{DD} Corrected typo in the footnote #23
*D	2606839	VKN / PYRS	11/13/08	Changed JTAG ID [31:29] from 001 to 000, Updated power up sequence waveform and its description, Changed Ambient Temperature with Power Applied from “–10°C to +85°C” to “–55°C to +125°C” in the “Maximum Ratings” on page 21, Included Thermal Resistance values, Changed the package size from 15 × 17 × 1.4 mm to 13 × 15 × 1.4 mm.
*E	2681899	VKN / PYRS	04/01/2009	Changed status from Preliminary to Final. Added note on top of the Ordering Information table Post to external web
*F	2870201	NJY	02/01/2010	No technical updates.
*G	3196159	NJY	03/15/2011	Obsolete document.
*H	3999679	PRIT	05/14/2013	Reactivated document. Updated Ordering Information (Updated part numbers). Updated Package Diagram: spec 51-85180 – Changed revision from *C to *F. Added Acronyms and Units of Measure. Updated to new template.
*I	4371742	PRIT	05/06/2014	Updated Application Example: Updated Figure 2. Updated Thermal Resistance: Updated values of Θ_{JA} parameter. Included Θ_{JB} parameter and its details.
*J	4567085	PRIT	11/11/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*K	4739556	PRIT	04/24/2015	Updated to new template. Completing Sunset Review.
*L	5210946	PRIT	04/07/2016	Updated Package Diagram: spec 51-85180 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.

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