CY7C197BN

256-Kbit (256 K × 1) Static RAM

Features

- Fast access time: 15 ns
- Wide voltage range: 5.0 V ± 10% (4.5 V to 5.5 V)
- CMOS for optimum speed and power
- TTL compatible inputs and outputs
- Available in 24-pin DIP and 24-pin SOJ

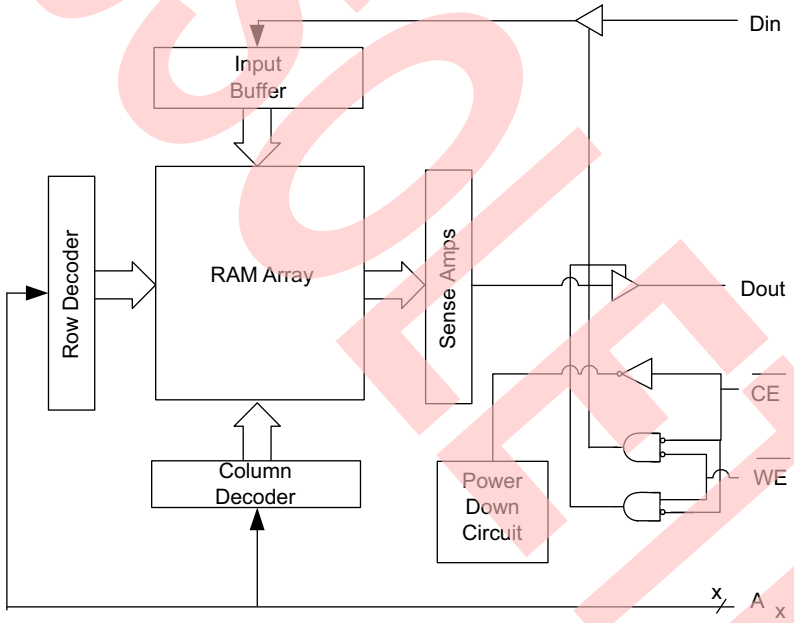
General Description

The CY7C197BN[1] is a high performance CMOS Asynchronous SRAM organized as 256 K × 1 bits that supports an asynchronous memory interface. The device features an automatic power down feature that significantly reduces power consumption when deselected.

See the Truth Table on page 10 for a complete description of Read and Write modes.

The CY7C197BN is available in 24-pin DIP and 24-pin SOJ package(s).

Logic Block Diagram



Product Portfolio

Description	-15	-25	Unit
Maximum Access Time	15	25	ns
Maximum Operating Current	150	95	mA
Maximum CMOS Standby Current	10	10	mA

Note
1. For best practice recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Contents

Pin Layout and Specification

Figure 1. 24-pin DIP pinout

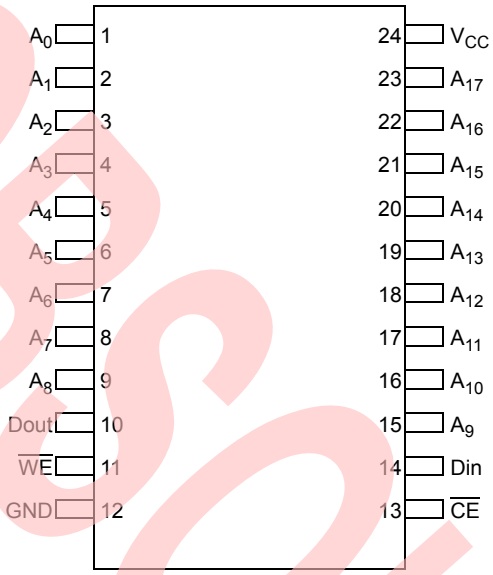
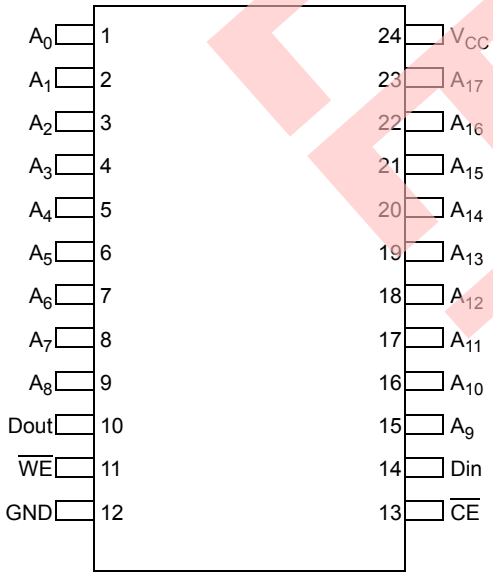


Figure 2. 24-pin SOJ pinout



Pin Description

Pin	Type	Description	DIP	SOJ
A_X	Input	Address Inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23
$\overline{CE}$	Control	Chip Enable	13	13
Din	Input	Data Input Pins	14	14
Dout	Output	Data Output Pins	10	10
V_{CC}	Supply	Power (5.0 V)	24	24
$\overline{WE}$	Control	Write Enable	11	11

Maximum Ratings

Exceeding the maximum rating may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND ..... –0.5 V to +7.0 V

DC Voltage Applied to Outputs in High Z State [2] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature [3]	V_{CC}
Commercial	0 °C to 70 °C	5.0 V ± 10%

DC Electrical Characteristics

Parameter [2]	Description	Condition	15 ns		25 ns		Unit
			Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	–	0.4	V
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	µA
I_{IX}	Input Leakage Current	GND ≤ Vi ≤ V_{CC}	–5	+5	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = F_{MAX} = $1/t_{RC}$	–	150	–	95	mA
I_{SB1}	Automatic $\overline{CE}$ Power Down Current TTL Inputs	V_{CC} = Max, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = F_{MAX}	–	30	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power Down Current CMOS Inputs	V_{CC} = Max, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} < 0.3 V, f = 0	–	10	–	10	mA

Capacitance

Parameter [4]	Description	Conditions	Max (ALL – PACKAGES)	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		10	

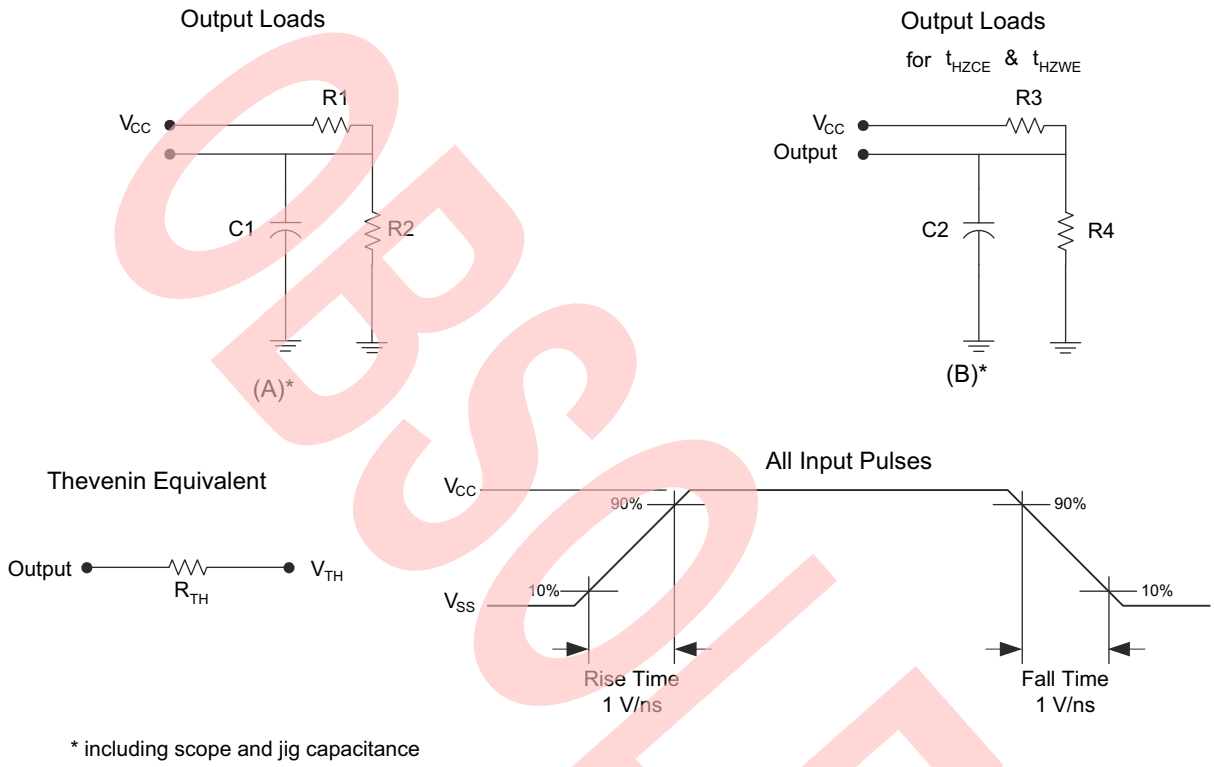
Thermal Resistance

Parameter [4]	Description	Conditions	24-pin DIP	24-pin SOJ	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
Θ_{JC}	Thermal resistance (junction to case)		33.80	37.56	

Notes
2. V_{IL}(min) = –2.0 V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads

Figure 3. AC Test Loads [5]



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Note
5. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

AC Electrical Characteristics

Parameter [6, 7, 8, 9]	Description	15 ns		25 ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15	–	25	–	ns
t_{AA}	Address to Data Valid	–	15	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	15	–	25	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	11	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	15	–	20	ns
t_{WC}	Write Cycle Time	15	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	20	–	ns
t_{AW}	Address Set-up to Write End	10	–	20	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	9	–	20	–	ns
t_{SD}	Data Set-Up to Write End	9	–	15	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	–	11	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2	–	3	–	ns

Notes

6. Tested initially and after any design or process change that may affect these parameters.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal Write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. t_{HZCE}, t_{HZWE} are specified as in part (b) of the Figure 3 on page 6. Transitions are measured ±200 mV from steady state voltage.

Timing Waveforms

Figure 4. Read Cycle No. 1 [10, 11]

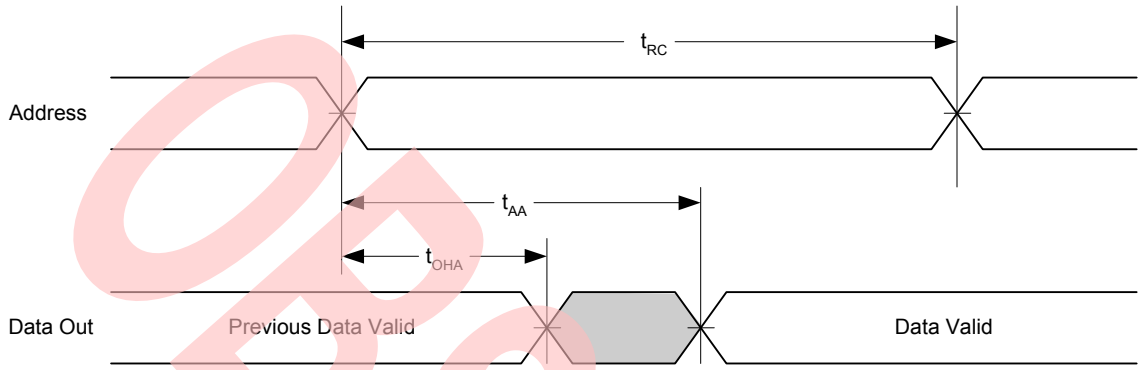
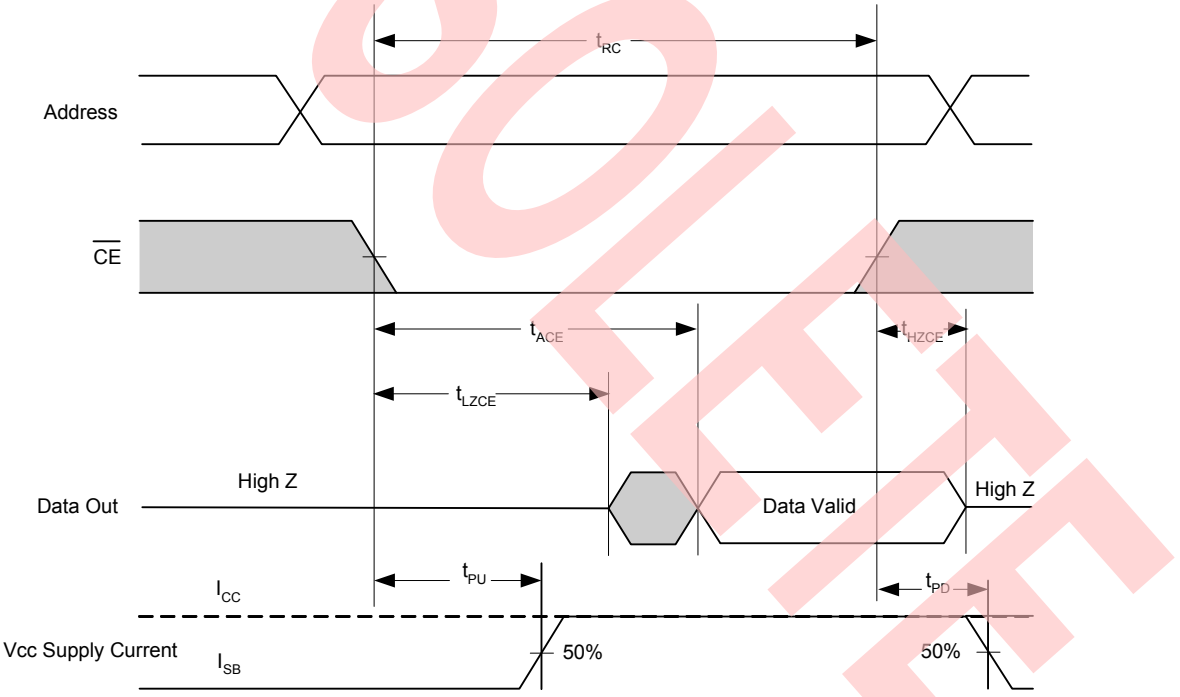


Figure 5. Read Cycle No. 2 [11, 12, 13]



Notes
10. Device is continuously selected. $\overline{CE} = V_{IL}$.
11. $\overline{WE}$ is HIGH in Read Cycle.
12. Tested initially and after any design or process change that may affect these parameters.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Timing Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [14, 15]

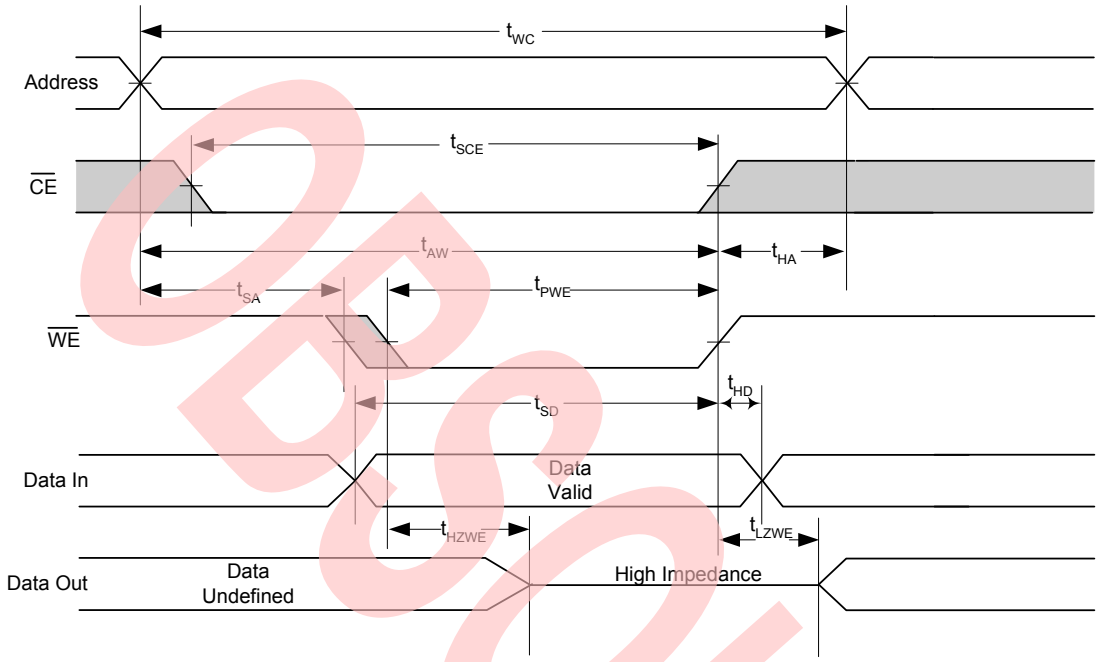
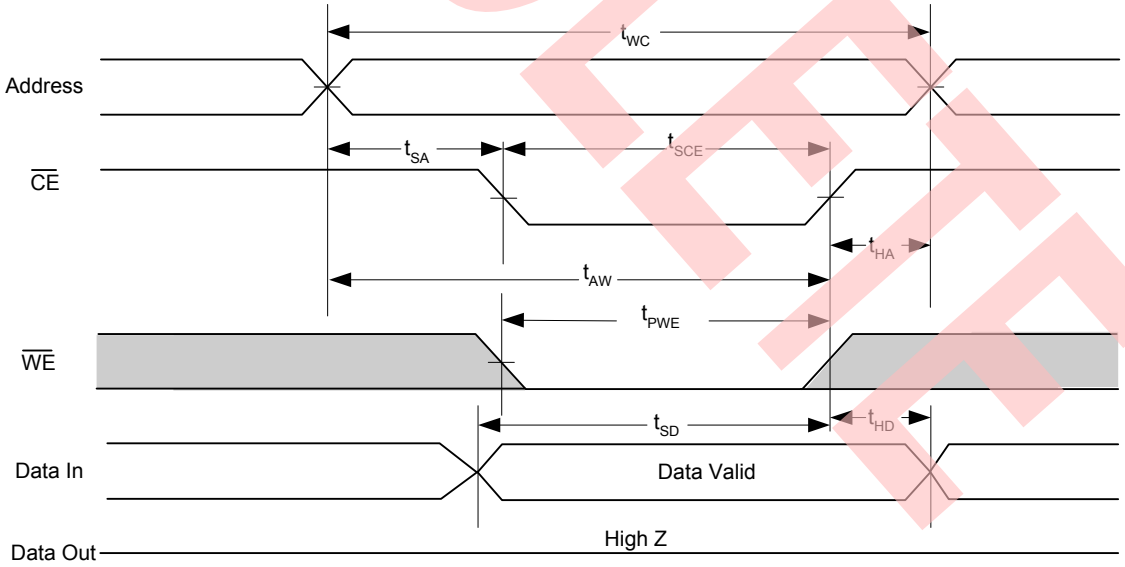


Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [16, 17]



Notes
14. Tested initially and after any design or process change that may affect these parameters.
15. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.
16. This cycle is $\overline{CE}$ controlled.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Truth Table

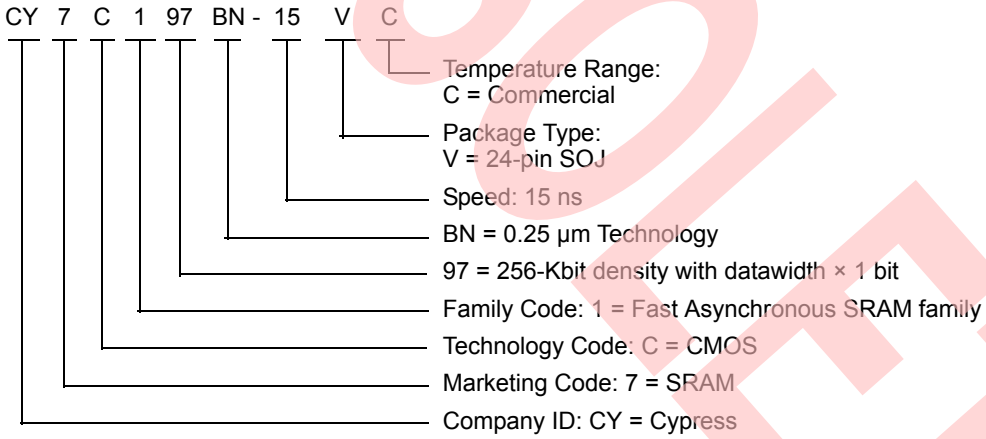
$\overline{CE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C197BN-15VC	51-85030	24-pin SOJ (8 × 15 × 3.5 mm)	Commercial

Please contact local sales representative regarding availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 8. 24-pin SOJ (300 Mils) V24.3/VZ24.3 (Molded SOJ V13) Package Outline, 51-85030

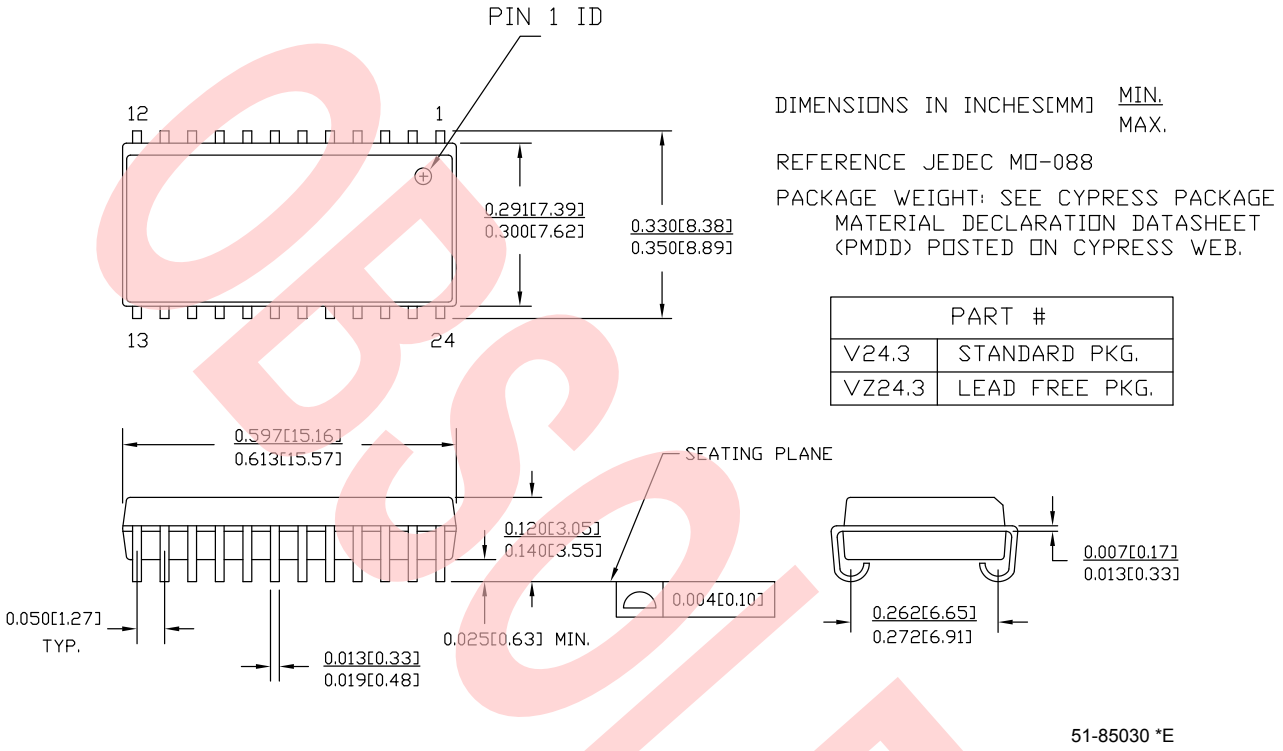
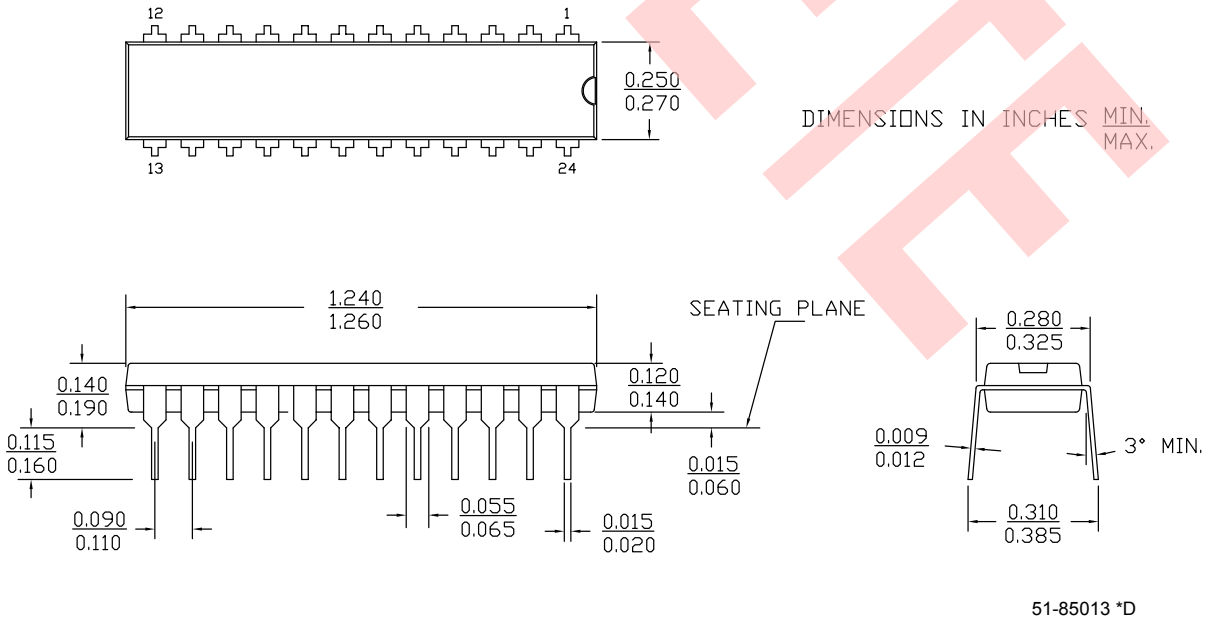


Figure 9. 24-pin PDIP (1.260 × .270 × .140 inches) P24.3 Package Outline, 51-85013



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
DIP	Dual In-line Package
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C197BN, 256-Kbit (256 K × 1) Static RAM Document Number: 001-06447				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	901742	See ECN	NXR	New data sheet.
*A	2892510	03/18/2010	VKN	Removed 12 ns speed bin information in all instances across the document. Updated Ordering Information. Updated Package Diagrams. Added Sales, Solutions, and Legal Information.
*B	3108898	12/13/2010	AJU	Added Ordering Code Definitions.
*C	3217480	04/06/2011	PRAS	Added Acronyms and Units of Measure. Updated in new template.
*D	3841481	12/14/2012	TAVA	Updated Ordering Information (Updated part numbers). Updated Package Diagrams (spec 51-85030 (Changed revision from *C to *E), spec 51-85013 (Changed revision from *C to *D)).
*E	4336876	04/08/2014	VINI	Updated in new template. Completing Sunset Review.
*F	4748562	04/30/2015	VINI	Obsolete document. Completing Sunset Review.

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