CY7C342
CY7C345

CYPRESS SEMICONDUCTOR

128-Macrocell MAX™ EPLDs

Features

CY7C342

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **Available in 68-pin HLCC, PLCC, and PGA**

CY7C345

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 28 bidirectional I/O pins**
- **256 expander product terms**
- **Programmable interconnect array**
- **Available in 44-pin HLCC or PLCC**

Functional Description

The CY7C342 and CY7C345 are Erasable Programmable Logic Devices (EPLDs) in which CMOS EPROM cells are used to configure logic functions within the devices. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342 are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342 allows it to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multi-function chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342 allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342 reduces board space, part count, and increases system reliability.

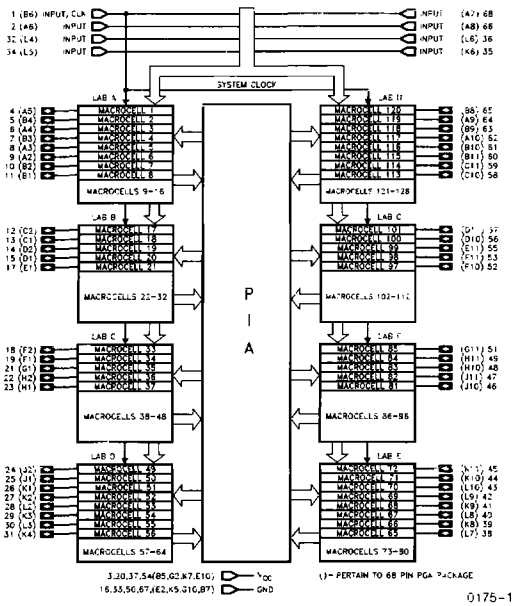
The CY7C345 packs the same LSI density of the CY7C342 into a smaller, 40-pin DIP or 44-pin HLCC package. Designed for applications in which large amounts of logic must be packed into a very small area, the CY7C345 is ideally suited for applications which require large amounts of buried logic.

It has the same number of macrocells and expanders as the CY7C342, and a programmable interconnect array to allow communications between the LABs. Each LAB has an I/O block, with LABs A, D, E and H having four bidirectional tri-stateable I/O pins, and the rest having three I/O pins. Like all other EPLDs in the MAX family, these I/O pins support dual feedback. In this way any macrocells may be buried, with only the output of macrocells needed off-chip connected to I/O pins.

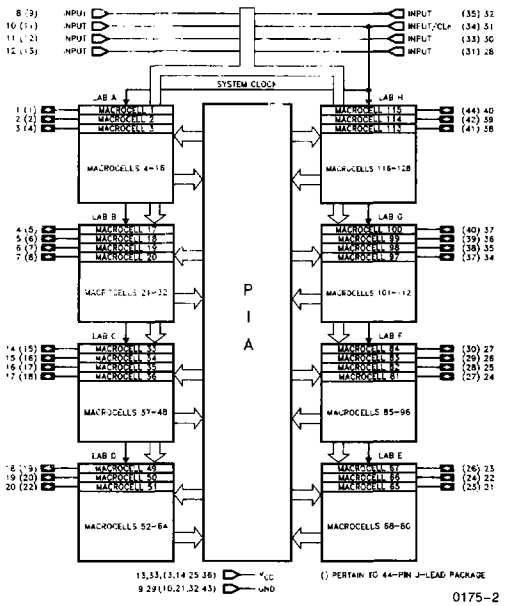
4

Logic Block Diagrams

CY7C342



CY7C345

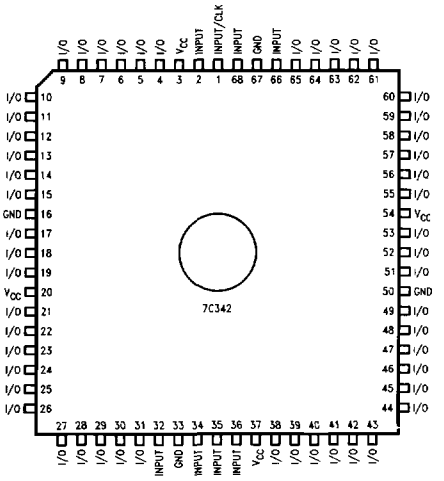


MAX and MAX+PLUS are trademarks of Altera Corporation.

Selection Guide

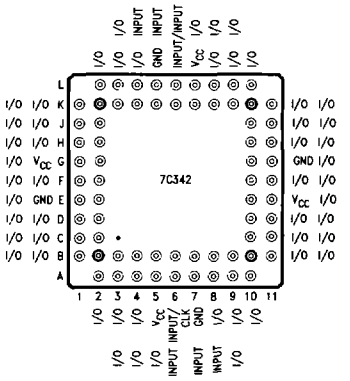
		7C342-30 7C345-30	7C342-35 7C345-35	7C342-40 7C345-40
Maximum Access Time (ns)		30	35	40
Maximum Operating Current (mA)	Commercial	310	310	
	Military		320	320
Maximum Standby Current (mA)	Commercial	200	200	
	Military		240	240

Pin Configurations

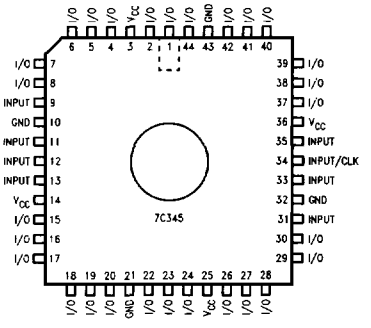


0175-3

PGA
Bottom View



0175-4



0175-6

Logic Array Blocks

There are eight logic array blocks in the CY7C342 and CY7C345. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342 provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins which may be individually configured for input, output, or bidirectional data flow.

The CY7C345 is internally identical to the CY7C342, but is packaged in a 40-pin DIP or 44-pin J-lead package. It has 8 dedicated inputs, and pin #31 may be used as a system clock. There are 28 I/O pins which may be individually configured for input, output, or bidirectional flow.

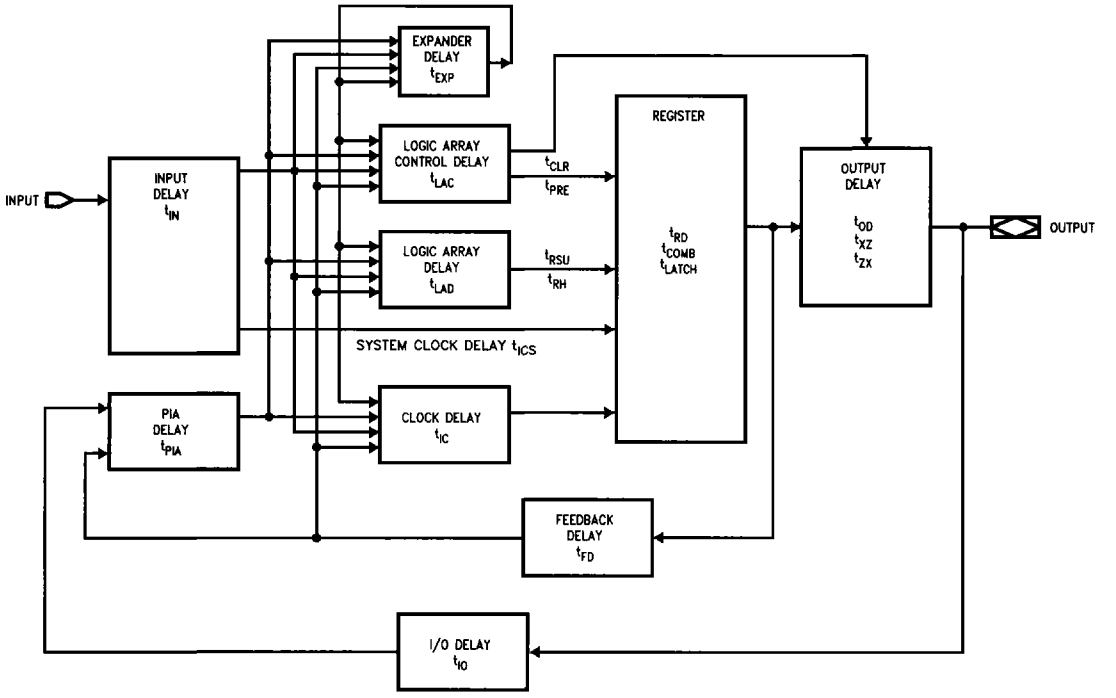


Figure 3. CY7C342/CY7C345 Internal Timing Model

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342 and CY7C345 may be easily determined using MAX + PLUS™ software or by the model shown in *Figure 3*. The CY7C342 and CY7C345 have fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX + PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342 and CY7C345 contain circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND $\leq$ (V_{IN} or V_{OUT}) $\leq$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

4

Design Security

The CY7C342 and CY7C345 contain a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a propriety design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

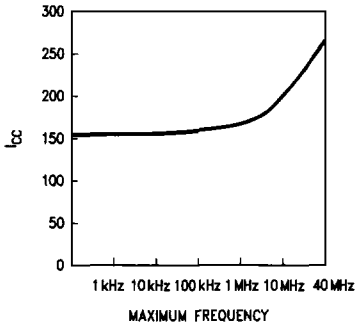


Figure 4. I_{CC} vs f_{MAX}

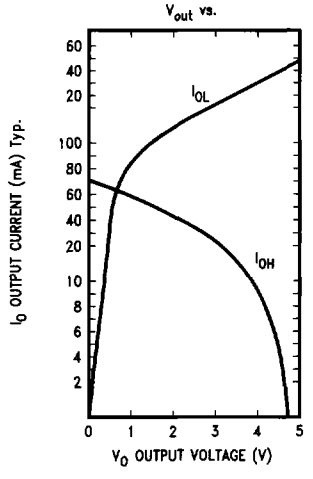


Figure 5. Output Drive Current

The CY7C342 and CY7C345 are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S_1} if all inputs are on dedicated input pins. The parameter t_{S_2} should be used if data is applied at an I/O pin. If t_{S_2} is greater than t_{CO_1}, $1/t_{S_2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S_2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S_1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO_1}$, or $1/(t_{EXP} + t_{S_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS_1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS_2} must be used as the required set up time. If $(t_{AS_2} + t_{AH})$ is greater than t_{ACO_1}, $1/(t_{AS_2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS_2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS_1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO_1}$, or $1/(t_{EXP} + t_{AS_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C342.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential .... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −2.0V to +7.0V

DC Program Voltage..... −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−30	−90	mA
I_{CC_1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		200	mA
			Military		240	mA
I_{CC_2}	Power Supply Current[3]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[3]	Commercial		310	mA
			Military		320	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	12	

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. This parameter is measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.
4. *Figure 1a* test load used for all parameters except t_{ER} and t_{EA}. *Figure 1b* test load used for t_{ER} and t_{EA}. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[4]

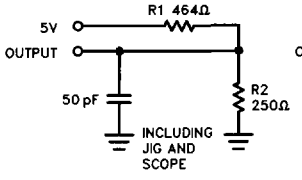
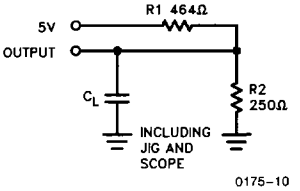


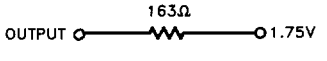
Figure 1a



0175-10

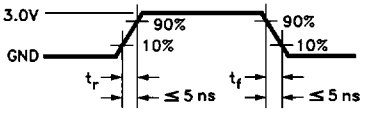
Figure 1b

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



0175-12

Input Pulses



0175-11

Figure 2

External Synchronous Switching Characteristics[4] Over Operating Range

Parameters	Description		CY7C342-30 CY7C345-30		CY7C342-35 CY7C345-35		CY7C342-40 CY7C345-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_1}	Dedicated Input to Combinatorial Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PD_2}	I/O Input to Combinatorial Output Delay[6]	Com'l		45		55			ns
		Mil				55		65	
t_{PD_3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[7]	Com'l		44		55			ns
		Mil				55		65	
t_{PD_4}	I/O Input to Combinatorial Output Delay with Expander Delay[8]	Com'l		60		75			ns
		Mil				75		90	
t_{EA}	Input to Output Enable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{ER}	Input to Output Disable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CO_1}	Synchronous Clock Input to Output Delay	Com'l		16		20			ns
		Mil				20		23	
t_{CO_2}	Synchronous Clock to Local Feedback to Combinatorial Output[9]	Com'l		35		42			ns
		Mil				42		50	
t_{S_1}	Dedicated Input or Feedback Setup Time to Synchronous Clock Input[5, 10]	Com'l	22		25				ns
		Mil			25		28		
t_{S_2}	I/O Input Setup Time to Synchronous Clock Input[5]	Com'l	39		45				ns
		Mil			45		52		
t_H	Input Hold Time from Synchronous Clock Input[5]	Com'l	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{RW}	Asynchronous Clear Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RR}	Asynchronous Clear Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PW}	Asynchronous Preset Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PR}	Asynchronous Preset Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PO}	Asynchronous Preset to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[11]	Com'l		3		6			ns
		Mil				6		9	
t_P	External Synchronous Clock Period ($t_{CO_1} + t_{S_1}$)	Com'l	38		45				ns
		Mil			45		51		

External Synchronous Switching Characteristics[4] Over Operating Range (Continued)

Parameters	Description		CY7C342-30 CY7C345-30		CY7C342-35 CY7C345-35		CY7C342-40 CY7C345-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_1}	External Feedback Maximum Frequency $(1/(t_{CO_1} + t_{S_1}))$[12]	Com'l	26.3		22.2				MHz
		Mil			22.2		19.6		
f_{MAX_2}	Internal Local Feedback Maximum Frequency, lesser of $1/(t_{S_1} + t_{CF})$ or $(1/t_{CO_1})$[13]	Com'l	40.0		32.2				MHz
		Mil			32.2		28.5		
f_{MAX_3}	Data Path Maximum Frequency, least of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S_1} + t_H))$ or $(1/t_{CO_1})$[14]	Com'l	45.4		40.0				MHz
		Mil			40.0		33.3		
f_{MAX_4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[15]	Com'l	50.0		40.0				MHz
		Mil			40.0		33.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[16]	Com'l	3		3				ns
		Mil			3		3		

Notes:

5. This specification is a measure of the delay from input signal applied to a dedicated input, (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
6. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
7. This specification is a measure of the delay from an input signal applied to a dedicated input, (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
8. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
9. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
10. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S_2} for synchronous operation and t_{AS_2} for asynchronous operation.
11. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S_1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
12. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
13. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO_1}$.
14. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S_2} is the appropriate t_S for calculation.
15. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
16. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

4

External Asynchronous Switching Characteristics[4] Over Operating Range

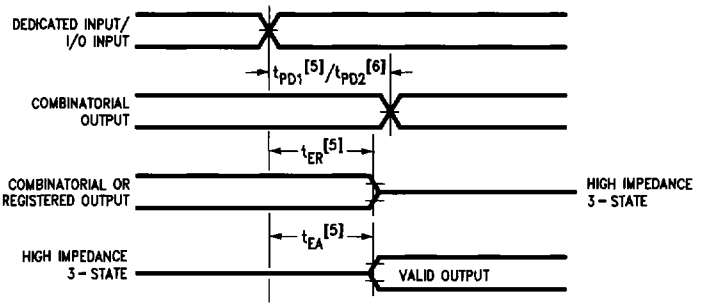
Parameters	Description		CY7C342-30 CY7C345-30		CY7C342-35 CY7C345-35		CY7C342-40 CY7C345-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO_1}	Asynchronous Clock Input to Output Delay[5]	Com'l		30		35			ns
		Mil				35		45	
t_{ACO_2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[17]	Com'l		46		55			ns
		Mil				55		64	
t_{AS_1}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input[5]	Com'l	10		10				ns
		Mil			10		10		
t_{AS_2}	I/O Input Setup Time to Asynchronous Clock Input[5]	Com'l	27		30				ns
		Mil			30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[5]	Com'l	15		15				ns
		Mil			15		15		
t_{AWH}	Asynchronous Clock Input High Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{AWL}	Asynchronous Clock Input Low Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{ACF}	Asynchronous Clock to Local Feedback Input[18]	Com'l		18		22			ns
		Mil				22		26	
t_{AP}	External Asynchronous Clock Period ($t_{ACO_1} + t_{AS_1}$) or ($t_{AWH} + t_{AWL}$)	Com'l	50		60				ns
		Mil			60		70		
f_{MAXA_1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[19]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_2}	Maximum Internal Asynchronous Frequency[22]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_3}	Data Path Maximum Frequency in Asynchronous Mode[21]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[20]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[23]	Com'l	15		15				ns
		Mil			15		15		

Notes:

17. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
18. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS_1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
19. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
20. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
21. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS_1} + t_{AH})$ or $1/t_{ACO_1}$. It asssumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO_1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
23. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

Switching Waveforms

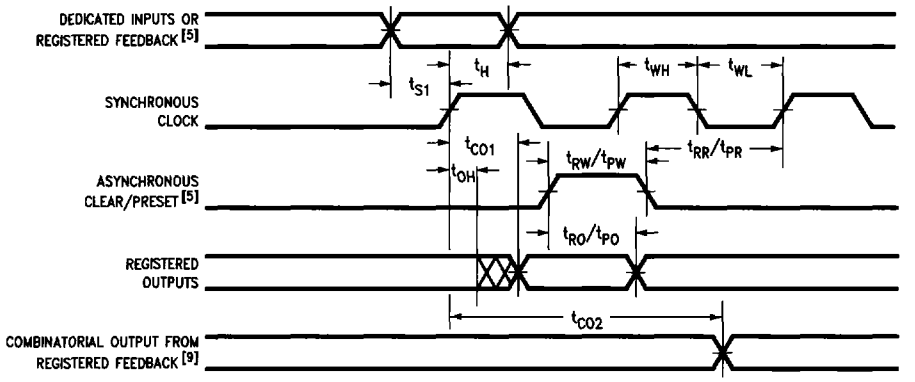
External Combinatorial



0175-13

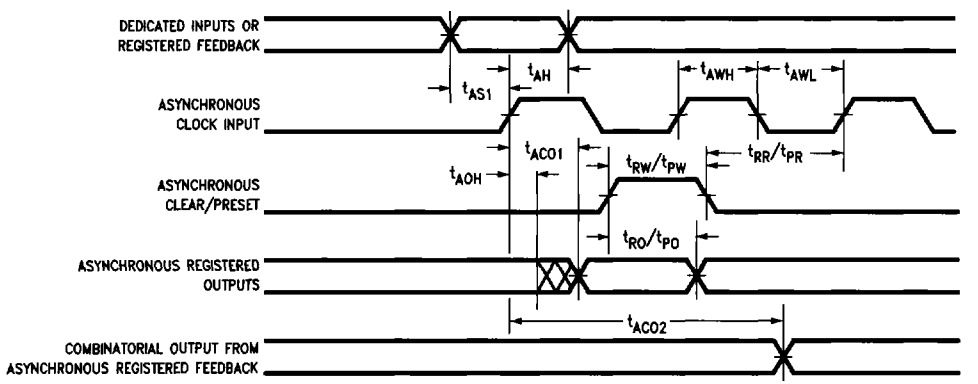
4

External Synchronous



0175-14

External Asynchronous



0175-15

Internal Switching Characteristics[1] Over Operating Range

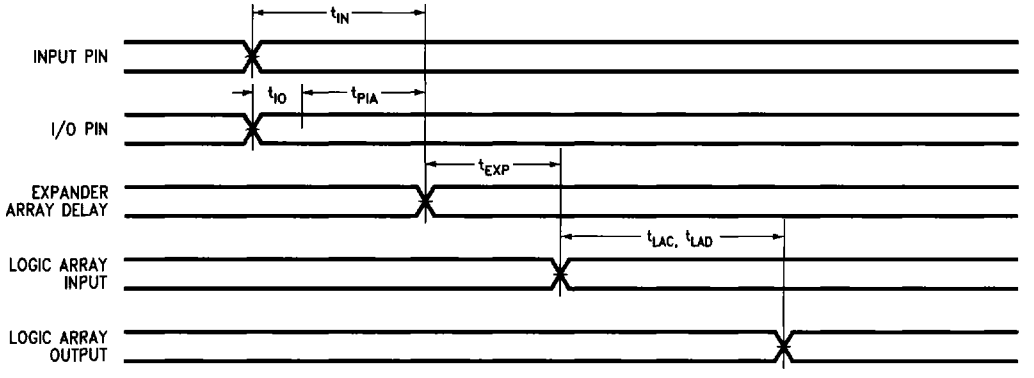
Parameters	Description		CY7C342-30 CY7C345-30		CY7C342-35 CY7C345-35		CY7C342-40 CY7C345-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		7		9			ns
		Mil				9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		6		9			ns
		Mil				9		12	
t_{EXP}	Expander Array Delay	Com'l		14		20			ns
		Mil				20		25	
t_{LAD}	Logic Array Data Delay	Com'l		14		16			ns
		Mil				16		18	
t_{LAC}	Logic Array Control Delay	Com'l		12		13			ns
		Mil				13		14	
t_{OD}	Output Buffer and Pad Delay[24]	Com'l		5		6			ns
		Mil				6		7	
t_{ZX}	Output Buffer Enable Delay[25]	Com'l		11		13			ns
		Mil				13		15	
t_{XZ}	Output Buffer Disable Delay[26]	Com'l		11		13			ns
		Mil				13		15	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil			10		12		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil			10		12		
t_{LATCH}	Flow Through Latch Delay	Com'l		4		4			ns
		Mil				4		4	
t_{RD}	Register Delay	Com'l		2		2			ns
		Mil				2		2	
t_{COMB}	Transparent Mode Delay[27]	Com'l		4		4			ns
		Mil				4		4	
t_{CH}	Clock High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{CL}	Clock Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		16		18			ns
		Mil				18		20	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil				3		4	
t_{FD}	Feedback Delay	Com'l		1		2			ns
		Mil				2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		7			ns
		Mil				7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		7			ns
		Mil				7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil			7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil			7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		16		20			ns
		Mil				20		24	

Notes:

24. t_{OD} is specified with C_L = 35 pF.
25. t_{ZX} is specified with C_L = 35 pF. Sample tested only for an output change of 500 mV.
26. t_{XZ} is specified with C_L = 5 pF.
27. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

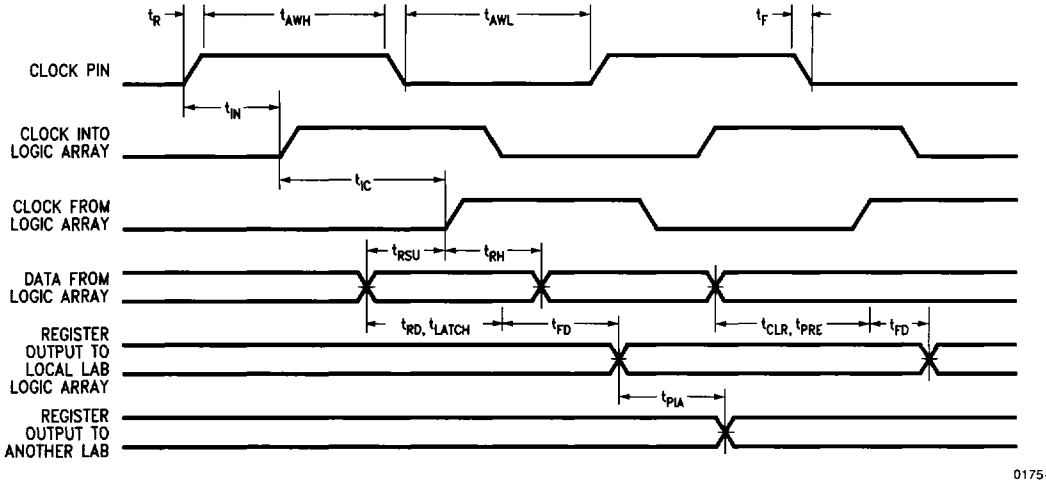
Switching Waveforms (Continued)

Internal Combinatorial



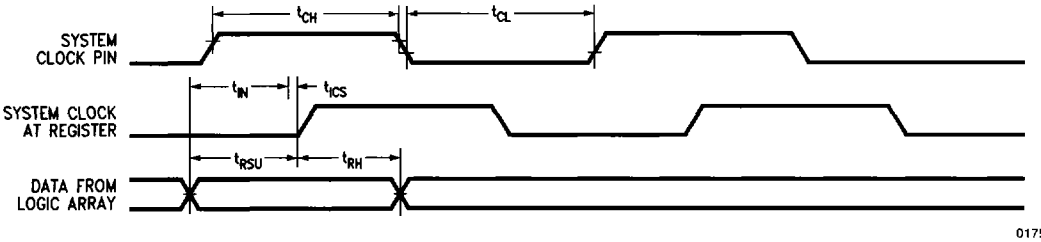
0175-16

Internal Asynchronous



0175-17

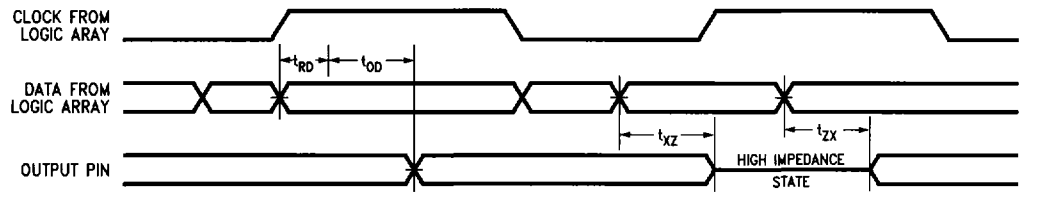
Internal Synchronous



0175-18

Switching Waveforms (Continued)

Internal Synchronous



0175-19

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C342-30HC	H81	Commercial
	CY7C342-30JC	J81	
	CY7C342-30RC	R68	
	CY7C342-30GC	G68	
35	CY7C342-35HC	H81	Commercial
	CY7C342-35JC	J81	
	CY7C342-35RC	R68	
	CY7C342-35GC	G68	
	CY7C342-35HMB	H81	Military
	CY7C342-35RMB	R68	
40	CY7C342-40HC	H81	Commercial
	CY7C342-40JC	J81	
	CY7C342-40RC	R68	
	CY7C342-40GC	G68	
	CY7C342-40HMB	H81	Military
	CY7C342-40RMB	R68	

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C345-30HC	H67	Commercial
	CY7C345-30JC	J67	
35	CY7C345-35HC	H67	Commercial
	CY7C345-35JC	J67	
	CY7C345-35HMB	H67	Military
40	CY7C345-40HC	H67	Commercial
	CY7C345-40JC	J67	
	CY7C345-40HMB	H67	Military