This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CY7C615

CYPRESS SEMICONDUCTOR

Interrupt Controller

Features

- Fifteen interrupt request levels for SPARC-based system design
- Levels one through fourteen individually maskable
- Level fifteen SPARC non-maskable interrupt
- Two built-in 32-bit counters clocked by dedicated reference clock input
- Built-in soft-reset register
- Built-in four-bit register designed to drive diagnostic LEDs
- Built-in 4-bit auxiliary I/O port

Introduction

The interrupt/timer chip implements the system-level interrupt logic for SPARC-based system designs. This chip handles the 15 SPARC interrupt levels. There is a mask register to individually enable or disable levels 1 through 14. Level 15, the SPARC non-maskable interrupt (NMI), is not affected by the mask. The chip synchronizes incoming hardware interrupts and generates a 4-bit interrupt level signal, indicating the highest-priority interrupt pending.

This chip contains two 32-bit counters clocked by a dedicated reference clock input. These counters can be used to generate clock interrupts for timekeeping and system profiling. A limit register associated with each counter specifies the interval, in reference clock cycles, between timer interrupts. There is also a soft-reset register and a 4-bit register designed to drive diagnostic LEDs. The CY7C615 is implemented in a standard 100-pin PQFP package.

Addressing

The interrupt/timer chip registers are accessed through byte-wide read and write operations. Three active LOW control lines—Chip Select ($\overline{CS}$), Read ($\overline{RD}$), and Write ($\overline{WR}$)—are used for register transfers. When writing 32-bit limit registers, accesses to bytes 0, 1, and 2 write to a holding register, and the 32-bit value is clocked into the desired register on the byte 3 access. When reading from 32-bit timer register, the byte 0 access clocks the full 32-bit value into an output register, and accesses to bytes 1, 2, and 3 read from this output register. The chip is commonly accessed through the CY7C614 M2SX interface chip, which transparently packs and unpacks MBus word and halfword transfers to SXBus byte accesses.

Logic Block Diagram