This is an abbreviated datasheet. Contact a Cypress representative for complete specifications.

CYPRESS SEMICONDUCTOR

CY7C616

MBus to SBus Interface Controller

Features

- MBus to SBus Interface (32-bit slice)
- Allows MBus byte, halfword, word, and doubleword transactions
- Allows SBus byte, halfword, and word transfers
- Contains SBus controller with the following features:
  - Arbitration for four SBus masters
  - Geographical selects for four SBus slaves (=slots)
  - Eight-entry fully associative TLB, with LRU replacement
  - Lockable TLB entries
  - Eight types of TLB flushing operations
  - 32-Mbyte address space for each SBus slot
  - Address translation enable/disable for each SBus slot
- Readable error register for debugging
- 40-MHz MBus operating frequency
- 25-MHz SBus operating frequency

Introduction

The CY7C616 contains the logic that connects the 64-bit MBus to the 32-bit SBus. This interface can behave as both a master or slave on either MBus or SBus. For transactions going from MBus to SBus, the CY7C616 is an MBus slave for an MBus master like the CPU. After receiving the transaction, the CY7C616 then becomes an SBus master and initiates a transfer to the targeted SBus slave. For transfers going from SBus to MBus, the CY7C616 is an SBus slave for an SBus master like a DVMA master. After receiving the transfer, the CY7C616 then becomes an MBus master and initiates a transaction to the targeted MBus slave.

Since MBus and SBus have different bus data widths, data buffers are needed to provide temporary storage while data is being packed or unpacked. There are two sets of 8-byte buffers, one for data transfers from MBus to SBus and the other for data transfers from SBus to MBus. This allows the CY7C616 to handle byte, halfword, word, and doubleword transfers on MBus and byte, halfword, and word transfers on SBus.

MBus and SBus may be running at different clock frequencies. MBus will be typically be running at 33 or 40 MHz while SBus has to run between 16.67 and 25 MHz. In order to keep both buses synchronized, the SBus clock will be at the same frequency as the MBus clock for clock frequencies of 25 MHz or less and at half of the MBus clock frequency for frequencies greater than 25 MHz.

The CY7C616 also contains the logic for an SBus controller. The SBus controller can arbitrate between four SBus masters, one being the M2S logic and the other three being external SBus masters. It supports geographically selecting four SBus slaves, one being the M2S logic, the other three being external SBus slots. Virtual-to-physical address translation is done through an eight-entry fully associative TLB with a Least Recently Used (LRU) replacement policy. The TLBs provide translation for a 32-MByte address space for each SBus slot. A pass-through mode is also provided so that the virtual address can be passed directly to the physical address.

Logic Block Diagram