This is an abbreviated datasheet.
Contact a Cypress representative
for complete specifications.

CY7C617

CYPRESS SEMICONDUCTOR

Mbus-to-Video Graphics Controller

Features

- Programmable shift register size and video transfer window size for performance
- Two-deep posting on MBus writes
- Compatible to Sun Microsystems' 1152 x 900 color or mono display systems
- Interfaces MBus to RAMDAC (Bt458) and VRAMs
- Supports 256-word color palette
- Programmable VSYNC, HSYNC, and BLANK signals for the CRT control
- Generates interrupt every 600 ms if enabled, for color palette updates

Introduction

The CY7C617 CRT controller is an MBus device used for displaying bitmapped graphics on raster scan CRT displays. The CRT controller provides a simple slave interface on the MBus providing a data path for read/write transactions to the VRAM array and the RAMDAC. The controller does not provide any support for MBus transactions. The MBus transaction sizes supported are:

- —bytes read/write
- —halfwords read/write
- —words read/write
- —doubleword read/write

If an unknown transaction type or size is encountered on the MBus, an ERROR is generated by activating the line $\overline{AERR}$. Typically, in a system this signal could be tied to an interrupt line to inform the processor of the failure. If a master issues an MBus address that is out of the controller's scope, it does nothing and lets the MBus time itself out. This could be a mechanism to size the controller's memory space.

The CY7C617 is fully user programmable. The timing of the CRT control signals such as HSYNC, VSYNC, and BLANK are controlled by a set of internal registers. These registers should be initialized at the boot-up time by the host processor for the controller to function properly. The controller also handles the serial data transfer from RAM to SAM and the memory refresh operations. The memory refresh is done by using the CAS before RAS refresh scheme. A definition of these registers and their functions are in the External Registers and Internal Registers sections.

The CY7C617 comes in a 208-pin package. Apart from the CY7C617, a designer needs only VRAMs, RAMDAC, crystal oscillator and a clock generator IC (for instance, see Brooktree part Bt438) to build a high-performance, Sun-compatible video system.

Logic Block Diagram