



# CYPRESS

## CY7C68300B/CY7C68301B CY7C68320/CY7C68321

### EZ-USB AT2LP™ USB 2.0 to ATA/ATAPI Bridge

#### 1.0 Features (CY7C68300B/CY7C68301B and CY7C68320/CY7C68321)

- Fixed-function mass storage device—requires no firmware code
- Two power modes: Self-powered and USB bus-powered to enable bus powered CF readers and truly portable USB hard drives
- Certified compliant for USB 2.0 (TID# 40460273), the USB Mass Storage Class, and the USB Mass Storage Class Bulk-Only Transport (BOT) Specification
- Operates at high (480-Mbps) or full (12-Mbps) speed USB
- Complies with ATA/ATAPI-6 specification
- Supports 48-bit addressing for large hard drives
- Supports ATA security features
- Supports all ATA commands via ATACB function
- Supports mode page 5 for BIOS boot support
- Supports ATAPI serial number VPD page retrieval for Digital Rights Management (DRM) compatibility
- Supports PIO modes 0, 3, 4, multiword DMA mode 2, and UDMA modes 2, 3, 4
- Uses one external serial EEPROM for storage of USB descriptors and device configuration data
- ATA interface IRQ signal support
- Support for one or two ATA/ATAPI devices

- Support for CompactFlash and one ATA/ATAPI device
- Can place the ATA interface in high-impedance (Hi-Z) to allow sharing of the ATA bus with another controller (e.g., an IEEE-1394 to ATA bridge chip or MP3 Decoder)
- Support for board-level manufacturing test via USB interface
- Low-power 3.3V operation
- Fully compatible with native USB mass storage class drivers
- Cypress mass storage class drivers available for Windows (98SE, ME, 2000, XP) and Mac OS X

#### 1.1 Features (CY7C68320/CY7C68321 only)

- Supports HID interface or custom GPIOs to enable features such as single button backup, power-off, LED-based notification, etc.
- Lead-free 56-pin QFN and 100-pin TQFP packages
- CY7C68321 is ideal for battery-powered designs
- CY7C68320 is ideal for self- and bus-powered designs

#### 1.2 Features (CY7C68300B/CY7C68301B only)

- Pin-compatible with CY7C68300A (using Backward Compatibility mode)
- Lead-free 56-pin SSOP and 56-pin QFN packages
- CY7C68301B is ideal for battery-powered designs
- CY7C68300B is ideal for self- and bus-powered designs

#### 2.0 Block Diagram

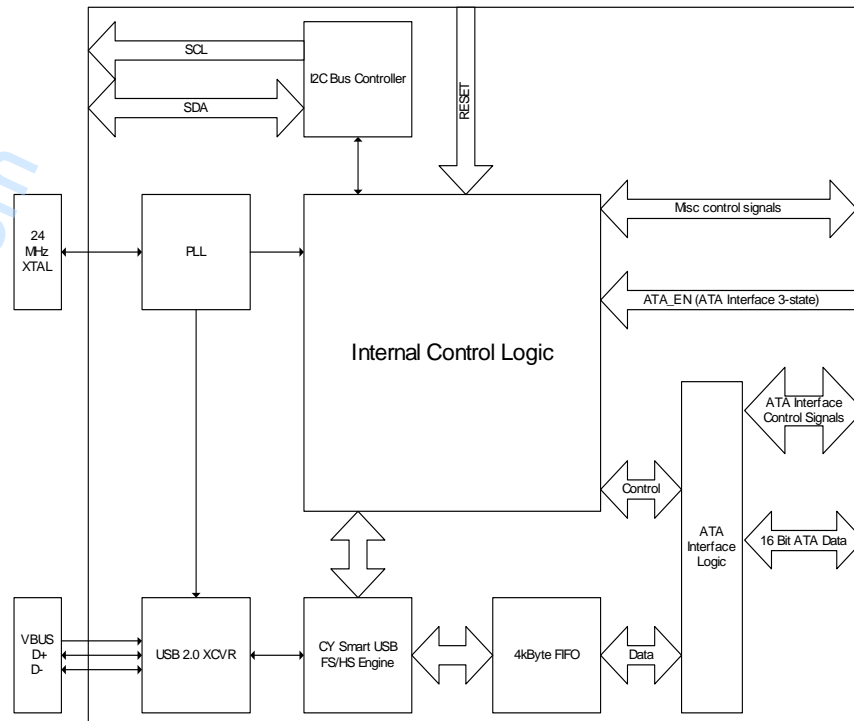


Figure 2-1. Block Diagram





### 3.0 Applications

The CY7C68300B/301B and CY7C68320/321 implement a USB 2.0 bridge for all ATA/ATAPI-6 compliant mass storage devices, such as the following.

- Hard drives
- CD-ROM, CD-R/W
- DVD-ROM, DVD-RAM, DVD+/-R/W
- MP3 players
- Personal media players
- CompactFlash
- Microdrives
- Tape drives
- Personal video recorders

The CY7C68300B/301B and CY7C68320/321 support one or two devices in the following configurations.

- ATA/ATAPI master only
- ATA/ATAPI slave only
- ATA/ATAPI master and slave
- CompactFlash only
- ATA/ATAPI slave and CompactFlash or other removable IDE master

### 3.1 Additional Resources

- CY4615B EZ-USB AT2LP Reference Design Kit
- *USB Specification* version 2.0
- *ATA Specification* T13/1410D Rev 3B
- *USB Mass Storage Class Bulk Only Transport Specification*, [www.usb.org](http://www.usb.org)

### 4.0 Introduction

The EZ-USB AT2LP™ (CY7C68300B/CY7C68301B and CY7C68320/CY7C68321) implements a fixed function bridge between one USB port and one or two ATA- or ATAPI-based

mass storage device ports. This bridge adheres to the *Mass Storage Class Bulk-Only Transport Specification* and is intended for bus- and self-powered devices.

The AT2LP is the latest addition to the Cypress USB mass storage portfolio, and is an ideal cost- and power-reduction path for designs that previously used the ISD-300A1, ISD-300LP, or EZ-USB AT2.

**Specifically, the CY7C68300B/CY7C68301B includes a mode that makes it pin-for-pin compatible with the EZ-USB AT2 (CY7C68300A).**

The USB port of the CY7C68300B/301B and CY7C68320/321 (AT2LP) are connected to a host computer directly or via the downstream port of a USB hub. Host software issues commands and data to the AT2LP and receives status and data from the AT2LP using standard USB protocol.

The ATA/ATAPI port of the AT2LP is connected to one or two mass storage devices. A 4-Kbyte buffer maximizes ATA/ATAPI data transfer rates by minimizing losses due to device seek times. The ATA interface supports ATA PIO modes 0, 3, and 4, multiword DMA mode 2 and Ultra DMA modes 2, 3, and 4.

The device initialization process is configurable, enabling the AT2LP to initialize ATA/ATAPI devices without software intervention.

### 5.0 68300A Compatibility

The CY7C68300B/301B and CY7C68320/321 are available in three package types that are pictured in the following sections. As mentioned above, the CY7C68300B/301B contains a backward compatibility mode that allows the CY7C68300B/301B to be used in existing EZ-USB AT2 (CY7C68300A) designs. Please refer to the logic flow below for more information on the pinout selection process.

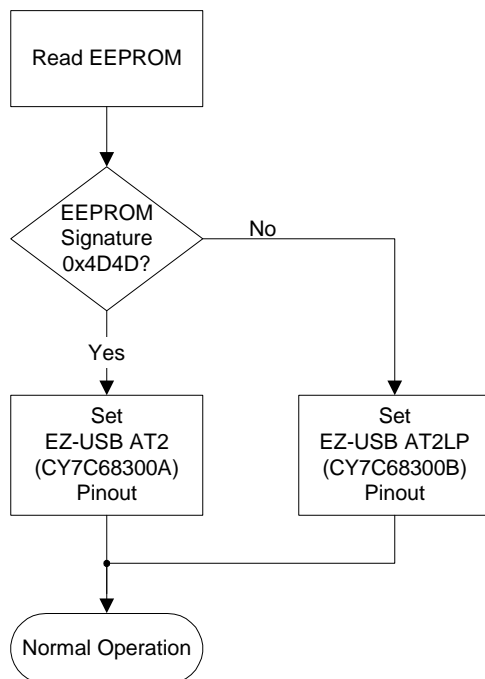


Figure 5-1. Simplified Startup Flowchart (68300B only)

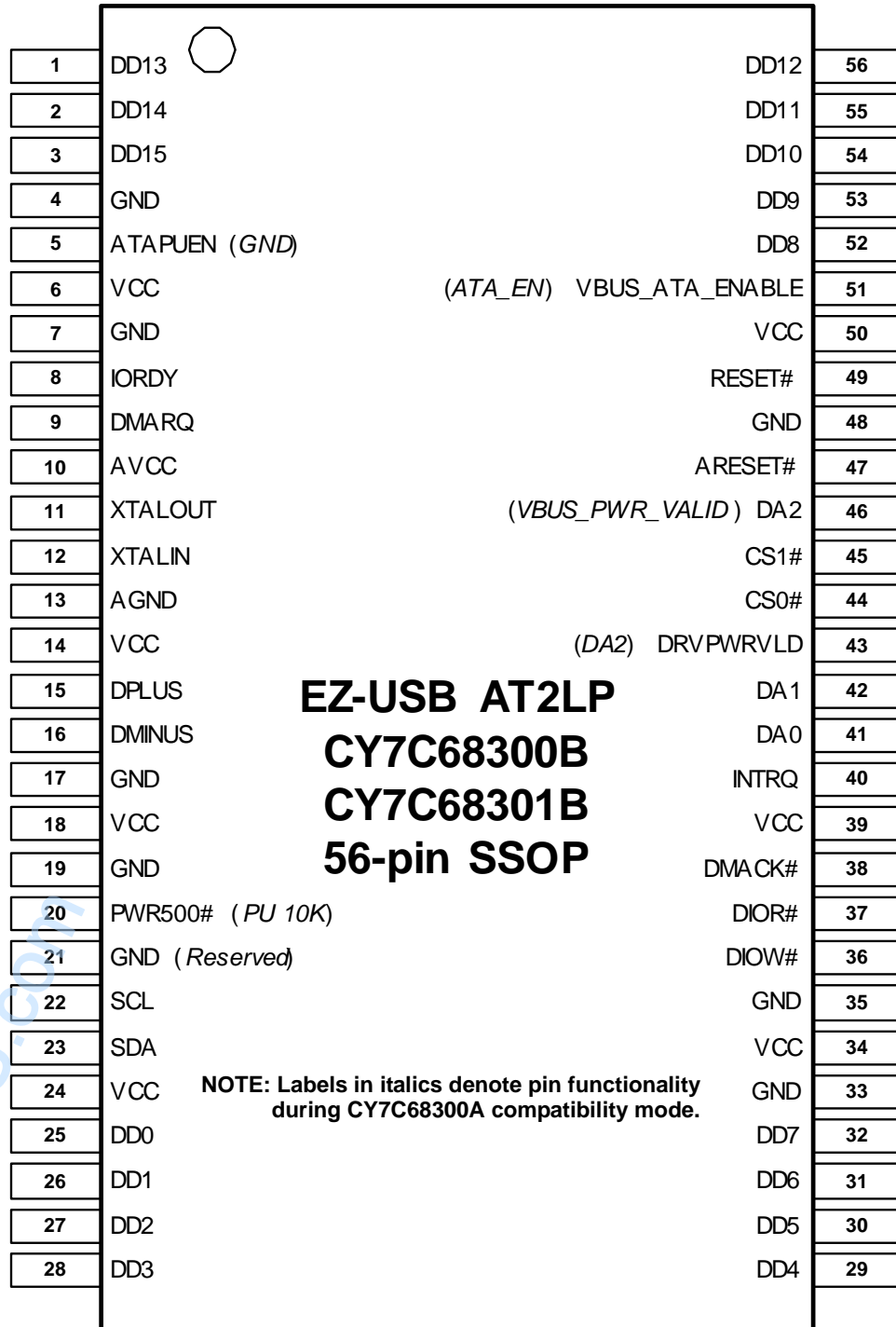

**5.1 Pin Diagrams**


Figure 5-2. 56-pin SSOP Pinout (CY7C68300B/CY7C68301B only)

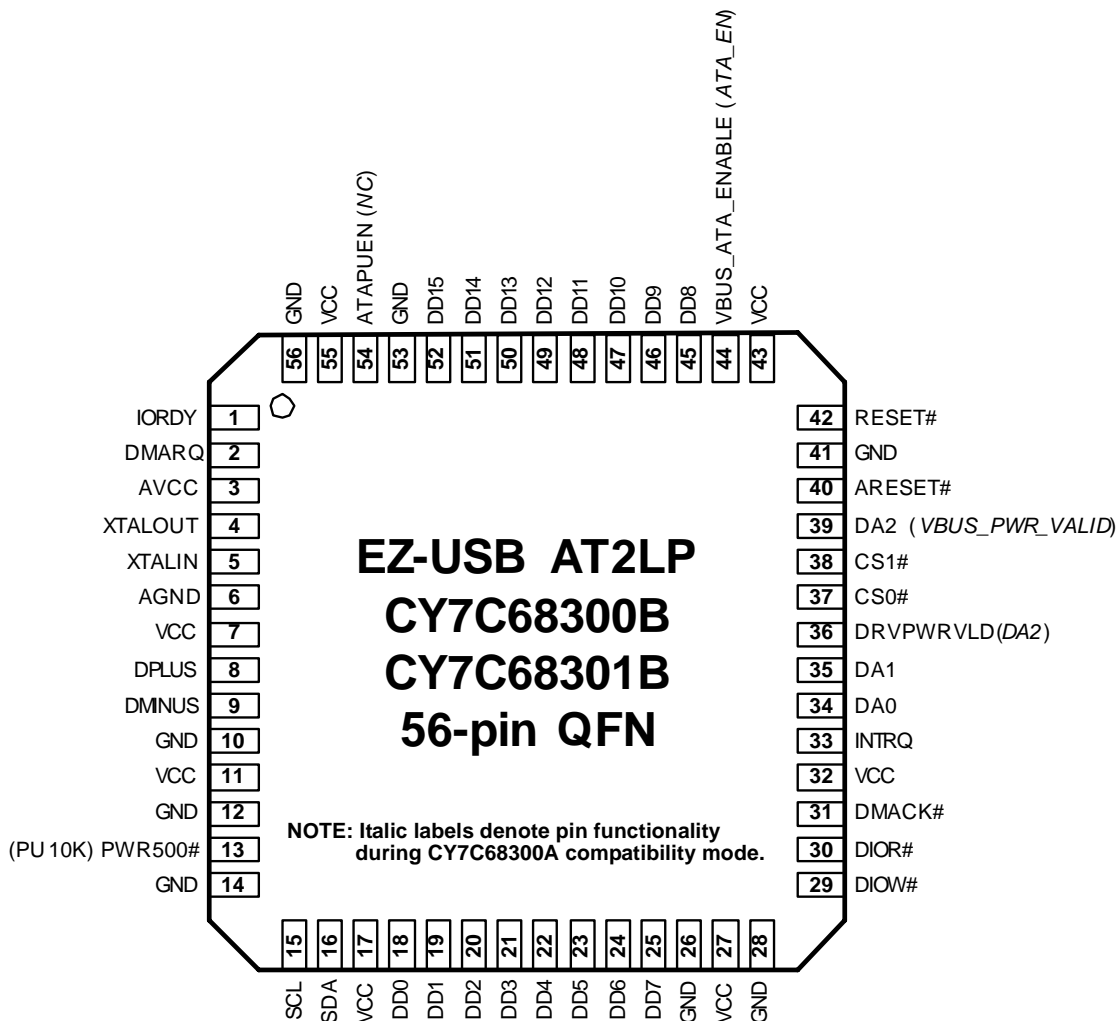


Figure 5-3. 56-pin QFN Pinout (CY7C68300B/CY7C68301B)

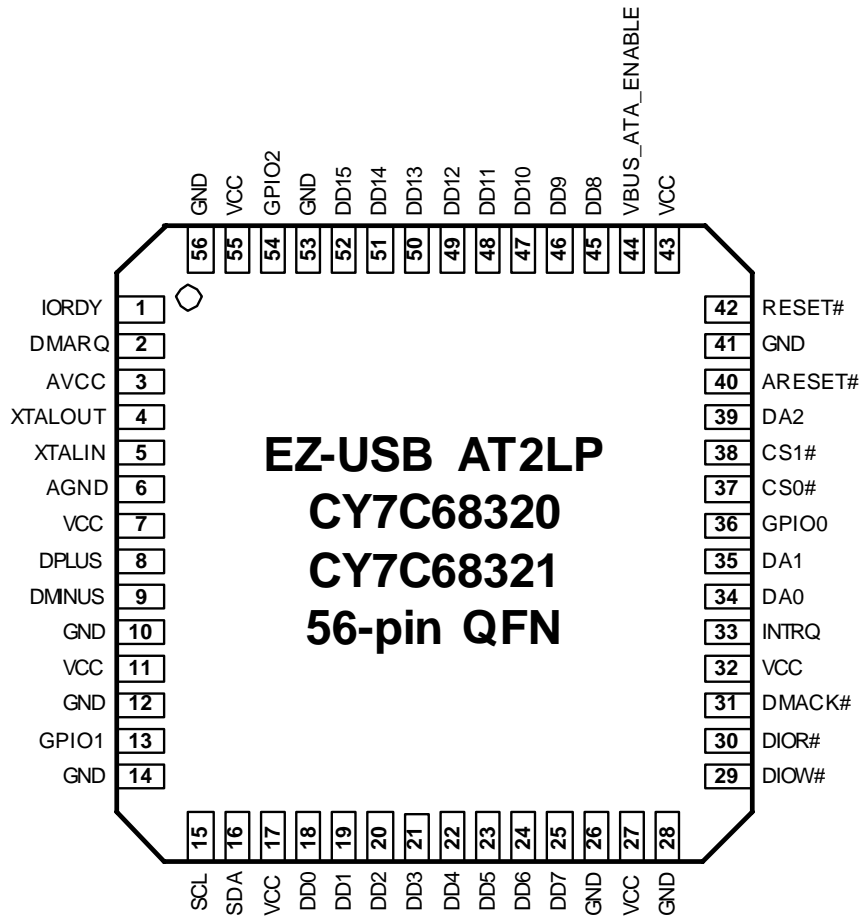


Figure 5-4. 56-pin QFN Pinout (CY7C68320/CY7C68321)

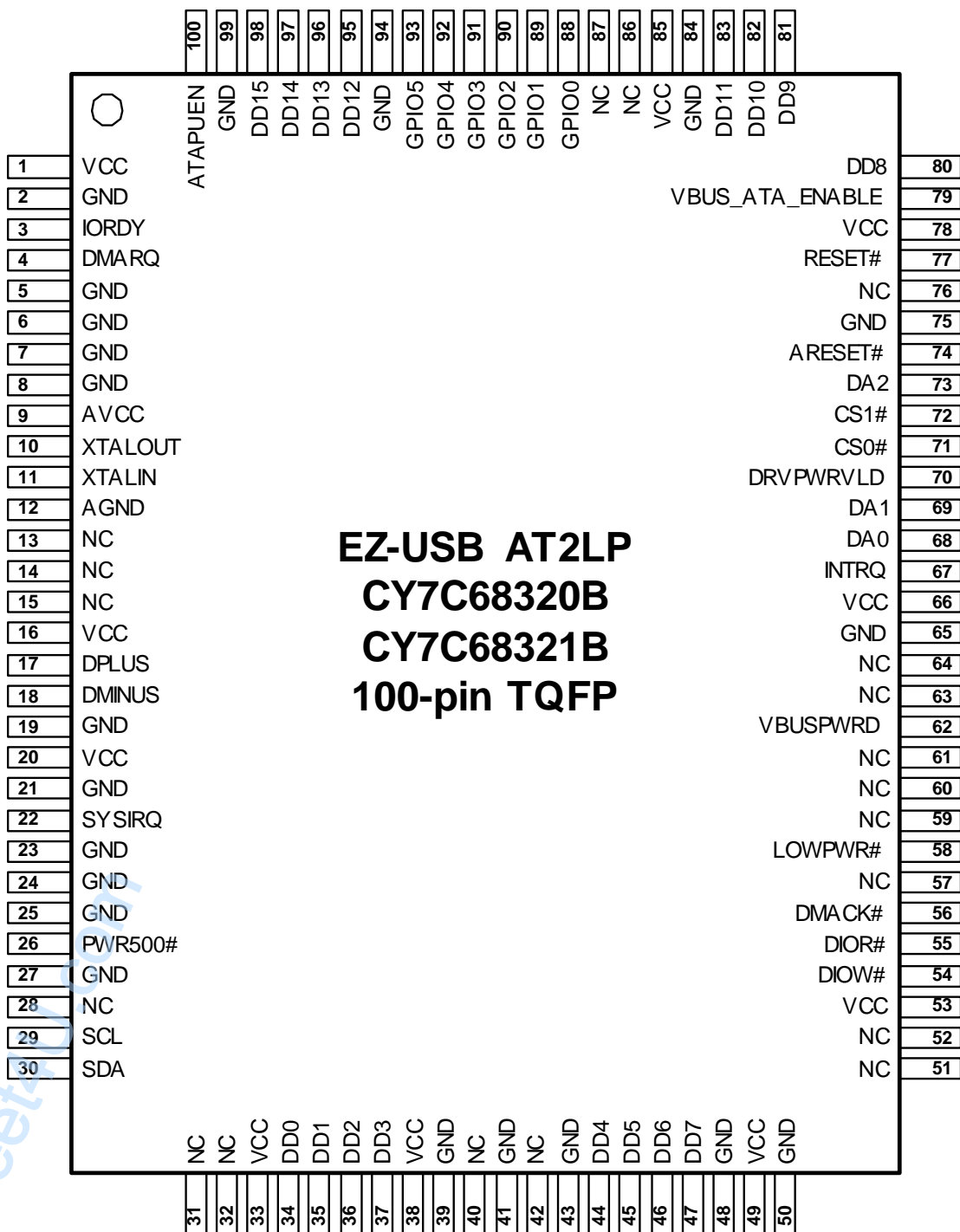


Figure 5-5. 100-pin TQFP Pinout (CY7C68320/CY7C68321 only)



## 5.2 Pin Descriptions

The following table lists the pinouts for the 56-pin SSOP, 56-pin QFN and 100-pin TQFP package options for the AT2LP. Please refer to the Pin Diagrams in section 5.1 for differences

between the 68300B/01B and 68320/321 pinouts for the 56-pin packages. For information on the CY7C68300A pinout, please refer to the CY7C68300A data sheet that is found in the "EZ-USB AT2" folder of the CY4615B reference design kit CD.

**Table 5-1. AT2LP Pin Descriptions**

**Note: (Italics pin names denote pin functionality during CY7C68300A-compatibility mode)**

| 56 SSOP | 56 QFN            | 100 TQFP           | Pin Name                           | Pin Type           | Default State at Start-up | Pin Description   |
|---------|-------------------|--------------------|------------------------------------|--------------------|---------------------------|---|
| 1       | 50                | 96                 | DD13                               | I/O <sup>[1]</sup> | Hi-Z                      | <b>ATA Data bit 13.</b>   |
| 2       | 51                | 97                 | DD14                               | I/O <sup>[1]</sup> | Hi-Z                      | <b>ATA Data bit 14.</b>   |
| 3       | 52                | 98                 | DD15                               | I/O <sup>[1]</sup> | Hi-Z                      | <b>ATA Data bit 15.</b>   |
| 4       | 53                | 99                 | GND                                | GND                |                           | <b>Ground.</b>  |
| 5       | 54 <sup>[3]</sup> | 100 <sup>[3]</sup> | ATAPUEN<br>(NC)                    | I/O                |                           | ATA pull-up voltage source for bus-powered applications (see section 5.3.10).<br><br><b>Alternate Function:</b> Input when the EEPROM configuration byte 8 has bit 7 set to one. The input value is reported through EP1IN (byte 0, bit 2). |
| 6       | 55                | 1                  | V <sub>CC</sub>                    | PWR                |                           | <b>V<sub>CC</sub>.</b> Connect to 3.3V power source.  |
| 7       | 56                | 2                  | GND                                | GND                |                           | <b>Ground.</b>  |
| 8       | 1                 | 3                  | IORDY                              | I <sup>[1]</sup>   | Input                     | <b>ATA Control.</b>   |
| 9       | 2                 | 4                  | DMARQ                              | I <sup>[1]</sup>   | Input                     | <b>ATA Control.</b>   |
| N/A     | N/A               | 5<br>6<br>7<br>8   | GND                                |                    |                           | <b>Ground.</b>  |
| 10      | 3                 | 9                  | AV <sub>CC</sub>                   | PWR                |                           | <b>Analog V<sub>CC</sub>.</b> Connect to V <sub>CC</sub> through the shortest path possible.  |
| 11      | 4                 | 10                 | XTALOUT                            | Xtal               | Xtal                      | <b>24-MHz Crystal Output</b> (see section 5.3.3).   |
| 12      | 5                 | 11                 | XTALIN                             | Xtal               | Xtal                      | <b>24-MHz Crystal Input</b> (see section 5.3.3).  |
| 13      | 6                 | 12                 | AGND                               | GND                |                           | <b>Analog Ground.</b> Connect to ground with as short a path as possible.   |
| N/A     | N/A               | 13<br>14<br>15     | NC                                 |                    |                           | <b>No Connect.</b>  |
| 14      | 7                 | 16                 | V <sub>CC</sub>                    | PWR                |                           | <b>V<sub>CC</sub>.</b> Connect to 3.3V power source.  |
| 15      | 8                 | 17                 | DPLUS                              | I/O                | Hi-Z                      | <b>USB D+ Signal</b> (see section 5.3.1).   |
| 16      | 9                 | 18                 | DMINUS                             | I/O                | Hi-Z                      | <b>USB D- Signal</b> (see section 5.3.1).   |
| 17      | 10                | 19                 | GND                                | GND                |                           | <b>Ground.</b>  |
| 18      | 11                | 20                 | V <sub>CC</sub>                    | PWR                |                           | <b>V<sub>CC</sub>.</b> Connect to 3.3V power source.  |
| 19      | 12                | 21                 | GND                                | GND                |                           | <b>Ground.</b>  |
| N/A     | N/A               | 22                 | SYSIRQ                             | I                  | Input                     | <b>Active HIGH.</b> USB interrupt request (see section 5.3.4). Tie to GND if functionality is not used.   |
| N/A     | N/A               | 23<br>24<br>25     | GND                                | GND                |                           | <b>Ground.</b>  |
| 20      | 13 <sup>[3]</sup> | 26 <sup>[3]</sup>  | PWR500# <sup>[2]</sup><br>(PU 10K) | I/O                |                           | <b>Active LOW.</b> VBUS power granted indicator used in bus-powered designs (see section 5.3.11).<br><br><b>Alternate Function</b> for 68320.   |
| 21      | 14                | 27                 | GND (RESERVED)                     |                    |                           | <b>Reserved.</b> Tie to GND.  |

**Notes:**

1. If byte 8, bit 4 of the EEPROM is set to '0', the ATA interface pins are only active when VBUS\_ATA\_EN is asserted. See section 5.3.9.
2. A '#' sign after the pin name indicates that it is active LOW.
3. The General Purpose inputs can be enabled on ATAPUEN, PWR500#, and DRVPWRVLD via EEPROM byte 8, bit 7 on CY7C68320/CY7C68321.


**Table 5-1. AT2LP Pin Descriptions**
**Note: (Italics pin names denote pin functionality during CY7C68300A-compatibility mode) (continued)**

| 56 SSOP | 56 QFN | 100 TQFP       | Pin Name                          | Pin Type           | Default State at Start-up          | Pin Description  |
|---------|--------|----------------|-----------------------------------|--------------------|------------------------------------|--|
| N/A     | N/A    | 28             | NC                                |                    |                                    | No Connect.  |
| 22      | 15     | 29             | SCL                               | O                  | Active for several ms at start-up. | Clock signal for I <sup>2</sup> C interface (see section 5.3.2).   |
| 23      | 16     | 30             | SDA                               | I/O                |                                    | Data signal for I <sup>2</sup> C interface (see section 5.3.2).  |
| N/A     | N/A    | 31<br>32       | NC                                |                    |                                    | No Connect.  |
| 24      | 17     | 33             | V <sub>CC</sub>                   | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| 25      | 18     | 34             | DD0                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 0.  |
| 26      | 19     | 35             | DD1                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 1.  |
| 27      | 20     | 36             | DD2                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 2.  |
| 28      | 21     | 37             | DD3                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 3.  |
| N/A     | N/A    | 38             | V <sub>CC</sub>                   | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| N/A     | N/A    | 39             | GND                               | GND                |                                    | Ground.  |
| N/A     | N/A    | 40             | NC                                | NC                 |                                    | No Connect.  |
| N/A     | N/A    | 41             | GND                               |                    |                                    | Ground.  |
| N/A     | N/A    | 42             | NC                                | NC                 |                                    | No Connect.  |
| N/A     | N/A    | 43             | GND                               |                    |                                    | Ground.  |
| 29      | 22     | 44             | DD4                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 4.  |
| 30      | 23     | 45             | DD5                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 5.  |
| 31      | 24     | 46             | DD6                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 6.  |
| 32      | 25     | 47             | DD7                               | I/O <sup>[1]</sup> | Hi-Z                               | ATA Data bit 7.  |
| 33      | 26     | 48             | GND                               | GND                |                                    | Ground.  |
| 34      | 27     | 49             | V <sub>CC</sub>                   | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| 35      | 28     | 50             | GND                               | GND                |                                    | Ground.  |
| N/A     | N/A    | 51<br>52       | NC                                | NC                 |                                    | No Connect.  |
| N/A     | N/A    | 53             | V <sub>CC</sub>                   | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| 36      | 29     | 54             | D <sub>IOW</sub> # <sup>[2]</sup> | O/Z <sup>[1]</sup> | Driven HIGH (CMOS)                 | ATA Control.   |
| 37      | 30     | 55             | D <sub>IOR</sub> #                | O/Z <sup>[1]</sup> | Driven HIGH (CMOS)                 | ATA Control.   |
| 38      | 31     | 56             | D <sub>MACK</sub> #               | O/Z <sup>[1]</sup> | Driven HIGH (CMOS)                 | ATA Control.   |
| N/A     | N/A    | 57             | NC                                | NC                 |                                    | No Connect.  |
| N/A     | N/A    | 58             | LOWPWR#                           | O                  |                                    | USB suspend indicator (see section 5.3.7).<br>'0' = Chip active. VBUS power draw governed by PWR500# pin.<br>'Hi-Z' = Chip suspend. VBUS system current limited to USB suspend mode value. |
| N/A     | N/A    | 59<br>60<br>61 | NC                                | NC                 |                                    | No Connect.  |
| N/A     | N/A    | 62             | VBUSPWRD                          | I                  | Input                              | Bus-powered operation selector. Used in systems that are capable of being bus or self-powered to indicate the current power mode.  |
| N/A     | N/A    | 63<br>64       | NC                                | NC                 |                                    | No Connect.  |
| N/A     | N/A    | 65             | GND                               | GND                |                                    | Ground.  |




**Table 5-1. AT2LP Pin Descriptions**
**Note: (Italics pin names denote pin functionality during CY7C68300A-compatibility mode) (continued)**

| 56<br>SSOP | 56<br>QFN   | 100<br>TQFP                      | Pin Name   | Pin<br>Type        | Default State<br>at Start-up       | Pin Description  |
|------------|---|----------------------------------|--|--------------------|------------------------------------|--|
| 39         | 32  | 66                               | V <sub>CC</sub>  | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| 40         | 33  | 67                               | INTRQ  | I <sup>[1]</sup>   | Input                              | <b>ATA Interrupt request.</b>  |
| 41         | 34  | 68                               | DA0  | O/Z <sup>[1]</sup> | Driven HIGH<br>after 2 ms<br>delay | <b>ATA Address.</b>  |
| 42         | 35  | 69                               | DA1  | O/Z <sup>[1]</sup> | Driven HIGH<br>after 2 ms<br>delay | <b>ATA Address.</b>  |
| 43         | 36 <sup>[3]</sup>   | 70 <sup>[3]</sup>                | DRV <sub>PWRVLD</sub><br>(DA2)                         | I                  | Input                              | <b>Device Presence Detect</b> (see section 5.3.5). Configurable polarity, controlled by EEPROM address 0x08. This pin must be connected to GND if functionality is not utilized.<br><br><b>Alternate Function:</b> Input when the EEPROM configuration byte 8 has bit 7 set to one. The input value is reported through EP1IN (byte 0, bit 0). |
| 44         | 37  | 71                               | CS0#   | O/Z <sup>[1]</sup> | Driven HIGH<br>after 2 ms<br>delay | <b>ATA Chip Select.</b>  |
| 45         | 38  | 72                               | CS1#   | O/Z <sup>[1]</sup> | Driven HIGH<br>after 2 ms<br>delay | <b>ATA Chip Select.</b>  |
| 46         | 39  | 73                               | DA2<br>(VBUS_PWR_VALID)                                | O/Z <sup>[1]</sup> | Driven HIGH<br>after 2 ms<br>delay | <b>ATA Address.</b>  |
| 47         | 40  | 74                               | ARESET#  | O/Z <sup>[1]</sup> |                                    | <b>ATA Reset.</b>  |
| 48         | 41  | 75                               | GND  | GND                |                                    | <b>Ground.</b>   |
| N/A        | N/A   | 76                               | NC   | NC                 |                                    | <b>No Connect.</b>   |
| 49         | 42  | 77                               | RESET#   | I                  | Input                              | <b>Chip Reset</b> (see section 5.3.13). This pin is normally tied to V <sub>CC</sub> through a 100K resistor, and to GND through a 0.1-μF capacitor, supplying a 10-ms reset.  |
| 50         | 43  | 78                               | V <sub>CC</sub>  | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| 51         | 44  | 79                               | VBUS_ATA_ENABLE<br>(ATA_EN)                            | I                  | Input                              | <b>VBUS detection</b> (see section 5.3.9). Indicates to the CY7C68300B/CY7C68301B that VBUS power is present.  |
| 52         | 45  | 80                               | DD8  | I/O <sup>[1]</sup> | Hi-Z                               | <b>ATA Data bit 8.</b>   |
| 53         | 46  | 81                               | DD9  | I/O <sup>[1]</sup> | Hi-Z                               | <b>ATA Data bit 9.</b>   |
| 54         | 47  | 82                               | DD10   | I/O <sup>[1]</sup> | Hi-Z                               | <b>ATA Data bit 10.</b>  |
| 55         | 48  | 83                               | DD11   | I/O <sup>[1]</sup> | Hi-Z                               | <b>ATA Data bit 11.</b>  |
| N/A        | N/A   | 84                               | GND  |                    |                                    | <b>Ground.</b>   |
| N/A        | N/A   | 85                               | V <sub>CC</sub>  | PWR                |                                    | V <sub>CC</sub> . Connect to 3.3V power source.  |
| N/A        | N/A   | 86<br>87                         | NC   | NC                 |                                    | <b>No Connect.</b>   |
| N/A        | 36 <sup>[3]</sup><br>13 <sup>[3]</sup><br>54 <sup>[3]</sup> | 88<br>89<br>90<br>91<br>92<br>93 | GPIO0<br>GPIO1<br>GPIO2_nHS<br>GPIO3<br>GPIO4<br>GPIO5 | I/O <sup>[3]</sup> |                                    | <b>General purpose I/O pins</b> (see section 5.3.6). The GPIO pins must be tied to GND if functionality is not utilized. If the hs_indicator config bit is set, the GPIO2_nHS pin will reflect the operating speed:<br>'1' = full-speed operation.<br>'0' = high-speed operation.  |
| N/A        | N/A   | 94                               | GND  | GND                |                                    | <b>Ground.</b>   |
| 56         | 49  | 95                               | DD12   | I/O <sup>[1]</sup> | Hi-Z                               | <b>ATA Data bit 12.</b>  |



### 5.3 Additional Pin Descriptions

#### 5.3.1 DPLUS, DMINUS

DPLUS and DMINUS are the USB signaling pins; they should be tied to the D+ and D- pins of the USB connector. Because they operate at high frequencies, the USB signals require special consideration when designing the layout of the PCB. See section 15.0 for PCB layout recommendations. When RESET# is released, the internal pull-up on D+ is controlled by VBUS\_ATA\_ENABLE. When VBUS\_ATA\_ENABLE is HIGH, D+ is pulled up.

#### 5.3.2 SCL, SDA

The clock and data pins for the I<sup>2</sup>C port should be connected to the configuration EEPROM and to 2.2K pull-up resistors tied to V<sub>CC</sub>. The SCL and SDA pins are active for several milliseconds at start-up.

#### 5.3.3 XTALIN, XTALOUT

The AT2LP requires a 24-MHz ( $\pm 100$ ppm) signal to derive internal timing. Typically, a 24-MHz (20-pF, 500- $\mu$ W, parallel-

resonant fundamental mode) crystal is used, but a 24-MHz square wave from another source can also be used. If a crystal is used, connect its pins to XTALIN and XTALOUT, and also through 12-pF capacitors to GND as shown in Figure 5-6. If an alternate clock source is used, apply it to XTALIN and leave XTALOUT open.

#### 5.3.4 SYSIRQ

The SYSIRQ pin provides a way for systems to request service from host software by using the USB Interrupt pipe. If the AT2LP has no pending interrupt data to return, USB interrupt pipe data requests are NAKed. If pending data is available, the AT2LP returns 16 bits of data; this data indicates the HS\_MODE signal (that indicates whether AT2LP is operating in high-speed or full-speed), the VBUSPWRD pin, and the GPIO pins. Table 5-2 gives the bitmap for the data returned on the interrupt pipe and Figure 5-7 depicts the latching algorithm incorporated by AT2LP.

The SYSIRQ pin must be tied low if the HID function is used (refer to Section 6.0).

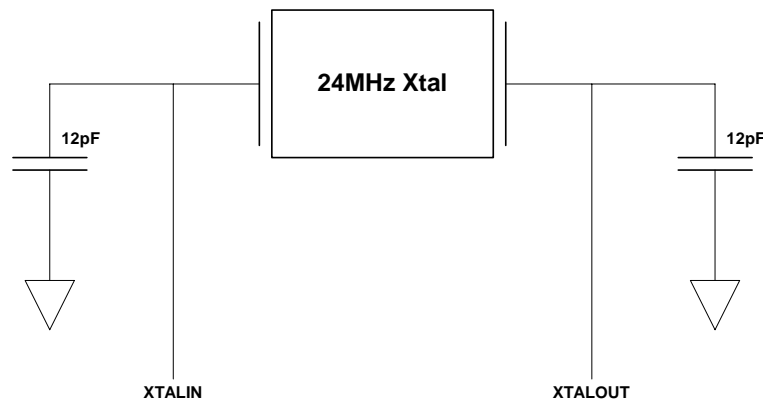
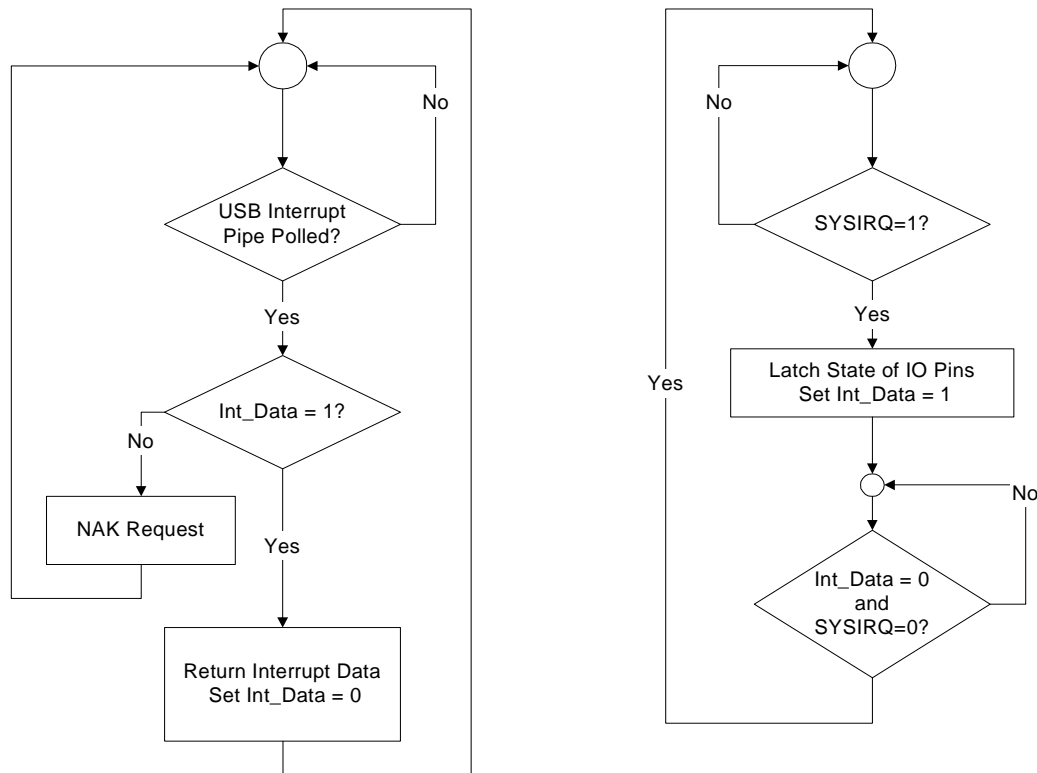


Figure 5-6. XTALIN / XTALOUT Diagram

Table 5-2. USB Interrupt Pipe Data Bitmap

| USB Interrupt Data Byte 1 |          |          |          |          |          |                |          | USB Interrupt Data Byte 0 |          |         |         |         |         |         |         |
|---------------------------|----------|----------|----------|----------|----------|----------------|----------|---------------------------|----------|---------|---------|---------|---------|---------|---------|
| 7                         | 6        | 5        | 4        | 3        | 2        | 1              | 0        | 7                         | 6        | 5       | 4       | 3       | 2       | 1       | 0       |
| RESERVED                  | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | USB High-Speed | VBUSPWRD | RESERVED                  | RESERVED | GPIO[5] | GPIO[4] | GPIO[3] | GPIO[2] | GPIO[1] | GPIO[0] |



**Figure 5-7. SYSIRQ Latching Algorithm**

### 5.3.5 DRVPWRVLD

When this pin is enabled via EEPROM byte 8, bit 0, the AT2LP will inform the host that a removable device, such as a CF card, is present. The CY7C68300B/CY7C68301B will use DRVPWRVLD to detect that the removable device is present. Pin polarity is controlled by bit 1 of EEPROM address 8. When DRVPWRVLD is deasserted, the AT2LP will report a “no media present” status (ASC = 0x3A, ASQ = 0x00) to the host. When the media has been detected again, the AT2LP will report a “media changed” status to the host (ASC = 0x28, ASQ = 0x00).

When a removable device is used, it is always the master device. Only one removable device may be attached to the AT2LP. If the system only contains a removable device, EEPROM byte 8, bit 6 must be set to ‘0’ to disable ATA device detection at start-up. If a non-removable device is connected in addition to a removable media device, it must be configured as a slave (device address 1).

DRVPWRVLD can also be configured as an input. See Section 6.0 HID Functions for Button Controls.

### 5.3.6 GPIO Pins

The GPIO pins allow for a general purpose Input/Output interface. There are several different interfaces to the GPIO pins:

- Configuration bytes 0x09 and 0x0A contain the default settings for the GPIO pins.
- The host can modify the settings of the GPIO pins during operation. This is done with vendor-specific commands described in Section 8.6.

- The status of the GPIO pins is also returned on the interrupt endpoint (EP1) in response to a SYSIRQ. See section 5.3.3 for SYSIRQ details.

GPIO2\_nHS also has an alternate function. If the “HS Indicator Enable” configuration (bit 2 of EEPROM address 8) is set, the GPIO2\_nHS pin will reflect the operating speed of the device (full- or high-speed USB).

### 5.3.7 LOWPWR#

LOWPWR# is an output pin that is driven to ‘0’ when the AT2LP is active. LOWPWR# is placed in Hi-Z when the AT2LP is in a suspend state.

### 5.3.8 ATA Interface Pins

Design practices for signal integrity as outlined in the ATA/ATAPI-6 Specification should be followed with systems that utilize a ribbon cable interconnect between the CY7C68300B/CY7C68301B’s ATA interface and the attached ATA/ATAPI device, especially if Ultra DMA Mode is utilized.

### 5.3.9 VBUS\_ATA\_ENABLE

VBUS\_ATA\_ENABLE is typically used to indicate to the AT2LP that power is present on VBUS. This pin is polled by the AT2LP at start-up and then every 20ms thereafter. If this pin is ‘1’, the internal 1.5K pull-up is attached to D+. If this pin is ‘0’, the AT2LP will release the pull-up on D+ as required by the USB specification. Also, If EEPROM byte 8, bit 4 is ‘0’, the ATA interface pins will be placed in a high impedance (Hi-Z) state when VBUS\_ATA\_ENABLE is ‘0’. If EEPROM byte 8, bit 4 is ‘1’, the ATA interface pins will still be driven when VBUS\_ATA\_ENABLE is ‘0’.



### 5.3.10 ATAPUEN

This output controls the required host pull-up resistors on the ATA interface. ATAPUEN is driven to '0' when the ATA bus is inactive. ATAPUEN is driven to '1' when the ATA bus is active. ATAPUEN is set to a Hi-Z state along with all other ATA interface pins if VBUS\_ATA\_ENABLE is deasserted and the ATA\_EN functionality (EEPROM byte 8, bit 4) is enabled. ATAPUEN can also be configured as an input. See *Section 6.0 HID Functions for Button Controls*

### 5.3.11 PWR500#

The AT2LP asserts PWR500# to indicate that VBUS current may be drawn up to the limit specified by the bMaxPower field of the USB configuration descriptors. In the 100-pin package, PWR500# will only be asserted if VBUSPWRD and DRVPWRVLD are also asserted. In the 56-pin package, PWR500# only functions during bus-powered operation. If the AT2LP enters a low-power state, PWR500# is deasserted. When normal operation is resumed, PWR500# is restored accordingly. Naturally, the PWR500# pin should never be used to control power sources for the AT2LP. In the 68320 parts, PWR500# can also be configured as an input. If the Drive Power Valid Enable bit is set (EEPROM byte 8, bit 1), PWR500# will ONLY be driven when Drive Power Valid is active. See *Section 6.0 HID Functions for Button Controls*.

### 5.3.12 VBUSPWRD

Some devices have the ability to be either self-powered or bus-powered. The VBUSPWRD input pin enables these devices to change between self-powered to bus-powered modes by changing the contents of the bMaxPower field and the self-powered bit in the configuration descriptor.

Note that current host drivers do not poll the device for this information, so this pin is only effective on a USB or power-up reset.

**Table 5-3. Bus-Power Description**

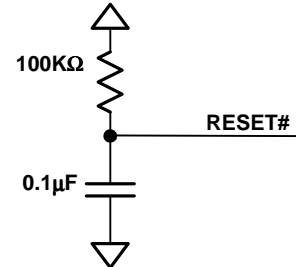
| VBUSPWRD value     | 1                                      | 0       | Not present (56-pin)                   |
|--------------------|--|---------|--|
| PWR500#            | 1 when Config = 0<br>0 when Config = 1 | 1       | 1 when Config = 0<br>0 when Config = 1 |
| bMaxPower          | 250 (500mA)                            | 1 (2mA) | EEPROM value used                      |
| bmAttributes bit 6 | 0                                      | 1       | EEPROM value used                      |

**Table 6-1. EP1 Data Bitmap**

| EP1 Data Byte 1 |          |          |          |          |          |                |          | EP1 Data Byte 0 |         |         |         |         |         |         |         |
|-----------------|----------|----------|----------|----------|----------|----------------|----------|-----------------|---------|---------|---------|---------|---------|---------|---------|
| 7               | 6        | 5        | 4        | 3        | 2        | 1              | 0        | 7               | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| RESERVED        | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | USB High-Speed | VBUSPWRD | DRVPWRVLD       | GPIO[4] | GPIO[3] | GPIO[2] | GPIO[1] | GPIO[0] | ATAPUEN | PWR500# |

### 5.3.13 RESET#

Asserting RESET# for 10 ms will reset the entire chip. This pin is normally tied to V<sub>CC</sub> through a 100k resistor, and to GND through a 0.1-μF capacitor, as shown in the figure below.



**Figure 5-8. Typical Reset Circuit**

Cypress does not recommend an RC reset circuit for bus-powered devices. See the application note *EZ-USB FX2™/AT2™/SX2™ Reset and Power Considerations* at [www.cypress.com](http://www.cypress.com) for more information.

## 6.0 HID Functions for Button Controls

Cypress' CY7C68320/CY7C68321 introduces the capability to support Human Interface Device (HID) signaling to the host for such functions as buttons. The ability to add buttons to a mass storage solution opens new applications for backup and other device-side notification to the host.

Optional HID functions can be added to the EEPROM descriptors by setting bit 7 of byte 8 of the EEPROM to a value of '1'. When this bit is set, several pins adopt alternate functions for the 56-pin package. This allows the pins to be used as button inputs. If there is a HID descriptor in the EEPROM, these pins are polled by the hardware approximately every 17 ms. If a change is detected in the pin(s) state, a report is sent via EP1. The report format for byte 0 and byte 1 are shown in *Table 6-1*.



## 7.0 Functional Overview

### 7.1 USB Signaling Speed

AT2LP operates at the following two of the three rates defined in the *USB Specification Revision 2.0* dated April 27, 2000:

- Full-speed, with a signaling bit rate of 12 Mbits/sec
- High-speed, with a signaling bit rate of 480 Mbits/sec.

AT2LP does not support the low-speed signaling rate of 1.5 Mbits/sec.

### 7.2 ATA Interface

The ATA/ATAPI port on the AT2LP is compatible with the *Information Technology—AT Attachment with Packet Interface—6 (ATA/ATAPI-6) Specification, T13/1410D Rev 2a*. The AT2LP supports both ATAPI packet commands as well as ATA commands (by use of ATA Command Blocks), as outlined in Section 7.2.1. Refer to the *USB Mass Storage Class (MSC) Bulk Only Transport (BOT) Specification* for information on Command Block formatting. Additionally, the AT2LP translates

ATAPI *SFF-8070i* commands to ATA commands for seamless integration of ATA devices with generic Mass Storage Class BOT drivers.

#### 7.2.1 ATA Command Block (ATACB)

The ATA Command Block (ATACB) functionality provides a means of passing ATA commands and ATA register accesses to the attached device for execution. ATACB commands are transferred in the Command Block Wrapper Command Block (CBWCB) portion of the Command Block Wrapper (CBW). The ATACB is distinguished from other command blocks by having the first two bytes of the command block match the bVSCBSignature and bVSCBSubCommand values that are defined in *Table 7-1*. Only command blocks that have a valid bVSCBSignature and bVSCBSubCommand are interpreted as ATA Command Blocks. All other fields of the CBW and restrictions on the CBWCB remain as defined in the USB Mass Storage Class Bulk-Only Transport Specification. The ATACB must be 16 bytes in length. The following table and text defines the fields of the ATACB.

**Table 7-1. ATACB Field Descriptions**

| Byte   | Field Name          | Field Description  |  |   |   |  |   |   |
|--|---------------------|--|--|---|---|--|---|---|
| 0  | bVSCBSignature      | This field indicates to the CY7C68300B/CY7C68301B that the ATACB contains a vendor-specific command block. This value of this field must match the value in EEPROM address 0x04 for this vendor-specific command to be recognized.   |  |   |   |  |   |   |
| 1  | bVSCBSubCommand     | This field must be set to 0x24 for ATACB commands.   |  |   |   |  |   |   |
| 2  | bmATACBActionSelect | This field controls the execution of the ATACB according to the bitfield values: <table border="1"> <tr> <td>Bit 7 <i>IdentifyPacketDevice</i> – This bit indicates that the data phase of the command will contain ATAPI (0xA1) or ATA (0xEC) IDENTIFY device data. Setting <i>IdentifyPacketDevice</i> when the data phase does not contain IDENTIFY device data will result in unspecified device behavior.<br/>0 = Data phase does not contain IDENTIFY device data<br/>1 = Data phase contains ATAPI or ATA IDENTIFY device data</td> </tr> <tr> <td>Bit 6 <i>UDMACommand</i> – This bit enables supported UDMA device transfers. Setting this bit when a non-UDMA capable device is attached will result in undetermined behavior.<br/>0 = Do not use UDMA device transfers (only use PIO mode)<br/>1 = Use UDMA device transfers</td> </tr> <tr> <td>Bit 5 <i>DEVOverride</i> – This bit determines whether the DEV bit value is taken from the value assigned to the LUN during start-up or from the ATACB.<br/>0 = The DEV bit will be taken from the value assigned to the LUN during start-up<br/>1 = The DEV bit will be taken from the ATACB field 0x0B, bit 4</td> </tr> <tr> <td>Bit 4 <i>DErrorOverride</i> – This bit controls the device error override feature. This bit should not be set during a bmATACBActionSelect TaskFileRead.<br/>0 = Data accesses are halted if a device error is detected<br/>1 = Data accesses are not halted if a device error is detected</td> </tr> <tr> <td>Bit 3 <i>PErrorOverride</i> – This bit controls the phase error override feature. This bit should not be set during a bmATACBActionSelect TaskFileRead.<br/>0 = Data accesses are halted if a phase error is detected<br/>1 = Data accesses are not halted if a phase error is detected</td> </tr> <tr> <td>Bit 2 <i>PollAltStatOverride</i> – This bit determines whether or not the Alternate Status register will be polled and the BSY bit will be used to qualify the ATACB operation.<br/>0 = The AltStat register will be polled until BSY=0 before proceeding with the ATACB operation<br/>1 = The ATACB operation will be executed without polling the AltStat register.</td> </tr> </table> | Bit 7 <i>IdentifyPacketDevice</i> – This bit indicates that the data phase of the command will contain ATAPI (0xA1) or ATA (0xEC) IDENTIFY device data. Setting <i>IdentifyPacketDevice</i> when the data phase does not contain IDENTIFY device data will result in unspecified device behavior.<br>0 = Data phase does not contain IDENTIFY device data<br>1 = Data phase contains ATAPI or ATA IDENTIFY device data | Bit 6 <i>UDMACommand</i> – This bit enables supported UDMA device transfers. Setting this bit when a non-UDMA capable device is attached will result in undetermined behavior.<br>0 = Do not use UDMA device transfers (only use PIO mode)<br>1 = Use UDMA device transfers | Bit 5 <i>DEVOverride</i> – This bit determines whether the DEV bit value is taken from the value assigned to the LUN during start-up or from the ATACB.<br>0 = The DEV bit will be taken from the value assigned to the LUN during start-up<br>1 = The DEV bit will be taken from the ATACB field 0x0B, bit 4 | Bit 4 <i>DErrorOverride</i> – This bit controls the device error override feature. This bit should not be set during a bmATACBActionSelect TaskFileRead.<br>0 = Data accesses are halted if a device error is detected<br>1 = Data accesses are not halted if a device error is detected | Bit 3 <i>PErrorOverride</i> – This bit controls the phase error override feature. This bit should not be set during a bmATACBActionSelect TaskFileRead.<br>0 = Data accesses are halted if a phase error is detected<br>1 = Data accesses are not halted if a phase error is detected | Bit 2 <i>PollAltStatOverride</i> – This bit determines whether or not the Alternate Status register will be polled and the BSY bit will be used to qualify the ATACB operation.<br>0 = The AltStat register will be polled until BSY=0 before proceeding with the ATACB operation<br>1 = The ATACB operation will be executed without polling the AltStat register. |
| Bit 7 <i>IdentifyPacketDevice</i> – This bit indicates that the data phase of the command will contain ATAPI (0xA1) or ATA (0xEC) IDENTIFY device data. Setting <i>IdentifyPacketDevice</i> when the data phase does not contain IDENTIFY device data will result in unspecified device behavior.<br>0 = Data phase does not contain IDENTIFY device data<br>1 = Data phase contains ATAPI or ATA IDENTIFY device data |                     |  |  |   |   |  |   |   |
| Bit 6 <i>UDMACommand</i> – This bit enables supported UDMA device transfers. Setting this bit when a non-UDMA capable device is attached will result in undetermined behavior.<br>0 = Do not use UDMA device transfers (only use PIO mode)<br>1 = Use UDMA device transfers  |                     |  |  |   |   |  |   |   |
| Bit 5 <i>DEVOverride</i> – This bit determines whether the DEV bit value is taken from the value assigned to the LUN during start-up or from the ATACB.<br>0 = The DEV bit will be taken from the value assigned to the LUN during start-up<br>1 = The DEV bit will be taken from the ATACB field 0x0B, bit 4  |                     |  |  |   |   |  |   |   |
| Bit 4 <i>DErrorOverride</i> – This bit controls the device error override feature. This bit should not be set during a bmATACBActionSelect TaskFileRead.<br>0 = Data accesses are halted if a device error is detected<br>1 = Data accesses are not halted if a device error is detected   |                     |  |  |   |   |  |   |   |
| Bit 3 <i>PErrorOverride</i> – This bit controls the phase error override feature. This bit should not be set during a bmATACBActionSelect TaskFileRead.<br>0 = Data accesses are halted if a phase error is detected<br>1 = Data accesses are not halted if a phase error is detected  |                     |  |  |   |   |  |   |   |
| Bit 2 <i>PollAltStatOverride</i> – This bit determines whether or not the Alternate Status register will be polled and the BSY bit will be used to qualify the ATACB operation.<br>0 = The AltStat register will be polled until BSY=0 before proceeding with the ATACB operation<br>1 = The ATACB operation will be executed without polling the AltStat register.  |                     |  |  |   |   |  |   |   |


**Table 7-1. ATACB Field Descriptions** (continued)

| Byte  | Field Name                      | Field Description  |
|-------|---------------------------------|--|
|       |                                 | <p>Bit 1 <i>DeviceSelectionOverride</i> – This bit determines when the device selection will be performed in relation to the command register write accesses.<br/>           0 = Device selection will be performed prior to command register write accesses<br/>           1 = Device selection will be performed following command register write accesses</p> <p>Bit 0 <i>TaskFileRead</i> – This bit determines whether or not the taskfile register data selected in <i>bmATACBRegisterSelect</i> is returned. If this bit is set, the <i>dCBWDataTransferLength</i> field must be set to 8.<br/>           0 = Execute ATACB command and data transfer (if any)<br/>           1 = Only read taskfile registers selected in <i>bmATACBRegisterSelect</i> and return 0x00h for all others. The format of the 12 bytes of returned data is as follows:</p> <ul style="list-style-type: none"> <li>• Address offset 0x00 (0x3F6) – Alternate Status</li> <li>• Address offset 0x01 (0x1F1) – Features / Error</li> <li>• Address offset 0x02 (0x1F2) – Sector Count</li> <li>• Address offset 0x03 (0x1F3) – Sector Number</li> <li>• Address offset 0x04 (0x1F4) – Cylinder Low</li> <li>• Address offset 0x05 (0x1F5) – Cylinder High</li> <li>• Address offset 0x06 (0x1F6) – Device / Head</li> <li>• Address offset 0x07 (0x1F7) – Command / Status</li> </ul> |
| 3     | <i>bmATACBRegisterSelect</i>    | <p>This field controls which of the taskfile register read or write accesses occur. Taskfile read data will always be 8 bytes in length, and unselected register data will be returned as 0x00. Register accesses occur in sequential order as outlined below (0 to 7).</p> <p>Bit 0 (0x3F6) Device Control / Alternate Status</p> <p>Bit 1 (0x1F1) Features / Error</p> <p>Bit 2 (0x1F2) Sector Count</p> <p>Bit 3 (0x1F3) Sector Number</p> <p>Bit 4 (0x1F4) Cylinder Low</p> <p>Bit 5 (0x1F5) Cylinder High</p> <p>Bit 6 (0x1F6) Device / Head</p> <p>Bit 7 (0x1F7) Command / Status</p>  |
| 4     | <i>bATACBTransferBlockCount</i> | <p>This value indicates the maximum requested block size in 512-byte increments. This value must be set to the last value used for the “Sectors per block” in the SET_MULTIPLE_MODE command. Legal values are 0, 1, 2, 4, 8, 16, 32, 64, and 128 where 0 indicates 256 sectors per block. A command failed status will be returned if an illegal value is used in the ATACB.</p>   |
| 5–12  | <i>bATACBTaskFileWriteData</i>  | <p>These bytes contain ATA register data used with ATA command or PIO write operations. Only registers selected in <i>bmATACBRegisterSelect</i> are required to hold valid data when accessed. The registers are as follows.</p> <p>ATACB Address Offset 0x05 (0x3F6) – Device Control</p> <p>ATACB Address Offset 0x06 (0x1F1) – Features</p> <p>ATACB Address Offset 0x07 (0x1F2) – Sector Count</p> <p>ATACB Address Offset 0x08 (0x1F3) – Sector Number</p> <p>ATACB Address Offset 0x09 (0x1F4) – Cylinder Low</p> <p>ATACB Address Offset 0x0A (0x1F5) – Cylinder High</p> <p>ATACB Address Offset 0x0B (0x1F6) – Device</p> <p>ATACB Address Offset 0x0C (0x1F7) – Command</p>  |
| 13–15 | Reserved                        | These bytes must be set to 0x00 for ATACB commands.  |



## 8.0 Operating Modes

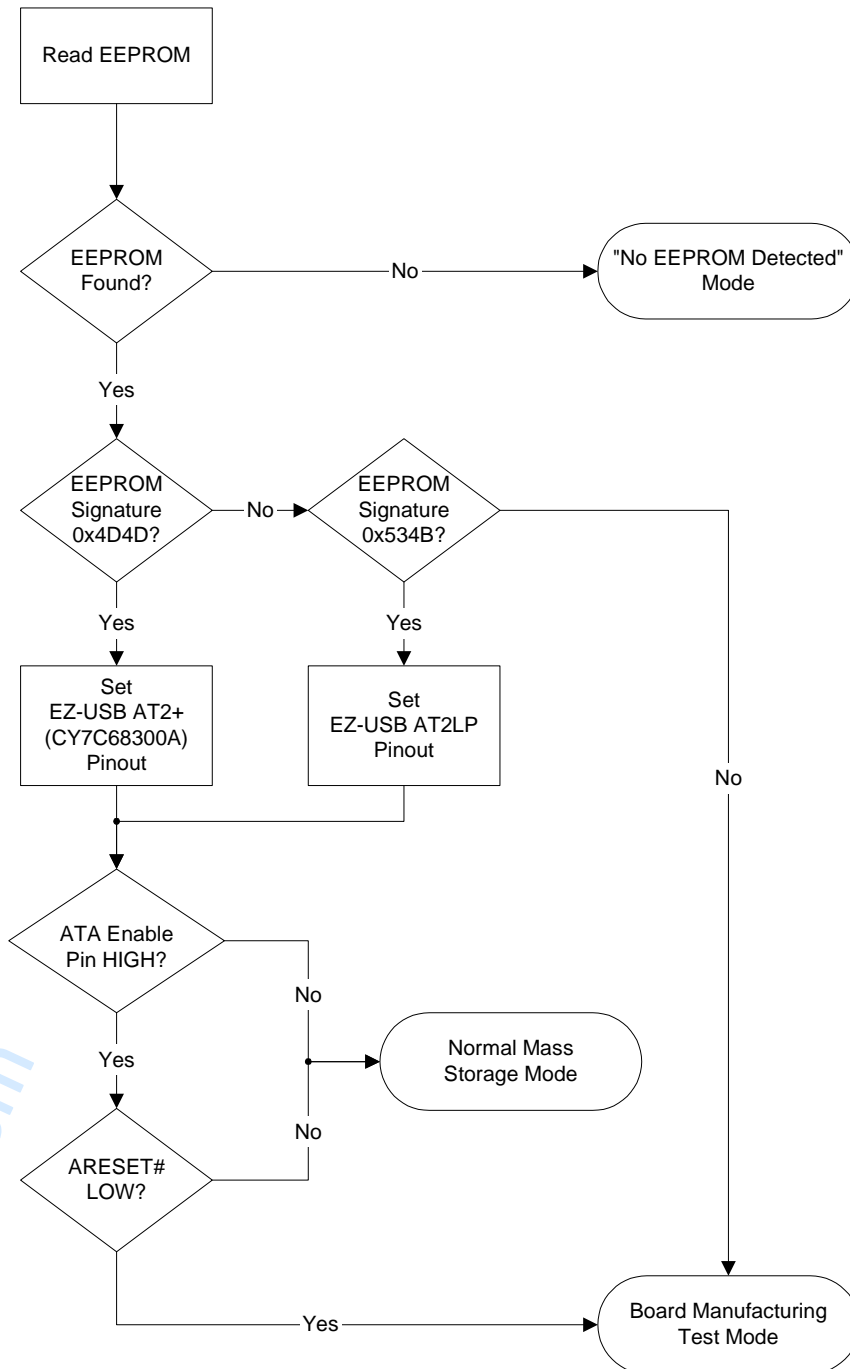


Figure 8-1. Operational Mode Selection

### 8.1 Operational Mode Selection Flow

During the power-up sequence, the AT2LP checks the I<sup>2</sup>C port for an EEPROM and checks to see if the ATA connector is configured for Board Manufacturing Test Mode. AT2LP then selects an operating mode as shown below.

- If an I<sup>2</sup>C EEPROM with a 0x4D4D signature is found, the CY7C68300B/CY7C68301B uses the same pinout and EEPROM format as the CY7C68300A (EZ-USB AT2).

- If the first two bytes of the EEPROM contain 0x534B the AT2LP uses the values stored in the EEPROM to configure the USB descriptors for normal operation.
- If no EEPROM is detected, the AT2LP uses a VID/PID of 0x00/0x00. This is not a valid mode of operation.
- If an invalid EEPROM signature is read, the AT2LP defaults into Board Manufacturing Test Mode.

There is an additional method available to put the AT2LP into Board Manufacturing Test Mode to allow reprogramming of



EEPROMs without an ATA/ATAPI device attached. If the ATA Reset (ARESET#) line is LOW on power-up, the AT2LP will enter Board Manufacturing Test Mode. A convenient way to pull the ARESET# line LOW is to short pins 1 and 3 on the ATA connector, which will tie the ARESET# line to the pull-down on DD7.

## 8.2 “No EEPROM Detected” Mode

When no EEPROM is detected at start-up, the AT2LP will enumerate with VID/PID/DID values that are all 0x00, which is not a valid mode of operation. These values can be factory programmed into the AT2LP for high-volume applications to avoid the need for an external EEPROM in some designs. Contact your local Cypress Semiconductor sales office for details.

## 8.3 Normal Mass Storage Mode

In Normal Mass Storage Mode, the chip behaves as a USB 2.0 to ATA/ATAPI bridge. This includes all typical USB device states (powered, configured, etc.). The USB descriptors are returned according to the values stored in the external EEPROM. An external EEPROM is required for Mass Storage Class Bulk-Only Transport compliance, since a unique serial number is required for each device. Also, Cypress requires customers to use their own Vendor and Product IDs for final products.

## 8.4 Board Manufacturing Test Mode

In Board Manufacturing Test Mode, the chip behaves as a USB 2.0 device but the ATA/ATAPI interface is not fully active.

In this mode, the AT2LP allows for reading from and writing to the EEPROM, and for board level testing through vendor specific ATAPI commands utilizing the CBW Command Block as described in the *USB Mass Storage Class Bulk-Only Transport Specification*. There is a vendor-specific ATAPI command for the EEPROM access (CfgCB) and one for the board level testing (MfgCB).

### 8.4.1 CfgCB

The `cfg_load` and `cfg_read` vendor-specific commands are passed down through the bulk pipe in the CBWCB portion of the CBW. The format of this CfgCB is shown below. Byte 0 will be a vendor-specific command designator whose value is configurable and set in the configuration data (EEPROM address 0x04). Byte 1 must be set to 0x26 to identify CfgCB. Byte 2 is reserved and must be set to zero. Byte 3 is used to determine the memory source to write/read. For the CY7C68300B/CY7C68301B, this byte must be set to 0x02, indicating the EEPROM is present. Bytes 4 and 5 are used to determine the start address. For the CY7C68300B/301B, this must always be 0x0000. Bytes 6 through 15 are reserved and must be set to zero.

The data transferred to the EEPROM must be in the format specified in *Table 8-6* of this data sheet. Maximum data transfer size is 255 bytes.

The data transfer length is determined by the CBW Data Transfer Length specified in bytes 8 through 11 (`dCBWDataTransferLength`) of the CBW (refer to *Table 8-1*). The type/direction of the command will be determined by the direction bit specified in byte 12, bit 7 (`bmCBWFlags`) of the CBW (refer to *Table 8-1*).

**Table 8-1. Command Block Wrapper**

| Offset         | Bits                   |          |              |   |              |   |   |   |
|----------------|------------------------|----------|--------------|---|--------------|---|---|---|
|                | 7                      | 6        | 5            | 4 | 3            | 2 | 1 | 0 |
| 0–3            | DCBWSignature          |          |              |   |              |   |   |   |
| 4–7            | dCBWTag                |          |              |   |              |   |   |   |
| 8–11 (08h–0Bh) | dCBWDataTransferLength |          |              |   |              |   |   |   |
| 12 (0Ch)       | bwCBWFLAGS             |          |              |   |              |   |   |   |
|                | Dir                    | Obsolete | Reserved (0) |   |              |   |   |   |
| 13 (0Dh)       | Reserved (0)           |          |              |   | bCBWLUN      |   |   |   |
| 14 (0Eh)       | Reserved (0)           |          |              |   | bCBWCBLength |   |   |   |
| 15–30 (0Fh1Eh) | CBWCB (CfgCB or MfgCB) |          |              |   |              |   |   |   |

**Table 8-2. Example CfgCB**

| Offset | CfgCB Byte Descriptions                     | Bits |   |   |   |   |   |   |   |
|--------|---|------|---|---|---|---|---|---|---|
|        |   | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0      | bVSCBSignature (set in configuration bytes) | 0    | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1      | bVSCBSubCommand (must be 0x26)              | 0    | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 2      | Reserved (must be set to zero)              | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3      | Data Source (must be set to 0x02)           | 0    | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 4      | Start Address (LSB) (must be set to zero)   | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5      | Start Address (MSB) (must be set to zero)   | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6–15   | Reserved (must be set to zero)              | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 |





### 8.4.2 MfgCB

The `mfg_load` and `mfg_read` vendor-specific commands will be passed down through the bulk pipe in the CBWCB portion of the CBW. The format of this MFGCB is shown below. Byte 0 is a vendor-specific command designator whose value is configurable and set in the configuration data. Byte 1 must be 0x27 to identify MfgCB. Byte 2–15 are reserved and must be set to zero.

The data transfer length will be determined by the CBW Data Transfer Length specified in bytes 8 through 11 (`dCBWDataTransferLength`) of the CBW. The type/direction of the command is determined by the direction bit specified in byte 12, bit 7 (`bmCBWFlags`) of the CBW.

**Table 8-3. Example MfgCB**

| Offset | MfgCB Byte Description                        | Bits |   |   |   |   |   |   |   |
|--------|---|------|---|---|---|---|---|---|---|
|        |   | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0      | 0 bVSCBSignature (set in configuration bytes) | 0    | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1      | 1 bVSCBSubCommand (hardcoded 0x27)            | 0    | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 2–15   | 2–15 Reserved (must be zero)                  | 0    | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### 8.4.2.1 Mfg\_load

During a `mfg_load`, the CY7C68300B/CY7C68301B goes into Manufacturing Test Mode. Manufacturing Test Mode is provided as a means to implement board or system level interconnect tests. During Manufacturing Test Mode operation, all outputs not directly associated with USB operation are controllable. Normal control of the output pins are disabled. Control of the select AT2LP IO pins and their three-state controls are mapped to the ATAPI data packet associated with this request. (See *Table 8-4* for an explanation of the required `Mfg_load` data format.) This requires a write of seven bytes. To exit Manufacturing Test Mode, a hard reset (RESET#) is required.

**Table 8-4. Mfg\_load Data Format**

| Byte | Bit(s) | Function  |
|------|--------|---|
| 0    | 7      | ARESET#   |
|      | 6      | Reserved  |
|      | 5:4    | CS#[1:0]  |
|      | 3:1    | DA[2:0]   |
|      | 0      | Reserved  |
| 1    | 7      | DD[15:0] Three-state (0 = Hi-Z all DD pins, 1 = drive DD pins). |
|      | 3:6    | Reserved  |
|      | 2      | DMACK#  |
|      | 1      | DIOR#   |
|      | 0      | DIOW#   |

**Table 8-4. Mfg\_load Data Format (continued)**

| Byte | Bit(s) | Function                 |
|------|--------|--------------------------|
| 2    | 7:0    | DD[7:0]                  |
| 3    | 7:0    | DD[15:8]                 |
| 4    | 7:6    | Reserved                 |
|      | 5:0    | GPIO Output Enable [5:0] |
| 5    | 7:6    | Reserved                 |
|      | 5:0    | GPIO Output Data [5:0]   |
| 6    | 7:0    | Reserved                 |

#### 8.4.2.2 Mfg\_read

This USB request returns a “snapshot in time” of select AT2LP input pins. AT2LP input pins not directly associated with USB operation, can be sampled at any time during Manufacturing Test Mode operation. See *Table 8-5* for an explanation of the `mfg_read` data format. The data length shall always be eight bytes.

**Table 8-5. Mfg\_read Data Format**

| Byte | Bit(s) | Data                                   |
|------|--------|--|
| 0    | 7      | ARESET# (output value only)            |
|      | 6      | VBUS_ATA_ENABLE                        |
|      | 5:1    | Reserved. This data should be ignored. |
|      | 0      | INTRQ                                  |
| 1    | 7      | DD[15:0] Three-state                   |
|      | 6      | Reserved. This data should be ignored. |
|      | 5      | Reserved. This data should be ignored. |
|      | 4      | DMARQ                                  |
| 1    | 3      | IORDY                                  |
|      | 2:0    | Reserved. This data should be ignored. |
| 2    | 7:0    | DD[7:0]                                |
| 3    | 7:0    | DD[15:8]                               |
| 4    | 7:6    | Reserved                               |
|      | 5:0    | GPIO Output Enable [5:0]               |
| 5    | 7:6    | Reserved                               |
|      | 5:0    | GPIO Output Data [5:0]                 |
| 6    | 7:0    | Reserved. This data should be ignored. |
| 7    | 7:0    | Reserved. This data should be ignored. |



## 8.5 EEPROM Organization

The contents of the 256-byte (2048-bit) I<sup>2</sup>C EEPROM are arranged as follows. In *Table 8-6*, the column labeled “Required Contents” contains the values that must be used for proper operation of the AT2LP. The column labeled “Suggested Contents” contains suggested values for the bytes that are defined by the customer. Some values, such as the Vendor ID, Product ID and device serial number, must be customized to meet USB compliance. The “AT2LP blaster” tool on the CY4615B CD can be used to edit and program these values into an AT2LP-based product (refer to *Figure 8-2*). The “AT2LP primer” tool can be used to program AT2LP-based

products in a manufacturing environment. See section 8.4 for details on how to use vendor-specific ATAPI commands to read and program the EEPROM.

The address pins on the serial EEPROM must be set such that the EEPROM is at address 2 (A0=0, A1=1, A2=0) or address 4 (A0=0, A1=0, A2=1) for memories that are internally byte-addressed memories.

**Note:** Devices running in Backward Compatibility Mode should use the 68300A EEPROM organization, and not the 68300B/301B/320/321 format shown in this document.

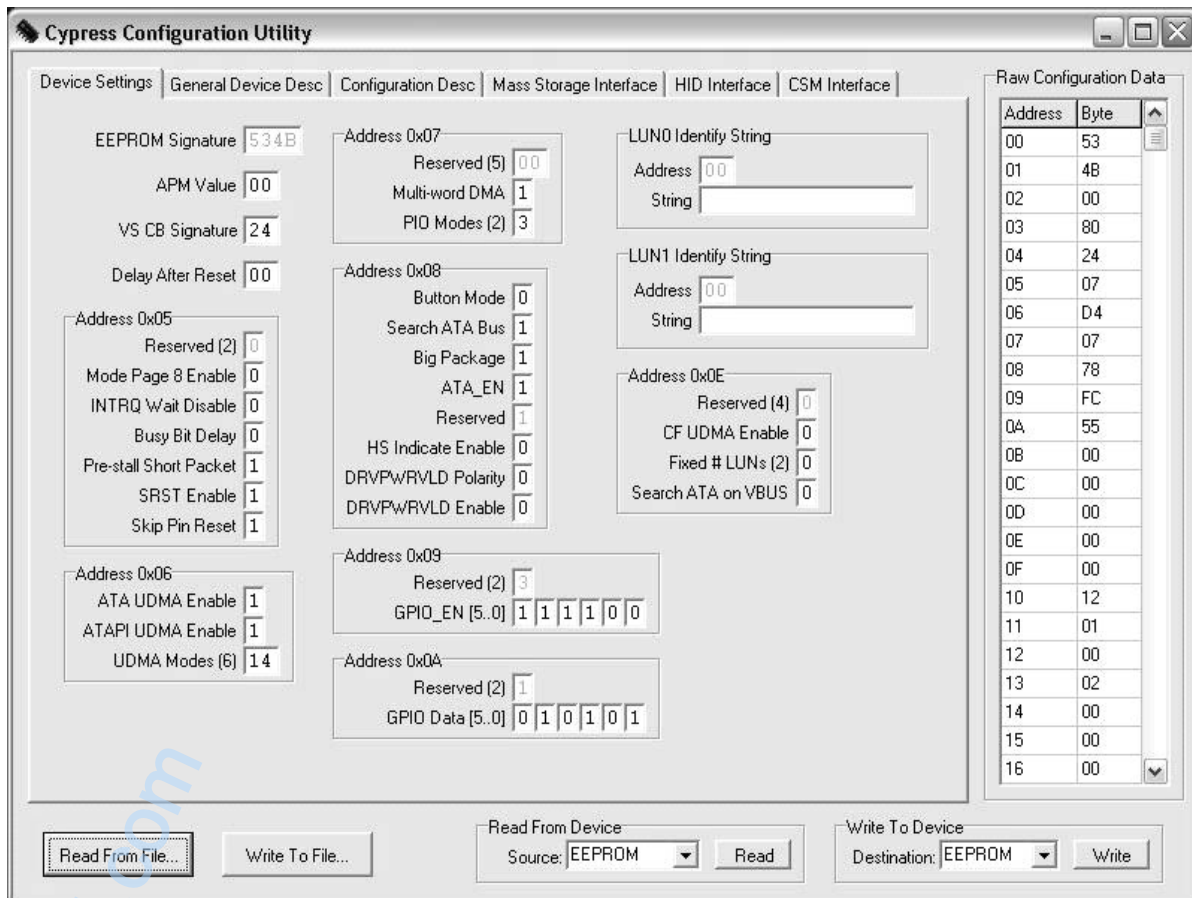


Figure 8-2. “AT2LP Blaster” Tool Screen


**Table 8-6. EEPROM Organization**

| EEPROM Address             | Field Name   | Field Description  | Required Contents | Suggested Contents |
|----------------------------|--|--|-------------------|--------------------|
| <b>AT2LP Configuration</b> |  |  |                   |                    |
| 0x00                       | I <sup>2</sup> C EEPROM signature byte 0   | I <sup>2</sup> C EEPROM signature byte 0. This byte must be 0x53. For CY7C68300A compatibility mode, these bytes should be set to 0x4D4D.  | 0x53              |                    |
| 0x01                       | I <sup>2</sup> C EEPROM signature byte 1   | I <sup>2</sup> C EEPROM signature byte 1. This byte must be 0x4B   | 0x4B              |                    |
| 0x02                       | APM Value  | ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the AT2LP will issue a SET_FEATURES command to Enable APM with this value during the drive initialization process. Setting APM Value to 0x00 disables this functionality. This value is ignored with ATAPI devices.   |                   | 0x00               |
| 0x03                       | Unused   |  |                   | 0x80               |
| 0x04                       | bVSCBSignature Value   | Value in the first byte of the CBW CB field that designates that the CB is to be decoded as vendor specific ATA commands instead of the ATAPI command block. See section 7.0 for more detail on how this byte is used.   |                   | 0x24               |
| 0x05                       | Reserved<br>Enable mode page 8<br><br>Disable wait for INTRQ<br><br>BUSY Bit Delay<br><br>Short Packet Before Stall<br><br>SRST Enable<br><br>Skip Pin Reset | Bits (7:6)<br><br>Bit (5)<br>Set to 1 to enable the write caching mode page (page 8). If this page is enabled, Windows will disable write caching by default which will limit write performance.<br><br>Bit (4)<br>Set to 1 to poll status register rather than waiting for INTRQ. Setting this bit to 1 will improve USB BOT test results but may introduce compatibility problems with some devices.<br><br>Bit (3)<br>Enables a delay of up to 120 ms at each read of the DRQ bit where the device data length does not match the host data length. This allows the CY7C68300B/CY7C68301B to work with most devices that incorrectly clear the BUSY bit before a valid status is present.<br><br>Bit (2)<br>Determines if a short packet is sent prior to the STALL of an IN endpoint. The <i>USB Mass Storage Class Bulk-Only Specification</i> allows a device to send a short or zero-length IN packet prior to returning a STALL handshake for certain cases. Certain host controller drivers may require a short packet prior to STALL.<br>1 = Force a short packet before STALL.<br>0 = Don't force a short packet before STALL.<br><br>Bit (1)<br>Determines if the AT2LP is to do an SRST reset during drive initialization. At least one reset must be enabled. Do not set SRST to 0 and Skip Pin Reset to 1 at the same time.<br>1 = Perform SRST during initialization.<br>0 = Don't perform SRST during initialization.<br><br>Bit (0)<br>Skip ARESET# assertion. When this bit is set, the AT2LP will bypass ARESET# during any initialization other than power up. Do not set SRST to 0 and Skip Pin Reset to 1 at the same time.<br>0 = Allow ARESET# assertion for all resets.<br>1 = Disable ARESET# assertion except for power-on reset cycles. |                   | 0x07               |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address | Field Name   | Field Description  | Required Contents | Suggested Contents |
|----------------|--|--|-------------------|--------------------|
| 0x06           | ATA UDMA Enable<br><br>ATAPI UDMA Enable<br><br>UDMA Modes                 | Bit (7)<br>Enable Ultra DMA data transfer support for ATAPI devices. If enabled, and if the ATAPI device reports UDMA support for the indicated modes, the AT2LP will utilize UDMA data transfers at the highest negotiated rate possible.<br>0 = Disable ATA device UDMA support.<br>1 = Enable ATA device UDMA support.<br><br>Bit (6)<br>Enable Ultra DMA data transfer support for ATAPI devices. If enabled, and if the ATAPI device reports UDMA support for the indicated modes, the AT2LP will utilize UDMA data transfers at the highest negotiated rate possible.<br>0 = Disable ATAPI device UDMA support.<br>1 = Enable ATAPI device UDMA support.<br><br>Bit (5:0)<br>These bits select which UDMA modes, if supported, are enabled. Setting to 1 enables. Multiple bits may be set. The AT2LP will operate in the highest enabled UDMA mode supported by the device. The AT2LP supports UDMA modes 2, 3, and 4 only.<br>Bit Descriptions<br>5 Reserved. Must be set to 0.<br>4 Enable UDMA mode 4.<br>3 Reserved. Must be set to 0.<br>2 Enable UDMA mode 2.<br>1 Reserved. Must be set to 0.<br>0 Reserved. Must be set to 0. |                   | 0xD4               |
| 0x07           | Reserved<br><br>Multiword DMA mode<br><br>PIO Modes                        | Bits(7:3)<br>Must be set to 0.<br>Bit (2)<br>This bit selects multi-word DMA. If this bit is set and the drive supports it, multi-word DMA is used.<br>Bits(1:0)<br>These bits select which PIO modes, if supported, are enabled. Setting to 1 enables. Multiple bits may be set. The AT2LP will operate in the highest enabled PIO mode supported by the device. The AT2LP supports PIO modes 0, 3, and 4 only. PIO mode 0 is always enabled by internal logic.<br>Bit Descriptions<br>1 Enable PIO mode 4.<br>0 Enable PIO mode 3.   |                   | 0x07               |
| 0x08           | Pin Configurations<br>BUTTON_MODE<br><br>SEARCH_ATA_BUS<br><br>BIG_PACKAGE | Bit (7)<br>Button mode. Set this bit to 1 to enable ATAPUEN, PWR500# and DRVPWRVLD to become button inputs returned on bits 2, 1, and 0 of EP1IN<br><br>Bit (6)<br>Enables a search performed at RESET to detect non-removable ATA and ATAPI devices. Systems with only a removable device (like CF readers) will set this bit to 0. Systems with one removable device and one non-removable device will set this bit to 1.<br><br>Bit (5)<br>Package Select. Set this bit to 1 when using the 100-pin device.   |                   | 0x78               |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address | Field Name                           | Field Description  | Required Contents | Suggested Contents |
|----------------|--------------------------------------|--|-------------------|--------------------|
|                | ATA_EN                               | Bit (4)<br>ATA sharing enable. Allows ATA bus sharing with other host devices. If ATA_EN=1 the ATA interface will be driven when VBUS_ATA_ENABLE is LOW. If ATA_EN=0 the ATA interface will be placed into Hi-Z state whenever VBUS_ATA_ENABLE is LOW.<br>'0' = ATA signals Hi-Z when VBUS_ATA_ENABLE is LOW.<br>'1' = ATA signals driven when VBUS_ATA_ENABLE is LOW. |                   |                    |
|                | DISKRDY Polarity                     | Bit (3)<br>DISKRDY active polarity.<br>'0' = Active LOW polarity.<br>'1' = Active HIGH polarity.   |                   |                    |
|                | HS Indicator Enable                  | Bit (2)<br>Enables GPIO2_nHS pin to indicate the current operating speed of the device (if output is enabled).<br>'0' = Normal GPIO operation.<br>'1' = High-speed indicator enable.   |                   |                    |
|                | Drive Power Valid Polarity           | Bit (1)<br>Controls the polarity of DRVPWRVLD pin<br>'0' = Active LOW ("connector ground" indication)<br>'1' = Active HIGH (power indication from device)  |                   |                    |
|                | Drive Power Valid Enable             | Bit (0)<br>Enable for the DRVPWRVLD pin. When this pin is enabled, the AT2LP will enumerate a removable IDE device (normally CompactFlash) as the master device.<br>'0' = pin disabled (most systems)<br>'1' = pin enabled (CompactFlash systems)  |                   |                    |
| 0x09           | Reserved                             | Bits (7:6)<br>Must be set to zero.   |                   | 0x00               |
|                | General Purpose IO Pin Output Enable | Bits (5:0)<br>GPIO[5:0] Hi-Z control.<br>'0' = Output enabled (GPIO pin is an output).<br>'1' = Hi-Z (GPIO pin is an input).   |                   |                    |
| 0x0A           | Reserved                             | Bits (7:6)<br>Must be set to zero.   |                   | 0x00               |
|                | General Purpose IO Pin Data          | Bits (5:0)<br>If the output enable bit is set, these bits select the value driven on the GPIO pins.  |                   |                    |
| 0x0B           | Identify Device String Pointer LUN0  | If this value is 00, the Identify Device data will be taken from the device. If this string is non-zero, it is used as a pointer to a 24 byte ASCII (non-Unicode) string in the EEPROM. This string will be used as the device identifier. This string is used by many operating systems as the user-visible name for the device.                                      |                   | 0x00               |
| 0x0C           | Identify Device String Pointer LUN1  |  |                   | 0x00               |
| 0x0D           | Delay after reset                    | Number of 20-ms ticks to wait between RESET and attempting to access the drive.  |                   | 0x00               |
| 0x0E           | Reserved                             | Bits (7:4)   |                   | 0x00               |
|                | Enable CF UDMA                       | Bit (3)<br>'1' = Allow UDMA to be used with removable-media devices<br>'0' = UDMA will not be used with removable-media devices<br>Some CF devices will interfere with UDMA if the UDMA lines are connected to them. This bit tells the AT2LP if the UDMA lines are connected to the removable-media device.   |                   |                    |
|                | Fixed number of logical units = 2    | Bit (2)<br>If bits 1 and 2 are both 0, the number of logical units will be determined by searching the ATA and CF buses for devices.   |                   |                    |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address           | Field Name  | Field Description  | Required Contents | Suggested Contents  |
|--------------------------|---|--|-------------------|---------------------|
|                          | Fixed number of logical units = 1<br><br>Search ATA on VBUS removed | Bit (1)<br>If bits 1 and 2 are both 0, the number of logical units will be determined by searching the ATA and CF buses for devices.<br><br>Bit (0)<br>Search for ATA devices when VBUS returns. If this bit is set, the ATA bus will be searched for ATA devices every time AT2LP is plugged into a computer. |                   |                     |
| 0x0F                     | Reserved  | Must be set to 0x00.   | 0x00              |                     |
| <b>Device Descriptor</b> |   |  |                   |                     |
| 0x10                     | bLength   | Length of device descriptor in bytes.  | 0x12              |                     |
| 0x11                     | bDescriptor Type  | Descriptor type.   | 0x01              |                     |
| 0x12                     | bcdUSB (LSB)  | USB Specification release number in BCD.   | 0x00              |                     |
| 0x13                     | bcdUSB (MSB)  |  | 0x02              |                     |
| 0x14                     | bDeviceClass  | Device class.  | 0x00              |                     |
| 0x15                     | bDeviceSubClass   | Device subclass.   | 0x00              |                     |
| 0x16                     | bDeviceProtocol   | Device protocol.   | 0x00              |                     |
| 0x17                     | bMaxPacketSize0   | USB packet size supported for default pipe.  | 0x40              |                     |
| 0x18                     | idVendor (LSB)  | Vendor ID. Cypress's Vendor ID may only be used for evaluation purposes, and not in released products.   |                   | Your Vendor ID      |
| 0x19                     | idVendor (MSB)  |  |                   |                     |
| 0x1A                     | idProduct (LSB)   | Product ID.  |                   | Your Product ID     |
| 0x1B                     | idProduct (MSB)   |  |                   |                     |
| 0x1C                     | bcdDevice (LSB)   | Device release number in BCD LSB (product release number).   |                   | Your release number |
| 0x1D                     | bcdDevice (MSB)   | Device release number in BCD MSB (silicon release number).   |                   |                     |
| 0x1E                     | iManufacturer   | Index to manufacturer string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.  |                   | 0x53                |
| 0x1F                     | iProduct  | Index to product string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.   |                   | 0x69                |
| 0x20                     | iSerialNumber   | Index to serial number string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist. The USB <i>Mass Storage Class Bulk-Only Transport Specification</i> requires a unique serial number (in upper case, hexadecimal characters) for each device.      |                   | 0x75                |
| 0x21                     | bNumConfigurations  | Number of configurations supported.<br>1 for mass storage; 2 for HID; 3 for CSM  |                   | 0x03                |
| <b>Device Qualifier</b>  |   |  |                   |                     |
| 0x22                     | bLength   | Length of device descriptor in bytes.  | 0x0A              |                     |
| 0x23                     | bDescriptor   | Type Descriptor type.  | 0x06              |                     |
| 0x24                     | bcdUSB (LSB)  | USB Specification release number in BCD.   | 0x00              |                     |
| 0x25                     | bcdUSB (MSB)  | USB Specification release number in BCD.   | 0x02              |                     |
| 0x26                     | bDeviceClass  | Device class.  | 0x00              |                     |
| 0x27                     | bDeviceSubClass   | Device subclass.   | 0x00              |                     |
| 0x28                     | bDeviceProtocol   | Device protocol.   | 0x00              |                     |
| 0x29                     | bMaxPacketSize0   | USB packet size supported for default pipe.  | 0x40              |                     |
| 0x2A                     | bNumConfigurations  | Number of configurations supported.  | 0x01              |                     |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address                            | Field Name           | Field Description  | Required Contents | Suggested Contents |
|---|----------------------|--|-------------------|--------------------|
| 0x2B                                      | bReserved            | Reserved for future use. Must be set to zero.  | 0x00              |                    |
| <b>Configuration Descriptor</b>           |                      |  |                   |                    |
| 0x2C                                      | bLength              | Length of configuration descriptor in bytes.   | 0x09              |                    |
| 0x2D                                      | bDescriptorType      | Descriptor type.   | 0x02              |                    |
| 0x2E                                      | bTotalLength (LSB)   | Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.  | 0x20              |                    |
| 0x2F                                      | bTotalLength (MSB)   |  | 0x00              |                    |
| 0x30                                      | bNumInterfaces       | Number of interfaces supported.  |                   | 0x01               |
| 0x31                                      | bConfiguration Value | The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x01.  | 0x01              |                    |
| 0x32                                      | iConfiguration       | Index to the configuration string. This entry must equal half of the address value where the string starts, or 0x00 if the string does not exist.  |                   | 0x00               |
| 0x33                                      | bmAttributes         | Device attributes for this configuration.<br>Bit (7) Reserved. Must be set to 1.<br>Bit (6) Self-powered. Must be set to 1.<br>Bit (5) Remote wake-up. Must be set to 0.<br>Bits (4–0) Reserved. Must be set to 0.   | 0xC0              |                    |
| 0x34                                      | bMaxPower            | Maximum power consumption for this configuration. Units used are mA*2 (i.e., 0x31 = 98 mA, 0xF9 = 498 mA). 0x00 reported for self-powered devices.<br><br><b>Note:</b> A value of 0x00 or 0x01 results in the 56-pin package configuring itself for self-powered mode, whereas a value greater than 0x01 results in the 56-pin package reporting itself as bus-powered. This is regardless of what address 0x33 is set to reflect in the 56-pin package. |                   | 0x01               |
| <b>Interface and Endpoint Descriptors</b> |                      |  |                   |                    |
| <i>Interface Descriptor</i>               |                      |  |                   |                    |
| 0x35                                      | bLength              | Length of interface descriptor in bytes.   | 0x09              |                    |
| 0x36                                      | bDescriptorType      | Descriptor type.   | 0x04              |                    |
| 0x37                                      | bInterfaceNumber     | Interface number.  | 0x00              |                    |
| 0x38                                      | bAlternateSetting    | Alternate setting.   | 0x00              |                    |
| 0x39                                      | bNumEndpoints        | Number of endpoints.   | 0x02              |                    |
| 0x3A                                      | bInterfaceClass      | Interface class.   | 0x08              |                    |
| 0x3B                                      | bInterfaceSubClass   | Interface subclass.  |                   | 0x06               |
| 0x3C                                      | bInterfaceProtocol   | Interface protocol.  | 0x50              |                    |
| 0x3D                                      | iInterface           | Index to first interface string. This entry must equal half of the address value where the string starts or 0x00 if the string does not exist.   |                   | 0x00               |
| <i>USB Bulk Out Endpoint</i>              |                      |  |                   |                    |
| 0x3E                                      | bLength              | Length of this descriptor in bytes.  | 0x07              |                    |
| 0x3F                                      | bDescriptorType      | Endpoint descriptor type.  | 0x05              |                    |
| 0x40                                      | bEndpointAddress     | This is an Out endpoint, endpoint number 2.  | 0x02              |                    |
| 0x41                                      | bmAttributes         | This is a bulk endpoint.   | 0x02              |                    |
| 0x42                                      | wMaxPacketSize (LSB) | Max data transfer size. To be set by speed (Full speed 0x0040; High speed 0x0200)  |                   | 0x00               |
| 0x43                                      | wMaxPacketSize (MSB) |  |                   | 0x02               |
| 0x44                                      | bInterval            | High-speed interval for polling (maximum NAK rate). Set to zero for full speed.  | 0x00              |                    |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address                             | Field Name              | Field Description   | Required Contents | Suggested Contents |
|--|-------------------------|---|-------------------|--------------------|
| <b>USB Bulk In Endpoint</b>                |                         |   |                   |                    |
| 0x45                                       | bLength                 | Length of this descriptor in bytes.   | 0x07              |                    |
| 0x46                                       | bDescriptorType         | Endpoint descriptor type.   | 0x05              |                    |
| 0x47                                       | bEndpointAddress        | This is an In endpoint, endpoint number 8.  | 0x88              |                    |
| 0x48                                       | bmAttributes            | This is a bulk endpoint.  | 0x02              |                    |
| 0x49                                       | wMaxPacketSize (LSB)    | Max data transfer size. Automatically set by AT2 (Full speed 0x0040; High speed 0x0200) |                   | 0x00               |
| 0x4A                                       | wMaxPacketSize (MSB)    |   |                   | 0x02               |
| 0x4B                                       | bInterval               | High-speed interval for polling (maximum NAK rate). Set to zero for full speed.         | 0x00              |                    |
| <b>(Optional) HID Interface Descriptor</b> |                         |   |                   |                    |
| 0x4C                                       | bLength                 | Length of HID interface descriptor  | 0x09              |                    |
| 0x4D                                       | bDescriptorTypes        | Interface descriptor type   | 0x04              |                    |
| 0x4E                                       | bInterfaceNumber        | Number of interfaces (2)  | 0x02              |                    |
| 0x4F                                       | bAlternateSetting       | Alternate setting   | 0x00              |                    |
| 0x50                                       | bNumEndpoints           | Number of endpoints used by this interface  | 0x01              |                    |
| 0x51                                       | bInterfaceClass         | Class code  | 0x03              |                    |
| 0x52                                       | bInterfaceSubClass      | Sub class   | 0x00              |                    |
| 0x53                                       | bInterfaceSubSubClass   | sub sub class   | 0x00              |                    |
| 0x54                                       | iInterface              | Index of string descriptor  | 0x00              |                    |
| <b>USB Interrupt In Endpoint</b>           |                         |   |                   |                    |
| 0x5E                                       | bLength                 | Length of this descriptor in bytes.   | 0x07              |                    |
| 0x5F                                       | bDescriptorType         | Endpoint descriptor type.   | 0x05              |                    |
| 0x60                                       | bEndpointAddress        | This is an In endpoint, endpoint number 1.  | 0x81              |                    |
| 0x61                                       | bmAttributes            | This is an interrupt endpoint.  | 0x03              |                    |
| 0x62                                       | wMaxPacketSize (LSB)    | Max data transfer size.   | 0x02              |                    |
| 0x63                                       | wMaxPacketSize (MSB)    |   | 0x00              |                    |
| 0x64                                       | bInterval               | Interval for polling (max. NAK rate).   |                   | 0x10               |
| <b>(Optional) HID Descriptor</b>           |                         |   |                   |                    |
| 0x55                                       | bLength                 | Length of HID descriptor  | 0x09              |                    |
| 0x56                                       | bDescriptorType         | Descriptor Type HID   | 0x21              |                    |
| 0x57                                       | bcdHID (LSB)            | HID Class Specification release number (1.10)   | 0x10              |                    |
| 0x58                                       | bcdHID (MSB)            |   | 0x01              |                    |
| 0x59                                       | bCountryCode            | Country Code  | 0x00              |                    |
| 0x5A                                       | bNumDescriptors         | Number of class descriptors (1 report descriptor)                                       | 0x01              |                    |
| 0x5B                                       | bDescriptorType         | Descriptor Type   | 0x22              |                    |
| 0x5C                                       | wDescriptorLength (LSB) | Length of HID report descriptor   | 0x22              |                    |
| 0x5D                                       | wDescriptorLength (MSB) |   | 0x00              |                    |
| <b>Terminator Descriptors</b>              |                         |   |                   |                    |
| 0x65                                       | Terminator              |   | 0x00              |                    |
| <b>(Optional) HID Report Descriptor</b>    |                         |   |                   |                    |
| 0x66                                       | Usage_Page              | Vendor defined - FFA0   | 0x06              |                    |
| 0x67                                       |                         |   | 0xA0              |                    |
| 0x68                                       |                         |   | 0xFF              |                    |




**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address   | Field Name         | Field Description  | Required Contents | Suggested Contents |
|--|--------------------|--|-------------------|--------------------|
| 0x69   | Usage              | Vendor defined   | 0x09              |                    |
| 0x6A   |                    |  | 0xA5              |                    |
| 0x6B   | Collection         | Application  | 0xA1              |                    |
| 0x6C   |                    |  | 0x01              |                    |
| 0x6D   | Usage              | Vendor defined   | 0x09              |                    |
| 0x6E   |                    |  | 0xA6              |                    |
| <b>Input Report</b>  |                    |  |                   |                    |
| 0x6F   | Usage              | Vendor defined   | 0x09              |                    |
| 0x70   |                    |  | 0xA7              |                    |
| 0x71   | Logical_Minimum    | -128   | 0x15              |                    |
| 0x72   |                    |  | 0x80              |                    |
| 0x73   | Logical_Maximum    | 127  | 0x25              |                    |
| 0x74   |                    |  | 0x7F              |                    |
| 0x75   | Report_Size        | 8 bits   | 0x75              |                    |
| 0x76   |                    |  | 0x08              |                    |
| 0x77   | Report_Count       | 2 fields   | 0x95              |                    |
| 0x78   |                    |  | 0x02              |                    |
| 0x79   | Input              | Input (Data, Variable, Absolute)   | 0x81              |                    |
| 0x7A   |                    |  | 0x02              |                    |
| <b>Output Report</b>   |                    |  |                   |                    |
| 0x7B   | Usage              | Usage - vendor defined   | 0x09              |                    |
| 0x7C   |                    |  | 0xA9              |                    |
| 0x7D   | Logical_Minimum    | Logical Minimum (-128)   | 0x15              |                    |
| 0x7E   |                    |  | 0x80              |                    |
| 0x7F   | Logical_Maximum    | Logical Maximum (127)  | 0x25              |                    |
| 0x80   |                    |  | 0x7F              |                    |
| 0x81   | Report_Size        | Report Size 8 bits   | 0x75              |                    |
| 0x82   |                    |  | 0x08              |                    |
| 0x83   | Report_Count       | Report Count 2 fields  | 0x95              |                    |
| 0x84   |                    |  | 0x02              |                    |
| 0x85   | Output             | Output (Data, Variable, Absolute)  | 0x91              |                    |
| 0x86   |                    |  | 0x02              |                    |
| 0x87   |                    | End Collection   | 0xC0              |                    |
| <b>(optional) Standard Content Security Interface Descriptor</b> |                    |  |                   |                    |
| 0x88   | bLength            | Byte length of this descriptor   | 0x09              |                    |
| 0x89   | bDescriptorType    | Interface Descriptor type  | 0x0D              |                    |
| 0x8A   | bInterfaceNumber   | Number of interface.   | 0x02              |                    |
| 0x8B   | bAlternateSetting  | Value used to select an alternate setting for the interface identified in prior field    |                   |                    |
| 0x8C   | bNumEndpoints      | Number of endpoints used by this interface (excluding endpoint 0) that are CSM dependent | 0x02              |                    |
| 0x8D   | bInterfaceClass    |  |                   | 0x0D               |
| 0x8E   | bInterfaceSubClass | Must be set to zero  | 0x00              |                    |
| 0x8F   | bInterfaceProtocol | Must be set to zero  | 0x00              |                    |
| 0x90   | iInterface         | Index of a string descriptor that describes this Interface                               |                   |                    |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address                                | Field Name            | Field Description   | Required Contents | Suggested Contents |
|---|-----------------------|---|-------------------|--------------------|
| <b>Channel Descriptor</b>                     |                       |   |                   |                    |
| 0x91  | bLength               | Byte length of this descriptor  | 0x09              |                    |
| 0x92  | bDescriptorType       | channel descriptor type   | 0x22              |                    |
| 0x93  | bChannelID            | Number of the channel, must be a zero based value that is unique across the device  |                   |                    |
| 0x94  | bmAttributes          | Bits(7:5)<br>Must be set to 0.  |                   |                    |
| 0x95  |                       | Bit (4:0)<br>0 = Not used<br>1 = Interface<br>2 = Endpoint<br>3...31 = Reserved values  |                   |                    |
| 0x96  | bRecipient            | Identifier of the target recipient<br>If Recipient type field of bmAttributes = 1 then bRecipient field is the bInterfaceNumber<br>If Recipient type field of bmAttributes = 2 then bRecipient field is an endpoint address, where:<br>D7: Direction (0 = Out, 1 = IN)<br>D6...D4: reserved and set to zero<br>D3...D0: Endpoint number |                   |                    |
| 0x97  | bRecipientAlt         | alternate setting for the interface to which this channel applies   | 0x00              |                    |
| 0x98  | bRecipientLogicalUnit | Recipient Logical Unit  |                   |                    |
| 0x99  | bMethod               | Index of a class-specific CSM descriptor That describes one of the Content Security Methods (CSM) offered by the device   |                   |                    |
| 0x9A  | bMethodVariant        | CSM Variant descriptor  |                   |                    |
| <b>CSM Descriptor</b>                         |                       |   |                   |                    |
| 0x9B  | bLength               | Byte length of this descriptor  | 0x06              |                    |
| 0x9C  | bDescriptorType       | CSM Descriptor type   | 0x23              |                    |
| 0x9D  | bMethodID             | Index of a class-specific CSM descriptor that describes one of the Content Security Methods offered by the device.  | 0x01              |                    |
| 0x9E  | iCSMDescriptor        | Index of string descriptor that describes the Content Security Method   |                   |                    |
| 0x9F  | bcdVersion (LSB)      | CSM Descriptor Version number   | 0x10              |                    |
| 0xA0  | bcsVersion (MSB)      |   | 0x02              |                    |
| 0xA1  | Terminator            |   | 0x00              |                    |
| <b>USB String Descriptor–Index 0 (LANGID)</b> |                       |   |                   |                    |
| 0xA2  | bLength               | LANGID string descriptor length in bytes.   | 0x04              |                    |
| 0xA3  | bDescriptorType       | Descriptor type.  | 0x03              |                    |
| 0xA4  | LANGID (LSB)          | Language supported. The CY7C68300B supports one LANGID value.   |                   | 0x09               |
| 0xA5  | LANGID (MSB)          |   |                   | 0x04               |
| <b>USB String Descriptor–Manufacturer</b>     |                       |   |                   |                    |
| 0xA6  | bLength               | String descriptor length in bytes (including bLength).  |                   | 0x2C               |
| 0xA7  | bDescriptorType       | Descriptor type.  | 0x03              |                    |
| 0xA8  | bString               | Unicode character LSB.  |                   | “C” 0x43           |
| 0xA9  | bString               | Unicode character MSB.  |                   | 0x00               |
| 0xAA  | bString               | Unicode character LSB.  |                   | “y” 0x79           |
| 0xAB  | bString               | Unicode character MSB.  |                   | 0x00               |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address                       | Field Name      | Field Description                                      | Required Contents | Suggested Contents |
|--------------------------------------|-----------------|--|-------------------|--------------------|
| 0xAC                                 | bString         | Unicode character LSB.                                 |                   | "p" 0x70           |
| 0xAD                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xAE                                 | bString         | Unicode character LSB.                                 |                   | "r" 0x72           |
| 0xAF                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xB0                                 | bString         | Unicode character LSB.                                 |                   | "e" 0x65           |
| 0xB1                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xB2                                 | bString         | Unicode character LSB.                                 |                   | "s" 0x73           |
| 0xB3                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xB4                                 | bString         | Unicode character LSB.                                 |                   | "s" 0x73           |
| 0xB5                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xB6                                 | bString         | Unicode character LSB.                                 |                   | " " 0x20           |
| 0xB7                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xB8                                 | bString         | Unicode character LSB.                                 |                   | "S" 0x53           |
| 0xB9                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xBA                                 | bString         | Unicode character LSB.                                 |                   | "e" 0x65           |
| 0xBB                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xBC                                 | bString         | Unicode character LSB.                                 |                   | "m" 0x6D           |
| 0xBD                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xBE                                 | bString         | Unicode character LSB.                                 |                   | "i" 0x69           |
| 0xBF                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xC0                                 | bString         | Unicode character LSB.                                 |                   | "c" 0x63           |
| 0xC1                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xC2                                 | bString         | Unicode character LSB.                                 |                   | "o" 0x6F           |
| 0xC3                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xC4                                 | bString         | Unicode character LSB.                                 |                   | "n" 0x6E           |
| 0xC5                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xC6                                 | bString         | Unicode character LSB.                                 |                   | "d" 0x64           |
| 0xC7                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xC8                                 | bString         | Unicode character LSB.                                 |                   | "u" 0x75           |
| 0xC9                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xCA                                 | bString         | Unicode character LSB.                                 |                   | "c" 0x63           |
| 0xCB                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xCC                                 | bString         | Unicode character LSB.                                 |                   | "t" 0x74           |
| 0xCD                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xCE                                 | bString         | Unicode character LSB.                                 |                   | "o" 0x6F           |
| 0xCF                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xD0                                 | bString         | Unicode character LSB.                                 |                   | "r" 0x72           |
| 0xD1                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| <b>USB String Descriptor–Product</b> |                 |  |                   |                    |
| 0xD2                                 | bLength         | String descriptor length in bytes (including bLength). |                   | 0x2C               |
| 0xD3                                 | bDescriptorType | Descriptor type.                                       | 0x03              |                    |
| 0xD4                                 | bString         | Unicode character LSB.                                 |                   | "U" 0x55           |
| 0xD5                                 | bString         | Unicode character MSB.                                 |                   | 0x00               |
| 0xD6                                 | bString         | Unicode character LSB.                                 |                   | "S" 0x53           |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address  | Field Name       | Field Description                                      | Required Contents | Suggested Contents |
|---|------------------|--|-------------------|--------------------|
| 0xD7  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xD8  | bString          | Unicode character LSB.                                 |                   | "B" 0x42           |
| 0xD9  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xDA  | bString          | Unicode character LSB.                                 |                   | "2" 0x32           |
| 0xDB  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xDC  | bString          | Unicode character LSB.                                 |                   | "." 0x2E           |
| 0xDD  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xDE  | bString          | Unicode character LSB.                                 |                   | "0" 0x30           |
| 0xDF  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xE0  | bString          | Unicode character LSB.                                 |                   | " " 0x20           |
| 0xE1  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xE2  | bString          | Unicode character LSB.                                 |                   | "D" 0x53           |
| 0xE3  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xE4  | bString          | Unicode character LSB.                                 |                   | "i" 0x74           |
| 0xE5  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xE6  | bString          | Unicode character LSB.                                 |                   | "s" 0x6F           |
| 0xE7  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xE8  | bString          | Unicode character LSB.                                 |                   | "k" 0x72           |
| 0xE9  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| <b>USB String Descriptor–Serial Number</b> (Note: The USB Mass Storage Class specification requires a unique serial number in each device. Not providing a unique serial number can cause the operating system to crash. The serial number must be at least 12 characters, but some USB hosts will only treat the last 12 characters of the serial number as unique.) |                  |  |                   |                    |
| 0xEA  | bLength          | String descriptor length in bytes (including bLength). |                   | 0x22               |
| 0xEB  | bDescriptor Type | Descriptor type.                                       | 0x03              |                    |
| 0xEC  | bString          | Unicode character LSB.                                 |                   | "1" 0x31           |
| 0xED  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xEE  | bString          | Unicode character LSB.                                 |                   | "2" 0x32           |
| 0xEF  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xF0  | bString          | Unicode character LSB.                                 |                   | "3" 0x33           |
| 0xF1  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xF2  | bString          | Unicode character LSB.                                 |                   | "4" 0x34           |
| 0xF3  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xF4  | bString          | Unicode character LSB.                                 |                   | "5" 0x35           |
| 0xF5  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xF6  | bString          | Unicode character LSB.                                 |                   | "6" 0x36           |
| 0xF7  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xF8  | bString          | Unicode character LSB.                                 |                   | "7" 0x37           |
| 0xF9  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xFA  | bString          | Unicode character LSB.                                 |                   | "8" 0x38           |
| 0xFB  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xFC  | bString          | Unicode character LSB.                                 |                   | "9" 0x39           |
| 0xFD  | bString          | Unicode character MSB.                                 |                   | 0x00               |
| 0xFE  | bString          | Unicode character LSB.                                 |                   | "0" 0x30           |
| 0xFF  | bString          | Unicode character MSB.                                 |                   | 0x00               |


**Table 8-6. EEPROM Organization** (continued)

| EEPROM Address  | Field Name          | Field Description  | Required Contents | Suggested Contents |
|---|---------------------|--|-------------------|--------------------|
| 0X100   | bString             | Unicode character LSB.                                     |                   | "A" 0x41           |
| 0X101   | bString             | Unicode character MSB.                                     |                   | 0x00               |
| 0X102   | bString             | Unicode character LSB.                                     |                   | "B" 0x42           |
| 0X103   | bString             | Unicode character MSB.                                     |                   | 0x00               |
| <b>Identify Device String (Note:</b> This is not a Unicode string. It is the ASCII string returned by the device in the Identify Device information. It is a fixed length (24 bytes). Changing this string may cause CD authoring software to incorrectly identify the device.) |                     |  |                   |                    |
| 0X104   | Device name byte 1  | ASCII Character  |                   | "C" 0x43           |
| 0X105   | Device name byte 2  | ASCII Character  |                   | "y" 0x79           |
| 0X106   | Device name byte 3  | ASCII Character  |                   | "p" 0x70           |
| 0X107   | Device name byte 4  | ASCII Character  |                   | "r" 0x72           |
| 0X108   | Device name byte 5  | ASCII Character  |                   | "e" 0x65           |
| 0X109   | Device name byte 6  | ASCII Character  |                   | "s" 0x73           |
| 0X10A   | Device name byte 7  | ASCII Character  |                   | "s" 0x73           |
| 0X10B   | Device name byte 8  | ASCII Character  |                   | " " 0x20           |
| 0X10C   | Device name byte 9  | ASCII Character  |                   | "C" 0x43           |
| 0X10D   | Device name byte 10 | ASCII Character  |                   | "u" 0x75           |
| 0X10E   | Device name byte 11 | ASCII Character  |                   | "s" 0x73           |
| 0X10F   | Device name byte 12 | ASCII Character  |                   | "t" 0x74           |
| 0X110   | Device name byte 13 | ASCII Character  |                   | "o" 0x6f           |
| 0X111   | Device name byte 14 | ASCII Character  |                   | "m" 0x6d           |
| 0X112   | Device name byte 15 | ASCII Character  |                   | " " 0x20           |
| 0X113   | Device name byte 16 | ASCII Character  |                   | "N" 0x4e           |
| 0X114   | Device name byte 17 | ASCII Character  |                   | "a" 0x61           |
| 0X115   | Device name byte 18 | ASCII Character  |                   | "m" 0x6d           |
| 0X116   | Device name byte 19 | ASCII Character  |                   | "e" 0x65           |
| 0X117   | Device name byte 20 | ASCII Character  |                   | " " 0x20           |
| 0X118   | Device name byte 21 | ASCII Character  |                   | "L" 0x4c           |
| 0X119   | Device name byte 22 | ASCII Character  |                   | "U" 0x55           |
| 0X11A   | Device name byte 23 | ASCII Character  |                   | "N" 0x4e           |
| 0X11B   | Device name byte 24 | ASCII Character  |                   | "O" 0x30           |
| 0x11C to 0x1FF  | Unused ROM Space    | Amount of unused ROM space will vary depending on strings. |                   | 0xFF               |

**Note:** More than 0X100 bytes of configuration are shown for example only. AT2LP only supports 0X100 total bytes.


**Table 8-7. EEPROM-related Vendor-specific Commands**

| Label            | bmRequestType | bRequest | wValue      | wIndex           | wLength     | Data               |
|------------------|---------------|----------|-------------|------------------|-------------|--------------------|
| LOAD_CONFIG_DATA | 0x40          | 0x01     | 0x0000      | 30x02 – 0x0F     | Data Length | Configuration Data |
| READ_CONFIG_DATA | 0xC0          | 0x02     | Data Source | Starting Address | Data Length | Configuration Data |

## 8.6 Programming the EEPROM

There are three methods to program the EEPROM:

- External device programmer
- USB commands listed in *Table 8-7*
- In-system programming on a bed-of-nails tester.

Any vendor-specific USB write request to the Serial ROM device configuration space will simultaneously update internal configuration register values as well. If the I<sup>2</sup>C device is programmed without vendor specific USB commands, AT2LP must be synchronously reset (RESET#) before configuration data is reloaded.

The AT2LP supports a subset of the “slow mode” specification (100 KHz) required for 24LCXXB EEPROM family device support. Features such as “Multi-Master,” “Clock Synchronization” (the SCL pin is output only), “10-bit addressing,” and “CBUS device support” are not supported. Vendor-specific USB commands allow the AT2LP to address up to 256 bytes of data.

### 8.6.1 LOAD\_CONFIG\_DATA

This request enables configuration data writes to the AT2LP’s configuration space. The wIndex field specifies the starting address and the wLength field denotes the data length in bytes.

Legal values for wValue are as follows:

- 0x0000 Configuration bytes, address range 0x2 – 0xF
- 0x0002 External I<sup>2</sup>C memory device

Configuration-byte writes must be constrained to addresses 0x2 through 0xF, as shown in *Table 8-7*. Attempts to write outside this address space will result in undefined operation. Configuration-byte writes only overwrite AT2LP Configuration Byte registers, the original data source (I<sup>2</sup>C memory device) remains unchanged.

### 8.6.2 READ\_CONFIG\_DATA

This USB request allows data retrieval from the data source specified by the wValue field. Data is retrieved beginning at the

address specified by the wIndex field. The wLength field denotes the length in bytes of data requested from the data source.

Legal values for wValue are as follows:

- 0x0000 Configuration bytes, addresses 0x0 – 0xF only
- 0x0002 External I<sup>2</sup>C memory device

Illegal values for wValue will result in undefined operation. Attempted reads from an I<sup>2</sup>C memory device when none is connected will result in undefined operation. Attempts to read configuration bytes with starting addresses greater than 0xF will also result in undefined operation.

## 9.0 Absolute Maximum Ratings

|   |                                   |
|---|-----------------------------------|
| Storage Temperature.....  | –65°C to +150°C                   |
| Ambient Temperature with Power Supplied .....                       | 0°C to +70°C                      |
| Supply Voltage to Ground Potential .....                            | –0.5 V to +4.0 V                  |
| DC Input Voltage to Any Input Pin.....                              | 5.25 V                            |
| DC Voltage Applied to Outputs<br>in Hi-Z State.....                 | –0.5 V to V <sub>CC</sub> + 0.5 V |
| Power Dissipation.....  | 300 mW                            |
| Static Discharge Voltage.....                                       | > 2000 V                          |
| Max Output Current Per I/O Port<br>(D0-D7, D8-15, ATA control)..... | 10 mA                             |

## 10.0 Operating Conditions

|   |  |
|---|--|
| T <sub>A</sub> (Ambient Temperature Under Bias).....    | 0°C to +70°C                                 |
| Supply Voltage .....                                    | +3.15V to +3.45V                             |
| Ground Voltage .....                                    | 0V   |
| F <sub>osc</sub> (Oscillator or Crystal Frequency) .... | 24 MHz ± 100 ppm,<br>..... Parallel Resonant |



## 11.0 DC Characteristics

| Parameter             | Description                             | Conditions   | Min. | Typ. | Max. | Unit |
|-----------------------|---|--|------|------|------|------|
| V <sub>CC</sub>       | Supply Voltage                          |  | 3.15 | 3.3  | 3.45 | V    |
| V <sub>CC</sub> Ramp  | Supply Ramp-up 0V to 3.3V               |  | 200  |      |      | μs   |
| V <sub>IH</sub>       | Input High Voltage                      |  | 2    |      | 5.25 | V    |
| V <sub>IL</sub>       | Input Low Voltage                       |  | -0.5 |      | 0.8  | V    |
| I <sub>I</sub>        | Input Leakage Current                   | 0 < V <sub>IH</sub> < V <sub>CC</sub>                                |      |      | ±10  | μA   |
| V <sub>IH_X</sub>     | Crystal Input HIGH Voltage              |  |      | 2    |      | 5.25 |
| V <sub>IL_X</sub>     | Crystal Input LOW Voltage               |  |      | -0.5 |      | 0.8  |
| V <sub>OH</sub>       | Output Voltage High                     | I <sub>OUT</sub> = 4 mA  | 2.4  |      |      | V    |
| V <sub>OL</sub>       | Output Voltage Low                      | I <sub>OUT</sub> = -4 mA   |      |      | 0.4  | V    |
| I <sub>OH</sub>       | Output Current High                     |  |      |      | 4    | mA   |
| I <sub>OL</sub>       | Output Current Low                      |  |      |      | 4    | mA   |
| C <sub>IN</sub>       | Input Pin Capacitance                   | All but D+/D-  |      |      | 10   | pF   |
|                       |   | D+/D-  |      |      | 15   | pF   |
| I <sub>SUSP</sub>     | Suspend Current<br>CY7C68300B/CY7C68320 | Connected:   |      | 0.5  | 1.2  | mA   |
|                       |   | Disconnected:  |      | 0.3  | 1.0  | mA   |
|                       | Suspend Current<br>CY7C68301B/CY7C68321 | Connected:   |      | 300  | 380  | μA   |
|                       |   | Disconnected:  |      | 100  | 150  | μA   |
| I <sub>CC</sub>       | Supply Current                          | USB High Speed:  |      | 50   | 85   | mA   |
|                       |   | USB Full Speed:  |      | 35   | 65   | mA   |
| I <sub>UNCONFIG</sub> | Unconfigured Current                    | Current before device is granted full current requested in bMaxPower |      | 43   |      | mA   |
| T <sub>RESET</sub>    | Reset Time After Valid Power            | V <sub>CC</sub> > 3.0V   | 5.0  |      |      | ms   |
|                       | Pin Reset After Power-Up                |  | 200  |      |      | μs   |

## 12.0 AC Electrical Characteristics

### 12.1 USB Transceiver

Complies with the USB 2.0 specification.

### 12.2 ATA Timing

The ATA interface supports ATA PIO modes 0, 3, and 4, Ultra DMA modes 2, 3, and 4, and multiword DMA mode 2 per the ATA/ATAPI 6 Specification. The AT2LP will select the highest common transfer rate.

## 13.0 Ordering Information

| Part Number       | Package Type   | GPIO Pins        |
|-------------------|--|------------------|
| CY7C68300B-56PVXC | 56 SSOP Lead-free for self- and bus-powered designs  | –                |
| CY7C68301B-56PVXC | 56 SSOP Lead-free for battery-powered designs        | –                |
| CY7C68300B-56LFXC | 56 QFN Lead-free for self- and bus-powered designs   | –                |
| CY7C68301B-56LFXC | 56 QFN Lead-free for battery-powered designs         | –                |
| CY7C68320-56LFXC  | 56 QFN Lead-free for self- and bus-powered designs   | 3 <sup>[4]</sup> |
| CY7C68321-56LFXC  | 56 QFN Lead-free for battery-powered designs         | 3 <sup>[4]</sup> |
| CY7C68320-100AXC  | 100 TQFP Lead-free for self- and bus-powered designs | 6                |
| CY7C68321-100AXC  | 100 TQFP Lead-free for battery-powered designs       | 6                |
| CY4615B           | EZ-USB AT2LP Reference Design Kit                    | n/a              |

**Note:**

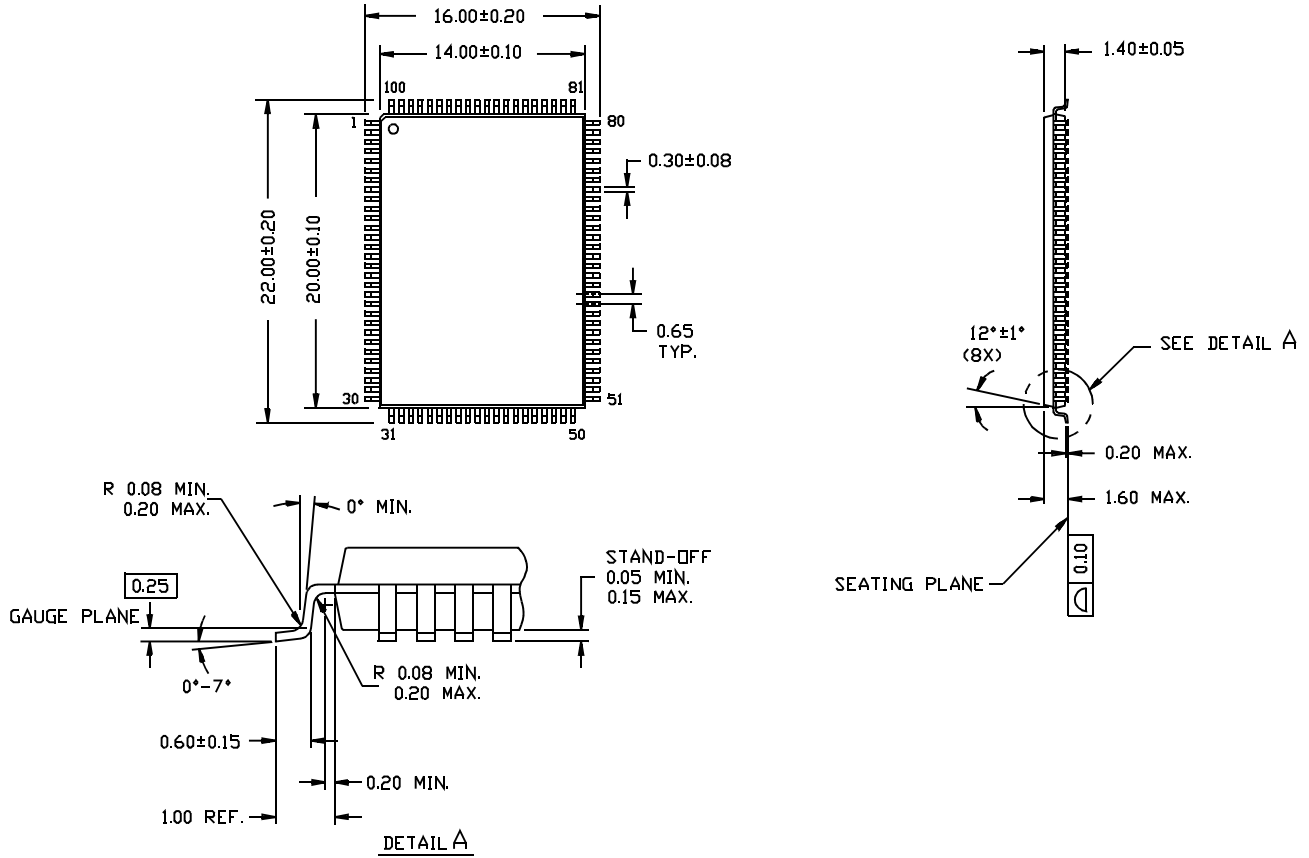
4. The General Purpose inputs can be enabled on ATAPUEN, PWR500#, and DRVPRVLD via EEPROM byte 8, bit 7 on CY7C68320/CY7C68321.



**14.0 Package Diagrams**

**100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101**

DIMENSIONS ARE IN MILLIMETERS.



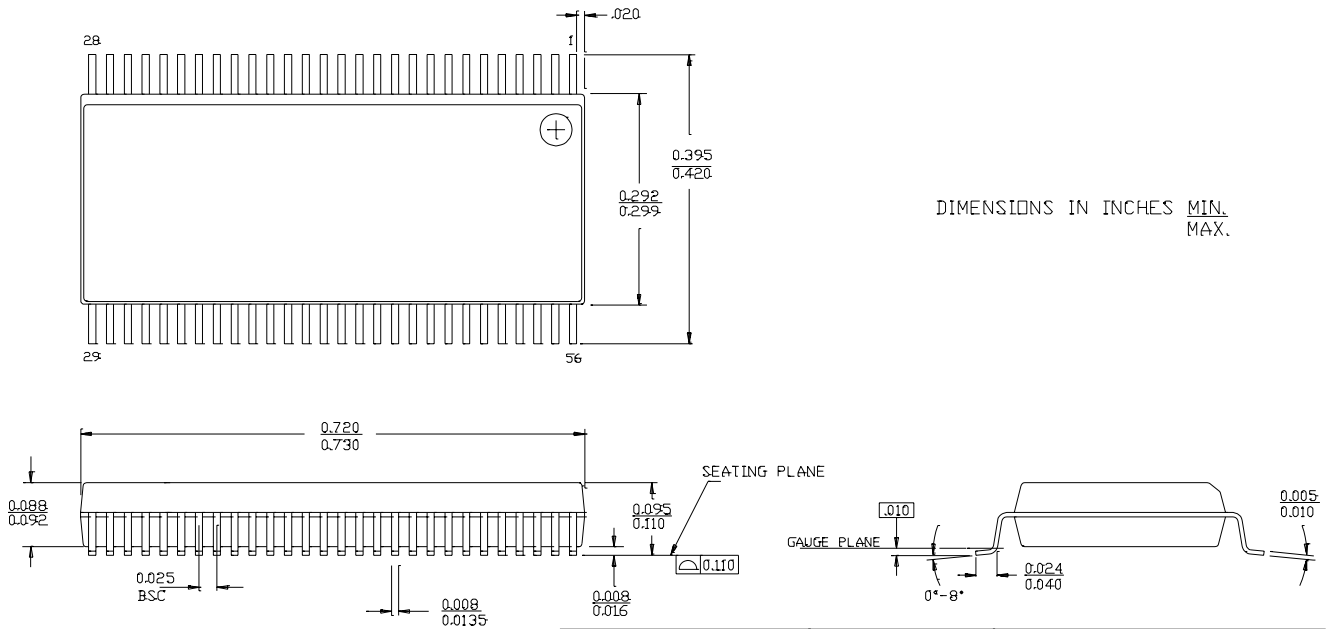
51-85050-\*A

**Figure 14-1. 100-lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)**



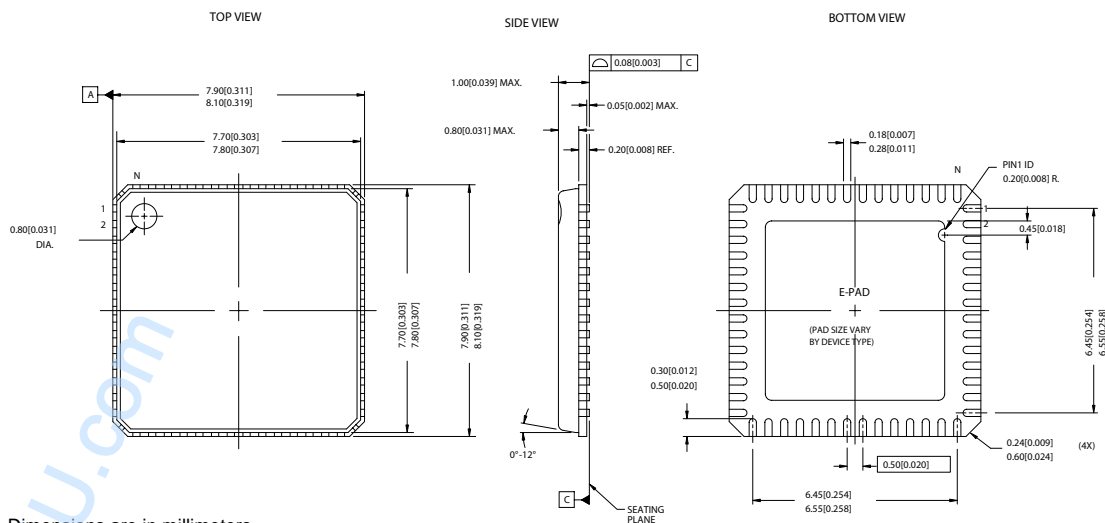


**14.0 Package Diagrams (continued)**



**Figure 14-2. 56-lead Shrunken Small Outline Package 056**

51-85062-\*C



**Figure 14-3. 56-Lead QFN 8 x 8 mm LF56A**

51-85144-\*D



## 15.0 PCB Layout Recommendations

The following recommendations should be followed to ensure reliable high-performance operation.

- At least a four-layer impedance controlled board is required to maintain signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- To control impedance, maintain uniform trace widths and trace spacing.
- To minimize reflected signals, minimize the number of stubs.
- Connections between the USB connector shell and signal ground must be done near the USB connector.
- Use bypass/flyback capacitors on VBus near the connector.
- DPLUS and DMINUS trace lengths should be kept to within 2 mm of each other in length, with preferred length of 20 – 30 mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to be split under these traces.
- For a more stable design, do not place vias on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm.
- Source for recommendations:
- EZ-USB FX2 PCB Design Recommendations, [http://www.cypress.com/cfuploads/support/app\\_notes/FX2\\_PCB.pdf](http://www.cypress.com/cfuploads/support/app_notes/FX2_PCB.pdf).
- High-speed USB Platform Design Guidelines, [http://www.usb.org/developers/data/hs\\_usb\\_pdg\\_r1\\_0.pdf](http://www.usb.org/developers/data/hs_usb_pdg_r1_0.pdf).

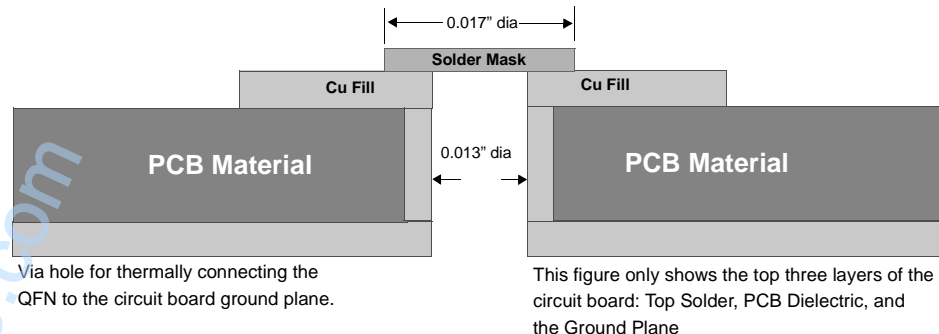
## 16.0 Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the package to the PCB. Hence, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. A Copper (Cu) fill is to be designed into the PCB as a thermal pad under the package. Heat is transferred from the AT2LP through the device's metal paddle on the bottom side of the package. Heat from here is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 5 x 5 array of vias. A via is a plated through-hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

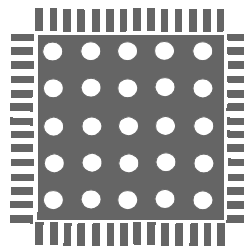
For further information on this package design please refer to the application note *Surface Mount Assembly of AMKOR's MicroLeadFrame (MLF) Technology*. The application note provides detailed information on board mounting guidelines, soldering flow, rework process, etc.

*Figure 16-1* displays a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template needs to be designed to allow at least 50% solder coverage. The thickness of the solder paste template should be 5 mil. It is recommended that "No Clean," type 3 solder paste is used for mounting the part. Nitrogen purge is recommended during reflow.

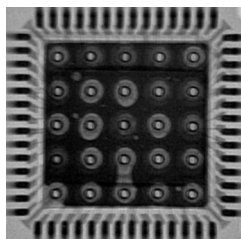
*Figure 16-2* is a plot of the solder mask pattern and *Figure 16-3* displays an X-Ray image of the assembly (darker areas indicate solder.)



**Figure 16-1. Cross-Section of the Area Under the QFN Package**



**Figure 16-2. Plot of the Solder Mask (White Area)**



**Figure 16-3. X-ray Image of the Assembly**

## 17.0 Other Design Considerations

Certain design considerations must be followed to ensure proper operation of the CY7C68300B/CY7C68301B. The following items should be taken into account when designing a USB device with the CY7C68300B/CY7C68301B.

### 17.1 Proper Power-up Sequence

Power must be applied to the CY7C68300B/CY7C68301B before, or at the same time as the ATA/ATAPI device. If power is supplied to the drive first, the CY7C68300B/CY7C68301B will start up in an undefined state. Designs that utilize separate power supplies for the CY7C68300B/CY7C68301B and the ATA/ATAPI device are not recommended.

### 17.2 IDE Removable Media Devices

The CY7C68300B/CY7C68301B does not fully support IDE removable media devices. Changes in media state are not reported to the operating system so users will be unable to eject/reinsert media properly. This may result in lost or corrupted data.

### 17.3 Devices With Small Buffers

The size of the ATA/ATAPI device's buffer can greatly affect the overall data transfer performance. Care should be taken to

ensure that devices have large enough buffers to handle the flow of data to/from the drive. The exact buffer size needed depends on a number of variables, but a good rule of thumb is:

$$(\text{approx min buffer}) = (\text{data rate}) * (\text{seek time} + \text{rotation time} + \text{other})$$

where *other* may include things like time to switch heads, power-up a laser, etc. Devices with buffers that are too small to handle the extra data may perform considerably slower than expected.

## 18.0 Disclaimers, Trademarks, and Copyrights

Purchase of I<sup>2</sup>C components from Cypress or one of its sub-licensed Associated Companies conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips. Microsoft and Windows are registered trademarks of Microsoft Corporation. Apple and Mac OS are registered trademarks of Apple Computer, Inc. EZ-USB AT2LP, EZ-USB AT2, EZ-USB FX2 and EZ-USB TX2 are trademarks, and EZ-USB is a registered trademark of Cypress Semiconductor Corporation. All product and company names mentioned in this document are the trademarks of their respective holders.


**Document History Page**
**Description Title: CY7C68300B/CY7C68301B/CY7C68320/CY7C68321 EZ-USB AT2LP™ USB 2.0 to ATA/ATAPI Bridge**  
**Document Number: 38-08033**

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
|------|---------|------------|-----------------|--|
| **   | 129739  | 12/04/03   | GIR             | New data sheet   |
| *A   | 215125  | SEE ECN    | KKU             | Added HID descriptor, Content Security Methods descriptor, alternate functions on 3 pins, and alternate EEPROM addressing                          |
| *B   | 274109  | SEE ECN    | ARI             | Incorporated CY7C68320 information. Updated graphics to reflect this change  |
| *C   | 318133  | SEE ECN    | GIR             | Incorporated CY7C68301B and CY7C68321 information. Updated graphics to reflect this change. Revised data for final release and posting to website. |
| *D   | 323408  | SEE ECN    | GIR             | Swapped the part numbers in the DC Characteristics table to match their correct $I_{SUSP}$ values.   |