OC-192c/STM-64/10-Gigabit Ethernet Framer - POSIC10G™

Features

- Four modes of operation:
  - LANPHY Mode: Supports the SFI4/XSBI, 645-MHz interface: in this mode the SONET framer block is bypassed
  - Packet-Over-SONET (POS) Mode: Supports Full-Duplex mapping of HDLC/PPP-like framing into STS-192c/STM-64 in accordance with RFC1662/2615 (PPP)
  - Direct Mode: Supports the full-duplex, direct mapping of system packets into the SONET STS-192c/STM-64 payload: In this mode the processing of packets is passed on to the link layer
  - Ethernet-over-SONET Mode (WANPHY): Supports Full-Duplex 10-Gigabit Ethernet mapping into STS-192c/STM-64 SONET/SDH payload in compliance with IEEE802.3ae/D4.0 standards
- Compliant with 802.3ae specifications[6]:
  - Full-duplex MAC data transmission and reception
  - 64B/66B PCS
  - Rate Adaptation
  - MII Management Interface specifications
  - WAN Interface Sub-layer (WIS)
- SONET Receiver/Transmitter Features:
  - Generates/extracts SONET/SDH Section, Line and Path overhead
  - Detects Loss of Signal (LOS), Loss of Frame (LOF), Line Alarm Indication (AIS-L), Line Remote Defects (RDI-L), Loss of Pointer (LOP), Path Alarm Indication (AIS-P) and Remote Path Defect Indication (RDI-P)
  - Performs count on B1, B2, and B3 errors
  - Detects Signal Degrade (SD) and Signal Fail (SF) threshold crossing alarms based on B2 errors
  - Filters and captures Automatic Protection Switching (APS) channel and implements the 1+1 APS architecture. Provides a separate interface for SONET framer protection port
  - Section Trace (J0/Z0) sequence and Path Trace (J1) sequence extraction and insertion
  - SONET/SDH payload scrambling/descrambling
  - Line and section DCC extraction and insertion
- Packet over SONET (POS) Features:
  - Full duplex mapping of packet over SONET/SDH per IETF RFC 1662/2615 (PPP)
  - Rate adaptation by insertion/deletion of flag patterns between packets
  - FCS (frame check sequence) insertion/deletion
  - Implements transparency processing
  - Selectable data scrambling/descrambling
  - Packet performance monitoring
- 10-Gigabit Ethernet features:
  - Performs flow control protocol per IEEE 802.3ae/D4.0
  - 48-Kbyte transmit FIFO and 160-Kbyte receive FIFO
  - Supports transmit and receive RMON statistics
  - Appends CRC code to the current frame under system request in the transmit direction and performs optional CRC check in the receive direction
  - Programmable data padding in support of the 64-byte minimum packet size in the transmit direction and optional pad extraction in the receive direction
  - Inserts Inter-Packet Gaps (IPG) in the transmit direction and extracts IPGs in the receive direction
  - Detects for packet Abort Sequence and aborts packets upon system command or FIFO overflow
  - Checks for the minimum and maximum packet length and marks packets exceeding the maximum packet length
  - The PCS block implements a self-synchronous scrambler and descrambler function
  - Detects and processes pause control frames in the receive direction
  - Supports generation of pause control frames under the request of Receive FIFO or as initiated by the system
  - Supports DA/SA/VLAN address filtering
- System/Link Layer interface
  - 312.5-MHz DDR, 16-bit bus OIF SPI-4-02.0[1]
- WAN SERDES Interface
  - 622.08-MHz (SDR),16-bit LVDS[2][3]
  - 311.04-MHz (DDR),16-bit LVDS
- LAN SERDES Interface
  - 644.53-MHz, 16-bit compliant with OIF SFI4-01.0 SFI4/XSBI specifications[5]
- CPU Interface
  - 32-bit CPU interface (up to 60 MHz)
  - Supports both Intel® and Motorola type microprocessors
- Three loop-back paths for diagnostic: system-side full-chip loop-back, system-side RS loop-back, and line-side loop-back
- Compliant with IEEE 1149.1 JTAG boundary scan logic standard
- 0.18-μm CMOS, 624-ball CBGA package
- +1.8V for core, +3.3V for LVTTL/LVDS