CY807/808 Datasheet

450M-1000MHz Receiver

DESCRIPTION

The CY807/808 is a UHF ASK receiver IC which operates 3.6V-5.5V, from 450MHz to 1000MHz with typical receiving sensitivity of -107dBm.

The CY807/808 is a super-heterodyne receiver for ASK and OOK modulation such as pulse width modulation, variable pulse modulation, Manchester modulation and so on. The down-conversion mixer also provides image rejection function to remove the image band and selects the desired signal. Any one-of-four filter bandwidths may be selected externally by the user in binary steps, from 1.25KHz to 10KHz. The user need only configure the device with a set of easily determined values, based upon data rate, code modulation format, and desired duty-cycle operation.

CY807 is the SSOP16 package version. CY808 is the SOP16 package version.

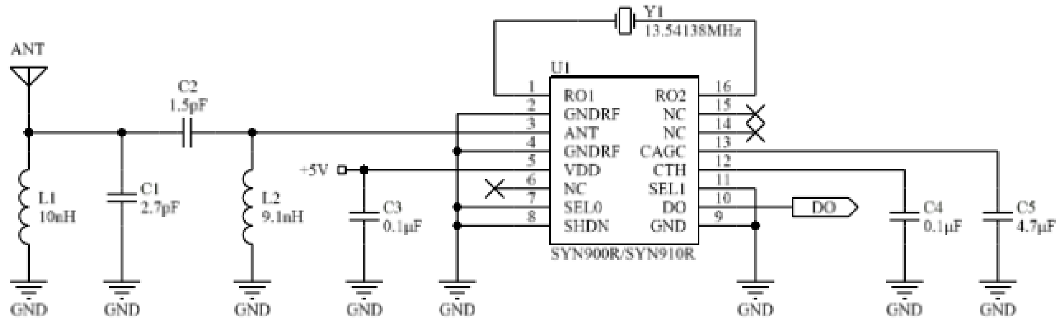
FEATURES

450MHz to 1000MHz Frequency Range
-107dBm High Sensitivity, 1Kbps and BER 10E-2@868MHz
Image Rejection Function
Low Power Consumption
Excellent Selectivity and Noise Rejection
No External IF Filter Required
Low External part count
SSOP16 Package Type for CY807
SOP16 Package Type for CY808

APPLICATIONS

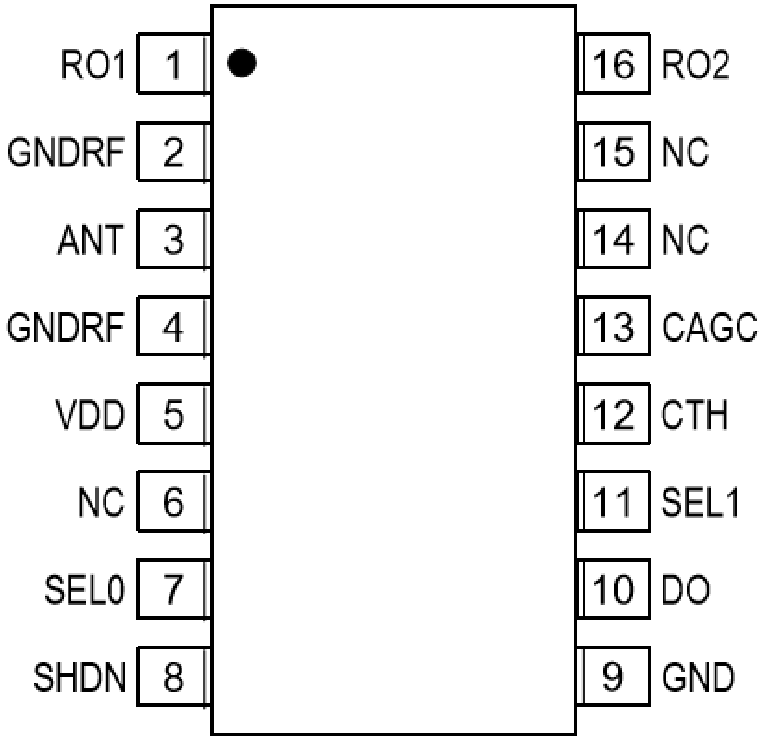
Automotive Remote Keyless Entry (RKE)
Remote Control System
Access Control System
Home Automation
Toys

TYPICAL APPLICATION



CY807/CY808-868MHz, 1KHz Baud Rate Application Circuit

PIN CONFIGURATION



CY807 SSOP-16 and CY808 SOP-16

PIN DESCRIPTION

Pin	Name	Function
1	RO1	Reference resonator input connection to Colpitts oscillator stage.
2	GNDRF	Negative supply connection associated with ANT RF input.
3	ANT	RF signal input from antenna.
4	GNDRF	Negative supply connection associated with ANT RF input.
5	VDD	Positive supply connection for all chip functions.
6	NC	Not Connected (Floating)
7	SEL0	Logic control input with active internal pull-up. Used in conjunction with SEL1 to control the demodulator low pass filter bandwidth.
8	SHDN	Shutdown logic control input. Active internal pull-up.
9	GND	Negative supply connection for all chip functions except RF input.
10	DO	Demodulated data output.
11	SEL1	Logic control input with active internal pull-up. Used in conjunction with SEL0 to control the demodulator low pass filter bandwidth.
12	CTH	Demodulation threshold voltage integration capacitor connection. Capacitor across CTH pin and GND to set the settling time for the demodulation data slicing level.
13	CAGC	AGC filter capacitor connection. CAGC capacitor, normally greater than 0.47µF, is connected from this pin to GND.
14	NC	Not Connected (Floating)
15	NC	Not Connected (Floating)
16	RO2	Reference resonator input connection to Colpitts oscillator stage.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
Input Voltage	7V
ESD Rating	Note 1
Storage Temperature Range	-65 ℃ to 150 ℃
Junction Temperature	150 ℃
Lead Temperature (soldering, 10sec.)	260 ℃

OPERATING RATINGS

RF Frequency Range	450-1000MHz
Supply Voltage	3.6V-5.5V
Input Voltage (Max.)	5.5V
Maximum Input RF Power	-20dBm
Ambient Temperature (TA)	-40 ℃ to 85 ℃

ELECTRICAL CHATACTERISTICS

Unless otherwise noted, VDD = 5V, CAGC = 4.7μF, CTH = 0.1μF, 1Kbps data rate (Manchester encoded, BER =10E-2), all test at TA = 25 ℃.

Receiver

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{RX}	Frequency Input Range			450 to 1000		MHz
$P_{IN,MAX}$	Maximum Input Power				10	dBm
P_{SENS}	Receiver Sensitivity (Note 2)	fRX = 868MHz		-107		dBm
	Image Rejection	fRX = 868MHz		20		dB
	IF Bandwidth	fRX = 868MHz		600		KHz
	Receive Modulation Duty Cycle	Note 3	20		80	%
V_{AGC}	AGC Dynamic Voltage	PIN = -40dBm		1.2		V
		PIN = -100dBm		1.8		V
	AGC pin leakage current	TA = 25 ℃		±2		nA
	CTH pin leakage current	TA = 25 ℃		±2		nA

Reference Oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{OSC}	Frequency	f_{RX} = 868MHz		13.54138		MHz
	Input Range		0.2		1.5	V_{PP}
I_{OSCSC}	Source Current	V(RO) = 0V		12		μA

DO Drive

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	DO pin Output Current	Source @ 0.8VDD		100		µA
		Sink @ 0.2 VDD		250	10	µA
T_{RISE}	Output Rise and Fall Times	C_L = 15pF, pin DO, 10-90%		3.5		µsec
T_{FALL}				1.5		µsec

Power Supply

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current	VDD = 5V, fRX = 868MHz		13		mA
I_{OFF}	Shut Down Current	SHDN = High			1	µA

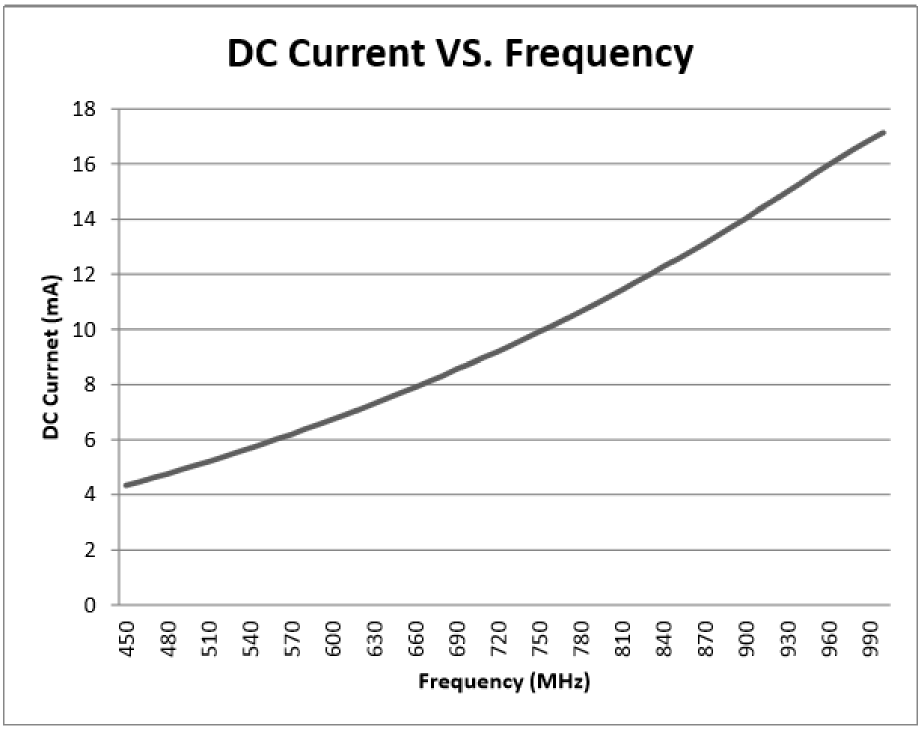
Note 1: Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.

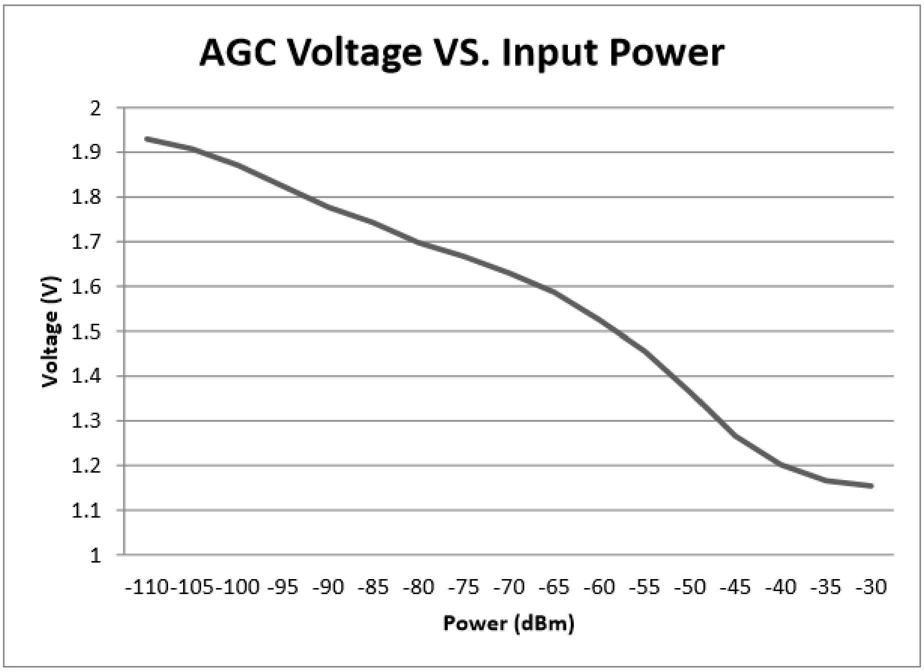
Note 2: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded) at a data rate of 1kbps.

Note 3: When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any "quiet" time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor CTH, then duty cycle is the effective duty cycle of the burst alone.
[For example, 100msec burst with 50% duty cycle, and 100msec "quiet" time between bursts. If burst includes preamble, duty cycle is $T_{ON}/(T_{ON} + T_{OFF})$ = 50%; without preamble, duty cycle is $T_{ON}/(T_{ON} + T_{OFF} + T_{QUIET})$ = 50msec/(200msec) = 25%. T_{ON} is the (Average number of 1's/burst) × bit time, and $T_{OFF} = T_{BURST}–T_{ON}$.

TYPICAL CHARACTERISTICS

Unless otherwise noted, VDD = 5V, CAGC = 4.7μF, CTH = 0.1μF, 1Kbps data rate (Manchester encoded, BER =10E-2), all test at TA = 25 ℃.





BLOCK DIAGRAM

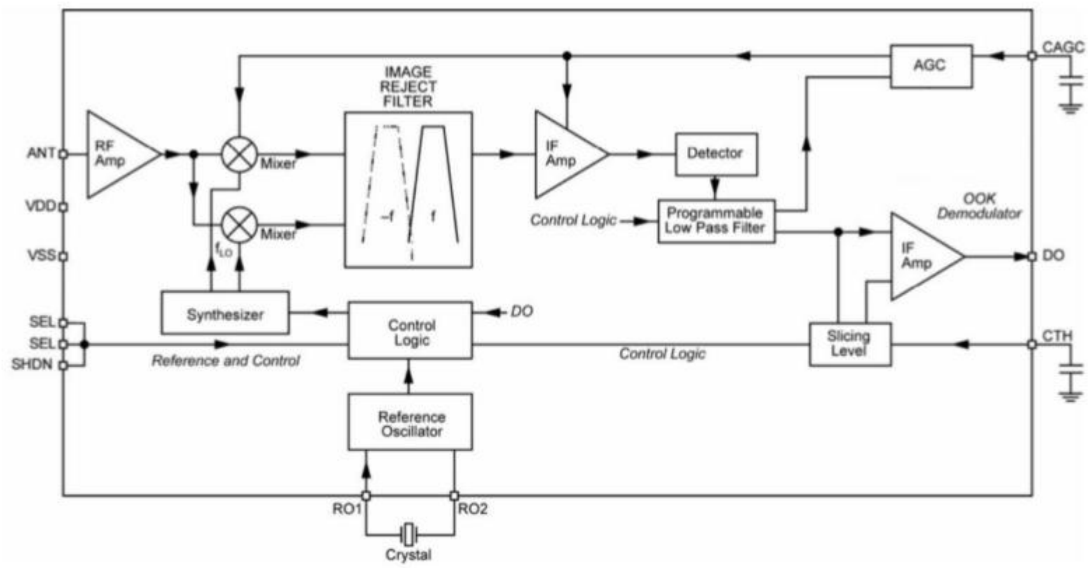


Figure 1 Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1. Simplified Block Diagram that illustrates the basic structure of the SYN900R /SYN910R. It is made of three sub-blocks; Image Rejection UHF Down-converter, the OOK Demodulator, and Reference and Control Logics. Outside the device, the SYN900R/SYN910R requires only three components to operate: two capacitors (CTH and CAGC) and the reference frequency device, usually a quartz crystal. An additional five components may be used to improve performance. These are: power supply decoupling capacitor, two components for the matching network, and two components for the pre-selector band pass filter.

LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA uses a Cascoded NMOS structure circuit, and the output is converted to differential signals for next stage mixers.

OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

Mixer and Synthesizer

The LO ports of the Mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal to allow suppression of the image frequency at twice the IF frequency below the wanted signal. The local oscillator is set to 64 times the crystal reference frequency via a phase-locked loop synthesizer with a fully integrated loop filter.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes base band information. The programmable low-pass filter further enhances the base band information. There are four programmable low-pass filter BW settings: 1625Hz, 3250Hz, 6500Hz, 13000Hz for 868MHz operation. Low pass filter BW will vary with RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. See equation below for filter BW calculation:

$$\text{BW Operating Freq} = \text{BW@868MHz} \times \text{Operating Freq. (MHz)} / 868$$

It is very important to choose the filter setting that best fits the intended data rate to minimize data distortion.

The low pass filter can be hardware set by external pins SEL0 and SEL1.

SEL0	SEL1	Demod BW (@ 868MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz

Table 1: Demodulation BW Selection

Slicer

The signal prior to slicer is still linear demodulated AM. Data slicer converts this signal into digital “1” and “0” by comparing with the threshold voltage built up on the CTH capacitor. This threshold is determined by detecting the positive and negative peaks of the data signal and storing the mean value. Slicing threshold is at 50%. After the slicer, the signal is now digital OOK data. During long periods of “0” or no data period, threshold voltage on the CTH capacitor may be very low. Large random noise spikes during this time may cause erroneous “1” at DO pin

AGC

The AGC comparator monitors the signal amplitude from the output of the Weaver receiver. When the output signal is less than 750mV, the threshold 1.5μA current is sourced into the external CAGC capacitor. When the output signal is greater than 750mV, a 15μA current sink discharges the CAGC capacitor. The voltage developed on the CAGC capacitor acts to adjust the gain of the mixers of Weaver receiver to compensate for RF input signal level variation.

Reference Control

There are 2 components in Reference and Control sub-block: 1) Reference Oscillator 2) Control Logic through parallel Inputs: SEL0, SEL1, SHDN.

Reference Oscillator

The reference oscillator in the CY807/CY808 uses a basic Colpitts crystal oscillator configuration with MOS transconductor to provide negative resistance. The RO pin external capacitor is integrated inside SYN900R/SYN910R. User only needs to connect reference oscillation crystal. Reference oscillator crystal frequency can be calculated:

$F_{OSC} = F_{RF}/(64 + 1.198/12)$

For 868 MHz, F_{OSC} = 13.54138MHz.

PACKAGE DESCRIPTION

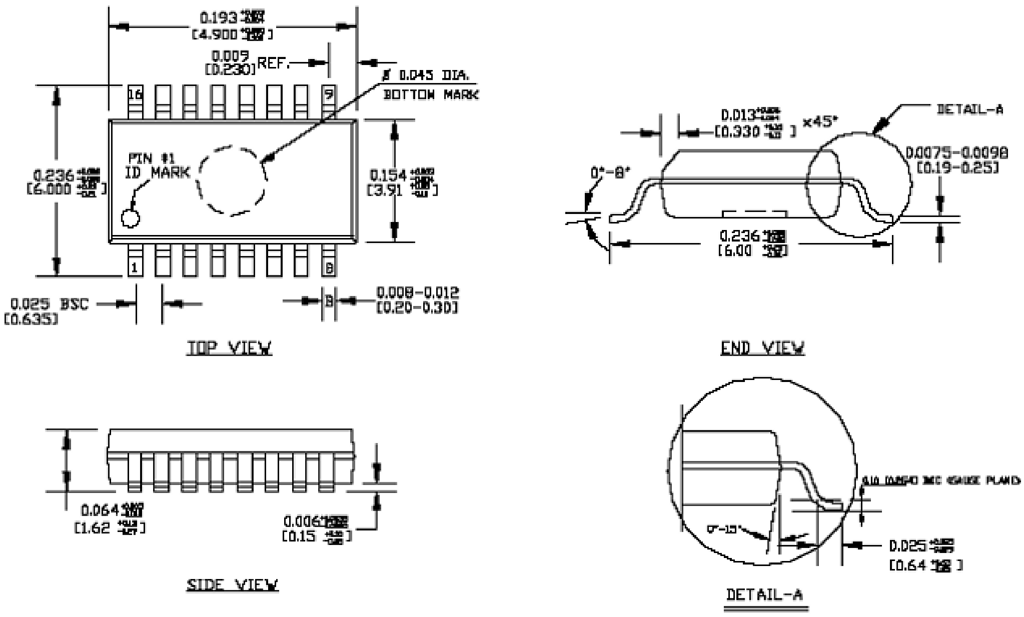


Figure 2: CY807 SSOP-16 Package Outline Dimensions shown in millimeters

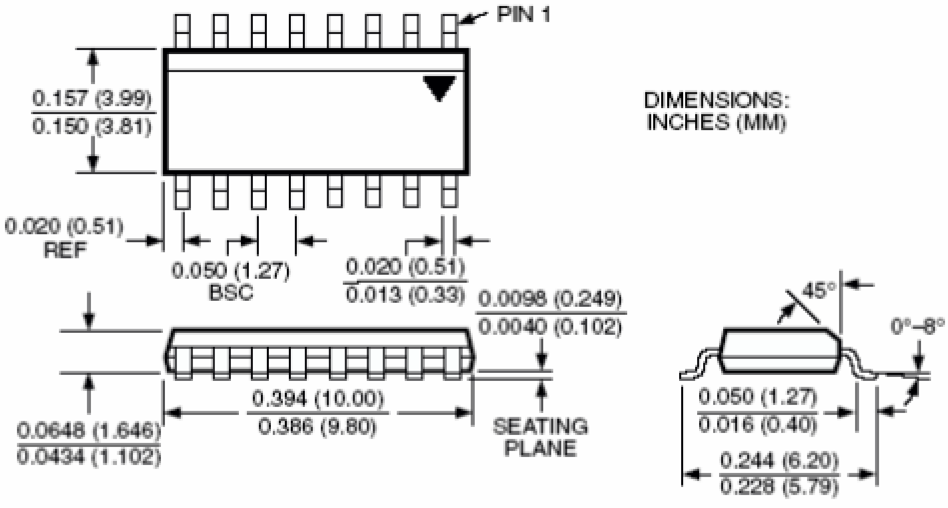


Figure 3: CY808 SOP-16 Package Outline Dimensions shown in millimeters and (inches)