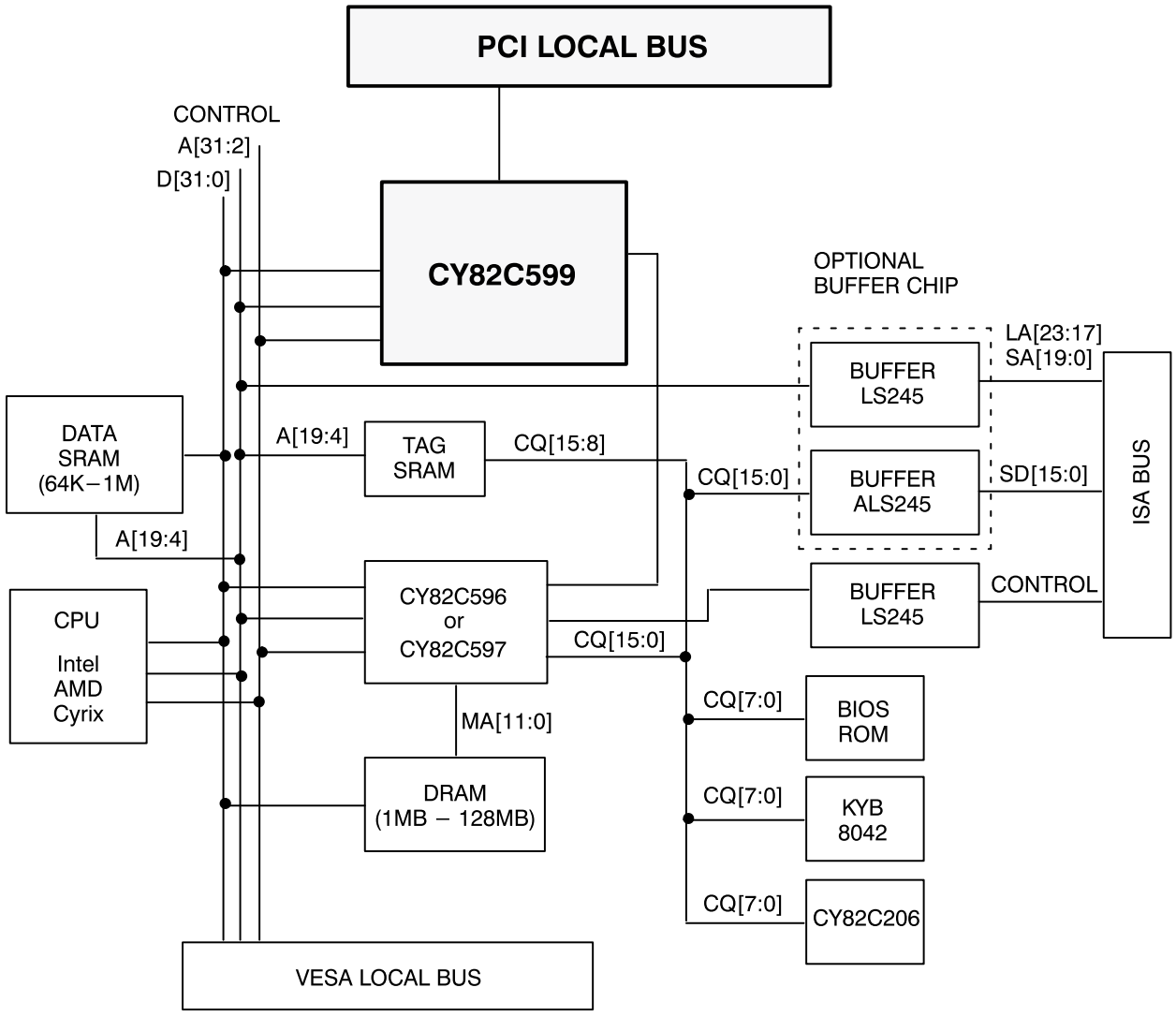
PRELIMINARY **CY82C599**

Intelligent PCI Bus Controller

Features

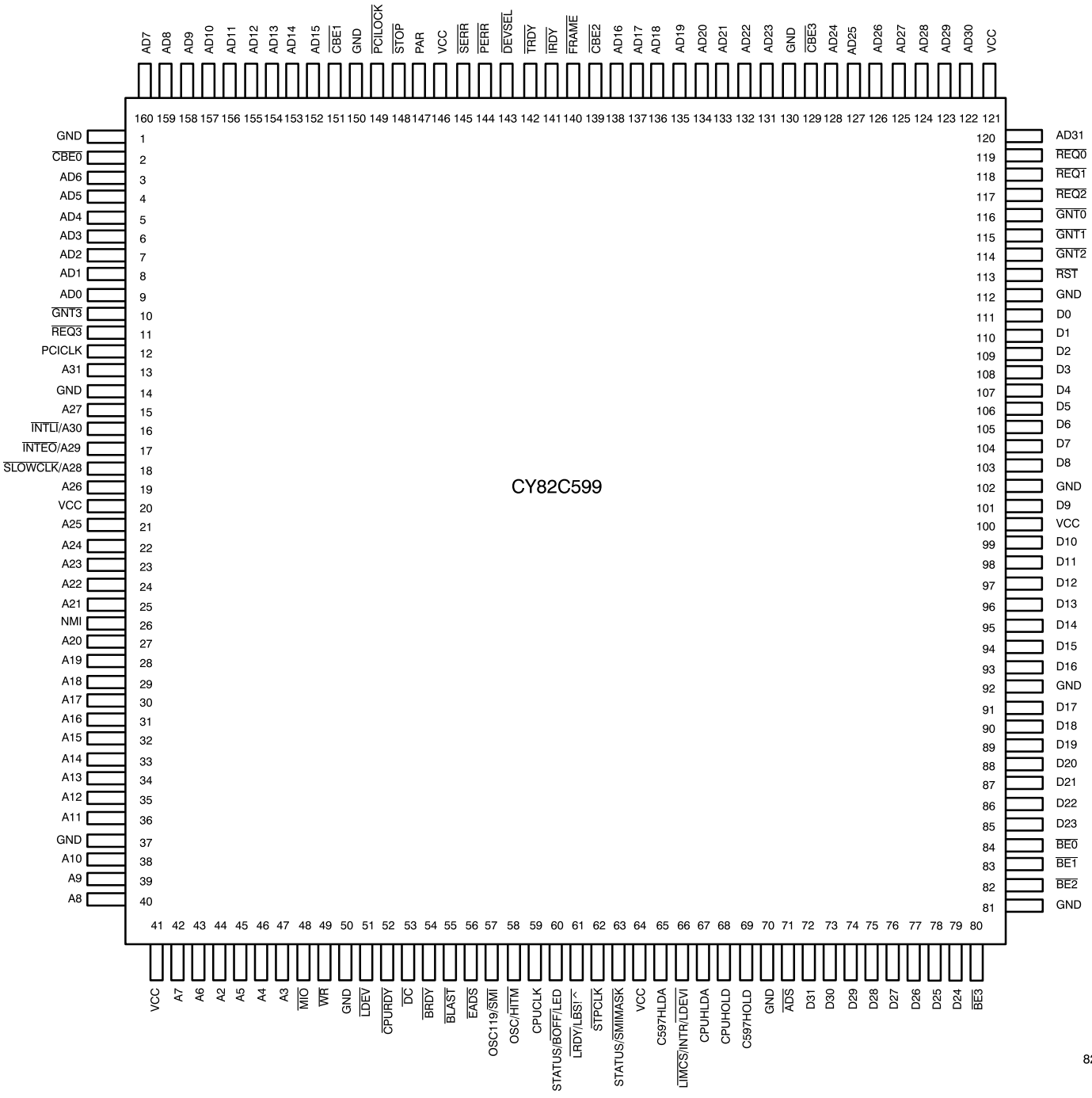
- Provides an interface between the PCI Local Bus and the CPU bus
- PCI Bus Rev. 2.0 compliant
- Supports Intel® 486DX, 486DX2, 486SX, 486SL, P24T, AMD AM486 and Cyrix Cx486S2 (M6/M7) CPUs
- Interfaces with Cypress CY82C596 or CY82C297 Core Logic devices to form a complete PC solution supporting PCI, VESA, and ISA buses
- Supports 4 PCI Masters
- Supports burst mode PCI accesses to memory space
- PCI pre-read support with 4-double-word-deep FIFO, each double-word is 32 Data bits wide
- PCI post-write support with 4-double-word-deep FIFO, each double-word is 32 Data bits wide
- Synchronous/Asynchronous PCI bus support
- Standby mode slows down CPU clock
- Power management timers
- SMI generation support for Intel, AMD, Cyrix CPUs
- Provides I/O trap for peripheral device power control
- Packaged in 160-pin PQFP

System Block Diagram



Pin Configurations

PQFP
Top View



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1.0 Introduction

The CY82C599 Intelligent PCI Bus Interface chip is designed to eliminate the ISA Bus I/O bottleneck by providing a glueless path to the high-performance PCI Local Bus. This chip connects the PCI Bus to the VESA Bus and the CPU simultaneously, allowing system designers to take advantage of the PCI Bus's high through-put while maintaining access to the large selection of ISA and VESA local bus expansion cards.

No TTL components are required to connect the CY82C599 to the PCI Bus. However, in applications with heavy loading on the Address/Data lines, buffers may be necessary to distribute the load. The CY82C599 simplifies the interface design by providing buffer control signals.

The CY82C599, along with the CY82C596 PC/AT Core Logic chip or the CY82C597 Green PC/AT Core Logic chip, implements a sophisticated and cost-effective 486-based PCI/VESA/ISA system.

2.0 Functional Overview

The CY82C599 provides the required functions in PCI Specification Revision 2.0 including bus arbitration, bus grant, master support, bus lock support and interrupt support. It supports all the CPU and bus commands except INTA and dual address cycles. INTA cycles are routed to the interrupt controller on the ISA bus. Dual address cycles are reserved for 64-bit addressing and they are ignored by the CY82C599.

The CY82C599 supports bursting in both CPU mode and PCI master mode. It also supports post-write buffering and pre-read buffering with a 4-word-deep bidirectional FIFO. Each word in the FIFO is 64 bits wide (32-bits address, 32-bits data). In addition, fast back-to-back write cycles are supported to enhance system performance.

The central arbiter of the CY82C599 supports two levels of arbitration. The first level arbiter arbitrates bus requests between the VESA and the PCI Buses. The second level arbiter handles bus requests from four PCI master channels. Both levels of arbitration can have either fixed or rotating priority. Optionally, a hold request on the ISA bus (for a refresh, DMA/MASTER, or VESA transactions) can prematurely terminate a PCI transaction.

The CY82C599 has built-in interrupt logic that can convert a level-sensitive interrupt signal to an edge-triggered interrupt signal. This feature enables the usage of popular interrupt controllers such as the 8259 or 83C206.

The preferred PCI Configuration Mechanism #1 is supported in the CY82C599 that allows PCI configuration cycles to be generated by software. To support hierarchical PCI buses, both Type 0 and Type 1 configuration access are implemented. BIOS support is available from AMI & AWARD.

3.0 PCI Bus

The purpose of this section is to give an overview of PCI, the motivation behind it, and its features. Basic transfers and rules are discussed. How the CY82C599 handles inter−bus transfers is discussed in later sections. For a detailed description of the PCI bus, all of the rules and requirements, see the PCI Specification 2.0.

The PCI Bus was defined in order to satisfy the growing need for a standardized high-speed local bus that is independent of the processors, operating system, and CPU bus speed. New generations of computers incorporating I/O intensive software will require bandwidth that cannot be satisfied with the traditional I/O architectures. The PCI specification 2.0 addresses these requirements and provides an upgrade path for future requirements. Some of the PCI features include:

- **Processor Independent**
- **Multiplexed, Burst Mode Operation**
- **120 MBytes/sec usable throughput (32−bit data path)**
- **Three physical address spaces**
  - **— Memory**
  - **— I/O**
  - **— Configuration**
- **Hidden Arbitration**

PCI is defined as a synchronous bus that can operate from 0 to 33MHz. All transfers take place on the rising edge of the clock (PCICLK). The basic data transfer in PCI is a burst. A burst transfer consists of an address phase, followed by one or more data phases. The address phase is defined as the first rising edge of the clock where $\overline{\text{FRAME}}$ is asserted (LOW). During the Address phase, the Master (also referred to as the initiator) asserts the appropriate address on the address/data lines (AD[31:0]) while also asserting the appropriate command on the Command/Byte Enable C/$\overline{\text{BE}}$[3:0] lines. With the information transferred during the address phase, all PCI devices, including the slave (or Target), can determine: 1) Whether the transaction falls within its designated address range, 2) The kind of transfer that will take place (e.g. a read or write to memory, I/O, or configuration space), and 3) How to respond to that particular command.

Once a device recognizes that it is the target for the transaction, it claims the transactions by asserting Device Select ($\overline{\text{DEVSEL}}$) LOW. $\overline{\text{DEVSEL}}$ must be asserted LOW in order for any information is be transferred.

The address phase is followed by one or more data phases. Whether the initial data phase occurs on the subsequent clock edge is determined by the type of transaction and the ability of either agent to provide/accept the data within the appropriate time period. Since the address and data lines are multiplexed, a normal read operation requires a 'turn−around' cycle to avoid bus contention. During this cycle, control of the Address/Data lines is transferred from the master to the slave, who must now use these lines to drive out the requested information. During a write operation, this 'turn-around' cycle is not required since the master is providing the write data and does not have to relinquish control of the bus. PCI also allows that both the master and slave have the ability to insert wait states should either require additional cycles in order to properly participate in the transfer. This is accomplished with the Initiator Ready signal ($\overline{\text{IRDY}}$) and the Target Ready signal ($\overline{\text{TRDY}}$) for the Initiator and Target, respectively. Either of these signals being de-asserted (HIGH) during the data phase of the transaction will insert a wait state, thereby preventing data from being transferred during that cycle. The data presented on the AD[31:0] lines is transferred during a data phase on the rising edge of the clock when ALL of the following signals are active (LOW): $\overline{\text{DEVSEL}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, and $\overline{\text{FRAME}}$ (except during the final data phase, when $\overline{\text{FRAME}}$ is HIGH, which is explained later). The bytes containing meaningful information are controlled by the C/$\overline{\text{BE}}$[3:0] signals. During the data phase, these signals behave as byte enable lines.

Transactions are normally terminated by the Master by de-asserting $\overline{\text{FRAME}}$ HIGH on the clock prior to the last data

phase. By doing so, all of the agents on the bus, including the Target and the Arbiter, recognize that the current transaction is coming to an end. This advanced notice allows the Arbiter to grant ownership of the bus to the next requesting agent. This is referred to as Hidden Arbitration since no additional clock cycles are consumed. The new Master will not start to drive the bus until the current transaction is actually completed. The Target has the ability to abort the transaction prematurely should the need arise, although this is not the typical method of termination.

Arbitration in PCI is access based instead of time slot based. This is accomplished through a simple request−grant handshaking scheme through a central arbiter. Each agent has dedicated request and grant lines to the arbiter. A bus Master must request and be granted bus ownership each time a transaction is desired.

PCI defines three different physical address spaces; memory, I/O, and configuration space. Each of these address spaces has its own characteristics. Therefore, transactions to each space are handled differently, particularly in regards to AD[0:1]. The memory and I/O address spaces are customary, but the configuration address space has been defined by PCI in order to support hardware configuration.

4.0 Address Space

The purpose of this section is to explain the memory and I/O address space mapping used by the CY82C599.

The CY82C599 recognizes two different physical address spaces; memory and I/O. Transactions to these two address spaces are handled differently, and therefore need to be distinguished from one another. The CY82C599 differentiates these two different type of transactions by monitoring the M/$\overline{IO}$ signal coming from the CPU bus, or the C/$\overline{BE}$ signals coming from the PCI bus. In order to recognize the destination of each transaction, each address space needs to be divided (or mapped) into the different target areas (ISA, PCI, VESA, or Local Memory). Each address map, memory and I/O, is discussed below.

4.1 I/O Address Space

Although the I/O address space can extend the full 32 bits (a possible 4 GB of I/O address space), x86 CPUs limit I/O transactions to the lower 64KB (0000h−FFFFh). The remaining address locations are not valid I/O address space. In addition, the lower 1KB (0000h−03FFh) of I/O space has been assigned as AT I/O space. Within the lower 1KB (AT space) resides numerous predefined I/O blocks that can be assigned to PCI or ISA/VESA through configuration registers. The remaining I/O address locations (0400h−FFFFh) can be mapped using three 100% user defined I/O blocks. The base address, block size, and bus location (e.g. PCI, VESA, or ISA) of these I/O blocks are determined by the configuration registers during boot-up (see configuration registers). If an I/O address area is excluded from the user defined blocks mentioned above, it is considered to be in an ‘unknown‘ I/O location. ‘Unknown’ I/O address locations are handled on a priority basis (see the I/O access priority sections for further details). Although the PCI base address can be placed anywhere within the lower 64KB using one of the three 100% user defined I/O blocks, it is recommended that the PCI base address be placed at 8000h or above to avoid contention with VESA devices. VESA and PCI devices should never occupy the same I/O address location. Doing so will cause a bus contention condition. How the CY82C599 responds to each I/O transaction is discussed in the following sections.

4.2 Memory Address Space

The CY82C599 supports up to 256MB of local memory space (128MB when used with the CY82C596/7). The full 4GB memory space can be mapped over the PCI, VESA, or ISA regions (see configuration registers). This mapping allows the CY82C599 to determine the destination of the transaction and respond appropriately. A minimum of 64KB (0000h−FFFFh) of memory address space is reserved for system usage. Up to 256MB can be defined as local memory. The Local memory ending address is user defined through configuration registers 20h and 21h. The CY82C599 also supports 4 user defined memory block. Blocks 0 & 1 can be mapped over the entire address space by defining the base address, block size, and bus location. Blocks 2 & 3 are simply enabled/disabled (through register 46h) and can only be mapped to PCI. With these memory blocks the user can define the memory map of the system. As with I/O address space, some memory areas can be excluded from the memory map, and are therefore defined as ‘unknown’. These ‘unknown’ locations are handled on a priority basis that is discussed in memory priority sections. How the CY82C599 responds to each transaction is discussed in each of the following sections.

4.3 PCI Configuration Space

The CY82C599 supports the preferred PCI Configuration Mechanism #1 that allows PCI configuration cycles to be generated by software. Both Type 0 and Type 1 configurations accesses are also supported. All required fields within the Configuration Header Space are also supported.

5.0 Device Operation

The purpose of this section is to describe the basic operation of the CY82C599 Intelligent PCI Bus Interface. The CY82C599 functional block diagram is shown in the functional block diagram. The core functionality of the CY82C599 is controlled by the Central Arbiter and the surrounding four state machines. These four state machines communicate with one another in order to properly conduct and synchronize all transactions. Supporting functions are conducted through control logic, interface and synchronization logic (PCI and CPU buses), configuration registers, and an internal bidirectional FIFO. The following sections describes the functionality of each of these major blocks within the CY82C599.

5.1 Central Arbiter

The Central Arbiter is responsible for delegating control of the CY82C599 Intelligent PCI Bus Interface. In addition, the Central Arbiter also performs the general arbitration on the PCI bus. The Central Arbiter monitors incoming requests from both the CPU and PCI buses and grants control of the Interface to either the PP (PCI Master Controlling PCI bus) or CC (CPU Master Controlling CPU bus) state machines. Once a request has been granted, control of the Interface is transferred to that particular state machine. Once the transaction is complete, the arbiter delegates control of the bridge to the next requesting agent. Should there be no pending requests, the default owner of the bridge is the CC (CPU Master Controlling CPU bus) state machine. When servicing a CPU master bus cycle, the Central Arbiter will not grant a PCI agent control of the PCI bus (although CY82C599 to PCI transfers are permitted during CPU to memory bus transactions due to Post-Write Operations). Also, when servicing a PCI agent, a CPU hold is established (HOLD asserted and HLDA acknowledged) prior to the PCI $\overline{GNT}$ signal

being asserted. The PCI arbitration algorithm is user selectable through register 30h, and can be either fixed or rotating priority.

5.1.1 PCI Arbitration

Arbitration on the PCI bus is controlled by the Central Arbiter within the CY82C599. PCI arbitration is conducted through a request-grant handshake between the requesting master and the arbiter (CY82C599). Request and grant lines are point-to-point signals that are not universally shared on the bus. The CY82C599 will hold off granting the bus to a PCI agent if the CY82C599 is involved with a transaction. The PCI arbitration algorithm can be either a rotating or fixed priority (see control register 30h). When a fixed priority scheme is selected, $\overline{REQ0}$ /$\overline{GNT0}$ has the highest priority and $\overline{REQ3}$/$\overline{GNT3}$ the lowest priority. A rotating priority scheme starts out with same priority as the fixed algorithm ($\overline{REQ0}$/$\overline{GNT0}$ highest,...etc.). After each agent gains control of the bus it is delegated to the lowest priority. The highest priority is defaulted to the agent that has had the longest time since having control of the bus.

5.1.2 CPU Arbitration

When used in conjunction with the CY82C596/7, the CY82C599 conducts the first level arbitration on the CPU bus. If the 82C596/7 (or any device controlled by the CY82C596/7 on the ISA or VESA buses) requests control of the CPU bus, it must first assert a hold request (C597HOLD) to the CY82C599. The CY82C599 will asserts a hold request to the CPU (through the CPUHOLD signal). After completing the current transaction, the CPU acknowledges the hold by asserting the CPUHLDA signal back to the 82C599. Upon receiving this acknowledge, the CY82C599 grants the original bus request by asserting a hold acknowledge back to the CY82C596/7 by asserting C597HLDA. The CY82C599 gives the CY82C596/7 the highest priority and will interrupt PCI transactions when a request, such as a request to refresh, is received.

5.2 PCI Master Controlling PCI Bus (PP) State Machine

The PCI Master Controlling PCI Bus (PP) State Machine is responsible for executing all PCI bus transactions based on inputs from the PCI bus. This includes claiming and administering all PCI transactions where the target is on the CPU bus side of the 82C599 Interface. Such transactions are broken into two separate transfers; 1) PCI master device to the CY82C599 as the target, and 2) CY82C599 as the CPU bus master to CPU bus target. The first portion of the transaction is controlled by the PP state machine, while the second transaction is handled with the PC state machine. The PP state machine conducts all PCI related operations, provides control information to the PC state machine, and delivers the address and data to the internal FIFO.

5.3 PCI Master Controlling CPU Bus (PC) State Machine

The PCI Controlling CPU Bus (PC) state machine is responsible for all transactions on the CPU bus initiated by PCI bus inputs. These transactions include conducting a CPU bus cycle in order to deliver data from the internal FIFO to the CPU bus target. Although the PC state machine acts as the master on the CPU bus, it is not considered in control of the CY82C599 during any transaction. Instead, the PC state machine receives control signals from the PP state machine, who is in control of the CY82C599 PCI Interface.

5.4 CPU Master Controlling CPU Bus (CC) State Machine

The CPU Master Controlling CPU Bus (CC) State Machine is responsible for handling all CPU bus transactions initiated by CPU bus inputs. This includes claiming all transactions that are within the PCI or 'unknown' address spaces (memory or I/O). When a CPU bus cycle is claimed by the CY82C599, the CC state machine is in control of the CY82C599 Interface. CPU-to-PCI transfers are broken into two separate transactions; 1) CPU bus master device to the CY82C599 as the CPU bus target, and 2) CY82C599 as the PCI master to PCI bus target. The first portion of the transaction is controlled by the CC state machine, while the second transaction is handled by the CP state machine. The CC state machine conducts all CPU bus related operations, provides control information to the CP state machine, and delivers the address and data to the internal FIFO. When there are no pending bus requests, the CC state machine is the default owner of the CY82C599 Interface.

5.5 CPU Master Controlling PCI Bus (CP) State Machine

The CPU Master Controlling the PCI Bus (PC) State Machine is responsible for all transactions on the PCI bus initiated by CPU bus inputs. These transactions include conducting PCI bus cycle in order to deliver data from the internal FIFO to the PCI bus target. Although the CP state machine acts as the master on the PCI bus, it is not considered in control of the CY82C599 during any transaction. Instead, the CP state machine receives control signal from the CC state machine, who is in control of the CY82C599 Interface.

5.6 Post Write Operation

The CY82C599 allows Post-Writing for both CPU-to-PCI bus, and PCI-to-CPU bus transactions. The Post-Write FIFO is a four deep, 64-bit wide circular FIFO designed to allow a CPU or PCI bus agents to Post-Write four full words (32 bits of address and 32 bits of data) to the CY82C599. Once the information arrives in the FIFO, the CY82C599 requests control of the PCI or CPU bus in order to complete the write transaction. Once a line of data has been read from the FIFO, an additional line can be written in order to keep the FIFO full and increase throughput. Should a Post-Write to a PCI agent go unclaimed, the CY82C599 will retry a predetermined number of attempts (see register 33h). Should the transaction still go unclaimed, the data will be lost. By providing this Post-Write feature, the CY82C599 allows the CPU to Post-Write to the CY82C599, and then proceed with other transactions.

5.7 PCI Burst Pre-Read Operation

The CY82C599 supports CPU-to-PCI Burst Pre-Read operations. Pre-Reads are similar to Post-Writes, and are handled with the use of the same on-chip FIFO. The CY82C599 can pre-fetch read data, fill the internal FIFO, and then burst read to the requesting master on the PCI bus. During this pre-fetch, the CY82C599 holds the requesting bus by inserting wait states. The CY82C599 will burst the data to the requesting PCI agent in a linear sequence.

5.8 Synchronous/Asynchronous PCI Operation

The CY82C599 allows for both synchronous and asynchronous PCI bus operation. Synchronous PCI bus operation is defined as when the PCI and CPU buses are operating from the same clock. Asynchronous PCI operation is defined as when the PCI and CPU clocks are either out of phase or running at different frequencies. The CY82C599 is able to accommodate the two asynchronous buses through the use of advanced synchronization circuitry. The asynchronous operation can support a CPU clock up to 50MHz, and a PCI clock from 0 to 40MHz.

6.0 Address Space Priority

The CY82C599 employs a priority scheme for all memory and I/O transactions. The purpose for this priority system is to achieve predictable results should there be an overlap in the

memory or I/O address space, as well as accesses to 'unknown' address locations. The purpose of the following sections is to explain the priorities of each type of transaction from each side of the CY82C599 Interface.

6.1 CPU Bus Master Priority-Memory Accesses

The highest priority in a CPU bus master memory access is when the target resides in Local memory. During these cycles, the CY82C599 monitors, but does not participate in the transaction.

The second highest priority in a CPU bus master memory access is when the target is in PCI or VESA memory address space. For transactions to PCI memory space, the CY82C599 will claim the transaction by asserting $\overline{\text{LDEV}}$. The transaction is allowed to proceed normally, and is terminated on the CPU bus with $\overline{\text{CPURDY}}$ from the CY82C599. If the transaction is claimed by a VESA device, the VESA target will drive $\overline{\text{LDEV}}$ and terminates the transaction with $\overline{\text{CPURDY}}$.

The lowest priorities are CPU bus master memory accesses to VESA or ISA address space. The CY82C599 will monitor, but will not participate in the transaction.

The CY82C599 will claim all memory transactions to 'unknown' address space on the CPU bus by asserting $\overline{\text{LDEV}}$ and will immediately initiate a PCI cycle. If the target is a PCI device (in 'unknown' space), the transaction is claimed by the PCI device and proceeds normally, with the CY82C599 terminating the transaction by asserting $\overline{\text{CPURDY}}$ to the CPU. If the PCI transaction goes unclaimed, the CY82C599 de-asserts $\overline{\text{LDEV}}$. The CY82C599 will automatically de-assert $\overline{\text{LDEV}}$ if $\overline{\text{CPURDY}}$ goes active (the transaction was claimed and completed by a VESA device). If the target is a VESA device (in 'unknown' space), it asserts $\overline{\text{LDEV}}$ and claims the transaction. Since $\overline{\text{LDEV}}$ from the CY82C599 and the VESA devices are ANDed together, the CY82C596/7 will only pass the cycle to the ISA bus if neither VESA or PCI claims the transaction. Since VESA and PCI agents share the same priority, two memory devices (one on VESA and the other PCI) should never share the same address space. Doing so will cause a clash condition by having both devices claim the same transaction.

6.2 CPU Bus Master Priority-I/O Accesses

The highest priority CPU bus master I/O transaction is PCI/VESA space. These two types of devices I/O address spaces are considered to have the same priority. The CY82C599 will claim I/O transactions to PCI address space by asserting $\overline{\text{LDEV}}$. The transaction is allowed to proceed normally, and is terminated on the CPU bus with $\overline{\text{CPURDY}}$ from the CY82C599. If the transaction is to VESA I/O address space, the VESA target will claim the transaction by asserting $\overline{\text{LDEV}}$.

The second priority CPU bus master access to I/O space is when the target resides in ISA space. The CY82C599 will monitor, but not participated in CPU bus master transactions to ISA space.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. The CY82C599 will claim all I/O transactions to 'unknown' address space on the CPU bus by asserting $\overline{\text{LDEV}}$ and will immediately initiate a PCI cycle. If the target is a PCI device (in 'unknown' space), the transaction is claimed by the PCI device and proceeds normally, with the CY82C599 terminating the transaction by asserting $\overline{\text{CPURDY}}$ to the CPU. If the PCI transaction goes unclaimed, the CY82C599 de-asserts $\overline{\text{LDEV}}$. The CY82C599 will automatically de-assert $\overline{\text{LDEV}}$ if $\overline{\text{CPURDY}}$ goes active (the transaction was claimed and completed by a VESA device). If the target is a VESA device (in 'unknown' space), it asserts $\overline{\text{LDEV}}$ and claims the transaction. Since $\overline{\text{LDEV}}$ from the CY82C599 and the VESA devices are ANDed together, the CY82C596/7 will only pass the cycle to the ISA bus if neither VESA or PCI claims the transaction. Since VESA and PCI agents share the same priority, two I/O devices (one on VESA and the other PCI) should never share the same address space. Doing so will cause a clash condition by having both devices claim the same transaction.

6.3 PCI Master Priority-Memory Accesses

The highest priority PCI master memory transaction is an access to Local memory. During such transactions the CY82C599 will claim the CPU bus as quickly as possible by asserting a hold request to the CPU. PCI bus ownership is not be granted until a hold acknowledge is received back from the CPU. Once bus ownership has been established, the transaction proceeds normally with the CY82C599 as the CPU bus master.

The second priority PCI master memory transaction is to PCI memory located on another PCI card. During these transactions the CY82C599 monitors, but does not participate in the transaction. In addition, the CY82C599 will hold the CPU bus during the entire transaction.

The third priority PCI master memory transaction is to ISA/VESA address space. During these types of transfers, the CY82C599 will claim the ISA/VESA bus as soon as possible and initiate an ISA/VESA cycle.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. PCI agents are given the first opportunity to claim PCI master accesses to 'unknown' memory space. The CY82C599 will wait for a PCI agent to claim the transaction by monitoring $\overline{\text{DEVSEL}}$. If the transaction goes unclaimed on the PCI bus, the CY82C599 will automatically start a CPU bus cycle. If the transaction goes unclaimed on the CPU bus, the 82C596/7 will automatically pass the transaction to the ISA bus.

6.4 PCI Master Priority-I/O Accesses

The highest priority PCI master I/O access is to PCI address space. During these transactions the CY82C599 monitors, but does not participate in the transaction. In addition, the CPU bus is held during the entire transaction.

The second priority PCI master I/O transaction is to the ISA bus. During such transactions, the CY82C599 will claim the transaction by asserting $\overline{\text{DEVSEL}}$ and behave as the PCI target. The CY82C599 will also start a CPU bus as soon as possible and initiate an ISA/VESA cycle.

If the address is not mapped to PCI/VESA or ISA space, then it is considered as 'unknown'. PCI agents are given the first opportunity to claim PCI master accesses to 'unknown' I/O space. The CY82C599 will wait for a PCI agent to claim the transaction by monitoring the $\overline{\text{DEVSEL}}$. If the transaction goes unclaimed on the PCI bus, the CY82C599 will automatically start a CPU bus cycle. If the transaction goes unclaimed on the CPU bus, the 82C596/7 will automatically pass the transaction to the ISA bus.

7.0 Level 1 Write-Back Cache Support

The CY82C599 also provides for chipsets that support Level 1 write-back cache. The CY82C599 adheres to the $\overline{\text{HITM}}$ protocol required to maintain cache coherency. When $\overline{\text{HITM}}$ is asserted, the CPU has detected a hit to a modified line in the Level 1 cache. In order to allow the CPU to write-back the modified line, the CY82C599 de-asserts the HOLD request to the CPU. The CPU then proceeds to write the modified line to DRAM and L2 cache (if a L2 cache hit is detected). The CY82C599 immediately requests another HOLD to the CPU so the initial transaction can continue.

8.0 Stand-Alone Mode

The CY82C599 can work in conjunction with the 82C596/7 to provide a high performance VESA/ISA/PCI PC/AT system. The CY82C599 also has the built-in flexibility to work with other chipsets to provide a CPU-to-PCI bus bridge. This is referred to as Stand Alone Mode. In Stand-Alone mode, the CY82C599 has enough flexibility to accommodate other chipset's logic and is able to pass transactions to 'unknown' space from one bus to another. In order to operate properly in Stand-Alone mode, the register set of the accompanying chipset must be compatible with the CY82C599 (contact the factory for details).

9.0 Power Management Mode

The CY82C599 implements flexible power management logic. When used with the CY82C597 (for a full VESA/ISA/PCI system), most of the power management functions are performed by the CY82C599. The CY82C597 will only perform the SMM memory mapping. All other power management functions in the CY82C597 are disabled. For VESA/ISA-only systems, the CY82C597 provides all of the chipset power management.

There are eleven event detectors and five user-programmable timers in the CY82C599 allowing it to support full hardware power management (for CPUs that do not support SMM, System Management Mode) and software power management (through SMM).

Events that can be Monitored

The CY82C599 allows the following events to be monitored:

1) VESA master request
2) Keyboard command
3) Serial Port command
4) Parallel Port command
5) Hard Disk command
6) DMA/MASTER request from the ISA bus
7) Non-motherboard memory access
8) Video memory access
9) A specific I/O address
10) A specific memory range
11) A specific I/O range

When events are detected, the CY82C599 will transition to different power-down states.

Hardware Power Management

For hardware power management, the CY82C599 supports Full-speed/Stand-by/Suspend/Off states. In Stand-by state, the CY82C599 will assert the $\overline{\text{SLOWCLK}}$ signal that can be used by the system to slow down the CPU's clock frequency. In the Suspend state, the CY82C599 will assert the $\overline{\text{STOPCLK}}$ signal. $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or turn off the monitor and other supported peripherals.

In the Full-speed state, the CY82C599 will monitor all stand-by events. Any monitored event will reset the stand-by timer. If no events occur within the period specified by the stand-by timer, the CY82C599 will enter the Stand-by state and assert the $\overline{\text{SLOWCLK}}$ signal. Once Stand-by state has been entered, the CY82C599 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C599 will assert $\overline{\text{STOPCLK}}$ and enter the Suspend state. In the Suspend state, the assertion of $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or power-down any supported peripherals. If any monitored event is detected, the CY82C599 will return to the Full-speed state and $\overline{\text{STOPCLK}}$/$\overline{\text{SLOWCLK}}$ will be deasserted.

Any interrupt will temporarily cause the $\overline{\text{STOPCLK}}$ signal (and optionally the $\overline{\text{SLOWCLK}}$ signal) to be deasserted (allowing the CPU to service the interrupt). If the interrupt timer expires before a monitored event occurs, the CY82C599 will automatically return to the power-down state it was in prior to the interrupt (with the appropriate signal asserted).

Software Power Management

For software power management, the CY82C599 can fully utilize Intel's, AMD's, and Cyrix's power management modes to reduce system power requirements.

In the Full-speed state, the CY82C599 will monitor all stand-by events. If no events occur within the period specified by the stand-by timer, the CY82C599 will enter the Stand-by state and assert the $\overline{\text{SMI}}$ signal. In Stand-by state, the system clock can be slowed down by the assertion of the $\overline{\text{SLOWCLK}}$ signal. $\overline{\text{SLOWCLK}}$ is controlled through software (See Register 64). Once Stand-by state has been entered, the CY82C599 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C599 will assert $\overline{\text{SMI}}$ and enter the Suspend state. In the Suspend state, software assertion of $\overline{\text{STOPCLK}}$ (See register 64) can be used to stop the CPU's clock, the monitor can be turned off using a software driver, or the hard disk can be spun down. Please note that the assertion/deassertion of $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ is fully software controlled and can be implemented in any power-down state (Stand-by and Suspend are customary).

The Suspend timer is fully reprogrammable. In the Suspend state, the Suspend timer can be disabled, the timer value changed, and the timer re-enabled. After the new timer value has expired, $\overline{\text{SMI}}$ will once again be activated to allow for a user-defined power management mode.

The CY82C599 also contains three independent timers that can be used during the power-down control period. Different events and different time periods can be specified for each timer. Each timer will cause $\overline{\text{SMI}}$ to be asserted after the specified time period has expired. The three timers allow for more user-defined, power-down system states.

In order to identify the source of the $\overline{\text{SMI}}$ (System Management Interrupt), the CY82C599 maintains a status register (register 58) that keeps track of which event caused $\overline{\text{SMI}}$ to be asserted. Power-management software should read the status register before determining a course of action. The CPU and peripherals can be individually powered-down based on the source of the System Management Interrupt.

If any specified event is detected during Stand-by, Suspend, or any other power-down state, the CY82C599 will automatically return to the Full-speed state (with the stand-by timer reset). If the system is using software power management, the CY82C599 will assert $\overline{\text{SMI}}$ and within the $\overline{\text{SMI}}$ handler, software should bring all of the system clocks to their full-speed, full-power states through the de-assertion of $\overline{\text{STOPCLK}}$/$\overline{\text{SLOWCLK}}$.

10.0 Control Registers

This section summarizes the registers in the CY82C599.

The on-chip registers are accessed via I/O sequence 22H and 23H. Each register is selected by writing a byte containing the register address index to I/O address 22H. A subsequent byte read/write to I/O address 23H will modify/read-out the contents of the selected register.

The CY82C599 provides five groups of registers :

Memory address space configuration registers (except PC/AT high memory)

I/O address space configuration registers

Power down configuration registers

State machine configuration registers

PC/AT high memory address space configuration registers

The Local DRAM Address Configuration Registers are used to establish the boundary of the Local DRAM in the system. Index 20H and 21H are used to specify the ending address of on-board DRAMs. Index 22H to 27H are the configuration registers for Memory Blocks 0 and 1. They contain the base address of each memory block, the block sizes, and the mapping selection for each block : Local DRAM region, PCI region or ISA region. It is best to specify all Non-Local DRAM memory areas below 16Mbytes as ISA region and remap all other Non-Local DRAM memory areas above 2 Gbytes as the PCI region.

I/O Block Configuration Registers are used to specify the base address, block size, and function select for the user selectable I/O blocks. The pre-defined I/O blocks are simply enabled or disabled.

Power Down Configuration Registers allow various hardware events to be monitored in order to invoke or come out of power down mode.

State Machine configuration registers control features of the PCI and CPU bus State Machines. These features include the number of wait states, and arbitration priority of both State Machines.

PC/AT High Memory Address Space Configuration Registers are used to specify the memory regions from 000A0000H to 000FFFFFH (blocks A, B, C, D, E, and F). These bits are used with CY82C59/67 to provide shadowing in a PC/AT system.

Index 20H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3:0	Local DRAM Ending Address: $\overline{A27}$: $\overline{A24}$	0000	User selectable

Index 21H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Local DRAM Ending Address: $\overline{A23}$: $\overline{A16}$	00000000	User selectable

Index 22H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 0 Base Address: A31 : A24	00000000	User selectable

Index 23H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 0 Base Address: A23 : A16	0000000	User selectable

Index 24H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:6	Memory Block 0 Base Address: A15 : A14	00	User selectable
5:4	Memory Block 0 Function Select 00: Disable (Default) 01: Local DRAM Region 10: PCI Region 11: ISA /VESA Region	00	User selectable
3:0	Memory Block 0 Size Select: 0000: 16KByte (Default) 0001: 32KByte 0010: 64KByte 0011: 128KByte 0100:: 256KByte 0101: 512KByte 0110: 1MByte 0111: 2MByte 1000: 4MByte 1001: 8MByte 1010: 16MByte 1011: 32MByte 1100: 64MByte 1110: 256MByte 1111: 512MByte	0000	User selectable

Index 25H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 1 Base Address: A31 : A24	00000000	User selectable

Index 26H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory Block 1 Base Address: A23 : A16	00000000	User selectable

Index 27H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:6	Memory Block 1 Base Address: A15 : A14	00	User selectable
5:4	Memory Block 1 Function Select 00: Disable (Default) 01: Local DRAM Region 10: PCI Region 11: ISA/VESA Region	00	User selectable
3:0	Memory Block 1 Size Select: 0000: 16KByte (Default) 0001: 32KByte 0010: 64KByte 0011: 128KByte 0100: 256KByte 0101: 512KByte 0110: 1MByte 0111: 2MByte 1000: 4MByte 1001: 8MByte 1010: 16MByte 1011: 32MByte 1100: 64MByte 1110: 256MByte 1111: 512MByte	0000	User selectable

Index 28H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Block 0 Base Address: A15 : A8	00000000	User selectable

Index 29H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	I/O Block 0 Base Address: A7 : A4	0000	User selectable
3:2	I/O Block 0 Function Select: 0X: Disable (Default) 10: PCI Region 11: ISA/VESA Region	00	User selectable
1:0	I/O Block 0 Size Select: 00: 16 Byte (Default) 01: 64 Byte 10: 256 Byte 11: 1024Byte	00	User selectable

Index 2AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Block 1 Base Address: A15 : A8	00000000	User selectable

Index 2BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	I/O Block 1 Base Address: A7 : A4	0000	User selectable
3:2	I/O Block 1 Function Select: 0X: Disable (Default) 10: PCI Region 11: ISA/VESA Region	00	User selectable
1:0	I/O Block 1 Size Select: 00: 16 Byte (Default) 01: 64 Byte 10: 256 Byte 11: 1024Byte	00	User selectable

Index 2CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Keyboard Detection Enable 0: Disable 1: Enable	0	User selectable
6	Serial Port Detection Enable 0: Disable 1: Enable	0	User selectable
5	Parallel Port Detection Enable 0: Disable 1: Enable	0	User selectable
4	Hard Disk Detection Enable 0: Disable 1: Enable	0	User selectable
3	CY82C599 Hold Detection Enable 0: Disable 1: Enable	0	User selectable
2	Non Motherboard Memory Detection Enable 0: Disable 1: Enable	0	User selectable
1	Non Motherboard I/O Detection Enable 0: Disable 1: Enable	0	User selectable
0	Video RAM Detection Enable 0: Disable 1: Enable	0	User selectable

Index 2DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved	0	0
6	Green Feature Timer Select (see Register 2DH, Bits 3:0).	0	User selectable
5	PCI Master Detection Enable 0: Disable 1: Enable	0	User selectable
4	Floppy Disk Detection Enable 0: Disable 1: Enable	0	User selectable
3:1	Green Feature Timer Delay Select Bit 6=0 / Bit 6=1 000: 30 Second / 000: 0.2 Seconds 001: 4 Minute / 001: 0.4 Seconds 010: 8 Minute / 010: 1.0 Seconds 011: 16 Minute / 011: 1.8 Seconds 100: 32 Minute / 100: 3.5 Seconds 101: 65 Minute / 101: 7.0 Seconds 110: 130 Minute / 110: 14.0 Seconds 111: 260 Minute / 111: 30.0 Seconds	000	User selectable
0	Green Feature Enable 0: Disable 1: Enable	0	User selectable

Index 2EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	I/O Trap Address: IOA7 : IOA0	00000000	User selectable

Index 2FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved	0000	0000
3	I/O Trap Detection Enable 0: Disable 1: Enable	0	User selectable
2	Reserved	0	0
1:0	I/O Trap Address: IOA9 : IOA8	00	User selectable

Index 30H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Function Enable 0: Disable 1: Enable	0	1
6	Reserved	0	0
5	$\overline{\text{LRDY}}$ Delay Enable 0: Disable 1: Enable	0	1
4	Reserved	0	0
3	Arbitration Fast Interface Enable 0: Disable 1: Enable	0	0
2	PCI Hidden Arbitration Mode Enable 0: Disable 1: Enable	0	0
1	Reserved	0	1
0	PCI Arbitration Rotate Priority Enable 0: Disable (Fixed) 1: Enable (Rotating)	0	0

Index 31H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Reserved.	00000000	00001000

Index 32H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Disable $\overline{\text{BOFF}}$ to CPU Control 0: Disable 1: Enable	0	1
6:5	Reserved	00	01
4	CPU Master Post Write Buffer Enable 0: Disable 1: Enable	0	1
3	CPU Master State Machine Fast Interface Enable 0: Disable 1: Enable	0	0
2	CPU Master CPU State Machine Address 0WS Enable 0: Disable (1 WS) 1: Enable (0 WS)	0	0
1	CPU Master CPU State Machine Data Write 0WS Enable 0: Disable (1 WS) 1: Enable (0 WS)	0	0
0	CPU Master CPU State Machine Data Read 0WS Enable 0: Disable (1 WS) 1: Enable (0 WS)	0	0

Index 33H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	CPU Master CPU State Machine I/O Post Write Cycle Enable 0: Disable 1: Enable	0	0
6	Reserved	0	1
5:4	CPU Master PCI Retry 00: Disable (Default) 01: 1 10: 3 11: Infinite	00	11
3	CPU Master Write Burst Mode Enable 0: Disable 1: Enable	0	0
2	CPU Master PCI State Machine Fast Back-to-Back Enable 0: Disable 1: Enable	0	0
1	CPU Master PCI State Machine Address OWS Enable 0: Disable 1: Enable	0	0
0	CPU Master PCI State Machine Data Write OWS Enable 0: Disable 1: Enable	0	0

Index 34H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved	0	0
6	PCI Master Post Write Buffer Enable 0: Disable 1: Enable Note: Register 34 Bit 6 and Register 35, Bit4 together control the Post write funcitonality. See below for desired register settings. Reg. 34 Bit6 / Reg. Bit 4 / Function 0 / X / Non Burst, No Post-Write 1 / 0 / Non Burst, Post-Write 1 / 1 / Burst, Post-Write	0	0
5	Burst Pre-Read Enable 0: Disable 1: Enable Note: Register 34 Bit 5 and Register 34, Bit4 together control the Burst Pre-Read funcitonality. See below for desired register settings. Reg. 34 Bit6 / Reg. Bit 4 / Function 0 / X / Burst Pre-Read Off 1 / 0 / Burst Pre-Read to Local Memory only. 1 / 1 / Burst Pre-Read to ISA, VESA, and Local memory	0	0
4	PCI Master Pre-read Buffer Enable 0: Disable 1: Enable	0	0
3	PCI Master PCI State Machine VESA+ISA Post Write Enable 0: Disable 1: Enable	0	0
2	PCI Master PCI State Machine Address 0WS Enable 0: Disable (1 WS) 1: Enable (0 WS)	0	0
1	PCI Master CPU State Machine Address 0WS Enable 0: Disable (1 WS) 1: Enable (0 WS)	0	0
0	PCI Master PCI State Machine Data Read 0WS Enable 0: Disable (1 WS) 1: Enable (0 WS)	0	0

Index 35H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Master PCI State Machine Data Write 0WS Enable 0: Disable 1: Enable	0	0
6	PCI Master PCI State Machine Burst Mode Enable 0: Disable 1: Enable	0	0
5	PCI Master State Machine Fast Interface Enable 0: Disable 1: Enable	0	0
4	PCI Master State Machine Generate Fast $\overline{ADS}$ Cycle Enable 0: Disable 1: Enable Note: See register 34, Bit6.	0	0
3:2	CPU Master PCI $\overline{DEVSEL}$ Time Out Period 00: 6 PCICLK (Default) 01: 5 PCICLK 10: 4 PCICLK 11: 3 PCICLK	00	00
1:0	PCI Master PCI Subtractive Decode $\overline{DEVSEL}$ Time Out Period 00: 6 PCICLK (Default) 01: 5 PCICLK 10: 4 PCICLK 11: 3 PCICLK	00	10

Note: PCI Master PCI Subtractive Decode $\overline{DEVSEL}$ Time Out Period must be equal or less than CPU Master PCI $\overline{DEVSEL}$ Time Out Period

Index 36H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Configuration Address Cycle Enable 0: Disable 1: Enable	0	1
6	Configuration Data Cycle Enable 0: Disable 1: Enable	0	1
5	Configuration Data Special Cycle Enable 0: Disable 1: Enable	0	1
4	PCI Master Configuration Address Cycle Enable 0: Disable 1: Enable	0	0
3	Reserved	0	0
2	Reserved.	0	0
1	First Level Arbitration Rotate Enable 0: Disable 1: Enable	0	0
0	Reserved	0	1

Index 37H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:3	Reserved	00000	11111
2	Configuration Register TARGET ABORT Status Bit Enable 0: Disable 1: Enable	0	0
1	$\overline{\text{PERR}}$ External Support Enable 0: Disable 1: Enable	0	0
0	$\overline{\text{SERR}}$ External Support Enable 0: Disable 1: Enable	0	0

Index 38H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block A0000h : A7FFFh Bits 7:6 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	0000
3:0	Shadow Block A8000h : AFFFFh Bits 3:2 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	1010

Index 39H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block B0000h : B7FFFh Bits 7:6 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	User selectable
3:0	Shadow Block B8000h : BFFFFh Bits 3:2 Function: 00: Disable; 01: Reserved; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Reserved; 10: PCI Write; 11: ISA/VESAWrite	0000	User selectable

Index 3AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block C0000h : C3FFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block C4000h : C7FFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block C8000h : CBFFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block CC000h : CFFFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D0000h : D3FFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block D4000h : D7FFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D8000h : DBFFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block DC000h : DFFFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Shadow Block D8000h : EFFFFh Bits 7:6 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 5:4 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable
3:0	Shadow Block F0000h : FFFFFh Bits 3:2 Function: 00: Disable; 01: Local DRAM Read; 10: PCI Read; 11: ISA/VESA Read Bits 1:0 Function: 00: Disable; 01: Local DRAM Write; 10: PCI Write; 11: ISA/VESA Write	0000	User selectable

Index 3FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved.	0000	0000
3:2	Pin 16,17 Function Select Bits 3:2 Function: 00: Disabled; 01: A30, A29 enabled; 10: $\overline{\text{INTLI}}/\overline{\text{INTEO}}$ enable; 11: Invalid condition, do not use.	00	User selectable
1:0	Pin 18 function Select Bits 1:0 Function: 00: Disabled; 01: A28 enabled; 10: SLOWCLK enable; 11: Invalid condition, do not use.	00	User selectable

Index 40H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved. Must be set to 1 after power-on.	0	1
6	Reserved.	0	1
5	Reserved, Must be set to 1 after power-on.	0	1
4	I/O write 22H, 23H, & 61H $\overline{\text{LDEV}}$ mask enable.	0	0
3	Reserved, must be set to 1 after power-on.	0	1
2	Configuration register Read Enable. 0: Write only. 1: Read/Write.	0	1
1	Monitor VESA VL Bus $\overline{\text{LDEV}}$ enable.	0	0
0	VESA to PCI Stand Alone enable.	0	0

Index 41H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	VESA VL Bus $\overline{\text{BS16}}$ support enable.	0	0
6:0	Reserved.	0000000	0010111

Index 42H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved.	0000	0001
3	Write back mode with no PCI Master HOLD support enable.	0	0
2:1	Reserved, set to 0 after power-on.	00	00
0	Level 1 Write back mode enable.	0	0

Index 43H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	$\overline{\text{LRDY}}$ delay 1 CPUCLK enable.	0	0
6:0	Reserved.	0000000	0000000

Index 44H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Not used, available for BIOS storage.	00000000	00000000

Index 45H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Not used, available for BIOS storage.	00000000	00000000

Index 46H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI Memory Block 2 Enable (A31=1, A27=0, A26=1 0: Disable 1: Enable	0	1
6:4	PCI Memory Block 2 Address Select A30, A29, A28	000	000
3	PCI Memory Block 3 Enable (A31=1, A27=1, A26=0 0: Disable 1: Enable	0	1
2:0	PCI Memory Block 2 Address Select A30, A29, A28	000	000

Index 47H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	PCI I/O Block 2 base address A15−A12. Note: A15−A12=0H disable PCI I/O block 2.	0000	0000
3	Reserved. Set to 0.	0	0
2:1	PCI I/O block 2 size select S1-S0. S1 S0 Size. 0 0 1KB 0 1 2KB 1 0 4KB 1 1 8KB	00	00
0	PCI I/O block 2 enable..	0	0

Index 48H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0100H to 010FH select enable.	0	User selectable
6	ISA/VESA I/O space 0110H to 011FH select enable.	0	User selectable
5	ISA/VESA I/O space 0120H to 012FH select enable.	0	User selectable
4	ISA/VESA I/O space 0130H to 013FH select enable.	0	User selectable
3	ISA/VESA I/O space 0140H to 014FH select enable.	0	User selectable
2	ISA/VESA I/O space 0150H to 015FH select enable.	0	User selectable
1	ISA/VESA I/O space 0160H to 016FH select enable.	0	User selectable
0	ISA/VESA I/O space 0170H to 017FH select enable.	0	User selectable

Index 49H

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0180H to 018FH select enable.	0	User selectable
6	ISA/VESA I/O space 0190H to 019FH select enable.	0	User selectable
5	ISA/VESA I/O space 01A0H to 01AFH select enable.	0	User selectable
4	ISA/VESA I/O space 01B0H to 01BFH select enable.	0	User selectable
3	ISA/VESA I/O space 01C0H to 01CFH select enable.	0	User selectable
2	ISA/VESA I/O space 01D0H to 01DFH select enable.	0	User selectable
1	ISA/VESA I/O space 01E0H to 01EFH select enable.	0	User selectable
0	ISA/VESA I/O space 01F0H to 01FFH select enable.	0	User selectable

Index 4AH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0200H to 020FH select enable.	0	User selectable
6	ISA/VESA I/O space 0210H to 021FH select enable.	0	User selectable
5	ISA/VESA I/O space 0220H to 022FH select enable.	0	User selectable
4	ISA/VESA I/O space 0230H to 023FH select enable.	0	User selectable
3	ISA/VESA I/O space 0240H to 024FH select enable.	0	User selectable
2	ISA/VESA I/O space 0250H to 025FH select enable.	0	User selectable
1	ISA/VESA I/O space 0260H to 026FH select enable.	0	User selectable
0	ISA/VESA I/O space 0270H to 027FH select enable.	0	User selectable

Index 4BH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0280H to 028FH select enable.	0	User selectable
6	ISA/VESA I/O space 0290H to 029FH select enable.	0	User selectable
5	ISA/VESA I/O space 02A0H to 02AFH select enable.	0	User selectable
4	ISA/VESA I/O space 02B0H to 02BFH select enable.	0	User selectable
3	ISA/VESA I/O space 02C0H to 02CFH select enable.	0	User selectable
2	ISA/VESA I/O space 02D0H to 02DFH select enable.	0	User selectable
1	ISA/VESA I/O space 02E0H to 02EFH select enable.	0	User selectable
0	ISA/VESA I/O space 02F0H to 02FFH select enable.	0	User selectable

Index 4CH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0300H to 030FH select enable.	0	User selectable
6	ISA/VESA I/O space 0310H to 031FH select enable.	0	User selectable
5	ISA/VESA I/O space 0320H to 032FH select enable.	0	User selectable
4	ISA/VESA I/O space 0330H to 033FH select enable.	0	User selectable
3	ISA/VESA I/O space 0340H to 034FH select enable.	0	User selectable
2	ISA/VESA I/O space 0350H to 035FH select enable.	0	User selectable
1	ISA/VESA I/O space 0360H to 036FH select enable.	0	User selectable
0	ISA/VESA I/O space 0370H to 037FH select enable.	0	User selectable

Index 4DH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 0378H to 037FH select enable.	0	User selectable
6	ISA/VESA I/O space 0380H to 038FH select enable.	0	User selectable
5	ISA/VESA I/O space 0390H to 039FH select enable.	0	User selectable
4	ISA/VESA I/O space 03A0H to 03AFH select enable.	0	User selectable
3	ISA/VESA I/O space 03B0H to 03BBH select enable.	0	User selectable
2	ISA/VESA I/O space 03BCH to 03BFH select enable.	0	User selectable
1	ISA/VESA I/O space 03C0H to 03CFH select enable.	0	User selectable
0	ISA/VESA I/O space 03D0H to 03DFH select enable.	0	User selectable

Index 4EH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	ISA/VESA I/O space 03E0H to 03E7H select enable.	0	User selectable
6	ISA/VESA I/O space 03E8H to 03EFH select enable.	0	User selectable
5	ISA/VESA I/O space 03F0H to 03F5H select enable.	0	User selectable
4	ISA/VESA I/O space 03F6H to 03F7H select enable.	0	User selectable
3	ISA/VESA I/O space 03F8H to 03FFH select enable.	0	User selectable
2	ISA/VESA I/O space 0000H to 00FFH select enable.	0	User selectable
1	ISA/VESA I/O space ignore A15:10 decode enable.	0	User selectable
0	ISA/VESA I/O space C.R. 48H-4EH overall enable.	0	User selectable

Index 4FH

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	PCI I/O space 01F0H to 01FFH select enable.	0	User selectable
6	PCI I/O space 03F6H to 03F7H select enable.	0	User selectable
5	PCI I/O space 0170H to 017FH select enable.	0	User selectable
4	PCI I/O space 0370H to 0377H select enable.	0	User selectable
3	PCI I/O space 03B0H to 03BBH select enable.	0	User selectable
2	PCI I/O space 03C0H to 03CFH select enable.	0	User selectable
1	PCI I/O space 03D0H to 03DFH select enable.	0	User selectable
0	PCI I/O space 03F0H to 03F5H select enable.	0	User selectable

Register 50: Suspend Timer and Interrupt Timer Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits (Suspend Timer Period) 0000: 3.8 min. 0001: 7.5 min. 0010: 15 min. 0011: 30 mins. 0100: 60 mins. 0101: 120 mins. 0110: 240 mins. 0111: 480 mins. 0000: 1 sec. 1001: 1.8 sec. 1010: 3.5 sec. 1011: 7 sec. 1100: 14 sec. 1101: 28 sec. 1110: 56 sec. 1111: 2 min.	0000	User selectable
3:0	Bits (Interrupt Timer Period) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 54 usec. 0110: 107 usec. 0111: 215 usec. 0000: 430 usec. 1001: 860 usec. 1010: 1.7 msec. 1011: 3.4 msec. 1100: 7 msec. 1101: 14 msec. 1110: 28 msec. 1111: 55 msec.	0000	User selectable

The suspend timer is enabled when register 52 bit 1=0. When enabled, the suspend timer always follows the stand-by timer (i.e., it will not start counting until the stand-by timer has reached its terminal count. For hardware Power-down mode, the 82C599 will assert $\overline{\text{STOPCLK}}$ after the suspend timer has reached its terminal count. For software Power-down mode, the 82C599 will generate an $\overline{\text{SMI}}$ after its terminal count $\overline{\text{STOPCLK}}$ and other power-down features can be implemented in an $\overline{\text{SMI}}$ subroutines.

When the INTR input becomes active, the 82C599 will deassert $\overline{\text{STOPCLK}}$ and start the interrupt timer. After the interrupt timer reaches its terminal count, the 82C599 will assert $\overline{\text{STOPCLK}}$ again (if no event occurs during the interrupt period). This timer is used for both hardware and software Power-down modes and is enabled by register 51, Bit 2.

Register 51: Power-down Mode

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable hardware Power-down mode 1: Enable hardware Power-down mode	0	User selectable
6	Bits 0: Disable software Power-down mode 1: Enable software Power-down mode	0	User selectable
5	Bits 0: Disable interrupt input (INTR) 1: Enable interrupt input (INTR) Should be 1 when Power-down mode	0	User selectable
4	Should be 0	0	0
3	Bits 0: $\overline{\text{SLOWCLK}}$ does not change when input INTR active 1: $\overline{\text{SLOWCLK}}$ will be inactive when input INTR active	0	User selectable
2	Bits 0: Enable interrupt timer (default) 1: Disable interrupt timer	0	User selectable
1	Reserved.	0	0
0	Must have the same value as bit 6.	0	See bit 6.

Hardware Power-down mode allows $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ to be controlled by the 82C599 hardware. Software Power-down mode will use System Management Mode ($\overline{\text{SMM}}$) subroutines to implement power-down control.

Register 52: Power-Down Mode Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits Software initial $\overline{SMI}$ 0: Normal 1: Writing an 1 to this bit will generate an $\overline{SMI}$ to the CPU. After a 1 is written, software should write a 0 to this bit.	0	User selectable
6	Bits $\overline{SMI}$ inactive control 0: Normal 1: Writing a 1 to this bit will deassert the $\overline{SMI}$ signal. This is the only way to cause the 82C599 to deassert $\overline{SMI}$. After a 1 is written, 0 should be written to this bit to allow $\overline{SMI}$ to be deasserted.	0	User selectable
5	Bits $\overline{STOPCLK}$ Active Control 0: Normal 1: Writing a 1 to this bit will assert the $\overline{STOPCLK}$ signal. Software should subsequently write a 0 to this bit to allow $\overline{STOPCLK}$ to be deasserted.	0	User selectable
4	Bits Software $\overline{STOPCLK}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{STOPCLK}$. Software should subsequently write a 0 to this bit to allow $\overline{STOPCLK}$ to be asserted.	0	User selectable
3	Bits Software $\overline{SLOWCLK}$ Active Control 0: Normal 1: Writing a 1 will assert $\overline{SLOWCLK}$. Software should subsequently write a 0 to this bit to allow $\overline{SLOWCLK}$ to be deasserted.	0	User selectable
2	Bits Software $\overline{SLOWCLK}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{SLOWCLK}$. Software should subsequently write a 0 to this bit to allow $\overline{SLOWCLK}$ to be asserted.	0	User selectable
1	Bits Suspender Time Control 0: Enable suspend timer (default) 1: Disable suspend timer The 82C599 allows a second Suspend mode to be started after the current suspend timer has reached its terminal count (i.e. When the current suspend timer expires, it will assert $\overline{SMI}$.) Within the $\overline{SMI}$ subroutine, the suspend timer can be disabled and the suspend timer reenabled. After the new terminal count has been reached, the 82C599 will initiate another $\overline{SMI}$.	0	User selectable
0	Disable Software Reset Mask 0: Normal 1: Force CY82C599 to inactivate pin 112. This bit should be set to ”1”, then set to ”0” before leaving SMI subroutine.	0	0

Register 53: Power Management Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Reserved.	0000	0000
3	Bits 0: Normal 1: Enable power down LED to flush when 82C599 is in power down mode. CY82C599 uses pin 60 to control LED.	0	User selectable
2	Bits 0: LED is active HIGH 1: LED is active LOW.	0	User selectable
1	Bits 0: INTEL SMM mode 1: CYRIX/AMD SMM mode.	0	User selectable
0	Reserved	0000	0000

Register 54: Special Memory and I/O Event Detection

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Memory cycle: memory address A31, A26, A25, A24, A23, A22, A21, A20 detection. I/O cycle: I/O address A7, A6, A5, A4, A3, A2, A1, A0 detection.	0	User selectable

Register 55: Special Memory and I/O Event Detection

Bit	Memory Cycle	I/O Cycle	Hardware Default	Recommended BIOS power-on setting
7	Mask A31	A15	0	User selectable
6	Mask A26	A14	0	User selectable
5	Mask A25	A13	0	User selectable
4	Mask A24	A12	0	User selectable
3	Mask A23	A11	0	User selectable
2	Mask A22	A10	0	User selectable
1	Mask A21	A9	0	User selectable
0	Mask A20	A8	0	User selectable

Register 56: Special Memory and I/O Event Detection

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable special memory I/O detection 1: Enable special memory I/O detection	0	User selectable
6	Bits 0: Detect I/O cycle 1: Detect memory cycle	0	User selectable
5	Bits 0: No write cycle detection 1: Detect write cycle	0	User selectable
4	Bits 0: No read cycle detection 1: Detect ready cycle	0	User selectable
3	I/O address A19	0	User selectable
2	I/O address A18	0	User selectable
1	I/O address A17	0	User selectable
0	I/O address A16	0	User selectable

Registers 54, 55, and 56 allow for special memory or I/O event detection. For memory detection, address A31, A26, A25, A24, A23, A22, A21, and A20 are monitored. Memory detection can also be limited to read cycles or write cycles. Certain memory addresses can also be masked. (Register 55) If the corresponding mask bit (e.g. mask A20) is set, then address (A20) will not be decoded. For I/O detection, addresses A19−A0 can be monitored. I/O detection can also be limited to read-only or write-only. I/O detection does not allow for address masking.

Register 57: Power Down Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved.	0	0
6:5	Bits (LED frequency control) 00: 0.4 sec. 01: 1.0 sec. 10: 1.8 sec. 11: 3.5 sec.	0	User selectable
4	Bits Quick Power Down control 0: Disable Quick Power Down mode. 1: Enable Quick Power Down mode.	0	User selectable
3:0	Reserved.	0	0

The 82C599 supports Quick Power Down through pin 18. When pin 18 is selected, the CY82C599 will bring itself into Power Down Mode in 3 seconds if no event is detected, and Register 57, Bit 4=1.

Register 58: 82C599 Status Register

Read Cycle:	Set A	Set B
7=1	SMI caused by start of stand-by mode	Reserved.
6=1	SMI caused by end of stand-by mode	Reserved.
5=1	SMI caused by suspend timer reaching its terminal count	82C599 is in power-down mode (stand-by or suspend mode)
4=1	SMI caused by register 52, bit 7	82C599 is in suspend mode. Once in suspend mode, this bit will stay 1 unless any suspend event becomes active, or power-down mode is disabled.
3=1	SMI caused by timer 3 reaching its terminal count	$\overline{\text{STOPCLK}}$ pin is active
2=1	SMI caused by timer 3 reset by an event	$\overline{\text{SLOWCLK}}$ pin is active
1=1	SMI caused by timer 4 reaching its terminal count	Suspend timer has reached its terminal count. It will be 0 if register 52, bit 1 is set to 1 later.
0=1	SMI caused by timer 4 reset by an event	$\overline{\text{SMI}}$ pin is active

The CY82C599 has two status registers (16 bits total) that can be read through register 58. Writing a 0 into bit 7 will cause A status set to be read on a read cycle. Writing a 1 into bit 7 will cause B status set to be read on a read cycle.

Register 58 contains the source of an $\overline{\text{SMI}}$ and some internal status. The status can be used to power-down/power-up individual system devices (monitor, CPU, hard disk, etc.).

Register 59: Power-Down Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Reserved.	0	0
6	Bits Timer 4 event control 0: Norml 1: Timer 4 will ignore all events (once enabled, timer 4 will start counting until it reaches the specified terminal count).	0	User selectable
5	Bits SMI retry timer 0: Disable SMI retry timer 1: Enable SMI retry timer	0	User selectable
4:3	Bits SMI retry timer terminal count 00: 55 msec. 01: 0.2 msec 10: 1 sec. 11: 3.5 sec Once the SMI retry timer is enabled and any system manage ment interrupt ($\overline{\text{SMI}}$) is active longer than the value specified by $\overline{\text{SMI}}$ retry timer, the 82C599 will generate a new $\overline{\text{SMI}}$.	0	User selectable
2	Bits $\overline{\text{STOPCLK}}$ timer control 0: Disable $\overline{\text{STOPCLK}}$ timer 1: Enable $\overline{\text{STOPCLK}}$ timer	0	User selectable
1:0	Bits $\overline{\text{STOPCLK}}$ timer 00: 430 usec. 01: 860 usec. 10: 1.7 msec. 11: 7 msec. In software power-down mode, the assertion of $\overline{\text{STOPCLK}}$ can be delayed. The delay time is determined by $\overline{\text{STOPCLK}}$ timer.	0	User selectable

Register 5A: Timer 3 Event Detection Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0	User selectable
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0	User selectable
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0	User selectable
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0	User selectable
3	DMA/ISA master / AT refresh detection 0: Disable DMA/ISA master / AT refresh detection 1: Enable DMA/ISA master / AT refresh detection.	0	User selectable
2	Bits 0: Disable non-motherboard memory detection 1: Enable non-motherboard memory detection	0	User selectable
1	Bits 0: Disable access floppy detection 1: Enable access floppy detection.	0	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0	User selectable

Index 5B: Timer 3 Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0	User selectable
3	Bits 0: Disable timer 3 1: Enable timer 3	0	User selectable
2	Bits 0: Disable special memroy I/O event detection (please see register 54, 55, and 56) 1: Enable special memory I/O event detection	0	User selectable
1	Bits 0: Disable I/O event detection 1: Enable I/O event detection (see Register 2EH and 2FH)	0	User selectable
0	Bits 0: Disable PCI/VESA master event detection 1: Enable PCI/VESA master event detection	0	User selectable

Index 5C: Timer 4 Event Detection Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0	User selectable
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0	User selectable
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0	User selectable
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0	User selectable
3	Bits 0: Disable DMA/ISA master / AT refresh event detection 1: Enable DMA/ISA master / AT refresh event detection	0	User selectable
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0	User selectable
1	Floppy Access Detection 0: Disable Floppy Disk Detection 1: Enable Floppy Disk Detection	0	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0	User selectable

Index 5D: Timer 4 Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0	User selectable
3	Bits 0: Disable timer 4 1: Enable timer 4	0	User selectable
2	Bits 0: Disable special memroy I/O event detection (please see register 54, 55, and 56) 1: Enable special memory I/O event detection	0	User selectable
1	Bits 0: Disable I/O event detection (Please see register 2E, 2F) 1: Enable I/O event detection	0	User selectable
0	Bits 0: Disable PCI/VESA master event detection 1: Enable PCI/VESA master event detection	0	User selectable

Index 5E

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Reserved.	00000000	00000000

Index 5F: Timer 5 Control

Bit	Function	Hardware Default	Recommended BIOS power-on setting
7:0	Reserved.	00000000	00000000

CY82C599 Pin Descriptions

PCI Interface

Name	I/O	Pin Number	Description
AD[31:0]	I/O	120, 122-128, 131-138, 152-160, 3-9	PCI Address and Data bus. During the address phase, AD[31:0] contain a physical address. During data phase, it contains 32-bit data.
$\overline{\text{CBE}}$[3:0]	I/O	129, 139, 151, 2	Bus Command and Byte Enables are multiplexed
PAR	I/O	147	Parity is even parity across AD[31:0]
$\overline{\text{FRAME}}$	I/O	140	Cycle Frame is driven by the current master to indicate the beginning and duration of an access.
$\overline{\text{IRDY}}$	I/O	141	Initiator Ready indicates the master's ability to complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	I/O	142	Target Ready indicates the target agent's ability to complete the current data phase of the transaction.
$\overline{\text{STOP}}$	I/O	148	Stop indicates the current target is requesting the master to stop the current transaction.
$\overline{\text{REQ}}$[3:0]	I	11, 117, 118, 119	Request indicate to the arbiter that this agent desires of the bus.
$\overline{\text{GNT}}$[3:0]	O	10, 114, 115, 116	Grant indicate to the agent that access to the bus has been granted.
$\overline{\text{RST}}$	I	113	Reset
PCICLK	I	12	Clock to every PCI device
$\overline{\text{PCILOCK}}$	I/O	149	Lock indicates an atomic operation that may require multiple transactions to complete.
$\overline{\text{DEVSEL}}$	I/O	143	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current address. As an input, it indicates whether any device on the bus has been selected.
$\overline{\text{SERR}}$	I	145	System Error
$\overline{\text{PERR}}$	I	144	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle.

CPU Interface

Name	I/O	Pin Number	Description
A31	I/O	13	Address bit 31
A[27:2]	I/O	15, 19, 21-25, 27-36, 38-40, 42-43, 45-47, 44	Address bit 27 to 2
$\overline{\text{SLOWCLK}}$/A28 /$\overline{\text{QPD}}$	I/O	18	Slow down clock signal. As and output, it can be used to control clock generator to slow down 486 CPU clock if power saving feature is supported. As an input, performed the quick power-down function. Or Address pin 28.
$\overline{\text{INTEO}}$/A29	I/O	17	Edge-triggered Interrupt Output or Address pin 29.
$\overline{\text{INTLI}}$/A30	I/O	16	Level-sensitive Interrupt input from PCI bus, or Address pin 30.
$\overline{\text{BE}}$[3:0]	I/O	80, 82, 83, 84	CPU Byte Enable
D[31:0]	I/O	72-79, 85-91, 93-99, 101, 103-111	Data bit 31 to 0.
CPUCLK	I	59	Clock for CPU
$\overline{\text{ADS}}$	I/O	71	CPU Address Strobe
$\overline{\text{MIO}}$	I/O	48	CPU Memory/IO cycle status
$\overline{\text{WR}}$	I/O	49	CPU Read/Write status
$\overline{\text{DC}}$	I/O	53	CPU Data/Code status
$\overline{\text{CPURDY}}$	I/O	52	Ready output to terminate CPU master cycle. Ready input to terminate PCI master cycle.
$\overline{\text{BLAST}}$	I/O	55	Burst Last signal indicates the completion of the burst cycle when the next $\overline{\text{BRDY}}$ is returned.
$\overline{\text{BRDY}}$	I/O	54	Burst Ready, when actively driven, indicates the end of burst transfer to CPU. As an input, it terminates PCI master cycle.
$\overline{\text{EADS}}$	O	56	External Address Strobe output to CPU
$\overline{\text{BOFF}}$/LED	O	60	Back Off output to back off CPU cycle, or Jumper. Resistor to ground places device in Stand-Alone mode, pull-up resistor places in normal mode.
$\overline{\text{LIMCS}}$/INTR/ $\overline{\text{LDEVI}}$	I/O	66	Multifunctional pin. As input, connect INTR signal from 82C206 or other VESA $\overline{\text{LDEV}}$ in stand-alone mode. As output, it drives $\overline{\text{LIMCS}}$ signal. $\overline{\text{LDEV}}$ input from other VESA devices in stand-alone mode.
NMI	O	26	Non-maskable interrupt output
$\overline{\text{STPCLK}}$	O	62	Stop Clock signal. Connect to 486 CPU to turn off the CLK input.

Miscellaneous

Name	I/O	Pin Number	Description
OSC/$\overline{\text{HITM}}$	I/O	58	Multifunctional pin. As OSC, connect to 14.31818MHz clock for the internal timer. As $\overline{\text{HITM}}$, connect to the $\overline{\text{HITM}}$ pin of 486.
OSC119/$\overline{\text{SMI}}$	I/O	57	Multifunctional pin. As output, it drives 1.19MHz clock output. As $\overline{\text{SMI}}$, connect to System Management Interupt pin of the 486.
$\overline{\text{SMIMASK}}$/ STATUS	O	63	Connect to $\overline{\text{IOCHCK}}$ signal of CY82C597. Jumper selects Synchronous or Asynchronous mode. Resistor to ground places device in Synchronous mode, pull-up resistor places in Asynchronous mode.
$\overline{\text{LDEV}}$	O	51	Local Device signal output
$\overline{\text{LRDY}}$/$\overline{\text{LBS16}}$	I	61	Connect to LRDY signal from VESA local bus or LBS16 signal from the VESA bus.

Arbitration

Name	I/O	Pin Number	Description
CPUHLDA	I	67	Input from CPU HLDA signal
CPUHOLD	O	68	Output to CPU HOLD signal
C597HOLD	I	69	Input from 82C597 HOLD signal
C597HLDA	O	65	Output to 82C597 HLDA signal

Ground and V_{CC}

Name	I/O	Pin Number	Description
V_{CC}	I	20, 41, 64, 100, 121, and 146	+5V power supply
GND	I	1, 14, 37, 50, 70, 81, 92, 102, 112, 130, and 150	Ground

CY82C599 DC Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... +7 V

Ambient Operating Temperature ..... −25°C to +70°C

Ambient Storage Temperature ..... −40°C to 125°C

DC Voltage Applied to Outputs ..... −0.5V to +5.5V

DC Input Voltage ..... −0.5V to +5.5V

Electrical Characteristics Over the Operating Range (0°C to 70°C, V_{CC} = +5V ± 5%)

Parameter	Description		CY82C599 Min.	CY82C599 Max.	Unit
V_{IL}	Input LOW Voltage		−.05	0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}+0.5	V
V_{OL}	Output LOW Voltage			0.4	V
V_{OH}	Output HIGH Voltage		2.4		V
I_{IL}	Input Leakage Current			10	µA
I_{OL}	Output Leakage			10	µA
C_{IN}	Input Capacitance			10	pF
C_{OUT}	Output Capacitance			10	pF
I_{CC}	Power Supply Current	33 MHz		100	mA

Switching Characteristics

Parameter	Description	CY82C599 Min.	CY82C599 Max.	Unit
CPU CLOCK TIMING				
T_{100}	CPUCLK Period	20		ns
T_{101}	CPUCLK HIGH time at 2.0V	7		ns
T_{102}	CPUCLK LOW time at 0.8V	7		ns
T_{103}	CPUCLK rise time		2	ns
T_{104}	CPUCLK fall time		2	ns
PCI CLOCK TIMING				
T_{200}	PCICLK Period	25		ns
T_{201}	PCICLK HIGH time at 2.0V	10		ns
T_{202}	PCICLK LOW time at 0.8V	10		ns
T_{203}	PCICLK rise time		4	ns
T_{204}	PCICLK fall time		4	ns
CPU BUS INTERFACE TIMING				
T_{300}	CPUCLK Rise to data out VALID A[31:2], $\overline{\text{INTEQ}}$, $\overline{\text{INTLI}}$, $\overline{\text{BE}}$[3:0], D[31:0], $\overline{\text{ADS}}$, M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, $\overline{\text{CPURDY}}$, $\overline{\text{BLAST}}$, $\overline{\text{BRDY}}$, $\overline{\text{EADS}}$, $\overline{\text{BOFF}}$, $\overline{\text{L1MCS}}$, $\overline{\text{NMI}}$, $\overline{\text{STOPCLK}}$, $\overline{\text{SLOWCLK}}$ and control signals to the CY82C596/7.		15	ns
T_{301}	CPUCLK Rise to data out HOLD A[31:2], $\overline{\text{INTEQ}}$, $\overline{\text{INTLI}}$, $\overline{\text{BE}}$[3:0], D[31:0], $\overline{\text{ADS}}$, M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, $\overline{\text{CPURDY}}$, $\overline{\text{BLAST}}$, $\overline{\text{BRDY}}$, $\overline{\text{EADS}}$, $\overline{\text{BOFF}}$, $\overline{\text{L1MCS}}$, $\overline{\text{NMI}}$, $\overline{\text{STOPCLK}}$, $\overline{\text{SLOWCLK}}$ and control signals to the CY82C596/7.	2		ns
T_{302}	Input SET-UP to CPUCLK Rise A[31:2], $\overline{\text{INTEQ}}$, $\overline{\text{INTLI}}$, $\overline{\text{BE}}$[3:0], D[31:0], $\overline{\text{ADS}}$, M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, $\overline{\text{CPURDY}}$, $\overline{\text{BLAST}}$, $\overline{\text{BRDY}}$, $\overline{\text{EADS}}$, $\overline{\text{BOFF}}$, $\overline{\text{L1MCS}}$, $\overline{\text{NMI}}$, $\overline{\text{STOPCLK}}$ and control signals to the CY82C596/7.	5		ns
T_{303}	Input HOLD to CPUCLK Rise A[31:2], $\overline{\text{INTEQ}}$, $\overline{\text{INTLI}}$, $\overline{\text{BE}}$[3:0], D[31:0], $\overline{\text{ADS}}$, M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, $\overline{\text{CPURDY}}$, $\overline{\text{BLAST}}$, $\overline{\text{BRDY}}$, $\overline{\text{EADS}}$, $\overline{\text{BOFF}}$, $\overline{\text{L1MCS}}$, $\overline{\text{NMI}}$, $\overline{\text{STOPCLK}}$ and control signals to the CY82C596/7.	2		ns
PCI BUS INTERFACE TIMING				
T_{400}	PCICLK Rise to data out VALID AD[31:0], $\overline{\text{C}}$/$\overline{\text{BE}}$[3:0], PAR, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{GNT}}$, $\overline{\text{PCILOCK}}$, $\overline{\text{DEVSEL}}$.		18	ns
T_{401}	PCICLK Rise to data out HOLD AD[31:0], $\overline{\text{C}}$/$\overline{\text{BE}}$[3:0], PAR, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{GNT}}$, $\overline{\text{PCILOCK}}$, $\overline{\text{DEVSEL}}$.	2		ns
T_{402}	Input SET-UP to PCICLK Rise AD[31:0], $\overline{\text{C}}$/$\overline{\text{BE}}$[3:0], PAR, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{GNT}}$, $\overline{\text{PCILOCK}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{REQ}}$[3:0], $\overline{\text{RST}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$.	5		ns
T_{403}	Input HOLD to PCICLK Rise AD[31:0], $\overline{\text{C}}$/$\overline{\text{BE}}$[3:0], PAR, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{TRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{GNT}}$, $\overline{\text{PCILOCK}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{REQ}}$[3:0], $\overline{\text{RST}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$.	0		ns

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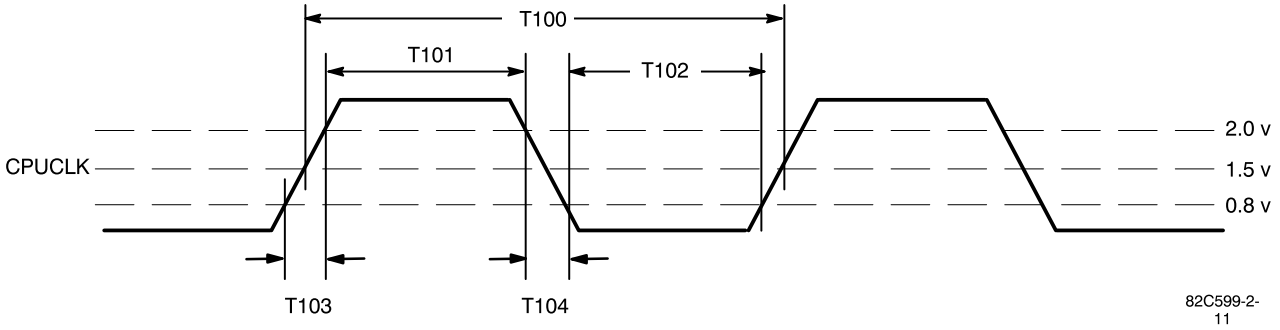
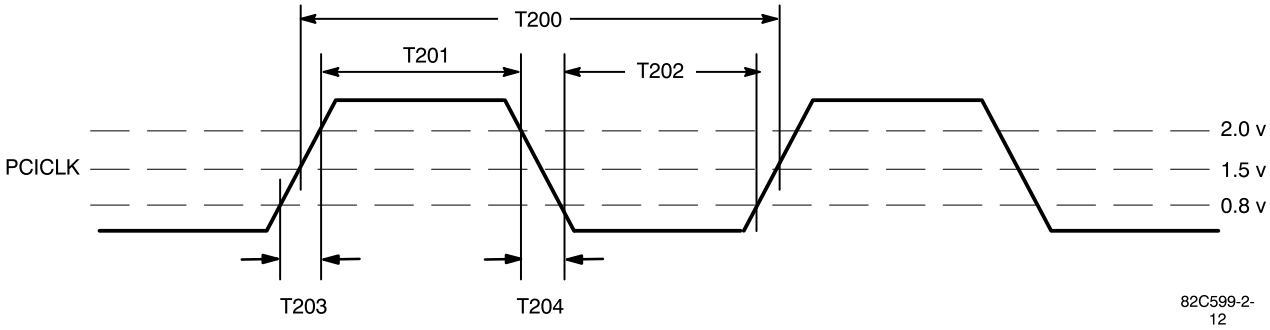
Switching Waveforms

CPUCLK Timing

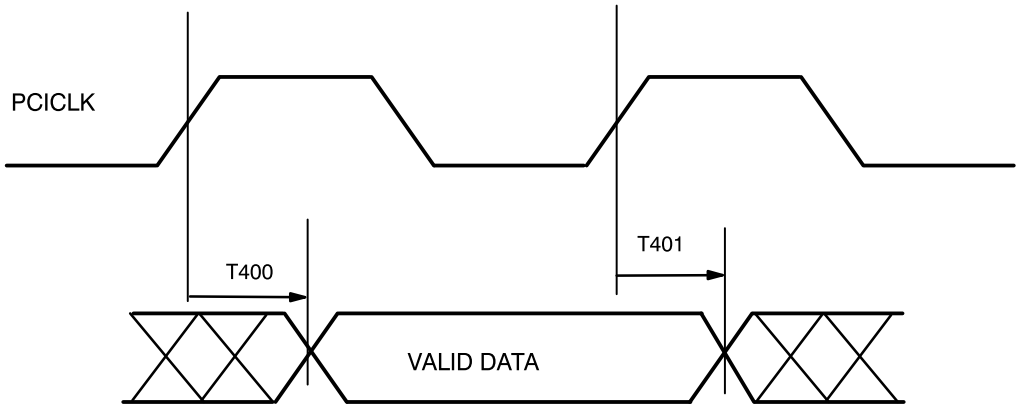


PCICLK Timing



Switching Waveforms (continued)

PCI BUS INTERFACE TIMING



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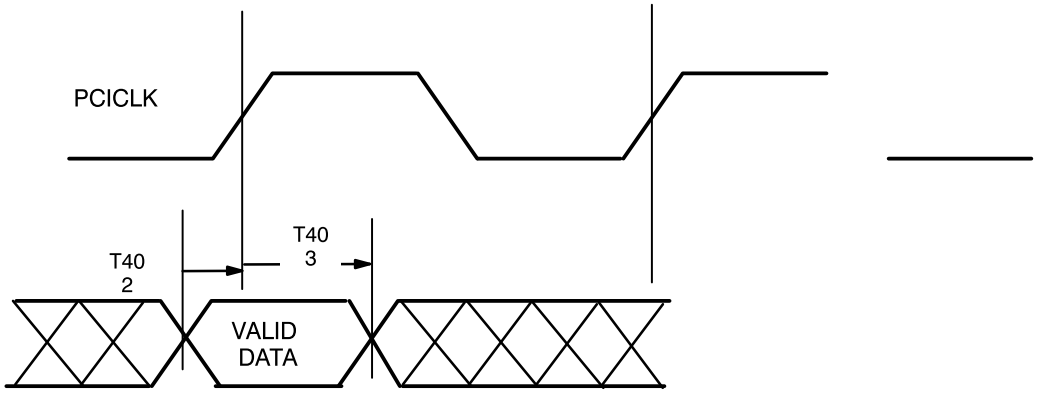
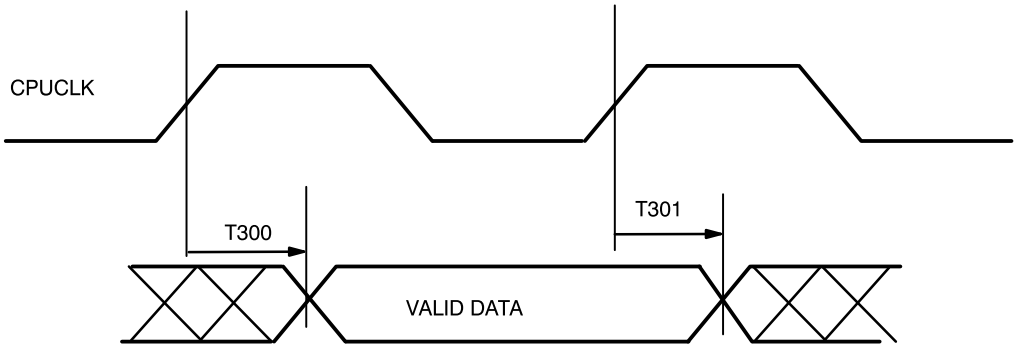


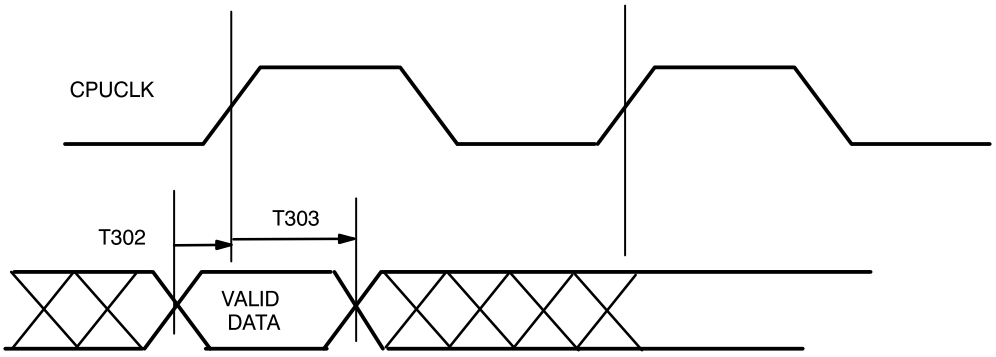
82C599-2-13

Switching Waveforms (continued)

CPU BUS INTERFACE TIMING



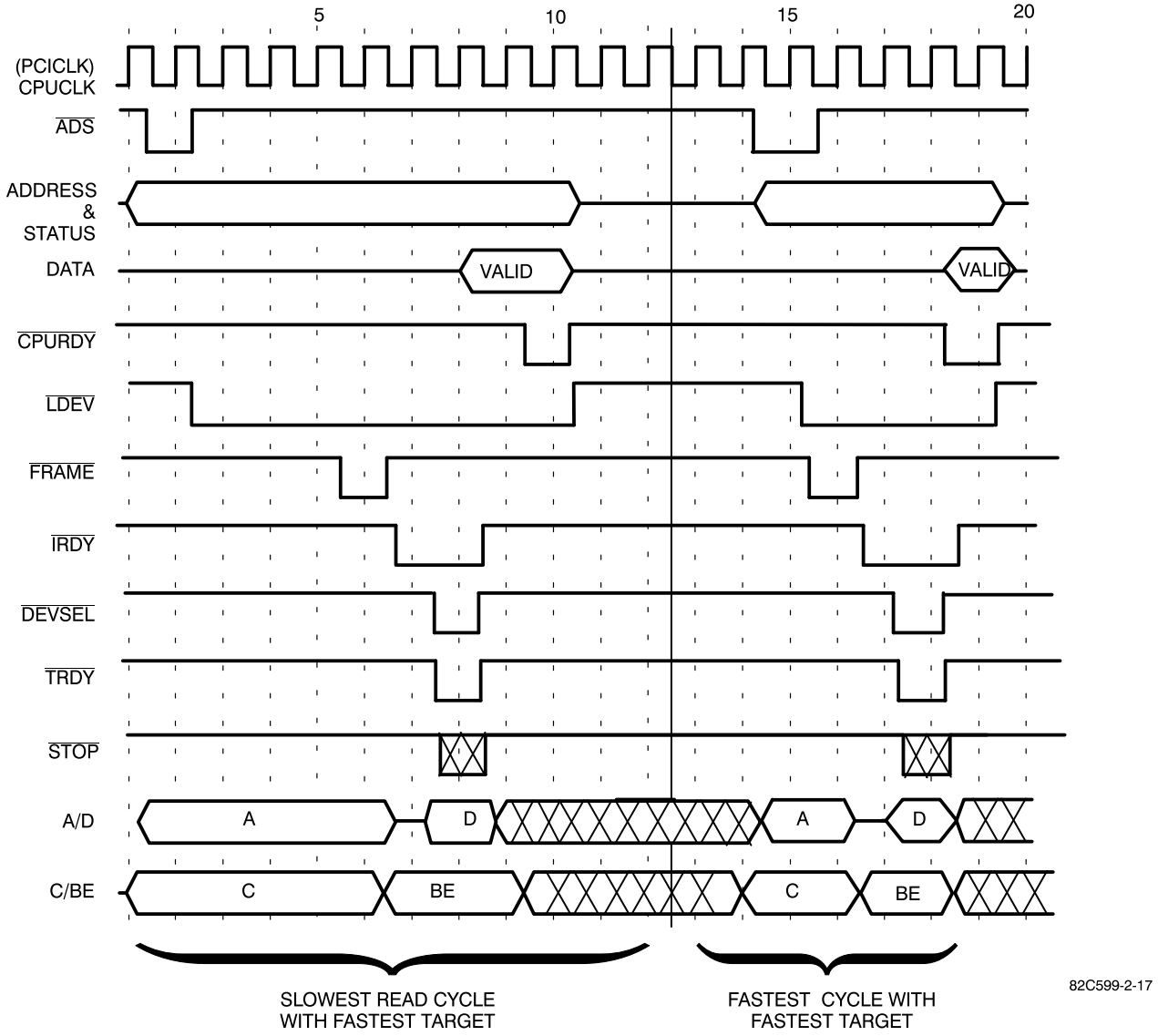
82C599-2-16



82C599-2-15

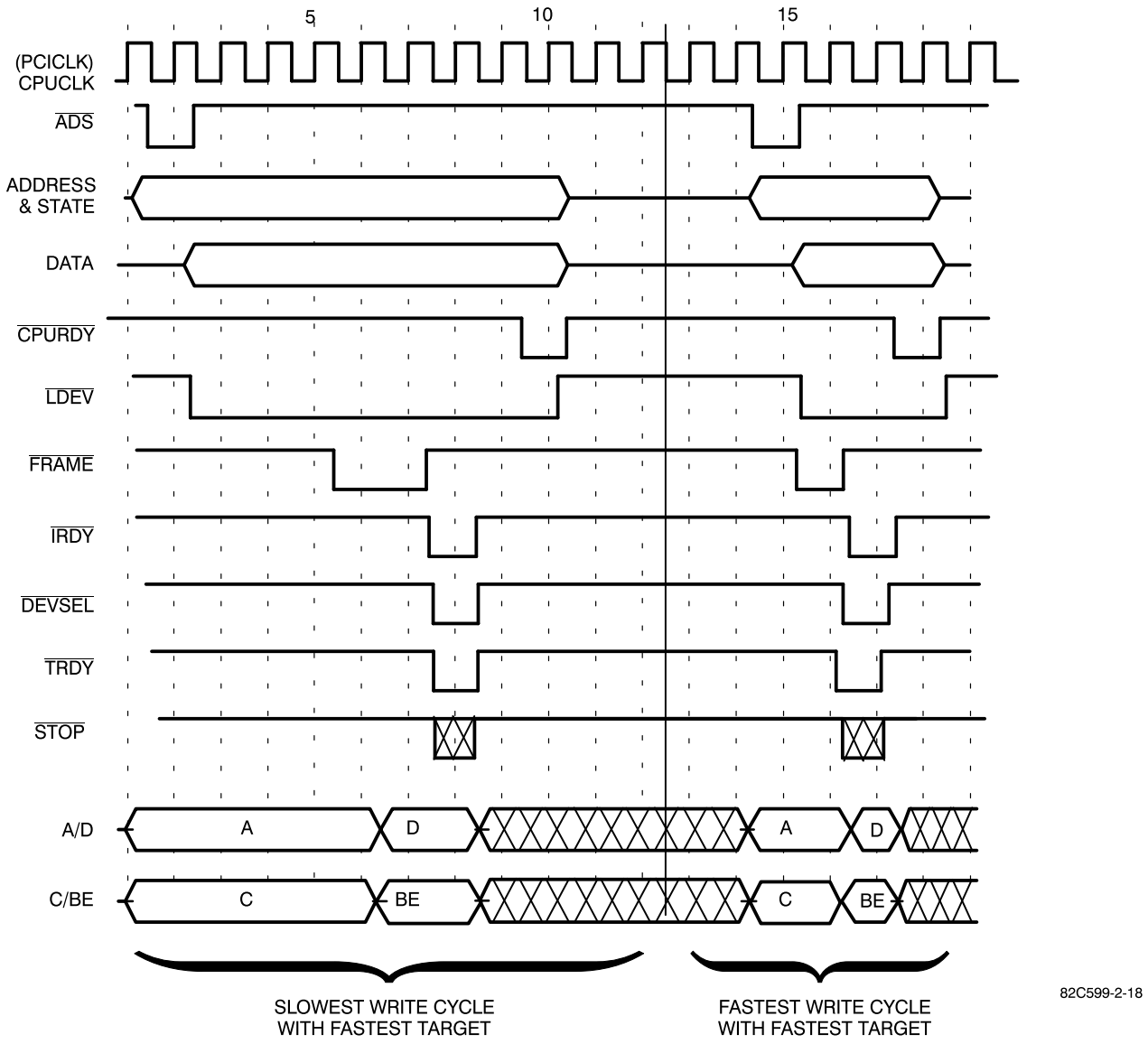
Switching Waveforms (continued)

CPU Master Read PCI Target



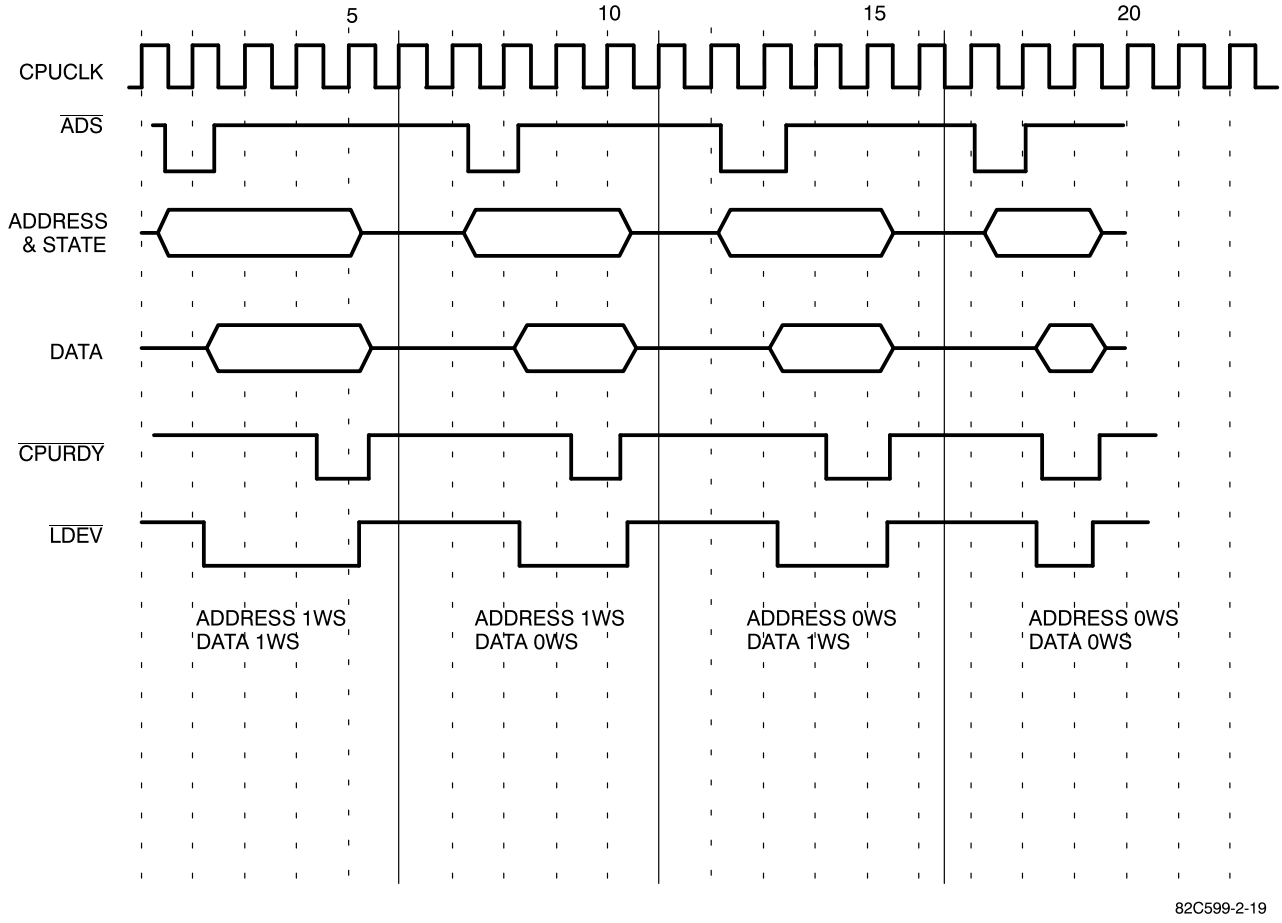
Switching Waveforms (continued)

CPU Master Write PCI Target



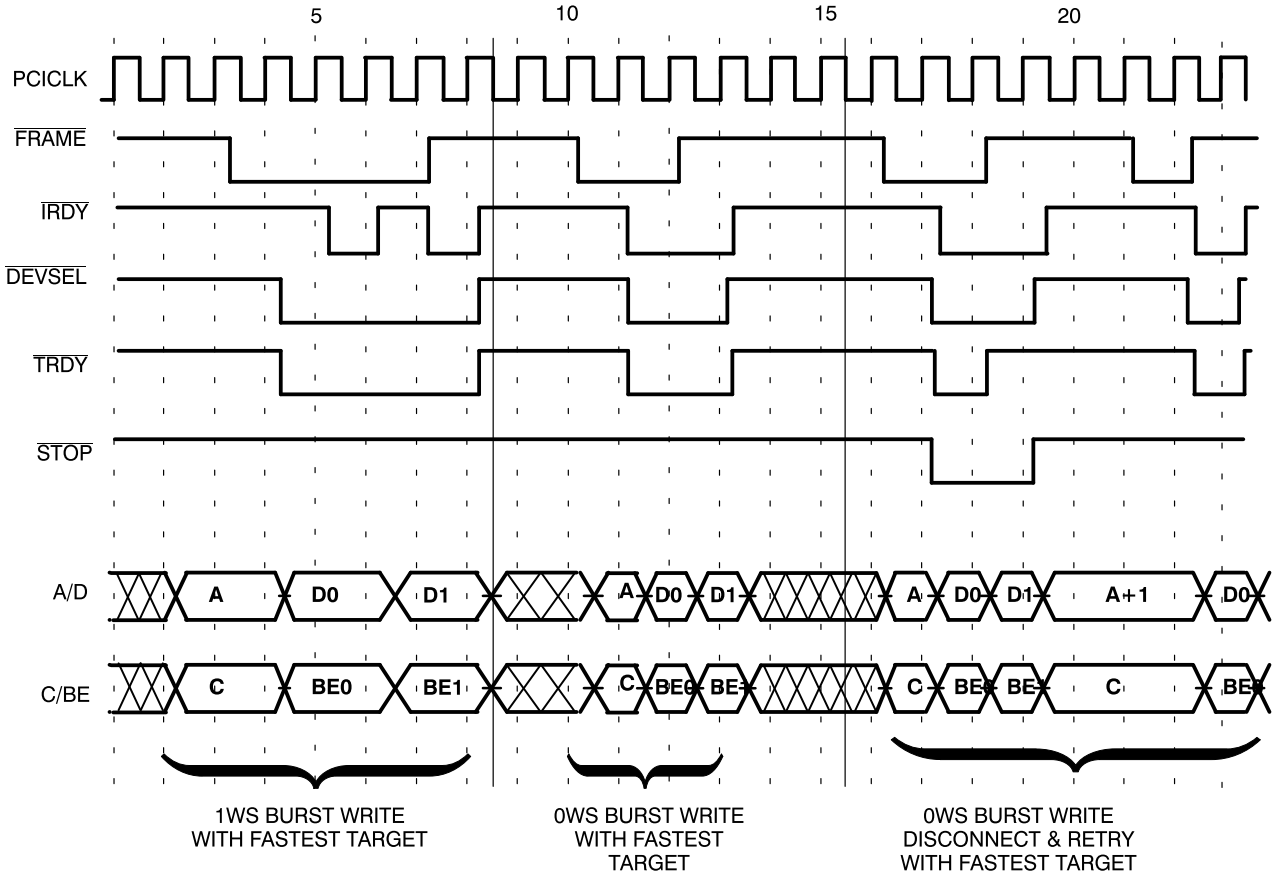
Switching Waveforms (continued)

CPU Master Post Write to PCI Target, CPU side, Buffer available.



Switching Waveforms (continued)

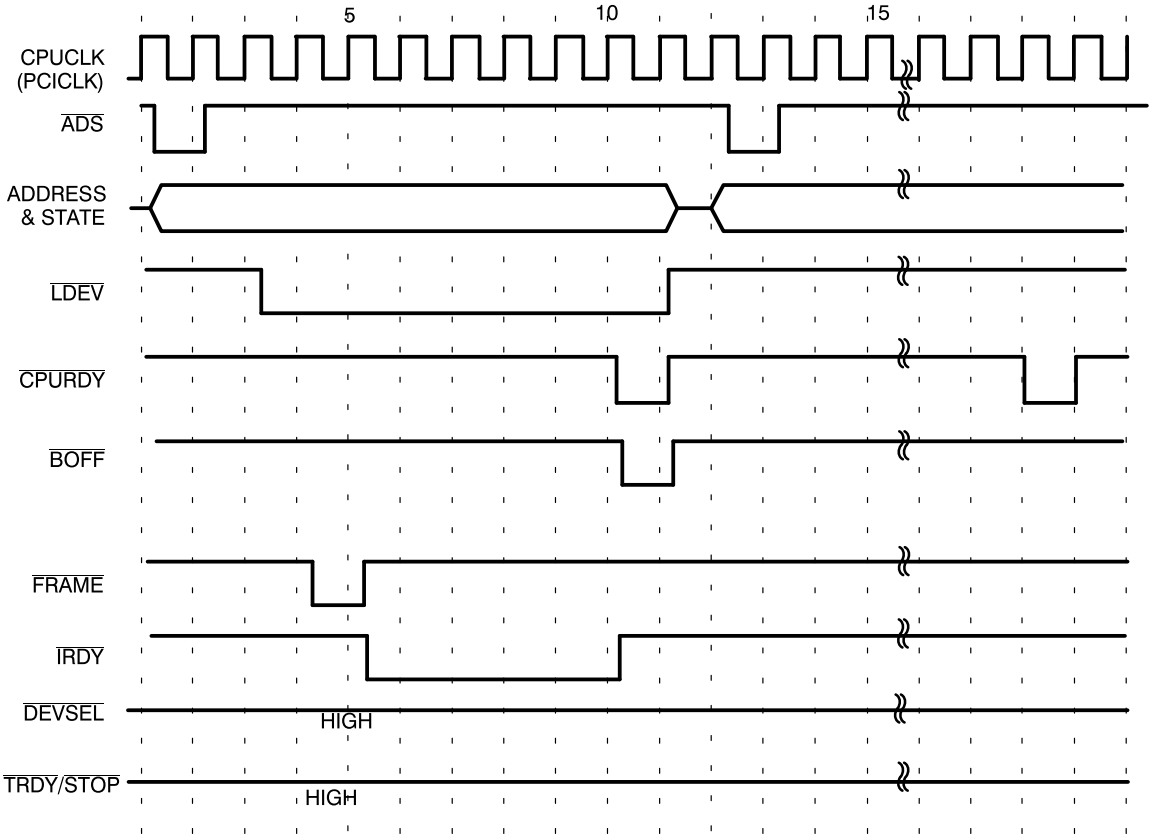
CPU Master Burst Post Write, to PCI Target (PCI side) Data Available in Buffer.



82C599-2-20

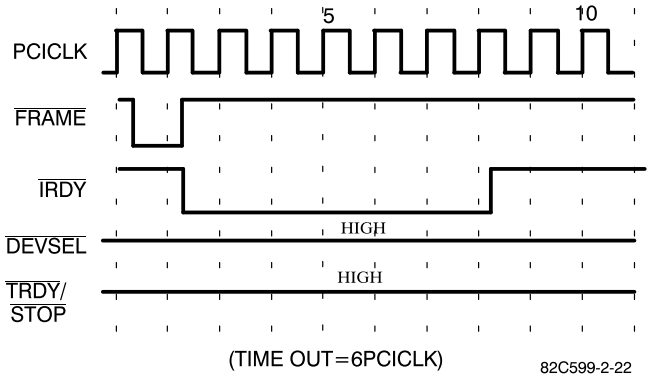
Switching Waveforms (continued)

CPU Master Read/Write to PCI Bus "Miss" Cycle, Stand-Alone Mode (to CPU without claiming the same cycle)



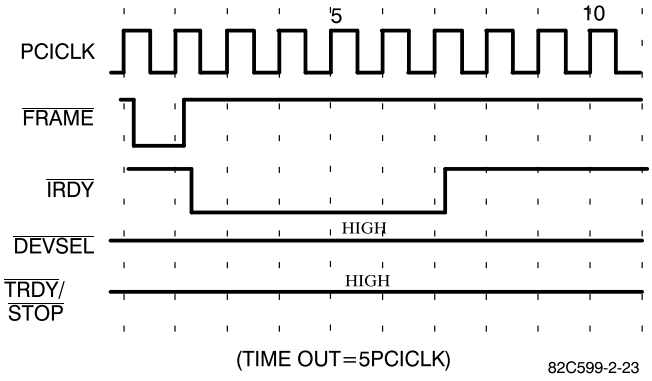
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



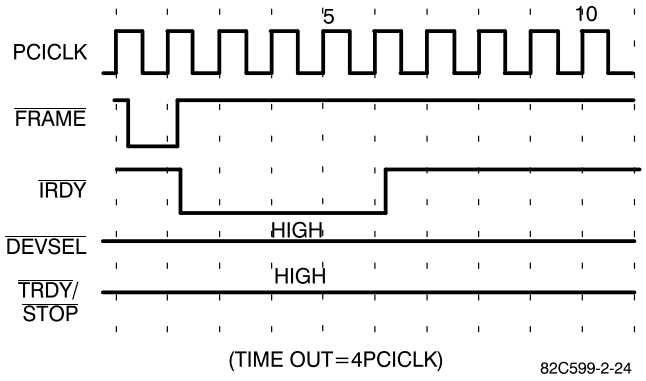
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



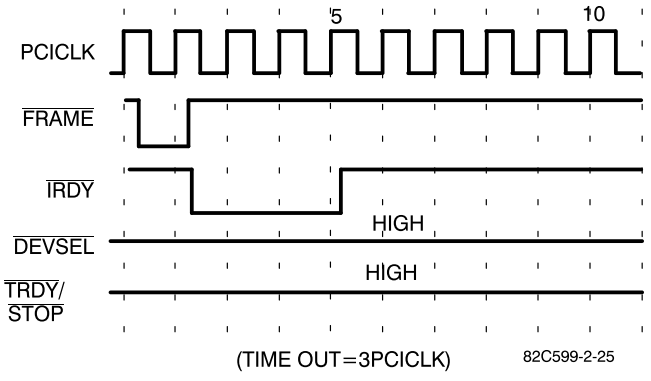
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



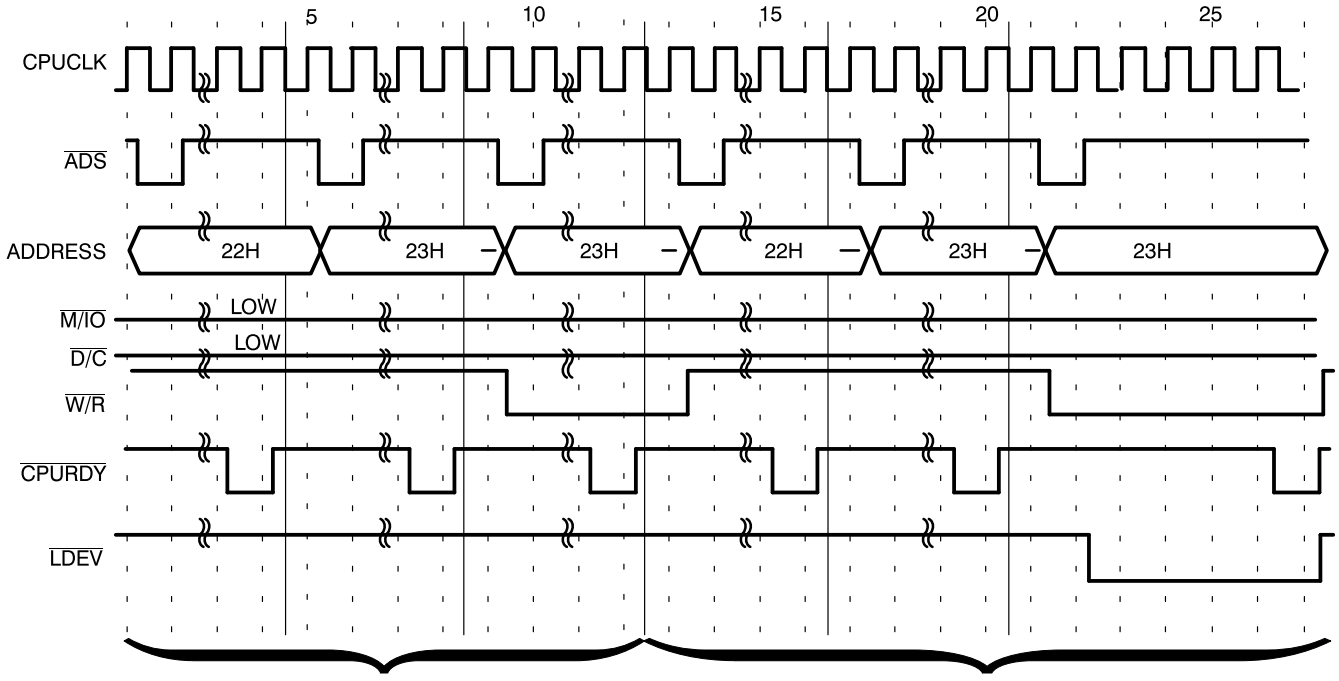
Switching Waveforms (continued)

CPU Master to PCI Bus "Master Abort" (DEVSEL) Time-Out Timing



Switching Waveforms (continued)

CPU Master I/O Read/Write to 22/23H location, Stand-Alone mode



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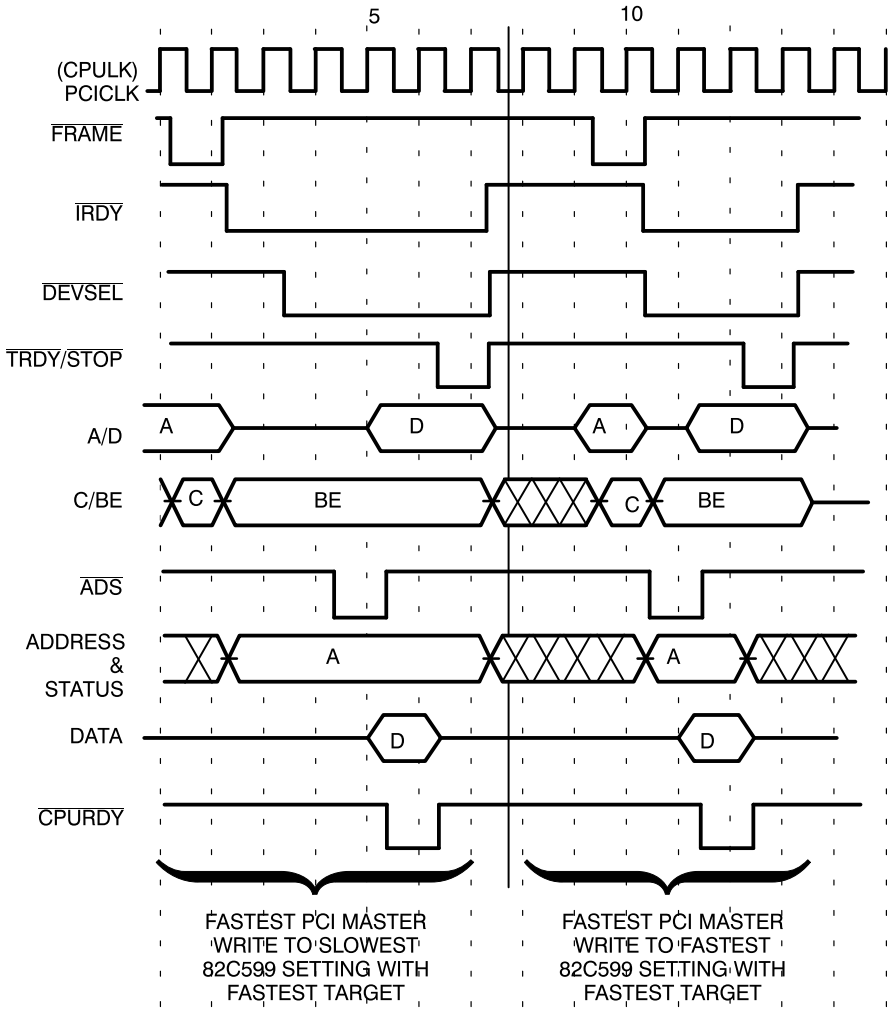
Switching Waveforms (continued)

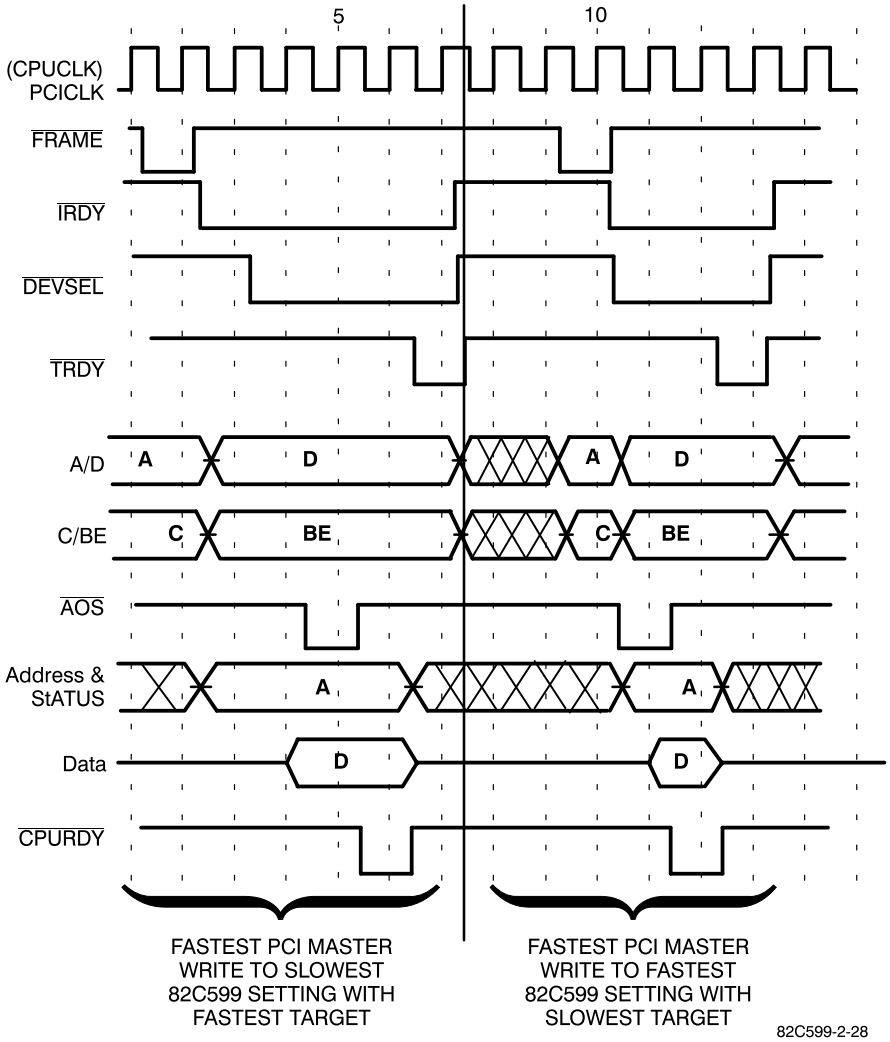
PCI Master Read From 82C599 Target



82C599-2-27

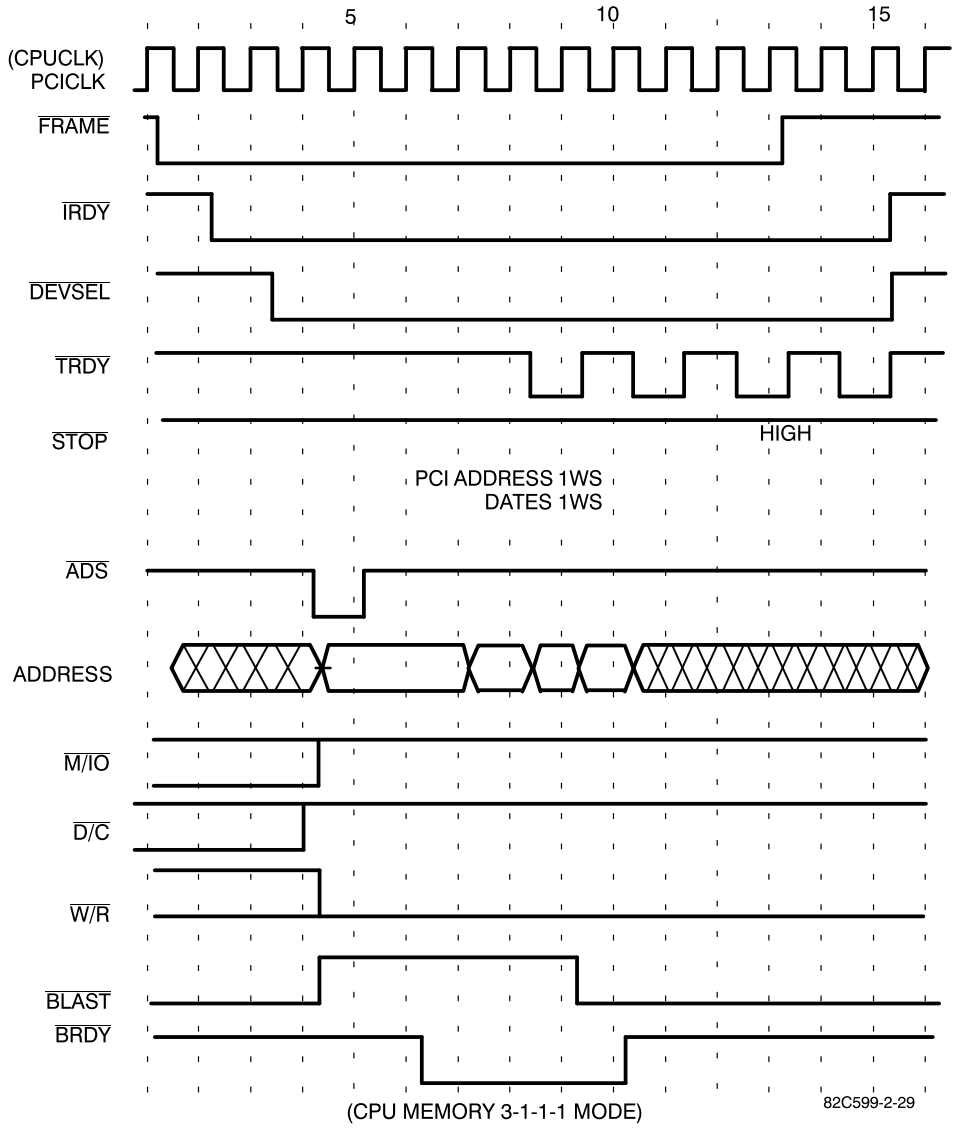
Switching Waveforms (continued)

PCI Master Write to 82C599 Target



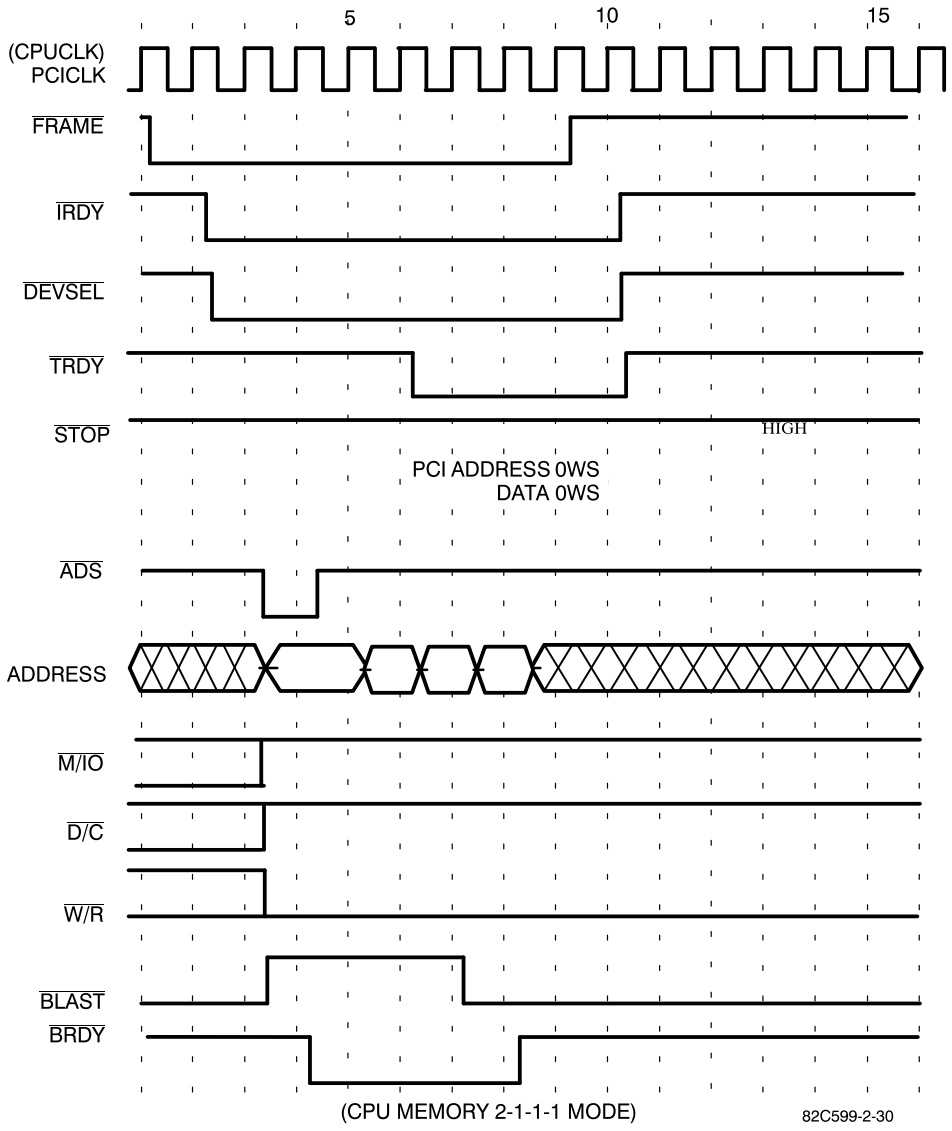
Switching Waveforms (continued)

PCI Master Burst Pre-Read to CPU



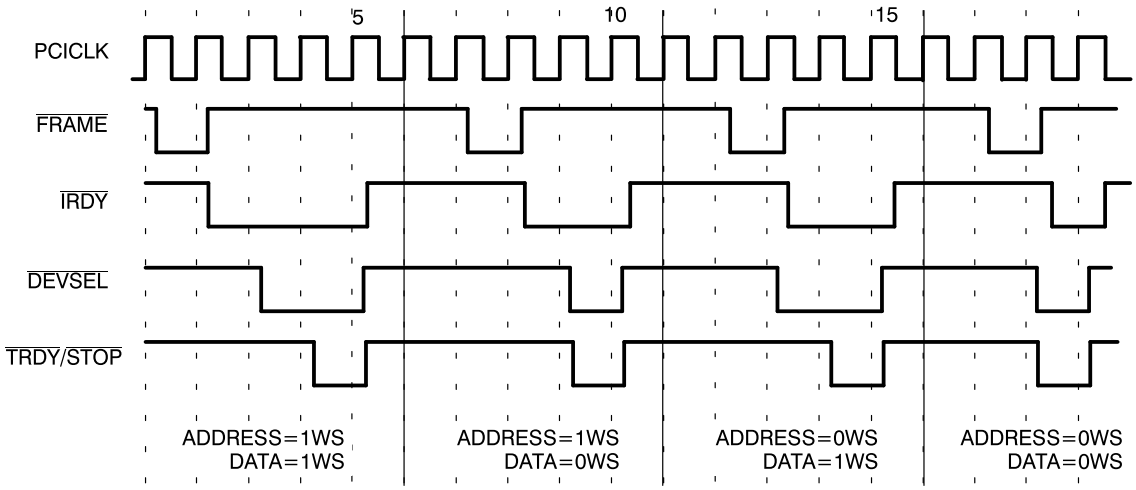
Switching Waveforms (continued)

PCI Master Burst Pre-Read to CPU



Switching Waveforms (continued)

PCI Master Post Write to CPU, PCI Side Buffer Available

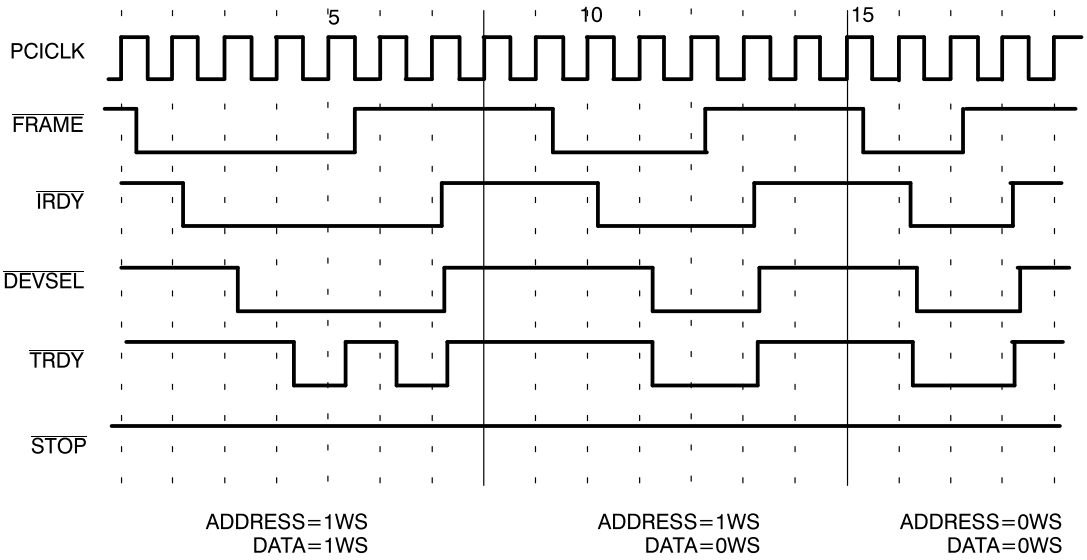


82C599-2-31

Note: CPU side same as 486 type CPU write cycle

Switching Waveforms (continued)

[**Master Burst Post Write to CPU, PCI Side Buffer Available**

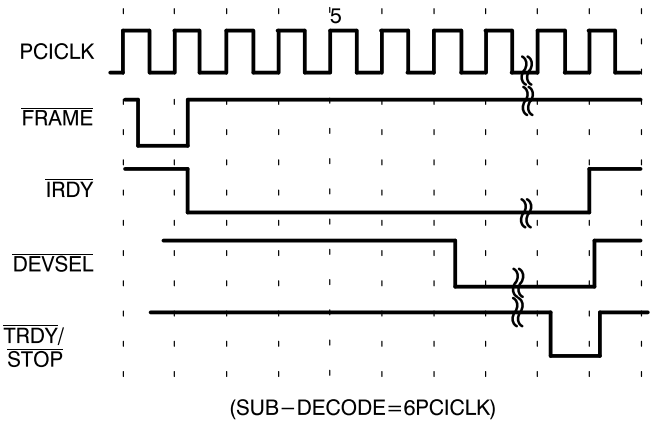


Note: CPU side same as 486 type CPU write cycle.

82C599-2-32

Switching Waveforms (continued)

PCI Master Subtractive Decode "$\overline{\text{DEVSEL}}$" Timing

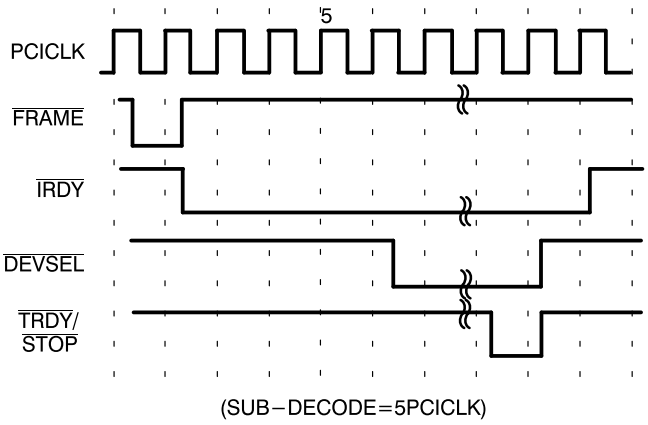


(SUB−DECODE=6PCICLK)

82C599-2-33

Switching Waveforms (continued)

PCI Master Subtractive Decode "$\overline{\text{DEVSEL}}$" Timing



(SUB−DECODE=5PCICLK)

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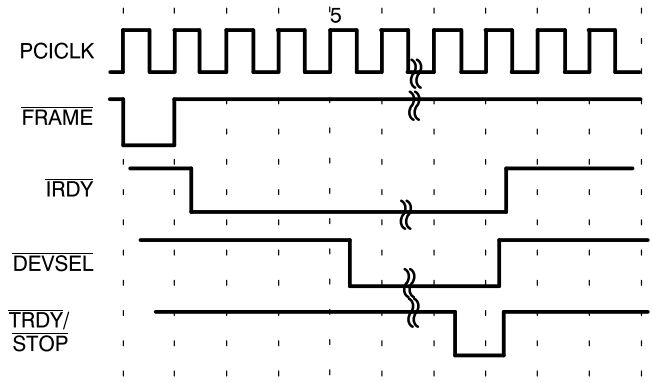
Switching Waveforms (continued)

PCI Master Subtractive Decode "$\overline{\text{DEVSEL}}$" Timing

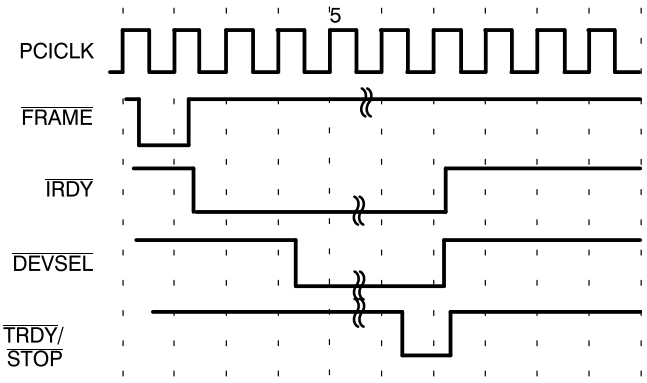


(SUB−DECODE=4PCICLK)

82C599-2-35

Switching Waveforms (continued)

PCI Master Subtractive Decode "$\overline{\text{DEVSEL}}$" Timing



(SUB−DECODE=3PCICLK)

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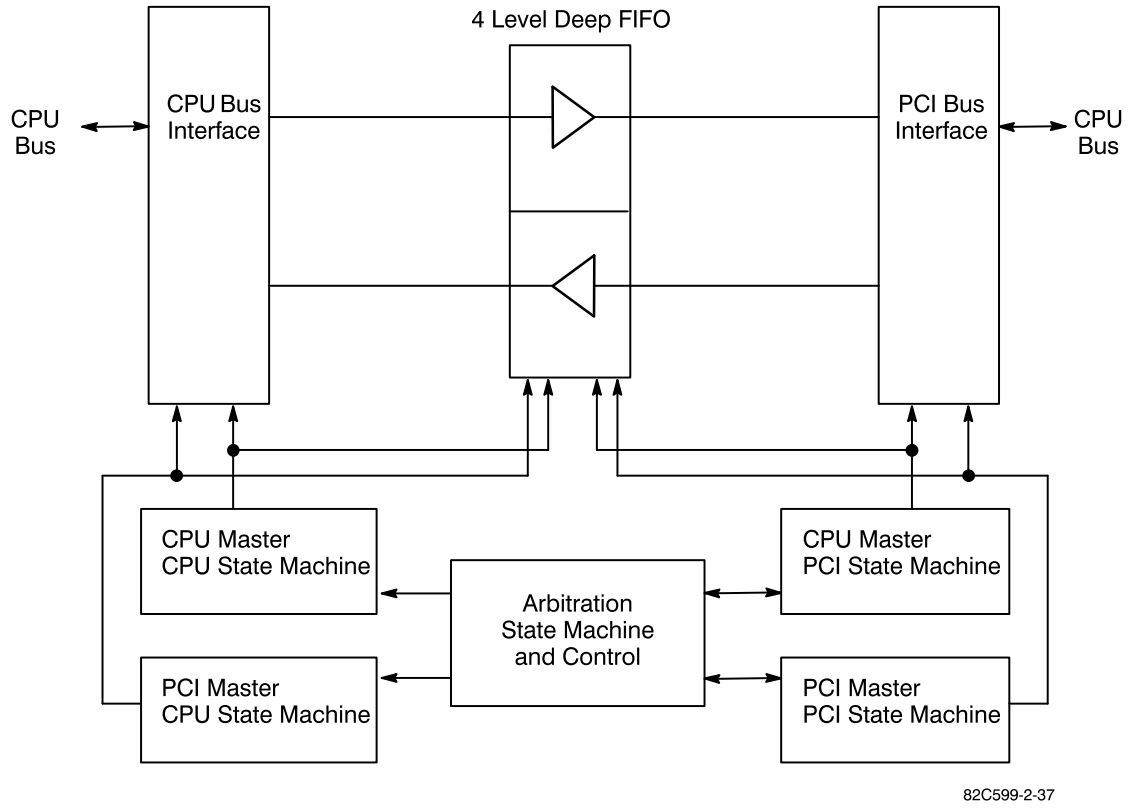
82C599 Block Diagram



Package Diagrams

160-Lead Plastic Quad Flatpack N160