CY8CLED04

EZ-Color™ HB LED Controller

Features

■ **HB LED Controller**
- ❏ Configurable Dimmers Support up to 4 Independent LED Channels
- ❏ 8-32 Bits of Resolution per Channel
- ❏ Dynamic Reconfiguration Enables LED Controller plus other Features; CapSense, Battery Charging, Motor Control…

■ **Visual Embedded Design, PSoC Express**
- ❏ LED Based Express Drivers
  - • Binning Compensation
  - • Temperature Feedback
  - • DMX512

■ **PrISM Modulation Technology**
- ❏ Reduces Radiated EMI
- ❏ Reduces Low Frequency Blinking

■ **Advanced Peripherals (PSoC Blocks)**
- ❏ 4 Digital PSoC Blocks Provide:
  - • 8 to 32-Bit Timers, Counters, and PWMs
  - • Up to 2 Full-Duplex UART
  - • Multiple SPI™ Masters or Slaves
  - • Connectable to all GPIO Pins
- ❏ 6 Rail-to-Rail Analog PSoC Blocks Provide:
  - • Up to 14-Bit ADCs
  - • Up to 9-Bit DACs
  - • Programmable Gain Amplifiers
  - • Programmable Filters and Comparators
- ❏ Complex Peripherals by Combining Blocks
- ❏ Capacitive Sensing Application Capability

■ **Complete Development Tools**
- ❏ Free Development Software
  - • PSoC Designer™
  - • PSoC Express™
- ❏ Full-Featured, In-Circuit Emulator and Programmer
- ❏ Full Speed Emulation
- ❏ Complex Breakpoint Structure
- ❏ 128 KBytes Trace Memory

■ **Programmable Pin Configurations**
- ❏ 25 mA Sink on all GPIO
- ❏ Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
- ❏ Up to 12 Analog Inputs on GPIO
- ❏ Four 30 mA Analog Outputs on GPIO
- ❏ Configurable Interrupt on all GPIO

■ **Flexible On-Chip Memory**
- ❏ 16K Flash Program Storage 50,000 Erase/Write Cycles
- ❏ 1K SRAM Data Storage
- ❏ In-System Serial Programming (ISSP)
- ❏ Partial Flash Updates
- ❏ Flexible Protection Modes
- ❏ EEPROM Emulation in Flash

■ **Full-Speed USB (12 Mbps)**
- ❏ Four Uni-Directional Endpoints
- ❏ One Bi-Directional Control Endpoint
- ❏ USB 2.0 Compliant
- ❏ Dedicated 256 Byte Buffer
- ❏ No External Crystal Required

Overview

Block Diagram
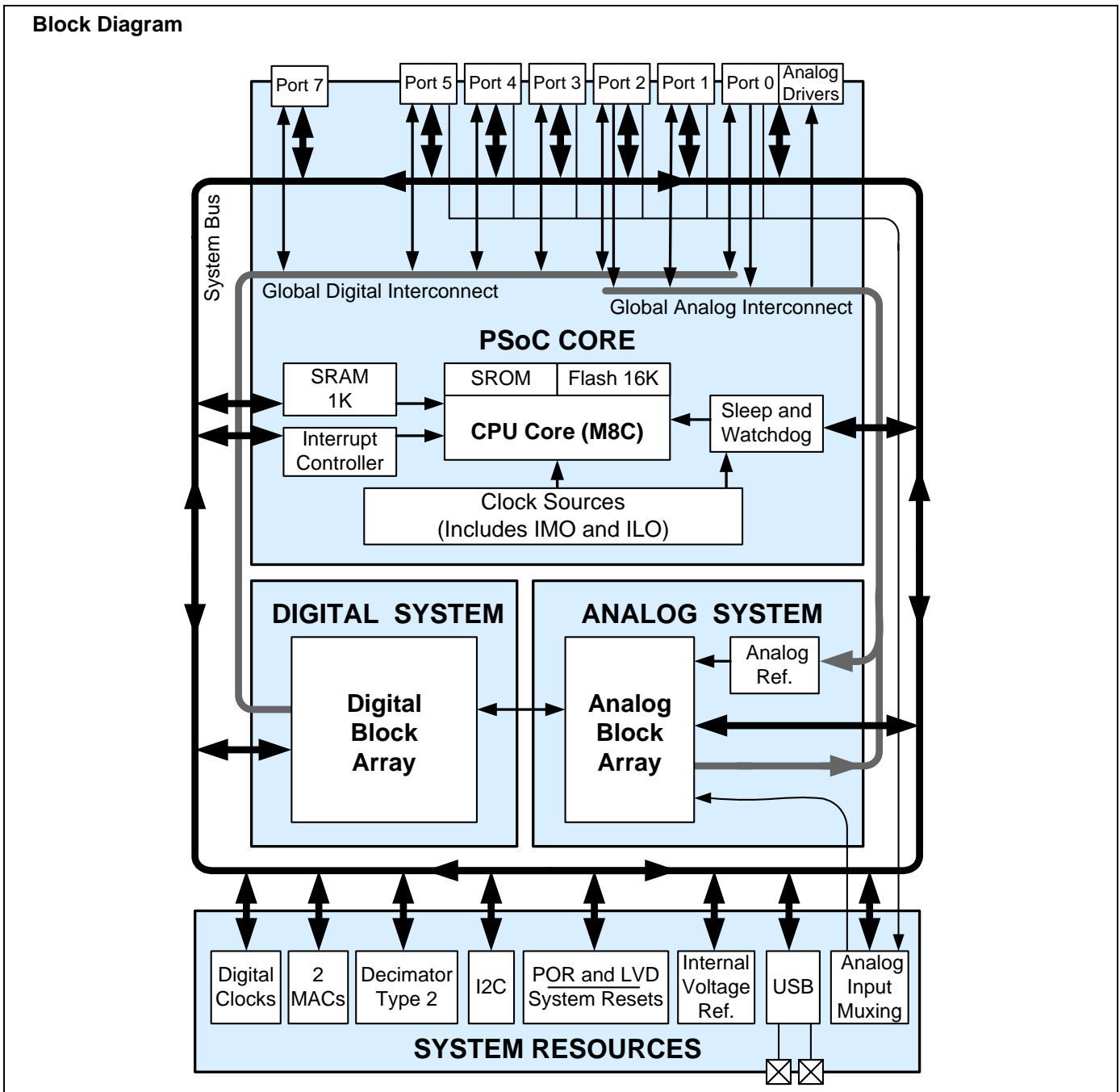
EZ-Color Functional Overview

Cypress' EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip™); with Cypress' PrISM (precise illumination signal modulation) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family support up to 16 independent LED channels with up to 32 bits of resolution per channel, enabling lighting designers the flexibility to choose the LED array size and color quality. PSoC Express software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature and LED binning compensation. EZ-Color's virtually limitless analog and digital customization allow for simple integration of features in addition to intelligent lighting, such as CapSense, Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress' best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

■ LCD Backlight

■ Large Signs

■ General Lighting

■ Architectural Lighting

■ Camera/Cell Phone Flash

■ Flashlights

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 68 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with up to 20 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The EZ-Color family incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 8% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the EZ-Color device. In USB systems, the IMO will self-tune to ± 0.25% accuracy for USB communication.

EZ-Color GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of 4 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include those listed below.

■ PrISM (8 to 32 bit)

■ Full-Speed USB (12 Mbps)

■ PWMs (8 to 32 bit)

■ PWMs with Dead band (8 to 24 bit)

■ Counters (8 to 32 bit)

■ Timers (8 to 32 bit)

■ UART 8 bit with selectable parity

■ SPI master and slave

■ I2C slave and multi-master

■ Cyclical Redundancy Checker/Generator (8 to 32 bit)

■ IrDA

■ Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by EZ-Color device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.
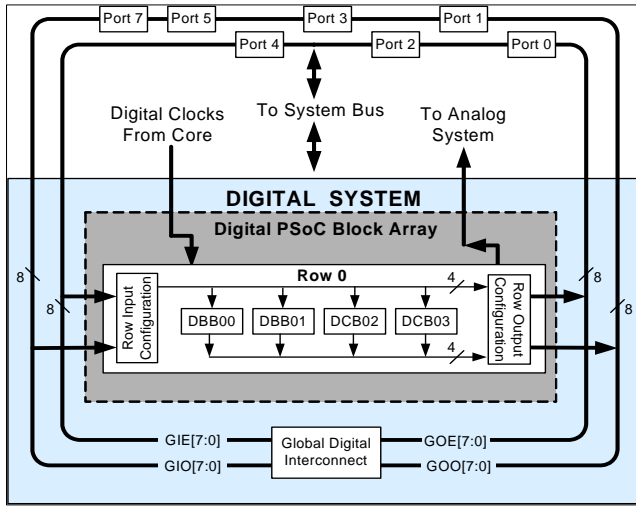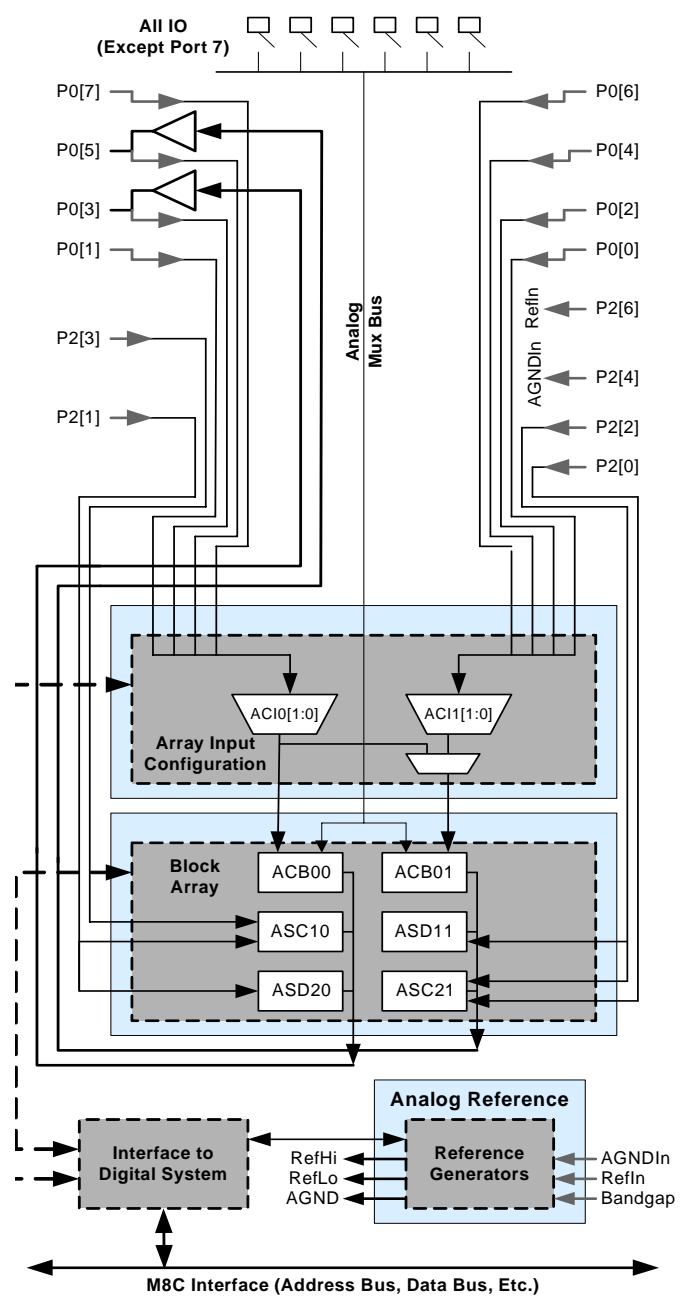
Figure 1. Digital System Block Diagram

Figure 2. Analog System Block Diagram

The Analog System

The Analog System is composed of 6 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 2, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)

- Filters (2 and 4 pole band-pass, low-pass, and notch)

- Amplifiers (up to 2, with selectable gain to 48x)

- Instrumentation amplifiers (1 with selectable gain to 93x)

- Comparators (up to 2, with 16 selectable thresholds)

- DACs (up to 2, with 6- to 9-bit resolution)

- Multiplying DACs (up to 2, with 6- to 9-bit resolution)

- High current output drivers (two with 30 mA drive as a PSoC Core Resource)

- 1.3V reference (as a System Resource)

- DTMF Dialer

- Modulators

- Correlators

- Peak Detectors

- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.

The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin in ports 0-5. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

■ Track pad, finger sensing.

■ Chip-wide mux that allows analog input from up to 48 IO pins.

■ Crosspoint connection between any IO pin combinations.

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements Application Notes, which can be found under http://www.cypress.com >> DESIGN RESOURCES >> Application Notes. In general, and unless otherwise noted in the relevant Application Notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

Additional System Resources

System Resources, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

■ Full-Speed USB (12 Mbps) with 5 configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Wider than commercial temperature USB operation (-10°C to +85°C).

■ Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.

■ Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math as well as digital filters.

■ Decimator provides a custom hardware filter for digital signal processing apps. including creation of Delta Sigma ADCs.

■ The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, multi-master are supported.

■ Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

■ An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.

■ Versatile analog multiplexer system.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table

Table 1. EZ-Color Device Characteristics

PSoC Part Number	LED Channels	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense
CY8CLED04	**4**	**56**	**1**	**4**	**48**	**2**	**2**	**6**	**1K**	**16K**	**Yes**
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	64	4	16	12	4	4	12	2K	32K	No

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this data sheet and using the PSoC Express Integrated Development Environment (IDE). This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest device data sheets on the web at http://www.cypress.com/ez-color.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click **EZ-Color** to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to http://www.cypress.com/techtrain.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

A long list of application notes will assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are listed by date as default.

Development Tools

PSoC Express is a high-level design tool for creating embedded systems using Cypress's PSoC mixed-signal technology. With PSoC Express you create a complete embedded solution including all necessary on-chip peripherals, block configuration, interrupt handling and application software without writing a single line of assembly or C code.

PSoC Express solves design problems the way you think about the system:

■ Select input and output devices based upon system requirements.

■ Add a communications interface and define its interface to system (using registers).

■ Define when and how an output device changes state based upon any and all other system devices.

Based upon the design, automatically select one or more PSoC Mixed-Signal Controllers that match system requirements.

Figure 3. PSoC Express
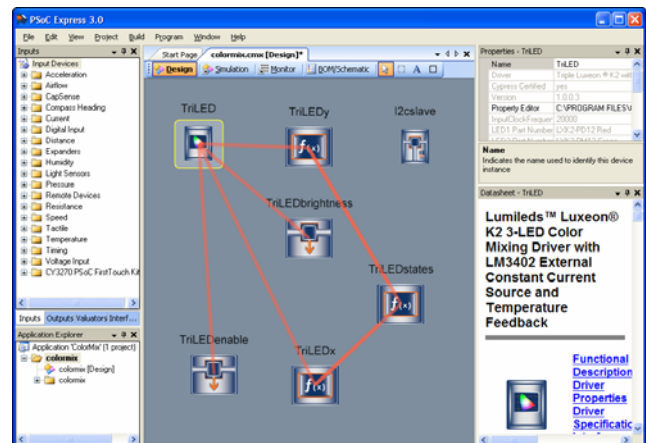
PSoC Express Subsystems

Express Editor

The Express Editor allows you to create designs visually by dragging and dropping inputs, outputs, communication interfaces, and other design elements, and then describing the logic that controls them.

Project Manager

The Project Manager allows you to work with your applications and projects in PSoC Express. A PSoC Express application is a top level container for projects and their associated files. Each project contains a design that uses a single PSoC device. An application can contain multiple projects so if you are creating an application that uses multiple PSoC devices you can keep all of the projects together in a single application.

Most of the files associated with a project are automatically generated by PSoC Express during the build process, but you can make changes directly to the custom.c and custom.h files

and also add your own custom code to the project in the Project Manager.

Application Editor

The Application Editor allows you to edit custom.c and custom.h as well as any C or assembly language source code that you add to your project. With PSoC Express you can create application software without writing a single line of assembly or C code, but you have a full featured application editor at your finger tips if you want it.

Build Manager

The Build Manager gives you the ability to build the application software, assign pins, and generate the data sheet, schematic, and BOM for your project.

Board Monitor

The Board Monitor is a debugging tool designed to be used while attached to a prototype board through a communication interface that allows you to monitor changes in the various design elements in real time.

The default communication for the board monitor is I^{2}C. It uses the CY3240-I2USB I^{2}C to USB Bridge Debugging/Communication Kit.

Tuners

A Tuner is a visual interface for the Board Monitor that allows you to view the performance of the HB LED drivers on your test board while your program is running, and manually override values and see the results.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Document Conventions

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 6 on page 12 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexidecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (e.g., '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms

| Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

Pin Information

68-Pin Part Pinout

This Section describes, lists, and illustrates the CY8CLED04 EZ-Color device pins and pinout configuration. The CY8CLED04 device is available in the following package. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, and XRES are not capable of Digital IO.

Table 3. 68-Pin Part Pinout (QFN**)

Pin No.	Type Digital	Type Analog	Name	Description
1	IO	M	P4[7]	
2	IO	M	P4[5]	
3	IO	M	P4[3]	
4	IO	M	P4[1]	
5			NC	No connection.
6			NC	No connection.
7	Power		Vss	Ground connection.
8	IO	M	P3[7]	
9	IO	M	P3[5]	
10	IO	M	P3[3]	
11	IO	M	P3[1]	
12	IO	M	P5[7]	
13	IO	M	P5[5]	
14	IO	M	P5[3]	
15	IO	M	P5[1]	
16	IO	M	P1[7]	I2C Serial Clock (SCL).
17	IO	M	P1[5]	I2C Serial Data (SDA).
18	IO	M	P1[3]	
19	IO	M	P1[1]	I2C Serial Clock (SCL) ISSP SCLK*.
20	Power		Vss	Ground connection.
21	USB		D+	
22	USB		D-	
23	Power		Vdd	Supply voltage.
24	IO		P7[7]	
25	IO		P7[6]	
26	IO		P7[5]	
27	IO		P7[4]	
28	IO		P7[3]	
29	IO		P7[2]	
30	IO		P7[1]	
31	IO		P7[0]	
32	IO	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA*.
33	IO	M	P1[2]	
34	IO	M	P1[4]	Optional External Clock Input (EXT-CLK).
35	IO	M	P1[6]	
36	IO	M	P5[0]	
37	IO	M	P5[2]	
38	IO	M	P5[4]	
39	IO	M	P5[6]	
40	IO	M	P3[0]	
41	IO	M	P3[2]	
42	IO	M	P3[4]	
43	IO	M	P3[6]	
44			NC	No connection.
45			NC	No connection.
46	Input		XRES	Active high pin reset with internal pull down.

68-Pin Device
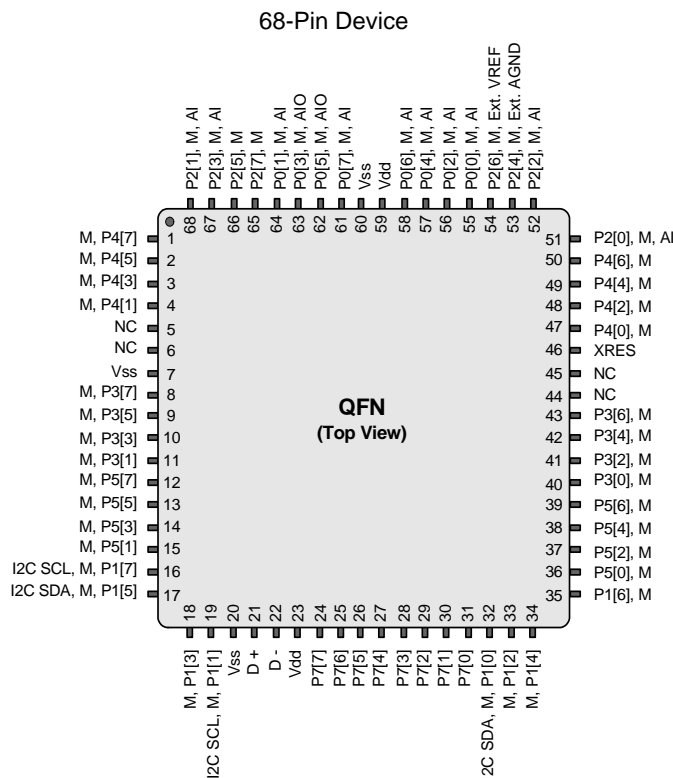
Pin No.	Type Digital	Type Analog	Name	Description
50	IO	M	P4[6]	
51	IO	I,M	P2[0]	Direct switched capacitor block input.
52	IO	I,M	P2[2]	Direct switched capacitor block input.
53	IO	M	P2[4]	External Analog Ground (AGND) input.
54	IO	M	P2[6]	External Voltage Reference (VREF) input.
55	IO	I,M	P0[0]	Analog column mux input.
56	IO	I,M	P0[2]	Analog column mux input and column output.
57	IO	I,M	P0[4]	Analog column mux input and column output.
58	IO	I,M	P0[6]	Analog column mux input.
59	Power		Vdd	Supply voltage.
60	Power		Vss	Ground connection.
61	IO	I,M	P0[7]	Analog column mux input, integration input #1
62	IO	IO,M	P0[5]	Analog column mux input and column output, integration input #2.
63	IO	IO,M	P0[3]	Analog column mux input and column output.
64	IO	I,M	P0[1]	Analog column mux input.
65	IO	M	P2[7]	

Table 3. 68-Pin Part Pinout (QFN**) (continued)

47	IO	M	P4[0]		66	IO	M	P2[5]	
48	IO	M	P4[2]		67	IO	I,M	P2[3]	Direct switched capacitor block input.
49	IO	M	P4[4]		68	IO	I,M	P2[1]	Direct switched capacitor block input.

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, M = Analog Mux Input.
* These are the ISSP pins, which are not High Z at POR.

** The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Register Conventions

This section lists the registers of the CY8CLED04 EZ-Color device.

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Table 4. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBIO_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBIO_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Table 4. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Table 5. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	PMA0_WA	40	RW	ASC10CR0	80	RW	USBIO_CR2	C0	RW
PRT0DM1	01	RW	PMA1_WA	41	RW	ASC10CR1	81	RW	USB_CR1	C1	#
PRT0IC0	02	RW	PMA2_WA	42	RW	ASC10CR2	82	RW			
PRT0IC1	03	RW	PMA3_WA	43	RW	ASC10CR3	83	RW			
PRT1DM0	04	RW	PMA4_WA	44	RW	ASD11CR0	84	RW	EP1_CR0	C4	#
PRT1DM1	05	RW	PMA5_WA	45	RW	ASD11CR1	85	RW	EP2_CR0	C5	#
PRT1IC0	06	RW	PMA6_WA	46	RW	ASD11CR2	86	RW	EP3_CR0	C6	#
PRT1IC1	07	RW	PMA7_WA	47	RW	ASD11CR3	87	RW	EP4_CR0	C7	#
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	PMA0_RA	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	PMA1_RA	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	PMA2_RA	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW	PMA3_RA	53	RW	ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	PMA4_RA	54	RW	ASC21CR0	94	RW		D4	

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Table 5. Register Map Bank 1 Table: Configuration Space (continued)

| Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT5DM1	15	RW	PMA5_RA	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	PMA6_RA	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW	PMA7_RA	57	RW	ASC21CR3	97	RW		D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
PRT7DM0	1C	RW		5C			9C			DC	
PRT7DM1	1D	RW		5D			9D		OSC_GO_EN	DD	RW
PRT7IC0	1E	RW		5E			9E		OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW	CMP_GO_EN1	65	RW		A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67			A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD		MUX_CR5	ED	RW
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/ez-color.

Specifications are valid for -40°C $\leq$ T$_A$ $\leq$ 85°C and T$_J$ $\leq$ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C $\leq$ T$_A$ $\leq$ 70°C and T$_J$ $\leq$ 82°C.

Figure 4.   Voltage versus CPU Frequency
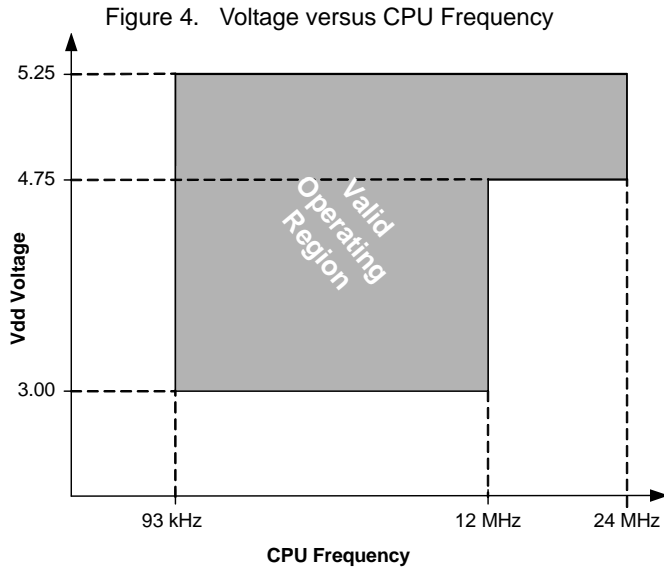
The following table lists the units of measure that are used in this chapter.

Table 6. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
^{o}C	degree Celsius	μW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	sps	samples per second
μV	microvolts	σ	sigma: one standard deviation
μVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C will degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IO2}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_{AUSB}	Ambient Temperature using USB	-10	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See "Thermal Impedance" on page 30. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 20 on page 20.
I_{DD5}	Supply Current, IMO = 24 MHz (5V)	–	14	27	mA	Conditions are Vdd = 5.0V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply Current, IMO = 24 MHz (3.3V)	–	8	14	mA	Conditions are Vdd = 3.3V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[a]	–	3	6.5	μA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C $\leq T_A \leq$ 55 °C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[a]	–	4	25	μA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < $T_A \leq$ 85 °C, analog power = off.

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull-Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 200 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–	–	V	Vdd = 3.0 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -10°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -10°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. DC Full-Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential Input Sensitivity	0.2	–	–	V	| (D+) - (D-) |
V_{CM}	Differential Input Common Mode Range	0.8	–	2.5	V	
V_{SE}	Single Ended Receiver Threshold	0.8	–	2.0	V	
C_{IN}	Transceiver Capacitance	–	–	20	pF	
I_{IO}	High-Z State Data Line Leakage	-10	–	10	μA	0V < V_{IN} < 3.3V.
R_{EXT}	External USB Series Resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static Output High, Driven	2.8	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull-up enabled.
V_{UOHI}	Static Output High, Idle	2.7	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull-up enabled.
V_{UOL}	Static Output Low	–	–	0.3	V	15 kΩ ± 5% to Ground. Internal pull-up enabled.
Z_O	USB Driver Output Impedance	28	–	44	Ω	Including R_{EXT} Resistor.
V_{CRS}	D+/D- Crossover Voltage	1.3	–	2.0	V	

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 12. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V$_{OSOA}$	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	–	1.6	10	mV	
	Power = Medium, Opamp Bias = High	–	1.3	8	mV	
	Power = High, Opamp Bias = High	–	1.2	7.5	mV	
TCV$_{OSOA}$	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I$_{EBOA}$	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C$_{INOA}$	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V$_{CMOA}$	Common Mode Voltage Range	0.0	–	Vdd	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	Vdd - 0.5		
G$_{OLOA}$	Open Loop Gain	–	–		dB	
	Power = Low, Opamp Bias = High	60				
	Power = Medium, Opamp Bias = High	60				
	Power = High, Opamp Bias = High	80				
V$_{OHIGHOA}$	High Output Voltage Swing (internal signals)					
	Power = Low, Opamp Bias = High	Vdd - 0.2	–	–	V	
	Power = Medium, Opamp Bias = High	Vdd - 0.2	–	–	V	
	Power = High, Opamp Bias = High	Vdd - 0.5	–	–	V	
V$_{OLOWOA}$	Low Output Voltage Swing (internal signals)					
	Power = Low, Opamp Bias = High	–	–	0.2	V	
	Power = Medium, Opamp Bias = High	–	–	0.2	V	
	Power = High, Opamp Bias = High	–	–	0.5	V	
I$_{SOA}$	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	400	800	µA	
	Power = Low, Opamp Bias = High	–	500	900	µA	
	Power = Medium, Opamp Bias = Low	–	800	1000	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High, Opamp Bias = Low	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	4600	6400	µA	
PSRR$_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss $\leq$ VIN $\leq$ (Vdd - 2.25) or (Vdd - 1.25V) $\leq$ VIN $\leq$ Vdd.

Table 13. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	–	1.65	10	mV	
	Power = Medium, Opamp Bias = High	–	1.32	8	mV	
	High Power is 5 Volts Only					
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	$\mu V/^oC$	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain		–	–	dB	
	Power = Low, Opamp Bias = Low	60				
	Power = Medium, Opamp Bias = Low	60				
	Power = High, Opamp Bias = Low	80				
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)					
	Power = Low, Opamp Bias = Low	Vdd - 0.2	–	–	V	
	Power = Medium, Opamp Bias = Low	Vdd - 0.2	–	–	V	
	Power = High is 5V only	Vdd - 0.2	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals)					
	Power = Low, Opamp Bias = Low	–	–	0.2	V	
	Power = Medium, Opamp Bias = Low	–	–	0.2	V	
	Power = High, Opamp Bias = Low	–	–	0.2	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	400	800	μA	
	Power = Low, Opamp Bias = High	–	500	900	μA	
	Power = Medium, Opamp Bias = Low	–	800	1000	μA	
	Power = Medium, Opamp Bias = High	–	1200	1600	μA	
	Power = High, Opamp Bias = Low	–	2400	3200	μA	
	Power = High, Opamp Bias = High	–	4600	6400	μA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss $\leq$ VIN $\leq$ (Vdd - 2.25) or (Vdd - 1.25V) $\leq$ VIN $\leq$ Vdd.

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 2.4V to 3.0V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC supply current	–	10	40	μA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40°C \leq T_A \leq 85°C$, or 3.0V to 3.6V and $-40°C \leq T_A \leq 85°C$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	– –	0.6 0.6	– –	Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	– –	– –	0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	– –	1.1 2.6	5.1 8.8	mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	53	64	–	dB	$(0.5 \times Vdd - 1.3) \leq V_{OUT} \leq (Vdd - 2.3)$.

Table 16. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	– –	1 1	– –	Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	– –	– –	0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	0.8 2.0	2.0 4.3	mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	34	64	–	dB	$(0.5 \times Vdd - 1.0) \leq V_{OUT} \leq (0.5 \times Vdd + 0.9)$.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 17. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[a]	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[a]	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[a]	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[a]	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

    a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

Table 18. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V	
–	AGND = Vdd/2[a]	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V	
–	AGND = 2 x BandGap[a]	Not Allowed				
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V	
–	AGND = BandGap[a]	BG - 0.009	BG + 0.005	BG + 0.015	V	
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V	
–	AGND Column to Column Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	V	
–	RefHi = Vdd/2 + BandGap	Not Allowed				
–	RefHi = 3 x BandGap	Not Allowed				
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed				
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed				
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V	
–	RefHi = 3.2 x BandGap	Not Allowed				
–	RefLo = Vdd/2 - BandGap	Not Allowed				
–	RefLo = BandGap	Not Allowed				
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed				
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed				
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]-P2[6] + 0.022	P2[4] - P2[6] + 0.092	V	

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V $\pm$ 0.02V.

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 19. DC Analog PSoC Block Specifications

| Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register.

Table 20. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR0R} V_{PPOR1R} V_{PPOR2R}	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.91 4.39 4.55	–	V V V	
V_{PPOR0} V_{PPOR1} V_{PPOR2}	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.39 4.55	–	V V V	
V_{PH0} V_{PH1} V_{PH2}	PPOR Hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	– – –	92 0 0	– – –	mV mV mV	
V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	2.98[a] 3.08 3.20 4.08 4.57 4.74[b] 4.82 4.91	V V V V V V V V	

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 21. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
b. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
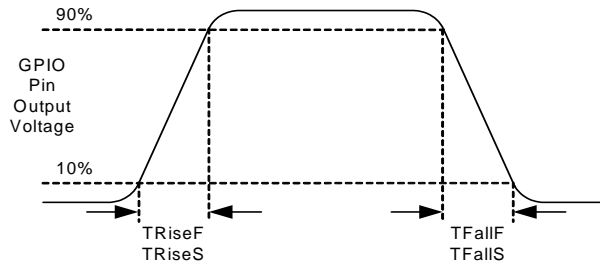
AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F$_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[a,b]	MHz	Trimmed for 5V operation using factory trim values.
F$_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[b,c]	MHz	Trimmed for 3.3V operation using factory trim values.
F$_{IMOUSB5V}$	Internal Main Oscillator Frequency with USB (5V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[b]	MHz	-10°C $\leq$ T$_A$ $\leq$ 85°C 4.35 $\leq$ Vdd $\leq$ 5.15
F$_{IMOUSB3V}$	Internal Main Oscillator Frequency with USB (3.3V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[b]	MHz	-0°C $\leq$ T$_A$ $\leq$ 70°C 3.15 $\leq$ Vdd $\leq$ 3.45
F$_{CPU1}$	CPU Frequency (5V Nominal)	0.93	24	24.96[a,b]	MHz	
F$_{CPU2}$	CPU Frequency (3.3V Nominal)	0.93	12	12.96[b,c]	MHz	
F$_{BLK5}$	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[a,b,d]	MHz	Refer to the AC Digital Block Specifications.
F$_{BLK3}$	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[b, d]	MHz	
F$_{32K1}$	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz Period Jitter	–	100		ns	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.08	48.0	49.92[a,c]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F$_{MAX}$	Maximum frequency of signal on row input or row output.	–	–	12.96	MHz	
T$_{RAMP}$	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.

b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.

c. 3.0V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

d. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 5. 24 MHz Period Jitter (IMO) Timing Diagram
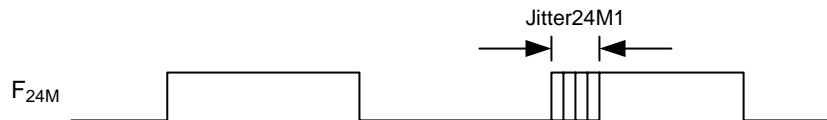
AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 23. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F$_{GPIO}$	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 6. GPIO Timing Diagram

AC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-10°C \leq T_A \leq 85°C$, or 3.0V to 3.6V and $-10°C \leq T_A \leq 85°C$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 24. AC Full-Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RFS}	Transition Rise Time	4	–	20	ns	For 50 pF load.
T_{FSS}	Transition Fall Time	4	–	20	ns	For 50 pF load.
T_{RFMFS}	Rise/Fall Time Matching: (T_R/T_F)	90	–	111	%	For 50 pF load.
$T_{DRATEFS}$	Full-Speed Data Rate	12 - 0.25%	12	12 + 0.25%	Mbps	

AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40°C \leq T_A \leq 85°C$, or 3.0V to 3.6V and $-40°C \leq T_A \leq 85°C$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 25. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	3.9	μs	
	Power = Medium, Opamp Bias = High	–	–	0.72	μs	
	Power = High, Opamp Bias = High	–	–	0.62	μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	5.9	μs	
	Power = Medium, Opamp Bias = High	–	–	0.92	μs	
	Power = High, Opamp Bias = High	–	–	0.72	μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.15	–	–	$V/\mu s$	
	Power = Medium, Opamp Bias = High	1.7	–	–	$V/\mu s$	
	Power = High, Opamp Bias = High	6.5	–	–	$V/\mu s$	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.01	–	–	$V/\mu s$	
	Power = Medium, Opamp Bias = High	0.5	–	–	$V/\mu s$	
	Power = High, Opamp Bias = High	4.0	–	–	$V/\mu s$	

Table 25. 5V AC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
BW$_{OA}$	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.75	–	–	MHz	
	Power = Medium, Opamp Bias = High	3.1	–	–	MHz	
	Power = High, Opamp Bias = High	5.4	–	–	MHz	
E$_{NOA}$	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

Table 26. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T$_{ROA}$	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	3.92	μs	
	Power = Medium, Opamp Bias = High	–	–	0.72	μs	
T$_{SOA}$	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	5.41	μs	
	Power = Medium, Opamp Bias = High	–	–	0.72	μs	
SR$_{ROA}$	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	–	–	V/μs	
	Power = Medium, Opamp Bias = High	2.7	–	–	V/μs	
SR$_{FOA}$	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.24	–	–	V/μs	
	Power = Medium, Opamp Bias = High	1.8	–	–	V/μs	
BW$_{OA}$	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.67	–	–	MHz	
	Power = Medium, Opamp Bias = High	2.8	–	–	MHz	
E$_{NOA}$	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 7. Typical AGND Noise with P2[4] Bypass
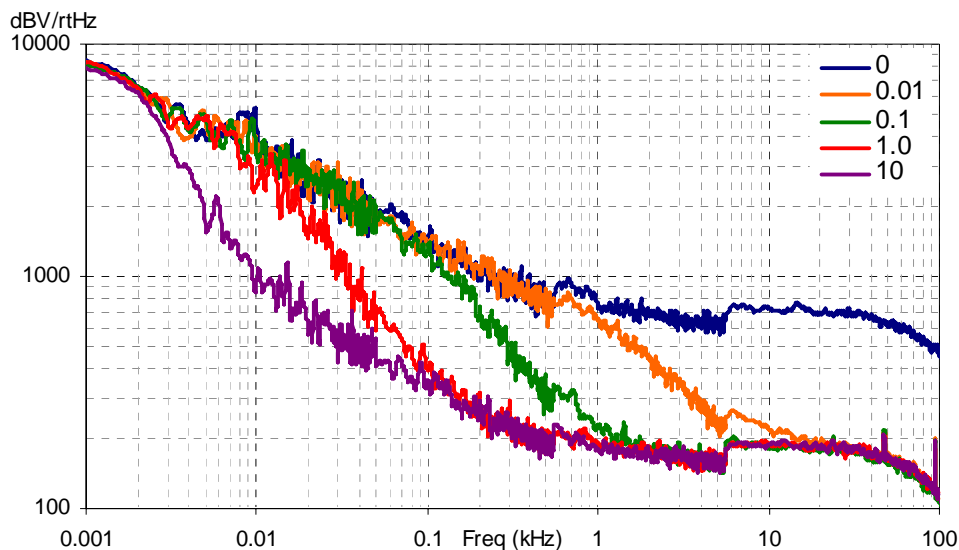
At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 8. Typical Opamp Noise
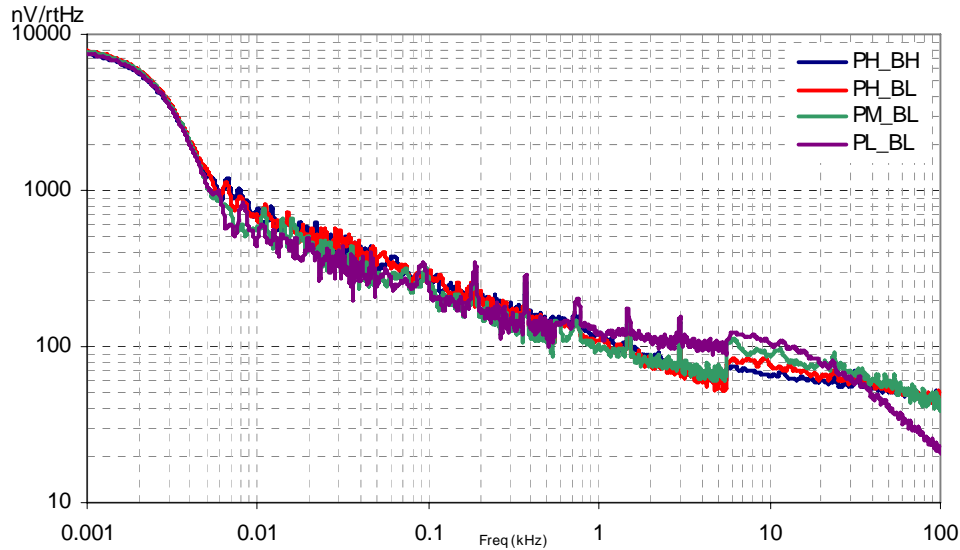
AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, or 2.4V to 3.0V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 27. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	μs	$\geq$ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 28. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	25.92	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	25.92	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 29. AC External Clock Specifications

| Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency for USB Applications	23.94	24	24.06	MHz	
–	Duty Cycle	47	50	53	%	
–	Power up to IMO Switch	150	–	–	µs	

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 30. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.5	µs	
	Power = High	–	–	2.5	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.2	µs	
	Power = High	–	–	2.2	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 31. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	3.8	µs	
	Power = High	–	–	3.8	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.6	µs	
	Power = High	–	–	2.6	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load					
	Power = Low	0.7	–	–	MHz	
	Power = High	0.7	–	–	MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 32. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T$_{RSCLK}$	Rise Time of SCLK	1	–	20	ns	
T$_{FSCLK}$	Fall Time of SCLK	1	–	20	ns	
T$_{SSCLK}$	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T$_{HSCLK}$	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F$_{SCLK}$	Frequency of SCLK	0	–	8	MHz	
T$_{ERASEB}$	Flash Erase Time (Block)	–	10	–	ms	
T$_{WRITE}$	Flash Block Write Time	–	30	–	ms	
T$_{DSCLK}$	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T$_{DSCLK3}$	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 $\leq$ Vdd $\leq$ 3.6

AC I^{2}C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq$ T$_A$ $\leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq$ T$_A$ $\leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 33. AC Characteristics of the I^{2}C SDA and SCL Pins for Vdd

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F$_{SCLI2C}$	SCL Clock Frequency	0	100	0	400	kHz	
T$_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
T$_{LOWI2C}$	LOW Period of the SCL Clock	4.7	–	1.3	–	μs	
T$_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs	
T$_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	μs	
T$_{HDDATI2C}$	Data Hold Time	0	–	0	–	μs	
T$_{SUDATI2C}$	Data Set-up Time	250	–	100[a]	–	ns	
T$_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	μs	
T$_{BUFI2C}$	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs	
T$_{SPI2C}$	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement t$_{SU;DAT}$ $\geq$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t$_{rmax}$ + t$_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 9. Definition for Timing for Fast/Standard Mode on the I^{2}C Bus
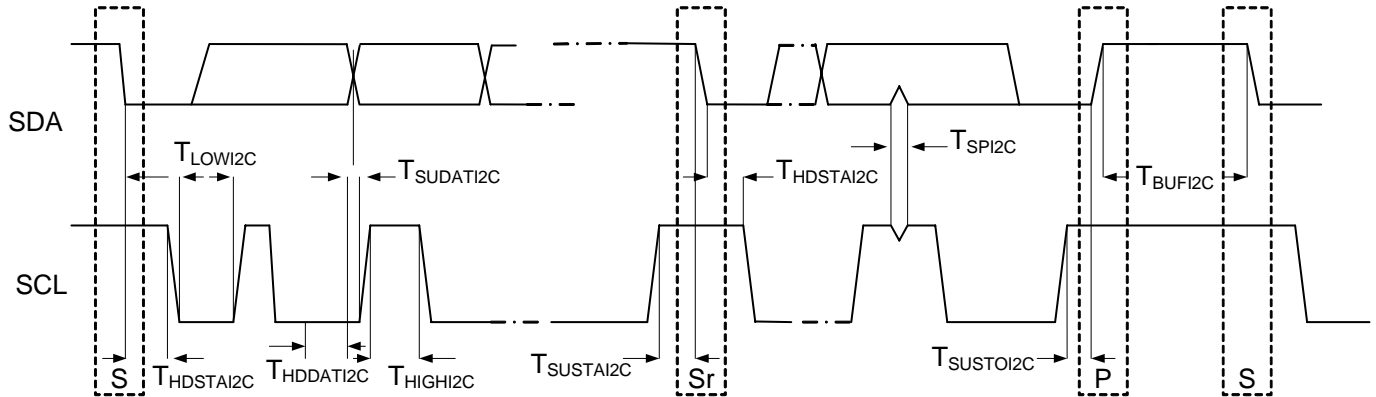
Packaging Information

Packaging Dimensions

This section illustrates the package specification for the CY8CLED04 EZ-Color device, along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 10. 68-Lead (8x8 mm x 0.89 mm) QFN
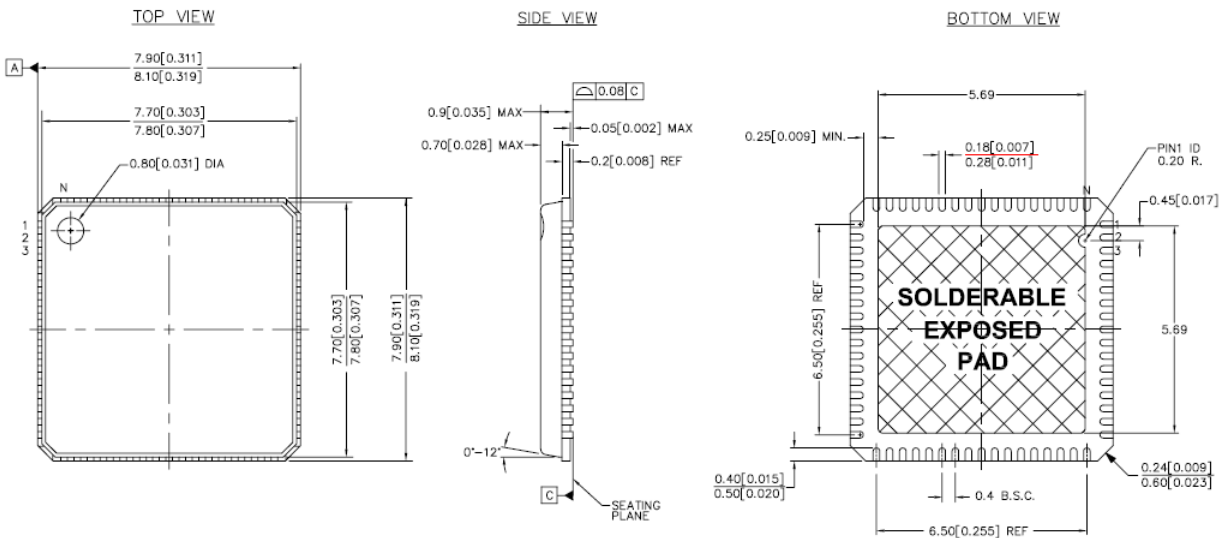
NOTES:
1. HATCH IS SOLDERABLE EXPOSED PAD.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.17g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF68	STANDARD
LY68	PB-FREE

NOTE: EXPOSED PAD DIMENSION VARIES BY LEADFRAME CAVITY (PADDLE) SIZE

51-85214 *C

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC device.

Thermal Impedance

Table 34. Thermal Impedance for the Package

Package	Typical θ_{JA} *
68 QFN**	13.05 ^{o}C/W

* $T_J = T_A + POWER \times \theta_{JA}$

** To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 35. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
68 QFN	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tools

Software

This section presents the development tools available for all current PSoC device families including the CY8CLED04 EZ-Color.

PSoC Express™

As the newest addition to the PSoC development software suite, PSoC Express is the first visual embedded system design tool that allows a user to create an entire PSoC project and generate a schematic, BOM, and data sheet without writing a single line of code. Users work directly with application objects such as LEDs, switches, sensors, and fans. PSoC Express is available free of charge at http://www.cypress.com/psocexpress.

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under DESIGN RESOURCES >> Software and Drivers.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3261A-RGB EZ-Color RGB Kit

The CY3261A-RGB board is a preprogrammed HB LED color mix board with seven pre-set colors using the CY8CLED16 EZ-Color HB LED Controller. The board is accompanied by a CD containing the color selector software application, PSoC Express 3.0 Beta 2, PSoC Programmer, and a suite of documents, schematics, and firmware examples. The color selector software application can be installed on a host PC and is used to control the EZ-Color HB LED controller using the included USB cable. The application enables you to select colors via a CIE 1931 chart or by entering coordinates. The kit includes:

■ Training Board (CY8CLED16)

■ One mini-A to mini-B USB Cable

■ PSoC Express CD-ROM

■ Design Files and Application Installation CD-ROM

To program and tune this kit via PSoC Express 3.0 you must use a Mini Programmer Unit (CY3217 Kit) and a CY3240-I2CUSB kit.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

■ MiniProg Programming Unit

■ MiniEval Socket Programming and Evaluation Board

■ 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample

■ 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

■ Evaluation Board with LCD Module

■ MiniProg Programming Unit

■ 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

■ Modular Programmer Base

■ 3 Programming Module Cards

■ MiniProg Programming Unit

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

■ CY3207 Programmer Unit

■ PSoC ISSP Software CD

■ 110 ~ 240V Power Supply, Euro-Plug Adapter

■ USB 2.0 Cable

3rd-Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at
http://www.cypress.com/an2323.

The following table lists the CY8CLED04 EZ-Color device key package features and ordering codes.

Ordering Information

Key Device Features

Table 36. Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Digital Blocks	Analog Blocks	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
68 Pin (8x8 mm) QFN	CY8CLED04-68LFXI	16K	1K	-40C to +85C	4	6	56	48	2	Yes
68 Pin (8x8 mm) QFN (Tape and Reel)	CY8CLED04-68LFXIT	16K	1K	-40C to +85C	4	6	56	48	2	Yes

Ordering Code Definitions

CY 8 C LED xx - xx xxxx

Package Type: ——————Thermal Rating:
  PX = PDIP Pb-Free   C = Commercial
  SX = SOIC Pb-Free   I = Industrial
  PVX = SSOP Pb-Free   E = Extended
  LFX/LKX = QFN Pb-Free
  AX = TQFP Pb-Free

Pin Count

Part Number

LED Family Code

Technology Code: C = CMOS

Marketing Code: 8 = Cypress PSoC

Company ID: CY = Cypress
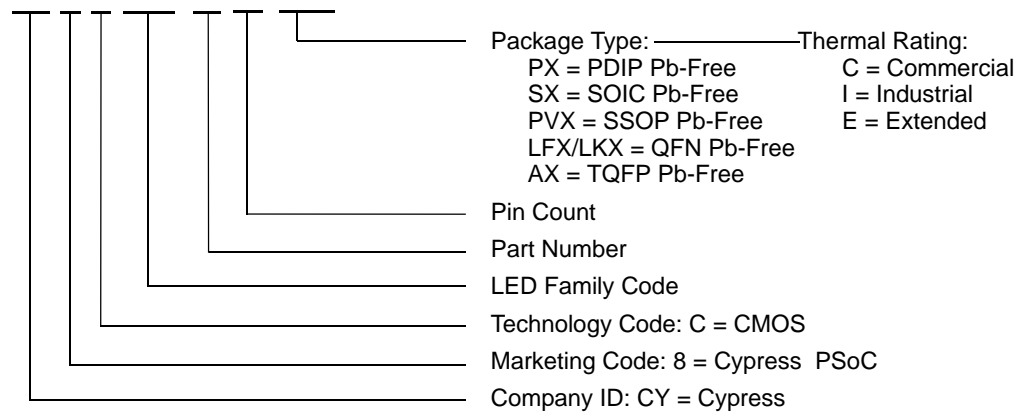
Revision History

Table 37. CY8CLED04 Data Sheet Revision History

Document Title: CY8CLED04 EZ-Color HB LED Controller				
Document Number: 001-13108				
Revision	**ECN #**	**Issue Date**	**Origin of Change**	**Description of Change**
**	1148504	See ECN	SFVTMP3	New document (revision **).
Distribution: External/Public		**Posting**: None		