CY8CMBR2044

Capacitive Button Controllers

Features

- Easiest to use capacitive button controller
  - Hardware configurable 4-button solution
  - No software tools or programming required
  - General purpose outputs (GPO) support direct LED drive
- Robust noise performance
  - High sensitivity, low noise capacitive sensing algorithm
  - Strong immunity to radio frequency (RF) and alternating current (AC) noise
  - Low radiated noise emission
- SmartSense™ auto tuning
  - No manual tuning required (reduces time to market)
  - All CapSense® parameters are automatically set in runtime
  - Ensures signal to noise ratio (SNR) of 5:1 or greater
  - Supports wide range of input capacitance (5 pF to 40 pF)
- Advanced features
  - Toggle feature on GPO
  - Flanking sensor suppression (FSS) provides robust sensing even with closely spaced sensors
  - Delay Off feature (configurable LED run time)
  - Easier production line testing
    - Serial data out for debug
    - Failure mode analysis of CapSense buttons
- Wide operating range
  - 1.71 V to 5.5 V ideal for unregulated battery applications
- Low power consumption
  - Supply current in run mode as low as 15 µA[1] for every button
  - Deep sleep current: 100 nA
- Industrial temperature range: –40 °C to + 85 °C
- 16-pad quad flat no leads (QFN) package (3 mm x 3 mm x 0.6 mm)

Overview

The CY8CMBR2044 incorporates several innovative features to save time, money, and can quickly enable a capacitive touch sensing UI in your next design. It does not require any software tools or coding because system configuration is done using hardware. These features enable a broader audience of designers to implement capacitive buttons without learning new tool sets and developing code. In addition, this device is enabled with Cypress's revolutionary SmartSense auto tuning algorithm. SmartSense ends the need to manually tune the UI during development as well as the required retuning during production ramp. This saves valuable engineering time, test time, production yield loss, and speeds the time to volume.

The CY8CMBR2044 CapSense controller supports up to four capacitive sensing buttons and four GPOs. The GPO is an active low output controlled directly by the CapSense input making it ideal for a wide variety of consumer, industrial, and medical applications. The wide operating range of 1.71 V to 5.5 V enables unregulated battery operation, further saving component cost.

This device supports ultra low power consumption in run mode as well as deep sleep modes to enhance battery life. In addition to this, the device also supports many advanced features which enhance the robustness and user interface of the end solution. Some of the key advanced features include FSS, which provides robust sensing even with closely spaced sensors. This is a critical requirement in small form factor applications. Another key feature is failure mode analysis that helps ease production line testing and reduces manufacturing costs.

Note

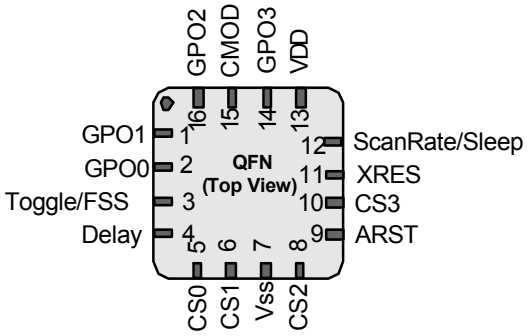
1. Power consumption calculated with 1.7% touch time, 500 ms scan rate, and C_P of each sensor < 19 pF.

Contents

Pinout

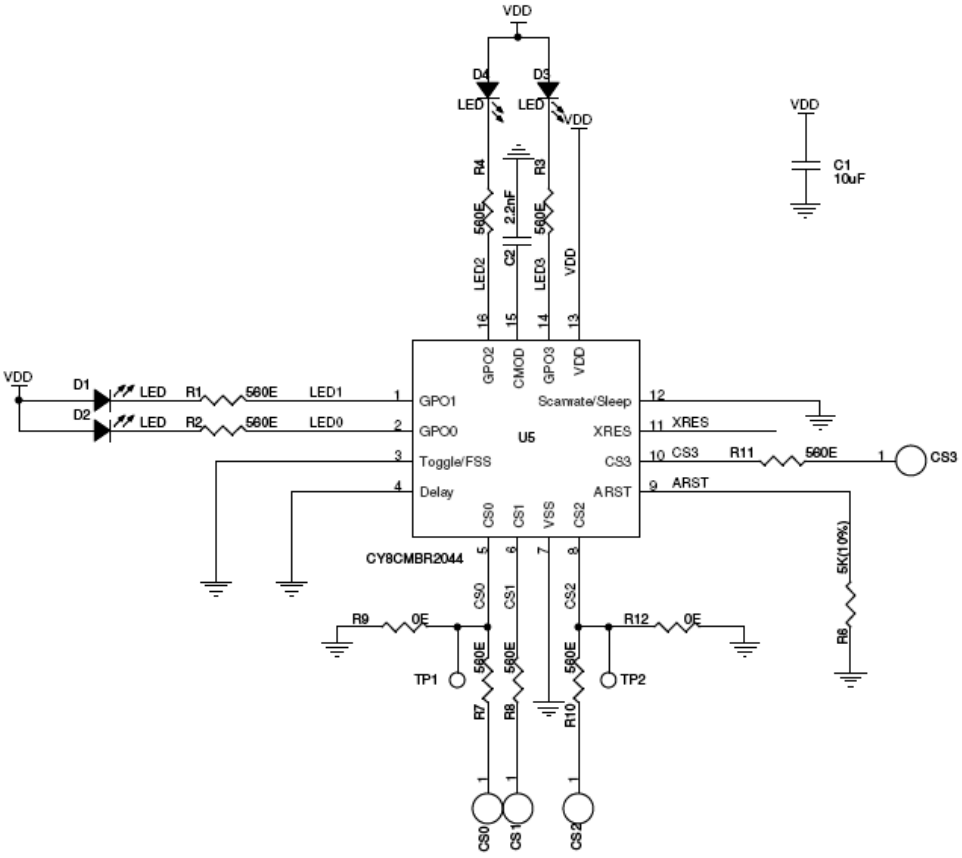
Table 1. Pin Diagram and Definitions – CY8CMBR2044

Pin	Label	Type	Description	If Unused
1	GPO1	DO	GPO activated by CS1	Leave open
2	GPO0	DO	GPO activated by CS0	Leave open
3	Toggle/ FSS	AI	Controls FSS and toggle. For details refer to Table 5 on page 7	Ground
4	Delay	AI	Controls delay off time. For details refer to Table 6 on page 8	Ground
5	CS0	AIO	CapSense input, controls GPO0 or serial debug data out	Ground
6	CS1	AIO	CapSense input, controls GPO1 or serial debug data out	Ground
7	V_{SS}	P	Ground	
8	CS2	AIO	CapSense input, controls GPO2 or serial debug data out	Ground
9	ARST	AIDO	Controls auto reset delay. For details on auto reset delay, refer to Table 4 on page 6	Leave open
10	CS3	AIO	CapSense input, controls GPO3 or serial debug data out	Ground
11	XRES	DI	Device reset, active high, with internal pull down	Leave open
12	ScanRate/ Sleep	AI	Controls scan rate and deep sleep. For details refer to Table 9 on page 13	Ground
13	V_{DD}	P	Power	
14	GPO3	DO	GPO activated by CS3	Leave open
15	CMOD	AI	External integrating capacitor, connect a 2.2 nF (±5%) to ground	
16	GPO2	DO	GPO activated by CS2	Leave open



Typical Circuits

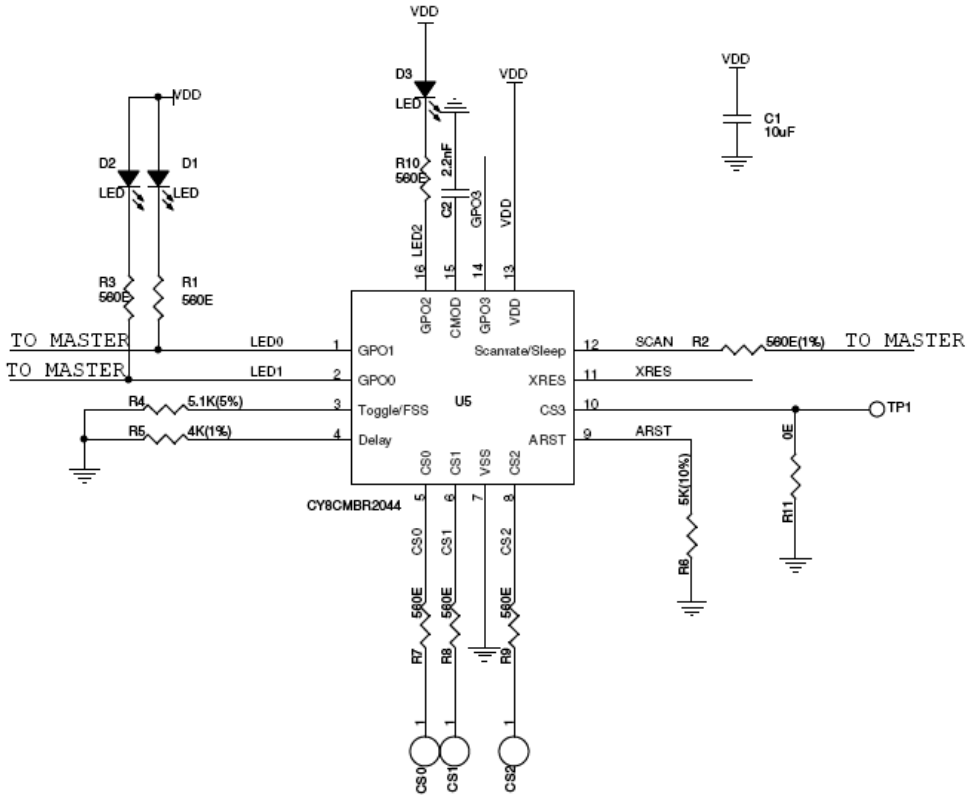
Schematic 1: 4-Buttons, 4-LEDs with Auto Reset Enabled



In the above schematic, the device is configured to support:

- Four CapSense buttons driving four LEDs
- Sensor auto reset (ARST) pin pulled down with a 5 KΩ resistor to set sensor auto reset time to 20 seconds
- Connect a 5.6 KΩ resistor on R9 or R12 to enable the serial debug data out feature

Schematic 2: 3-Buttons, 3-LEDs, 2-Outputs to Master, and Advanced Features Enabled



In the above schematic the device is configured to support:

- Three CapSense buttons driving three outputs
- Three LEDs driven by GPO0, GPO1, and GPO2
- CS3 is disabled (grounded); therefore, GPO3 is left floating
- FSS enabled, toggle disabled
- Delay off – 1 second
- Scan rate – 30 ms
- Sensor auto reset – 20 seconds
- Connect a 5.6 KΩ on resistor R11 to enable serial debug data out feature

Device Features

Table 2. Device Feature List

Feature	Benefits/ End Application Problem Solved
Four GPOs	Driving LED, mechanical button replacement
Flanking sensor suppression	Provides more discrimination between closely spaced sensors
Toggle	Mechanical button replacement
Sensor auto reset (ARST)	Prevents stuck sensor, i.e. metal object placed close to sensor
Delay Off	Provides better feedback based on button press
Failure mode analysis	Support for production testing and debugging
Serial debug data	Support for production testing and validating design
Sleep and deep sleep	Low power consumption

CapSense Buttons

- Device supports up to four CapSense buttons
- Ground the CSx pin to disable CapSense input
- 2.2 nF capacitor must be connected on the CMOD pin for proper CapSense operation

SmartSense Auto Tuning

- Device supports auto tuning of CapSense parameters
- No manual tuning required; all parameters are set by the device
- Compensates printed circuit board (PCB), device process variations, and PCB vendor changes
- The parasitic capacitance (C_P) of each button must be less than 40 pF for proper CapSense operation

General Purpose Outputs

- The GPOx is driven by CSx
- Active low output – supports sinking configuration
- If CSx is disabled (grounded), then GPOx must be left floating
- A 5 ms pulse is triggered on the GPOx if the CSx fails the power on self test (POST)

Hardware Configuration

- Advanced features are configured in hardware using external resistors
- The resistances on hardware configurable pins are determined once at power on

Sensor Auto Reset

- The sensor auto reset time is controlled by the hardware configuration on the ARST pin. Refer to Table 4 for details
- This feature decides the maximum time the GPOx is driven when CSx is continuously pressed
- After the sensor auto reset has been triggered, the CSx hold time of that sensor after the button has been released is given in Table 3. Scan rate is determined by the hardware configuration as shown in Table 9 on page 13

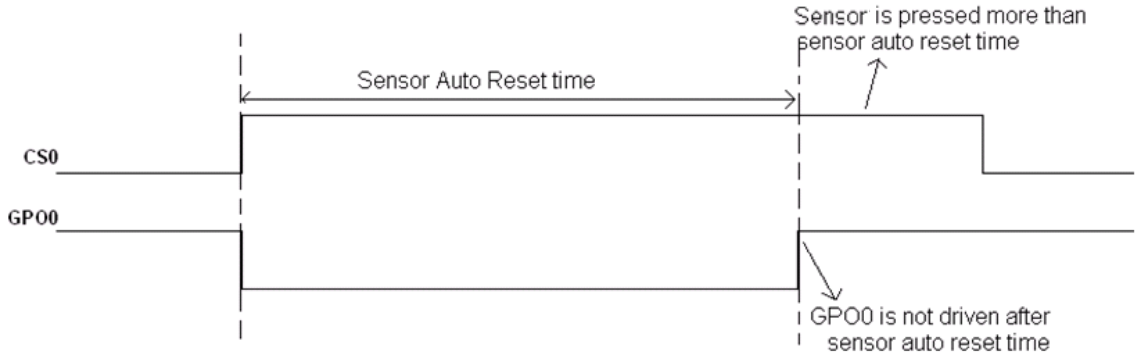
Table 3. Sensor Hold Time After Auto Reset

Sensor Press Time after Sensor Auto Reset	Sensor Hold Time (ms)
< 2 sec	220
> 2 sec	ScanRate + 200

Table 4. ARST Pin Hardware Configuration

Hardware Configuration	Sensor Max ON Time (sec)
Pin connected to ground	5
Resistor of 5 K (10%) ohms connected to ground	20
Pin connected to V_{DD} or left floating	No limit

Figure 1. Example of Sensor Auto Reset on GP0



Toggle

- The Toggle feature is controlled by the hardware configuration on Toggle/FSS pin. For details, refer to Table 5
- The state of GPx changes on every rising edge of CSx CapSense status
- When Toggle is enabled, Delay Off is disabled

Figure 2. Example of Toggle Feature on GP0

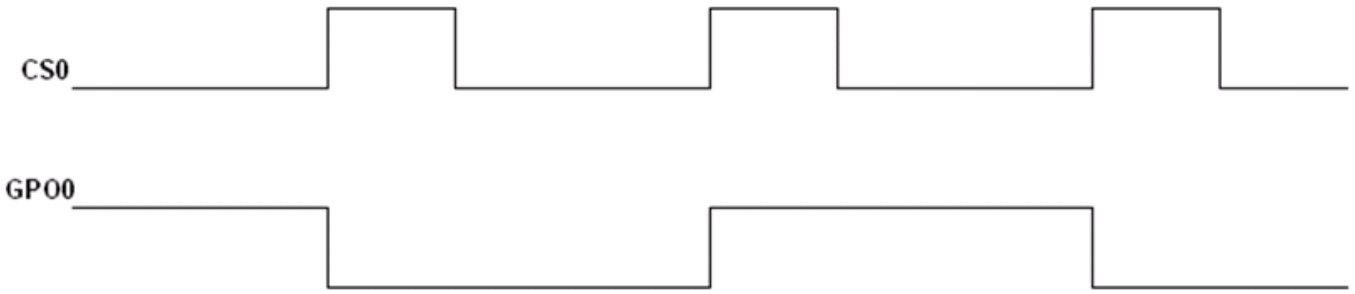


Table 5. Toggle/FSS Hardware Pin Configuration

Sl. No.	Toggle/FSS Pin Hardware Configuration	Toggle Enabled	FSS Enabled
1	Pin connected to ground or left floating	No	No
2	1.5 kΩ (5%) resistor to ground	Yes	No
3	5.1 kΩ (5%) resistor to ground	No	Yes
4	Pin connected to V_{DD}	Yes	Yes

Delay Off

- Delay off time is controlled by the hardware configuration on the delay pin. For details, see Table 6 on page 8
- To enable delay off with Delay ‘D’ (multiple of 20 ms), a resistor ‘R’ should be connected between the delay pin and ground where R = (Dx4) + 40 Ωs
- Delay off value specifies the duration for which the GPOx is driven low after the corresponding CapSense input CSx is released. See Figure 3 on page 8
- When a button gets reset, delay off is not applied on the corresponding GPO
- Delay off feature is applicable to only one GPO at any point of time. In Figure 3 on page 8, GPO0 goes high prematurely (prior to delay off time) because CS1 button is released. Therefore, the delay counter is reset. Now, GPO1 remains low for delay off time after releasing CS1
- Delay off feature is applicable to the GPO of the last button released
- Delay off range: 0 ms to 2000 ms

Figure 3. Example Delay Off Timing Diagram on GP0 and GP1

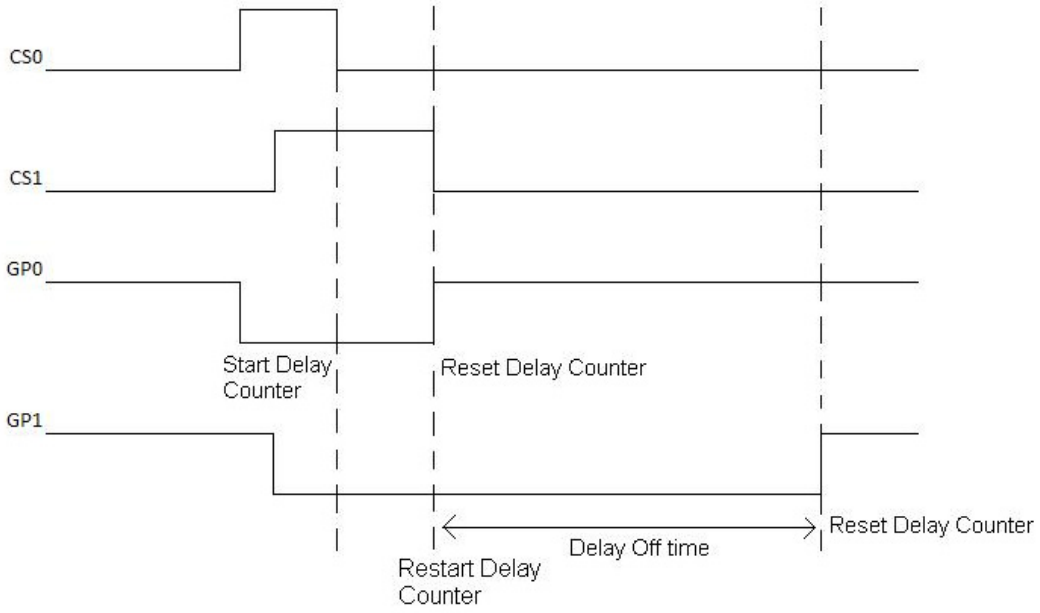


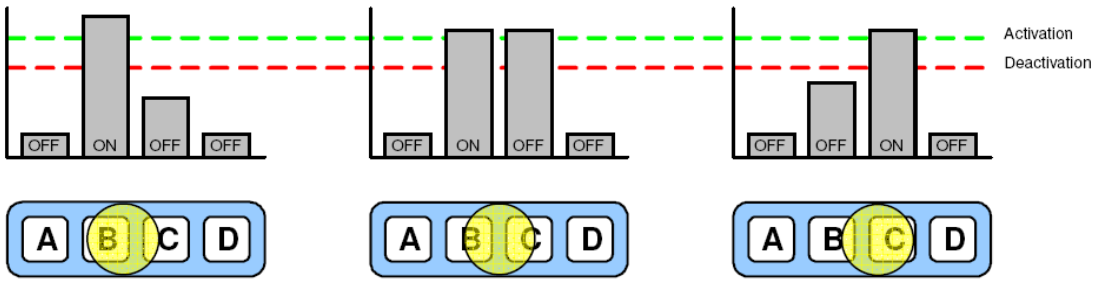
Table 6. Delay Off Pin Hardware Configuration

Pin Configuration	Approximate Delay Off Time (in ms)
Grounded (default)	0
120 Ωs (1%) to ground	20
200 Ωs (1%) to ground	40
280 Ωs (1%) to ground	60
. .	. .
7960 Ωs (1%) to ground	1980
8040 Ωs (1%) to ground	2000
> 8040 Ωs (1%) to ground	2000
Pulled to V_{DD}	2000
Floating	2000

Flanking Sensor Suppression

- Provides discrimination between closely spaced sensors
- At any point of time, only one sensor is reported as ON
- The first sensor touched is reported as ON until it is released, even if other sensors are pressed

Figure 4. Sensor Status with Respect to Finger Touch when FSS is Enabled



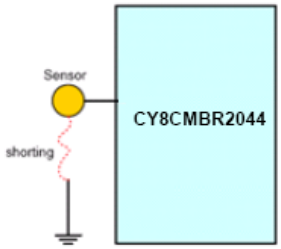
Failure Mode Analysis

A built-in Power On Self Test (POST) mechanism detects the following at power on reset (POR), which can be useful in production testing.

Sensor Shorted to Ground

If a sensor is disabled a 5 ms pulse is sent out on the corresponding GPO within 175 ms of power on.

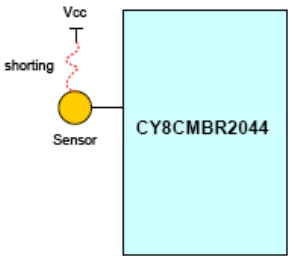
Figure 5. Sensor Shorted to Ground



Sensor Shorted to VDD

If any sensor is shorted to VDD that sensor is disabled and a 5 ms pulse is sent out on the corresponding GPO within 175 ms of power on.

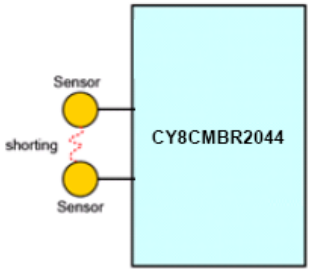
Figure 6. Sensor Shorted to VDD



Sensor to Sensor Short

Any Sensors that are shorted together is disabled and 5ms pulse is sent out on the GPOs of the shorted sensors within 175ms of power on.

Figure 7. Sensor to Sensor Short



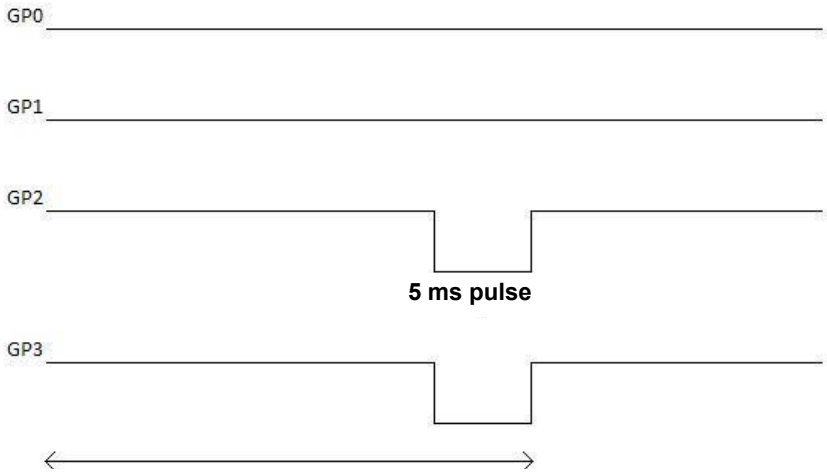
Proper Value of CMOD

- Recommended value of CMOD is 2 nF to 2.4 nF.
- If CMOD of < 1 nF or > 4 nF is connected, all sensors are disabled and a 5 ms pulse is sent out on all the GPOs within 175 ms of power on.

Sensor C_P > 40 pF

If the parasitic capacitance (C_P) of any sensor exceeds 40 pF that sensor is disabled and a 5 ms pulse is sent out on the corresponding GPO within 175 ms of power on.

Figure 8. Example Showing CS0 and CS1 Passing the POST and CS2 and CS3 are Failing



In Figure 8 CS0 and CS1 are enabled; CS2 and CS3 are disabled because the POST failed for these sensors. Therefore, a 5 ms pulse is observed on GPO2 and GPO3.

Debug Data

- To enable this feature pull down any one of the CapSense pins with a 5.6 kΩ resistor to ground. Data is sent out on the same CapSense pin
- If more than one CapSense pin is pulled down, debug data is sent out only on one CapSense pin and the priority is CS0 > CS1 > CS2 > CS3
- The Cypress multi chart tool (see application note AN2397) can be used to view the data
- Serial data is sent out with ~115,200 baud rate
- Firmware revision, CapSense status, GPO status, raw count, baseline, difference count, and parasitic capacitance of all sensors are sent out
- For designs having a maximum of three CapSense buttons, Cypress recommends to take the debug data on a CapSense button that is not used in design
- For designs with four CapSense buttons, Cypress recommends taking debug data on two CapSense buttons. For example, pull down CS0 with a 5.6 kΩ resistor and read data of CS1, CS2, and CS3. Next, pull down CS1 with a 5.6 kΩ resistor and read data of CS0, CS2, and CS3

Table 7. Data Format in Multi-chart: Serial TX8

Sl No	Raw Count Array		Baseline Array		Signal Array	
	MSB	LSB	MSB	LSB	MSB	LSB
0	0x00	FW_Revision	CS _Status	GPO_Status	0x00	CS2_C_P
1	0x00	CS0_ C_P	0x00	CS1_C_P	0x00	CS3_ C_P
2	CS0_RawCount		CS0_Baseline		CS0_DiffCount	
3	CS1_RawCount		CS1_Baseline		CS1_DiffCount	
4	CS2_RawCount		CS2_Baseline		CS2_DiffCount	
5	CS3_RawCount		CS3_Baseline		CS3_DiffCount	

Table 8. Serial Data Output

Byte	Data	Notes
0	0x0D	Dummy data for multi chart
1	0x0A	
2	0x00	–
3	FW_Revision	–
4	0x00	–
5	CS0_C_P	CS0 parasitic capacitance in Hex
6	CS0_RawCount_LSB	Unsigned 16-bit integer
7	CS0_RawCount_MSB	–
8	CS1_RawCount_LSB	Unsigned 16-bit integer
9	CS1_RawCount_MSB	–
10	CS2_RawCount_LSB	Unsigned 16-bit integer
11	CS2_RawCount_MSB	–
12	CS3_RawCount_LSB	Unsigned 16-bit integer
13	CS3_RawCount_MSB	–
14	CS _Status	Gives CapSense button status, least significant bit (LSB) contains CS0 status
15	GPO_Status	Gives GPO status, LSB contains GP0 status
16	0x00	–
17	CS1_C_P	CS1 parasitic capacitance in Hex
18	CS0_ Baseline _LSB	Unsigned 16-bit integer
19	CS0_ Baseline _MSB	–
20	CS1_ Baseline _LSB	Unsigned 16-bit integer
21	CS1_ Baseline _MSB	–
22	CS2_ Baseline _LSB	Unsigned 16-bit integer
23	CS2_ Baseline _MSB	–
24	CS3_ Baseline _LSB	Unsigned 16-bit integer
25	CS3_ Baseline _MSB	–
26	0x00	–
27	CS2_C_P	CS2 parasitic capacitance in Hex
28	0x00	–
29	CS3_C_P	CS3 parasitic capacitance in Hex
30	CS0_ DiffCount _LSB	Unsigned 16-bit integer
31	CS0_ DiffCount _MSB	–
32	CS1_ DiffCount _LSB	Unsigned 16-bit integer
33	CS1_ DiffCount _MSB	–
34	CS2_ DiffCount _LSB	Unsigned 16-bit integer
35	CS2_ DiffCount _MSB	–
36	CS3_ DiffCount _LSB	Unsigned 16-bit integer
37	CS3_ DiffCount _MSB	–
38	0x00	Dummy data for multi chart
39	0xFF	
40	0xFF	

Device Operating Modes

There are two device operating modes:

- Low power sleep mode
- Deep sleep mode

Low Power Sleep Mode

The following flow chart describes the low power sleep mode operation.

Figure 9. Low Power Sleep Mode Operation

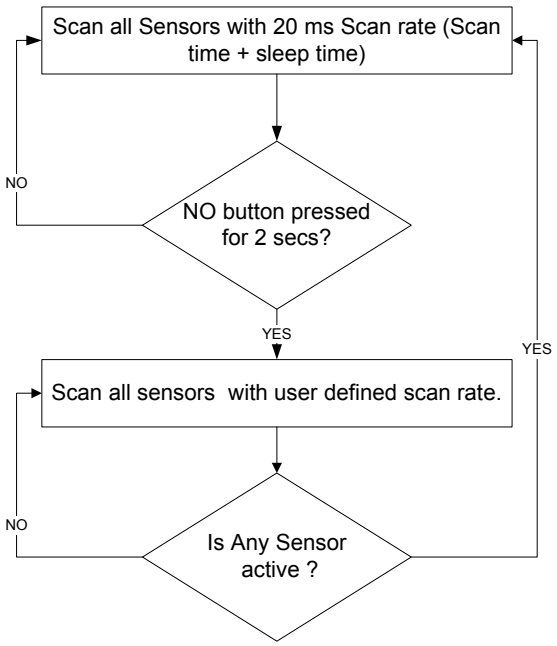
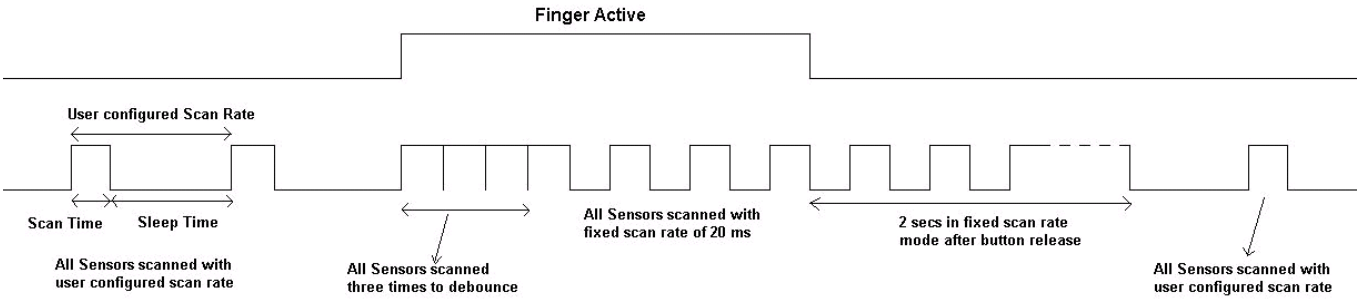


Figure 10. Low Power Sleep Mode Implementation



- To enable low power sleep mode, the hardware configurable pin ScanRate/Sleep should be pulled down to ground with resistor ‘R’ (1%). The scan rate values for different resistor values are given in Table 9 on page 13.
- The range of scan rate is 20 to 530 ms.

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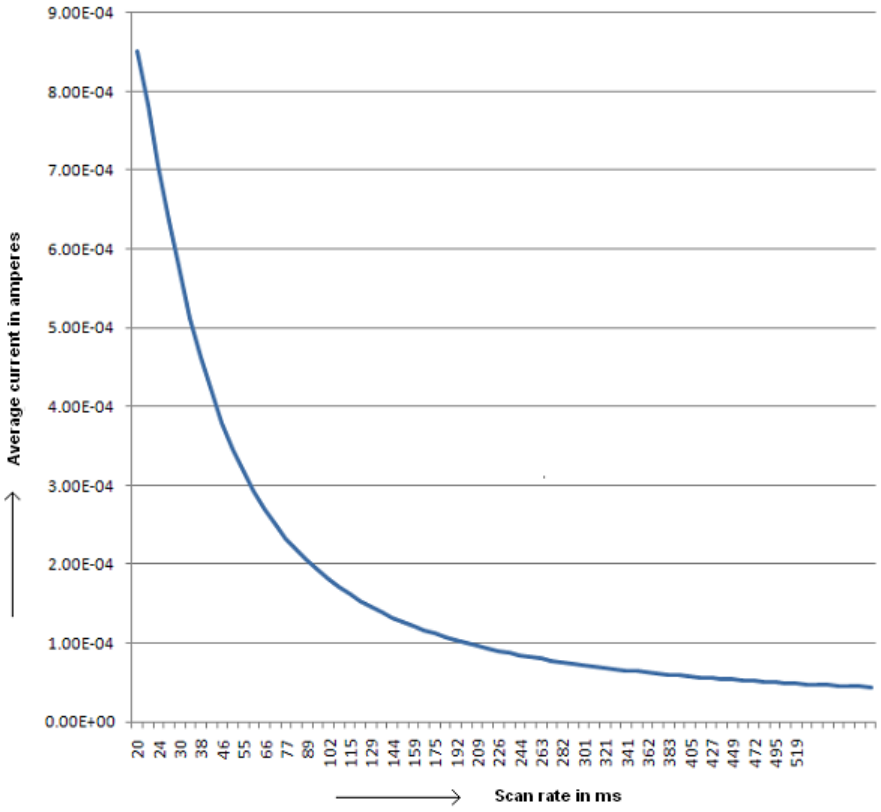
Table 9. ScanRate/Sleep Pin Hardware Configuration

Resistor R (1%) in ohms	Approximate ScanRate (in ms)	Resistor R (1%) in ohms	Approximate ScanRate (in ms)
60	20	4060	209
185	22	4185	217
310	24	4310	226
435	27	4435	235
560	30	4560	244
685	34	4685	253
810	38	4810	263
935	42	4935	272
1060	46	5060	282
1185	51	5185	291
1310	55	5310	301
1435	61	5435	311
1560	66	5560	321
1685	71	5685	331
1810	77	5810	341
1935	83	5935	352
2060	89	6060	362
2185	96	6185	373
2310	102	6310	383
2435	107	6435	394
2560	115	6560	405
2685	122	6685	416
2810	129	6810	427
2935	137	6935	438
3060	144	7060	449
3185	152	7185	461
3310	159	7310	472
3435	167	7435	484
3560	175	7560	495
3685	183	7685	507
3810	192	7810	519
3935	200	7935	531

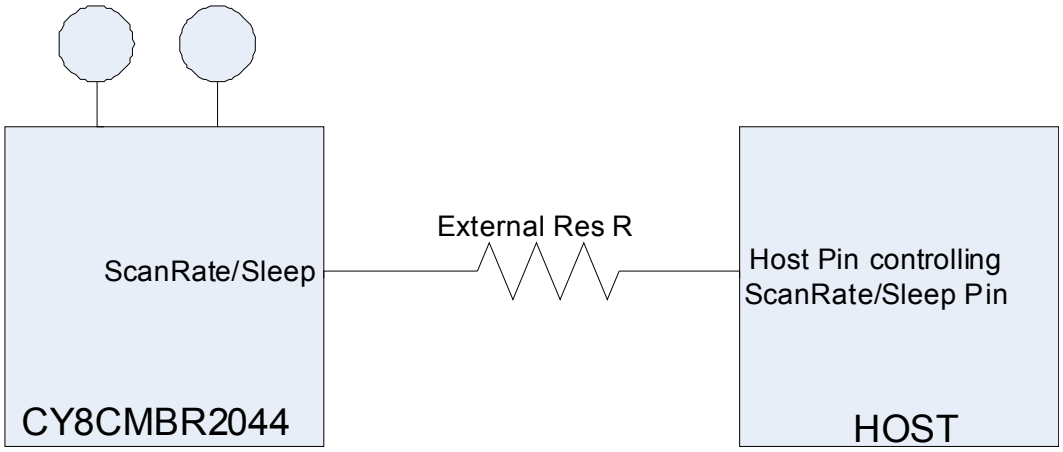
Figure 11. Average Current vs Scan Rate[2]



Note
2. Number of sensors = 3, Cp<19 pF, 0% touch time, V_{DD} = 3 V

Deep Sleep Mode

Figure 12. ScanRate/Sleep Pin Connection to Enable Deep Sleep Mode



- To enable the deep sleep mode, the hardware configuration pin ScanRate/Sleep should be connected to the master device as shown in Figure 9 on page 12.
- ScanRate/Sleep pin should be connected to V_{DD} for the device to go into deep sleep.
- In deep sleep mode, all blocks are turned off and the device power consumption is 0.1 µA.
- There is no CapSense scanning in deep sleep mode.
- ScanRate/Sleep pin should be pulled low for the device to wake up from deep sleep.
- When device comes out of deep sleep mode, the CapSense system is reinitialized. Typical time for reinitialization is 8 ms. Any button press within this time is not reported.
- After the device comes out of deep sleep, the device operates in low power sleep mode.
- If the ScanRate/Sleep pin is pulled high at power on, then the device does not go to deep sleep immediately. The device goes to deep sleep after initializing all internal blocks and scanning all sensors once.
- If the ScanRate/Sleep pin is pulled high at power on, then the scan rate is calculated when the device is taken out of Deep Sleep by the master.

Additional Components to Enable Advanced Features

Sl. No	Feature	Resistors required	Notes
1	Low power sleep and deep sleep	1	Deep sleep is controlled by a master device. When the device comes out of deep sleep, it enters into low power sleep mode based on settings. Resistor is not required if both features are not used.
2	Toggle/FSS	1	To enable both the features only one resistor is required. Resistor is not required if both features are not used.
3	Delay Off	1	Resistor is not required if the feature is not used.
4	Sensor auto reset	1	Resistor is not required if the feature is not used.

Response Time

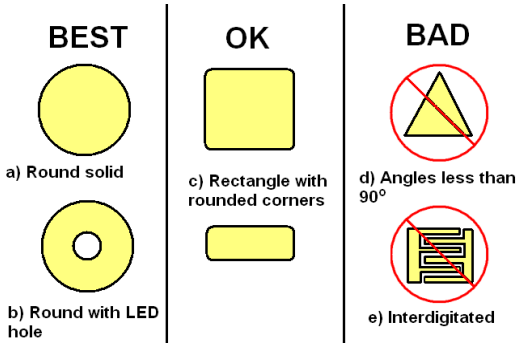
Response time is the minimum amount of time the button should be touched for the device to detect as valid button press.

Condition	Response time (in ms)
First button press	Scan rate value + 20. For scan rate value, see Table 9 on page 13.
Consecutive button press after first button press	80

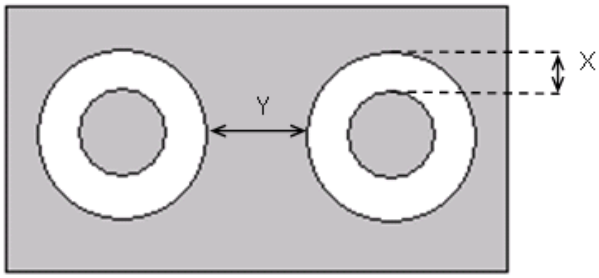
Layout Guidelines and Best Practices

Sl. No.	Category	Min	Max	Recommendations/Remarks
1	Button shape	–	–	Solid round pattern, round with LED hole, rectangle with round corners
2	Button size	5 mm	15 mm	10 mm
3	Button-button spacing	= Button Ground Clearance	–	8 mm (Y dimension in Button Layout Design on page 17)
4	Button ground clearance	0.5 mm	2 mm	Button ground clearance = Overlay thickness (X dimension in Button Layout Design on page 17)
5	Ground flood – top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
6	Ground flood – bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
7	Trace length from sensor to CapSense IC pins	–	200 mm	< 100 mm
8	Trace width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace routing	–	–	Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal
10	Via position for the sensors	–	–	Via should be placed near the edge of the button/slider to reduce trace length thereby increasing sensitivity
11	Via hole size for sensor traces	–	–	10 mil
12	No. of via on sensor trace	1	2	1
13	Distance of CapSense series resistor from sensor pin	–	10 mm	Place CapSense series resistors close to the device for noise suppression. CapSense resistors have highest priority; place them first
14	Distance between any CapSense trace to ground flood	10 mil	20 mil	20 mil
15	Device placement	–	–	Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum (see trace length above)
16	Placement of components in two layer PCB	–	–	Top layer – sensors and bottom layer – device, other components and traces
17	Placement of components in four layer PCB	–	–	Top layer – sensors, second layer – CapSense traces and V_{DD} (avoid V_{DD} traces below the sensors), third layer – hatched ground, bottom layer – CapSense IC or device, other components, and non CapSense traces
18	Overlay Thickness	0 mm	5 mm	1 mm
19	Overlay material	–	–	Should be non-conductive material. Glass, ABS plastic, formica, wood, and so on. There should be no air gap between PCB and overlay. Use adhesive to stick the PCB and overlay
20	Overlay Adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467MP and 468MP adhesives made by 3M are recommended
21	LED Back Lighting	–	–	Cut a hole in the sensor pad and use rear mountable LEDs. Refer to "Example PCB Layout Design with Four CapSense Buttons and Four LEDs" on page 18
22	Board Thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm

CapSense Button Shapes



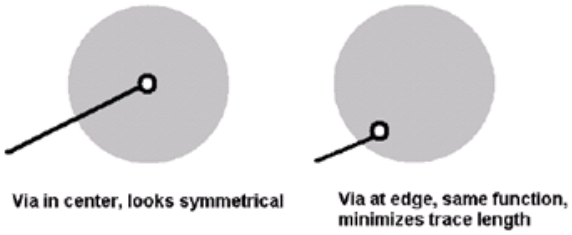
Button Layout Design



X: Button to ground clearance (Refer to Layout Guidelines and Best Practices on page 16)

Y: Button to button clearance (Refer to Layout Guidelines and Best Practices on page 16)

Recommended Via Hole Placement



Example PCB Layout Design with Four CapSense Buttons and Four LEDs

Figure 13. Top Layer

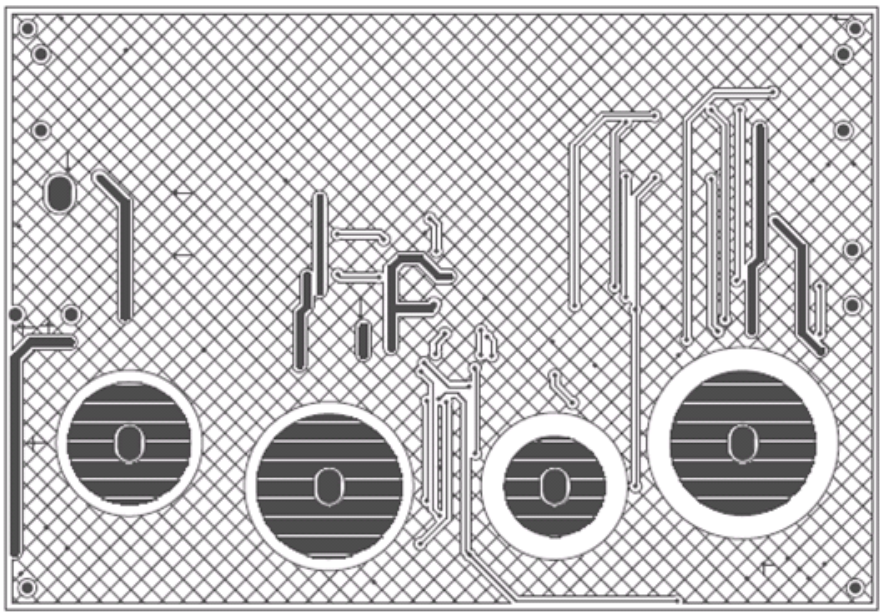
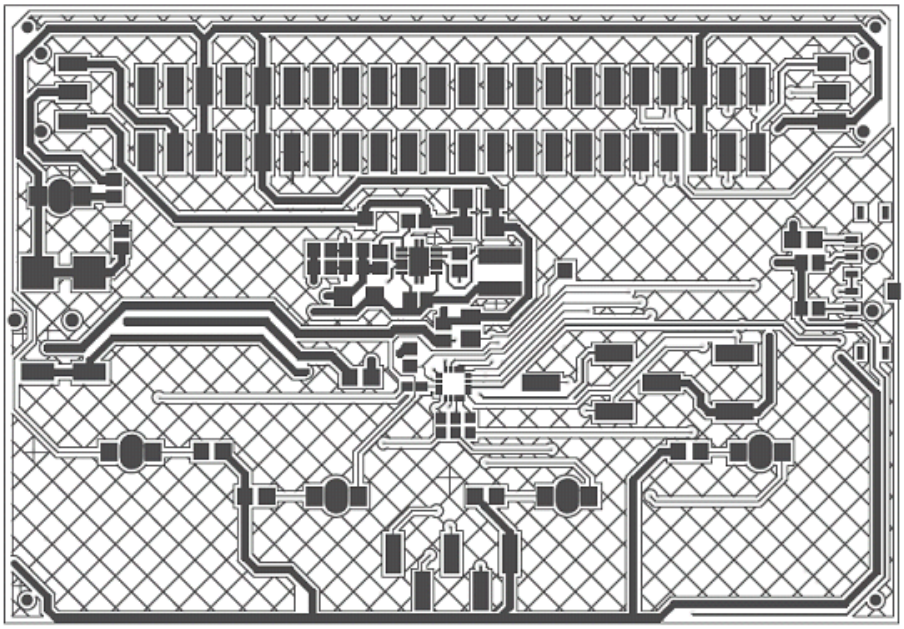


Figure 14. Bottom Layer



Electrical Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.
V_{DD}	Supply voltage relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC voltage on CapSense inputs and digital output pins	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIG}	Maximum current into any GPO output pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	In accordance with JESD78 standard

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Operational die temperature	–40	–	+100	°C	

DC Electrical Characteristics

DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}[1, 2, 3]	Supply voltage	1.71	–	5.5	V	
I_{DD}	Supply current	–	2.88	4.0	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C
I_{DA}	Active current	–	2.88	4.0	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, continuous sensor scan
I_{DS}	Deep sleep current	–	0.1	0.5	µA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C
I_{AV1}	Average current	–	40	–	µA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, 4 – buttons used, 0% touch time, C_P of all sensors<19 pF and scan rate = 530 ms
I_{AV2}	Average current	–	63	–	µA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, 4 – buttons used, 0% touch time, C_P of all sensors>19 pF and scan rate = 530 ms
I_{AV3}	Average current	–	1	–	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, 4 – buttons used, 100% touch time, C_P of all sensors<19 pF and scan rate = 20 ms
I_{AV4}	Average current	–	1.6	–	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, 4 – buttons used, 100% touch time, C_P of all sensors>19 pF and <40 pF, scan rate = 20 ms

1. When V_{DD} remains in the range from 1.75 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.75 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs. This helps to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
2. If you power down the device, make sure that V_{DD} falls below 100 mV before powering back up.
3. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.

DC General Purpose I/O Specifications

These tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C = TA = 85°C, 2.4 V to 3.0 V and –40 °C = TA = 85 °C, or 1.71 V to 2.4 V and –40 °C = TA = 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10. 3.0 V to 5 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GP0, GP1, GP2, GP3	V_{DD} – 0.2	–	–	V	IOH < 10 µA, maximum of 40 µA source current in all I/Os
V_{OH2}	High output voltage on GP0, GP1	V_{DD} – 0.9	–	–	V	IOH = 1 mA, maximum of 2 mA source current in all I/Os
V_{OH3}	High output voltage on GP2, GP3	V_{DD} – 0.9	–	–	V	IOH = 5 mA, maximum of 10 mA source current in all I/Os
V_{OL}	Low output voltage	–	–	0.75	V	IOL = 25 mA/pin, V_{DD} > 3.30, maximum of 60 mA sink current on GPO0, GPO1, GPO2, GPO3

Table 11. 2.4 V to 3.0 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GP0, GP1, GP2, GP3	V_{DD} – 0.2	–	–	V	IOH < 10 µA, maximum of 40 µA source current in all I/Os
V_{OH2}	High output voltage on GP0, GP1	V_{DD} – 0.4	–	–	V	IOH = 0.2 mA, maximum of 0.4 mA source current in all I/Os
V_{OH3}	High output voltage on GP2, GP3	V_{DD} – 0.5	–	–	V	IOH = 2 mA, maximum of 4 mA source current in all I/Os
V_{OL}	Low output voltage	–	–	0.72	V	IOL = 10 mA/pin, maximum of 30 mA sink current on GPO0, GPO1, GPO2, GPO3

Table 12. 1.71V to 2.4V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GP0,GP1	V_{DD} – 0.2	–	–	V	IOH =10 µA, maximum of 20 µA source current in all I/Os
V_{OH2}	High output voltage on GP0,GP1	V_{DD} – 0.5	–	–	V	IOH = 0.5 mA, maximum of 1 mA source current in all I/Os
V_{OH3}	High output voltage on GP2,GP3	V_{DD} – 0.2	–	–	V	IOH = 100 µA, maximum of 200 µA source current in all I/Os
V_{OH4}	High output voltage on GP2,GP3	V_{DD} – 0.5	–	–	V	IOH = 2 mA, maximum of 4 mA source current in all I/Os
V_{OL}	Low output voltage	–	–	0.4	V	IOL = 5 mA/pin, maximum of 20 mA sink current on GPO0, GPO1, GPO2, GPO3

AC Electrical Specifications

AC Chip Level Specifications

Parameter	Description	Min	Max	Unit	Notes
SR_{POWER_UP}	Power supply slew rate	–	250	V/ms	V_{DD} slew rate during power up
T_{XRST}	External reset pulse width at power up	1	–	ms	After supply voltage is valid
T_{XRST2}	External reset pulse width after power up	10	–	µs	Applies after part has booted

AC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
TRise1	Rise time on GPO0 and GPO1, Cload = 50 pF	15	–	80	ns	V_{DD} = 3.0 to 3.6 V, 10% – 90%
TRise2	Rise time on GPO2 and GPO3, Cload = 50 pF	10	–	50	ns	V_{DD} = 3.0 to 3.6 V, 10% – 90%
TRise3	Rise time on GPO0 and GPO1, Cload = 50 pF	15	–	80	ns	V_{DD} = 1.71 to 3.0V, 10% – 90%
TRise2	Rise time on GPO2 and GPO3, Cload = 50 pF	10	–	80	ns	V_{DD} = 1.71 to 3.0 V, 10% – 90%
TRise4	Fall time, Cload=50 pF all GPO outputs	10	–	50	ns	V_{DD} = 3.0 to 3.6 V, 90% – 10%
TFall2	Fall time, Cload=50 pF all GPO outputs	10	–	70	ns	V_{DD} = 1.71 to 3.0 V, 90% – 10%

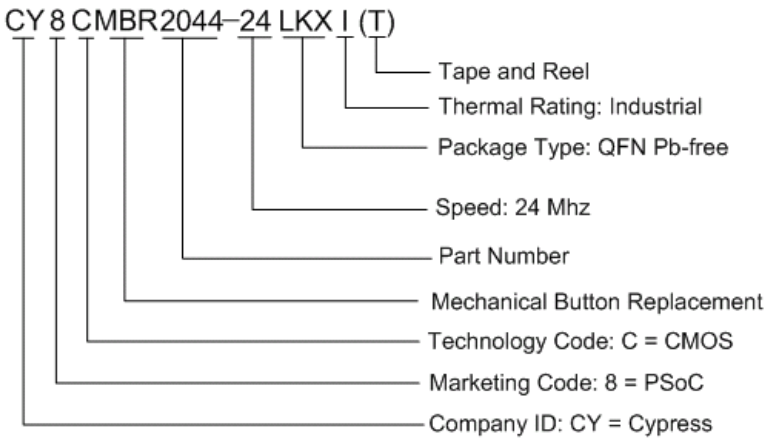
CapSense Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
C_P	Parasitic capacitance	5.0	–	$(C_P+C_F)<40$	pF	C_P is the total capacitance seen by the pin when no finger is present. C_P is sum of C_sensor, C_trace, and Capacitance of the vias and C_{PIN}
C_{PMAX}	Maximum parasitic capacitance till which sensor works	37	40	43	pF	
C_F	Finger capacitance	0.25	–	$(C_P+C_F)<40$	pF	C_F is the capacitance added by the finger touch
C_{PIN}	Capacitive load on pins as input	0.5	1.7	7	pF	
CMOD	External integrating capacitor	2	2.2	2.4	nF	Mandatory for CapSense to work
Rs	Series resistor between pin and the sensor	–	560	–	Ω	Reduces the RF noise

Ordering Information

Ordering Code	Package Type	Operating Temperature	CapSense Block	CapSense Inputs	GPOs	XRES Pin
CY8CMBR2044-24LKXI	16 Pad (3 x 3 x 0.6 mm) QFN	Industrial	Yes	4	4	Yes
CY8CMBR2044-24LKXIT	16 Pad (3 x 3 x 0.6 mm) QFN (Tape and Reel)	Industrial	Yes	4	4	Yes

Ordering Code Definitions



Package Information

Thermal Impedances by Package

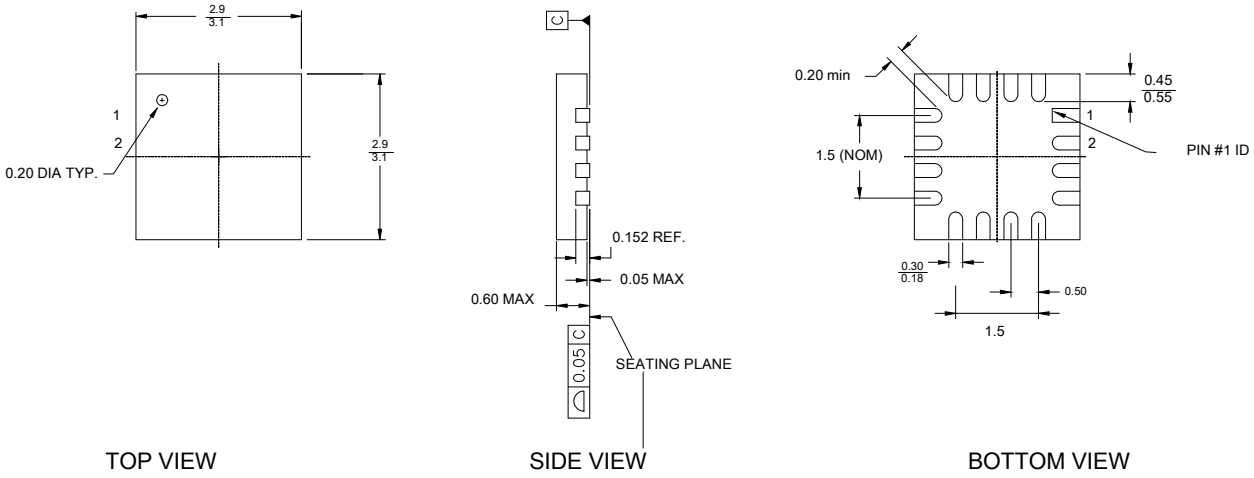
Package	Typical θ_{JA}[3]
16 QFN	32.7 °C/W

Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[4]	Maximum Peak Temperature
16 QFN	240 °C	260 °C

Package Diagram

Figure 15. 16-Pad Quad Flat No Leads (QFN) No E-pad 3x3 mm Package Outline (Sawn)



NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN MAX

001-09116 *E

Notes
3. TJ = TA + Power x θ_{JA}
4. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 13. Acronyms

Acronym	Description
AC	alternating current
AI	analog input
AIO	analog input/output
AIDO	analog input/digital output
DO	digital output
P	power pins
C_F	finger capacitance
C_P	parasitic capacitance
CS	CapSense
FSS	flanking sensor suppression
GPO	general purpose output
LSB	least significant bit
MSB	most significant bit
PCB	printed circuit board
POR	power on reset
POST	power on self test
RF	radio frequency

Units of Measure

The following table lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Table 14. Units of Measure

Acronym	Description
°C	degree Celsius
kΩ	Kilohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolts
nA	nanoampere
Ω	ohm
pF	picofarad
V	volts

Document History Page

Document Title: CY8CMBR2044 Capacitive Button Controllers Document Number: 001-57451				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2807997	SLAN	12/03/2009	New Data sheet
*A	2949368	SLAN	06/10/2010	Updated Features and Overview Added Units of Measure and numeric naming sections Updated Pinout Updated Schematic1 and Schematic2 Added Device Feature List Changed H/W configuration on the delay pin Added Figure 4, Figure 5, and Figure 7 Added Debug Data Updated Deep Sleep Mode Updated CapSense Button Shapes Updated Table 7 and Table 8 Changed Example PCB Layout Design with Four CapSense Buttons and Four LEDs Updated Electrical Specifications Added Ordering Code Definitions
*B	2975370	SLAN	07/09/2010	Updated Features Updated Pinout Updated Typical Circuits Added Device Feature List Added Figure 3, Figure 5, and Figure 7 Added Debug Data Updated Deep Sleep Mode Added Ordering Information
*C	2996393	SLAN	07/29/2010	Updated Features

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