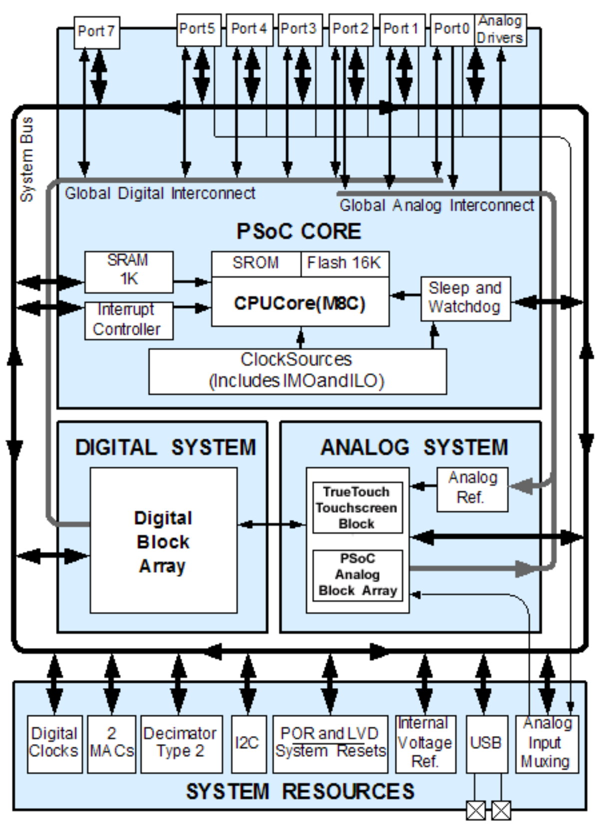
CY8CTMA120

TrueTouch™ Multi-Touch All-Point Touchscreen Controller

Features

- TrueTouch™ Capacitive Touchscreen Controller
  - Supports Multi-Touch All-Point Touchscreen Applications
  - Supports up to 37 X/Y Sensor Inputs
  - Supports Screen Sizes 7.3” and Below (Typical)
  - Fast Scan Rates: Typical 120 us per X/Y Crossing
  - High Resolution: Typical 480 x 360 for 3.5” Screen
  - Available in 56-Pin QFN Package
- Multi-Touch All-Point Addressable Detection
  - Capable of Tracking up to 10 Independent Fingers
  - Allows Development of Customized Multi-Finger Gestures
- Lowest Noise TrueTouch Device
- Highly Configurable Sensing Circuitry
  - Allows Maximum Design Flexibility
  - Allows Trade-Off Between Scan Time and Noise Performance
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Two 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 3V to 5.25V Operating Voltage
  - Industrial Temperature Range: –40°C to +85°C
  - USB Temperature Range: –10°C to +85°C
- Full-Speed USB (12 Mbps)
  - Four Uni-Directional Endpoints
  - One Bi-Directional Control Endpoint
  - USB 2.0 Compliant
  - Dedicated 256 Byte Buffer
  - No External Crystal Required
- Flexible On-Chip Memory
  - 16K Flash Program Storage, 50000 Erase/Write Cycles
  - 1K SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Precision, Programmable Clocking
  - Internal ±4% 24 and 48 MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
  - 0.25% Accuracy for USB with no External Components
- Additional System Resources
  - I^2C™ Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - TrueTouch Touchscreen Tuner
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory
- Programmable Pin Configurations
  - 25 mA Sink, 10 mA Drive on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO

Logic Block Diagram



TrueTouch Functional Overview

The TrueTouch family provides the fastest and most efficient way to develop and tune a capacitive touchscreen application. A TrueTouch device includes the configurable TrueTouch block, configurable analog and digital logic, programmable interconnect, and an 8-bit CPU to run custom firmware. This architecture enables the user to create flexible, customized touchscreen configurations to match the requirements of each individual touchscreen application. Various configurations of Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The TrueTouch architecture is comprised of four main areas: the Core, Digital System, the TrueTouch Analog System, and System Resources including a full speed USB port. Configurable global busing allows all the device resources to be combined into a complete custom touchscreen system. The CY8CTMA120 device can have up to seven IO ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks. Implementation of touchscreen application allows additional digital and analog resources to be used, depending on the touchscreen design. The CY8CTMA120 is offered in a 56-pin QFN package with up to 48 general purpose IO (GPIO), and support of up to 37 X/Y sensors.

When designing touchscreen applications, refer to the UM data sheet for performance requirements to meet and detailed design process explanation.

The TrueTouch Core

The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

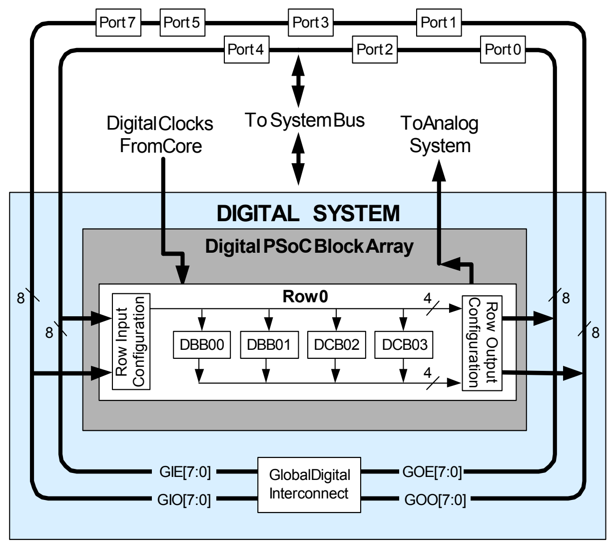
The TrueTouch device incorporates flexible internal clock generators, including a 24 MHz IMO (Internal Main Oscillator) accurate to 8% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (Internal Low speed Oscillator) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the TrueTouch device. In USB systems, the IMO self-tunes to ± 0.25% accuracy for USB communication.

The GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin is also capable of generating a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of four digital resources. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include those listed below.

- Full-Speed USB (12 Mbps)
- PWMs (8 to 32 bit)
- PWMs with dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave and multi-master
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees the designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by TrueTouch device family. This allows optimum choice of system resources for your application. Family characteristics are shown in Table 1 on page 4.

The Analog System

The Analog System is composed of 6 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Implementation of touchscreen application allows additional analog resources to be used, depending on the touchscreen design. Analog peripherals are very flexible and are customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 2, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6- to 9-bit resolution)
- Multiplying DACs (up to 2, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core Resource)
- 1.3V reference (as a System Resource)
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 2.

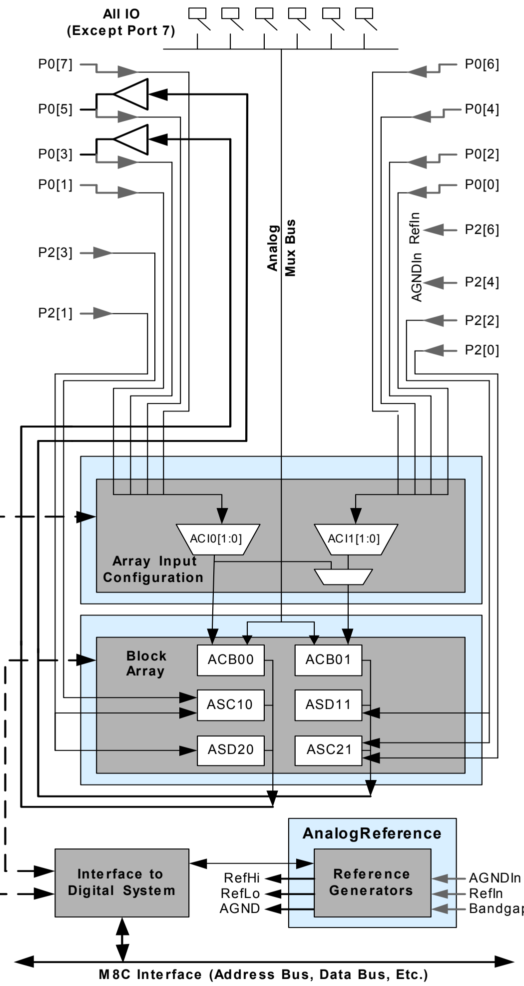
The Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0-5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for capacitive sensing with the TrueTouch block comparator. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to switch dynamically under hardware control. This enables capacitive measurement for the touchscreen applications. Other multiplexer applications include:

- Chip-wide mux that allows analog input from up to 48 IO pins.
- Electrical connection between any IO pin combinations.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Full-Speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Wider than commercial temperature USB operation (-10°C to +85°C).
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks are routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- Decimator provides a custom hardware filter for digital signal processing applications, including creation of Delta Sigma ADCs.

- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, multi-master are supported.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

Getting Started

To understand the TrueTouch device, read this data sheet and use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents general silicon and electrical specifications. For in depth touchscreen application information, including touchscreen specific specifications, read the touchscreen user module data sheet that is supported by this specific device.

TrueTouch Device Characteristics

Depending on the TrueTouch device selected for a touchscreen application, characteristics and capabilities of each device change. Table 1 lists the touchscreen sensing capabilities available for specific TrueTouch devices. The TrueTouch device covered by this data sheet is highlighted in this table.

Table 1. TrueTouch Device Characteristics

TrueTouch Part Number	Sensor Inputs	Max Screen Size (Inches)	Single-Touch	Multi-Touch Gesture	Multi-Touch All-Point	Scan Speed (ms)[1]	Current Consumption[2]	Flash Size	SRAM Size
CY8CTST110	up to 24	4.3”	Y	N	N	0.5	3	8K	512 Bytes
CY8CTST120	up to 44	8.4”	Y	N	N	0.5	16	16K	1K
CY8CTMG110	up to 24	4.3”	Y	Y	N	0.5	3	8K	512 Bytes
CY8CTMG120	up to 44	8.4	Y	Y	N	0.5	16	16K	1K
CY8CTMA120	up to 37	7.3”	Y	Y	Y	0.12	16	16K	1K

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to http://www.cypress.com/training.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They are available with a four hour guaranteed response at http://www.cypress.com/support.

Application Notes

A long list of application notes assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are listed by date as default.

Development Tools

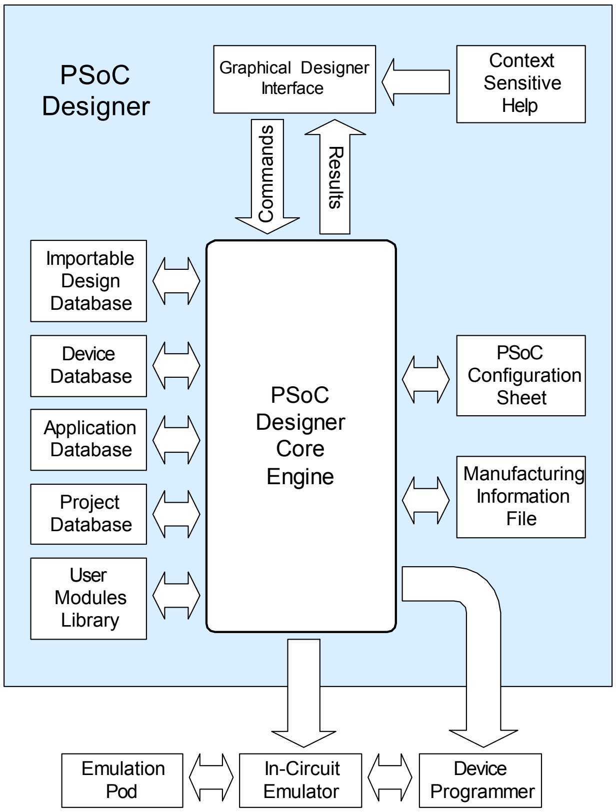
PSoC Designer is a Microsoft® Windows based, integrated development environment for the Programmable System-on-Chip™ (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP (see Figure 3 on page 5).

PSoC Designer helps to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high level C language compiler developed specifically for the devices in the family.

Notes
1. Per sensor typical. Depends on touchscreen panel. For MA120 per X/Y crossing Vcc = 3.3V.
2. Average mA supply current. Based on 8 ms report rate, except for MA120.

Figure 3. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, amplifiers, and filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components. If the project uses more than one operating configuration, then it contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer prints out a configuration sheet for a given project configuration for use during application programming in conjunction with the device data sheet. After the framework is generated, the user can add application specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

The Application Editor edits the C language and assembly language source code. It also assembles, compiles, links, and builds.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports the PSoC family of devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

TrueTouch Touchscreen Tuner

The TrueTouch tuner is a Microsoft® Windows based graphical user interface allowing developers to set critical parameters and observe changes to the touchscreen application in real time. Optimal configuration from the tuner are immediately applied to the TrueTouch user module settings.

Designing with User Modules

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility. It pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware and the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

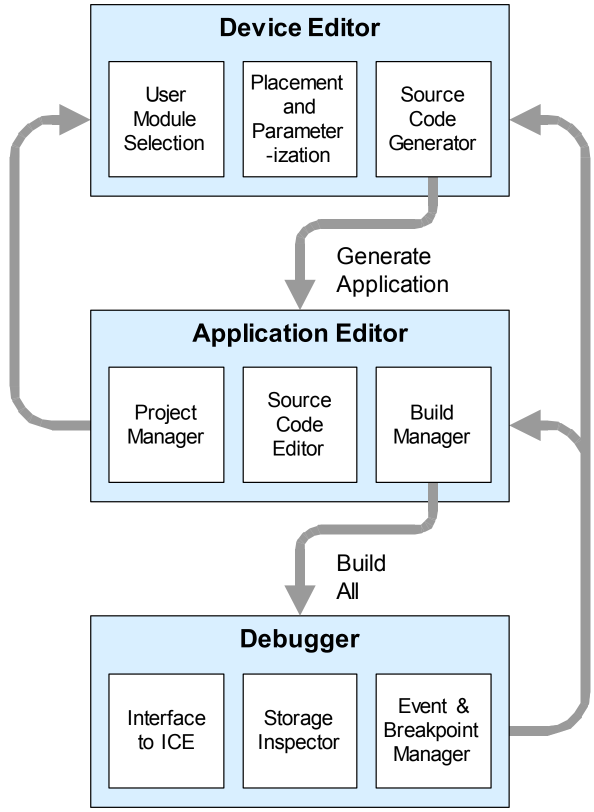
To speed the development process, the PSoC Designer IDE provides a library of pre-built, pre-tested hardware peripheral functions, called "User Modules." User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard user module library contains over 50 common peripherals such as ADCs, DACs timers, counters, UARTs, and other not so common peripherals such as DTMF generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allows to tailor its precise configuration to a particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit to establish the pulse width and duty cycle. User modules also provide tested software to cut development time. The user module application programming interface (API) provides high level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that are adapted as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. Pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, build signal chains by interconnecting user modules to each other and the IO pins. At this stage, also configure the clock source connections and enter parameter values directly or by selecting values from drop down menus. When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high level user module API functions.

Figure 4. User Module/Source Code Development Flows



The next step is to write the main program and any sub-routines using PSoC Designer's Application Editor subsystem. The Application Editor includes a Project Manager that allows to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive "grep-style" patterns. A single mouse click invokes the Build Manager. It employs a professional-strength "makefile" system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double click the error message to view the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events such as monitoring address and data bus values, memory locations, and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 5 on page 12 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers are also represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘0x’, or ‘b’ are decimal.

Pinouts

This section describes, lists, and illustrates the CY8CTMA120 TrueTouch family pins and pinout configuration. The CY8CTMA120 TrueTouch device is available in the following packages, all of which are shown on the following pages. Every port pin (labeled "P") is capable of Digital IO. However, Vss, Vdd, and XRES are not capable of Digital IO.

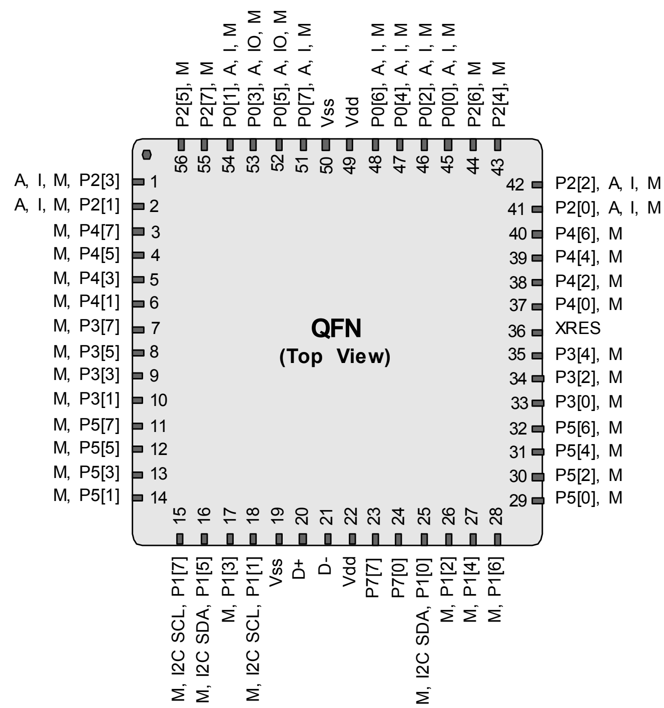
56-Pin Part Pinout

Table 2. 56-Pin Part Pinout (QFN)

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P2[3]	VREF
2	IO	I, M	P2[1]	SNS_OUT(Output of external OP-AMP)
3	IO	M	P4[7]	
4	IO	M	P4[5]	
5	IO	M	P4[3]	
6	IO	M	P4[1]	
7	IO	M	P3[7]	
8	IO	M	P3[5]	
9	IO	M	P3[3]	
10	IO	M	P3[1]	
11	IO	M	P5[7]	
12	IO	M	P5[5]	
13	IO	M	P5[3]	
14	IO	M	P5[1]	
15	IO	M	P1[7]	phi2 (Control for high precision switches)
16	IO	M	P1[5]	phi1 (Control for high precision switches).
17	IO	M	P1[3]	
18	IO	M	P1[1]	I2C Serial Data (SDA), ISSP DATA[3].
19	Power		Vss	Ground. Connect to circuit ground.
20	USB		D+	
21	USB		D-	
22	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.
23	IO		P7[7]	
24	IO		P7[0]	SHDN
25	IO	M	P1[0]	I2C Serial IRQ (Interrupt), ISSP CLK[3].
26	IO	M	P1[2]	
27	IO	M	P1[4]	
28	IO	M	P1[6]	
29	IO	M	P5[0]	
30	IO	M	P5[2]	
31	IO	M	P5[4]	
32	IO	M	P5[6]	
33	IO	M	P3[0]	
34	IO	M	P3[2]	
35	IO	M	P3[4]	
36	Input		XRES	Active high external reset with internal pull down.
37	IO	M	P4[0]	
38	IO	M	P4[2]	
39	IO	M	P4[4]	
40	IO	M	P4[6]	
41	IO	I, M	P2[0]	Direct switched capacitor block input.
42	IO	I, M	P2[2]	Direct switched capacitor block input.
43	IO	M	P2[4]	VREF.
44	IO	M	P2[6]	VREF.
45	IO	I, M	P0[0]	Analog column mux input.
46	IO	I, M	P0[2]	Analog column mux input.
47	IO	I, M	P0[4]	Analog column mux input.
48	IO	I, M	P0[6]	Analog column mux input.
49	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.
50	Power		Vss	Ground. Connect to circuit ground.
51	IO	I, M	P0[7]	Rx.
52	IO	IO, M	P0[5]	Tx.
53	IO	IO, M	P0[3]	Analog column mux input and column output.
54	IO	I, M	P0[1]	Analog column mux input.
55	IO	M	P2[7]	
56	IO	M	P2[5]	
EP	Power		Vss	Exposed pad is internally connected to ground. Connect to circuit ground.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 5. CY8CTMA120 56-Pin PSoC Device



Note
3. These are the ISSP pins, which are not High Z at POR

[+] Feedback

100-Ball VFBGA Part Pinout

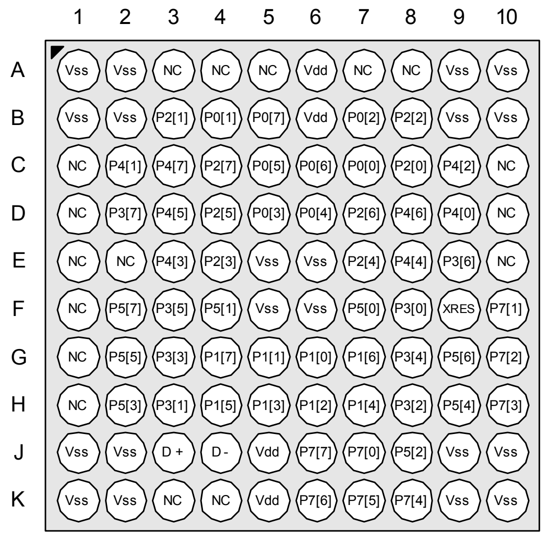
The 100-ball VFBGA part is for the CY8CTMA120 device.

Table 3. 100-Ball Part Pinout (VFBGA)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
A1	Power		Vss	Ground connection.	F1			NC	No connection.
A2	Power		Vss	Ground connection.	F2	IO	M	P5[7]	
A3			NC	No connection.	F3	IO	M	P3[5]	
A4			NC	No connection.	F4	IO	M	P5[1]	
A5			NC	No connection.	F5	Power		Vss	Ground connection.
A6	Power		Vdd	Supply voltage.	F6	Power		Vss	Ground connection.
A7			NC	No connection.	F7	IO	M	P5[0]	
A8			NC	No connection.	F8	IO	M	P3[0]	
A9	Power		Vss	Ground connection.	F9			XRES	Active high pin reset with internal pull down.
A10	Power		Vss	Ground connection.	F10	IO		P7[1]	
B1	Power		Vss	Ground connection.	G1			NC	No connection.
B2	Power		Vss	Ground connection.	G2	IO	M	P5[5]	
B3	IO	I,M	P2[1]	Direct switched capacitor block input.	G3	IO	M	P3[3]	
B4	IO	I,M	P0[1]	Analog column mux input.	G4	IO	M	P1[7]	I2C Serial Clock (SCL).
B5	IO	I,M	P0[7]	Analog column mux input.	G5	IO	M	P1[1]	I2C Serial Clock (SCL), ISSP SCLK.
B6	Power		Vdd	Supply voltage.	G6	IO	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA.
B7	IO	I,M	P0[2]	Analog column mux input.	G7	IO	M	P1[6]	
B8	IO	I,M	P2[2]	Direct switched capacitor block input.	G8	IO	M	P3[4]	
B9	Power		Vss	Ground connection.	G9	IO	M	P5[6]	
B10	Power		Vss	Ground connection.	G10	IO		P7[2]	
C1			NC	No connection.	H1			NC	No connection.
C2	IO	M	P4[1]		H2	IO	M	P5[3]	
C3	IO	M	P4[7]		H3	IO	M	P3[1]	
C4	IO	M	P2[7]		H4	IO	M	P1[5]	I2C Serial Data (SDA).
C5	IO	IO,M	P0[5]	Analog column mux input and column output.	H5	IO	M	P1[3]	
C6	IO	I,M	P0[6]	Analog column mux input.	H6	IO	M	P1[2]	
C7	IO	I,M	P0[0]	Analog column mux input.	H7	IO	M	P1[4]	Optional External Clock Input (EXTCLK).
C8	IO	I,M	P2[0]	Direct switched capacitor block input.	H8	IO	M	P3[2]	
C9	IO	M	P4[2]		H9	IO	M	P5[4]	
C10			NC	No connection.	H10	IO		P7[3]	
D1			NC	No connection.	J1	Power		Vss	Ground connection.
D2	IO	M	P3[7]		J2	Power		Vss	Ground connection.
D3	IO	M	P4[5]		J3	USB		D+	
D4	IO	M	P2[5]		J4	USB		D-	
D5	IO	IO,M	P0[3]	Analog column mux input and column output.	J5	Power		Vdd	Supply voltage.
D6	IO	I,M	P0[4]	Analog column mux input.	J6	IO		P7[7]	
D7	IO	M	P2[6]	External Voltage Reference (VREF) input.	J7	IO		P7[0]	
D8	IO	M	P4[6]		J8	IO	M	P5[2]	
D9	IO	M	P4[0]		J9	Power		Vss	Ground connection.
D10			NC	No connection.	J10	Power		Vss	Ground connection.
E1			NC	No connection.	K1	Power		Vss	Ground connection.
E2			NC	No connection.	K2	Power		Vss	Ground connection.
E3	IO	M	P4[3]		K3			NC	No connection.
E4	IO	I,M	P2[3]	Direct switched capacitor block input.	K4			NC	No connection.
E5	Power		Vss	Ground connection.	K5	Power		Vdd	Supply voltage.
E6	Power		Vss	Ground connection.	K6	IO		P7[6]	
E7	IO	M	P2[4]	External Analog Ground (AGND) input.	K7	IO		P7[5]	
E8	IO	M	P4[4]		K8	IO		P7[4]	
E9	IO	M	P3[6]		K9	Power		Vss	Ground connection.
E10			NC	No connection.	K10	Power		Vss	Ground connection.

LEGENDA = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No Connection.

Figure 6. CY8CTMA120 OCD (Not for Production)



BGA (Top View)

100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is the CY8CTMA120 On-Chip Debug (OCD) TrueTouch device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 4. 100-Pin Part Pinout (TQFP)

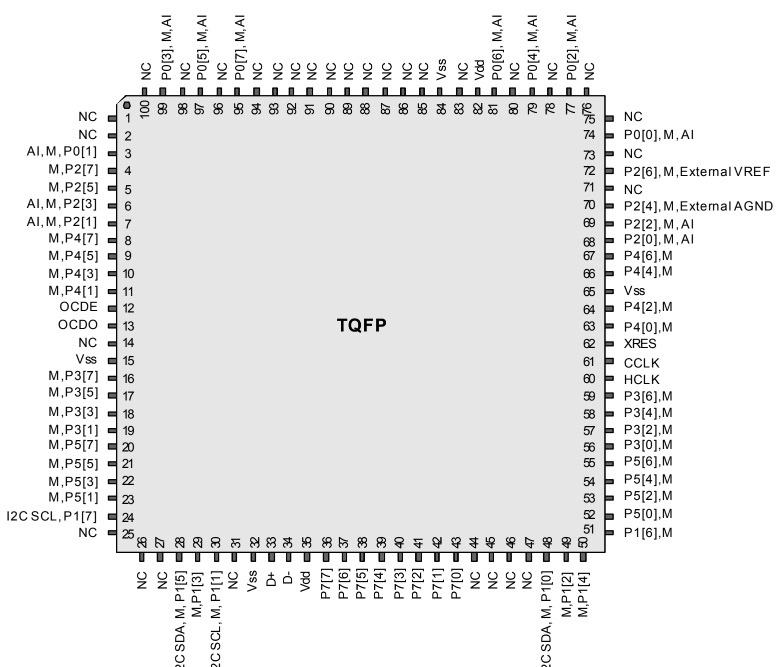
Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No connection. Leave floating.	51	IO	M	P1[6]	
2			NC	No connection. Leave floating.	52	IO	M	P5[0]	
3	IO	I, M	P0[1]	Analog column mux input.	53	IO	M	P5[2]	
4	IO	M	P2[7]		54	IO	M	P5[4]	
5	IO	M	P2[5]		55	IO	M	P5[6]	
6	IO	I, M	P2[3]	Direct switched capacitor block input.	56	IO	M	P3[0]	
7	IO	I, M	P2[1]	Direct switched capacitor block input.	57	IO	M	P3[2]	
8	IO	M	P4[7]		58	IO	M	P3[4]	
9	IO	M	P4[5]		59	IO	M	P3[6]	
10	IO	M	P4[3]		60			HCLK	OCD high speed clock output.
11	IO	M	P4[1]		61			CCLK	OCD CPU clock output.
12			OCDE	OCD even data IO.	62	Input		XRES	Active high pin reset with internal pull down.
13			OCDO	OCD odd data output.	63	IO	M	P4[0]	
14			NC	No connection. Leave floating.	64	IO	M	P4[2]	
15	Power		Vss	Ground. Connect to circuit ground.	65	Power		Vss	Ground. Connect to circuit ground.
16	IO	M	P3[7]		66	IO	M	P4[4]	
17	IO	M	P3[5]		67	IO	M	P4[6]	
18	IO	M	P3[3]		68	IO	I, M	P2[0]	Direct switched capacitor block input.
19	IO	M	P3[1]		69	IO	I, M	P2[2]	Direct switched capacitor block input.
20	IO	M	P5[7]		70	IO		P2[4]	External Analog Ground (AGND) input.
21	IO	M	P5[5]		71			NC	No connection. Leave floating.
Pin No.	**Digital**	**Analog**	**Name**	**Description**	**Pin No.**	**Digital**	**Analog**	**Name**	**Description**
22	IO	M	P5[3]		72	IO		P2[6]	External Voltage Reference (VREF) input.
23	IO	M	P5[1]		73			NC	No connection. Leave floating.
24	IO	M	P1[7]	I2C Serial Clock (SCL).	74	IO	I	P0[0]	Analog column mux input.
25			NC	No connection. Leave floating.	75			NC	No connection. Leave floating.

Table 4. 100-Pin Part Pinout (TQFP) *(continued)*

26			NC	No connection. Leave floating.	76			NC	No connection. Leave floating.
27			NC	No connection. Leave floating.	77	IO	I, M	P0[2]	Analog column mux input and column output.
28	IO		P1[5]	I2C Serial Data (SDA)	78			NC	No connection. Leave floating.
29	IO		P1[3]		79	IO	I, M	P0[4]	Analog column mux input and column output.
30	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP SCLK[3].	80			NC	No connection. Leave floating.
31			NC	No connection. Leave floating.	81	IO	I, M	P0[6]	Analog column mux input.
32	Power		Vss	Ground. Connect to circuit ground.	82	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.
33	USB		D+		83			NC	No connection. Leave floating.
34	USB		D-		84	Power		Vss	Ground. Connect to circuit ground.
35	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.	85			NC	No connection. Leave floating.
36	IO		P7[7]		86			NC	No connection. Leave floating.
37	IO		P7[6]		87			NC	No connection. Leave floating.
38	IO		P7[5]		88			NC	No connection. Leave floating.
39	IO		P7[4]		89			NC	No connection. Leave floating.
40	IO		P7[3]		90			NC	No connection. Leave floating.
41	IO		P7[2]		91			NC	No connection. Leave floating.
42	IO		P7[1]		92			NC	No connection. Leave floating.
43	IO		P7[0]		93			NC	No connection. Leave floating.
44			NC	No connection. Leave floating.	94			NC	No connection. Leave floating.
45			NC	No connection. Leave floating.	95	IO	I, M	P0[7]	Analog column mux input.
46			NC	No connection. Leave floating.	96			NC	No connection. Leave floating.
47			NC	No connection. Leave floating.	97	IO	IO, M	P0[5]	Analog column mux input and column output.
48	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP SDATA[3].	98			NC	No connection. Leave floating.
49	IO		P1[2]		99	IO	IO, M	P0[3]	Analog column mux input and column output.
50	IO		P1[4]	Optional External Clock Input (EXTCLK).	100			NC	No connection. Leave floating.

LEGENDA = Analog, I = Input, O = Output, NC = No Connection, M = Analog Mux Input, OCD = On-Chip Debugger.

Figure 7. CY8CTMA120 OCD (Not for Production)



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CTMA120 TrueTouch device family. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

Figure 8. Voltage versus CPU Frequency

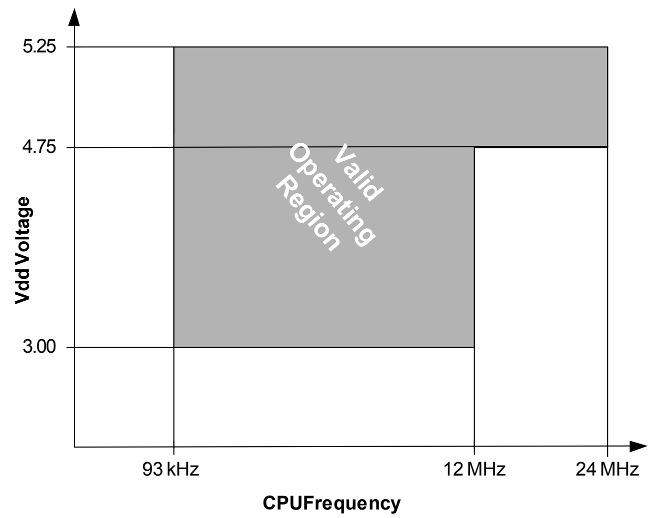


Table 5 lists the units of measure that are used in this section.

Table 5. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

[+] Feedback

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	^oC	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25^oC ± 25^oC. Extended duration storage temperatures above 65^oC degrades reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	^oC	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IO2}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage[4]	2000	–	–	V	Human Body Model ESD.
LU	Latch Up Current	–	–	200	mA	

Operating Temperature

Table 7. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature[5]	-40	–	+85	^oC	
T_{AUSB}	Ambient Temperature using USB	-10	–	+85	^oC	
T_J	Junction Temperature	-40	–	+100	^oC	The temperature rise from ambient to junction is package specific. See Thermal Impedance for the Package on page 32. The user must limit the power consumption to comply with this requirement.

Notes
4. See the user module data sheet for touchscreen application related ESD testing.
5. See the user module data sheet for touchscreen application related temperature testing.

DC Electrical Characteristics

The following electrical characteristics are for proper CPU core and IO operation. For capacitive touchscreen electrical characteristics, refer to the touchscreen user module data sheet.

DC Chip Level Specifications

Table 8 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 8. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 20 on page 21.
I_{DD5}	Supply Current, IMO = 24 MHz (5V)	–	14	27	mA	Conditions are Vdd = 5.0V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply Current, IMO = 24 MHz (3.3V)	–	8	14	mA	Conditions are Vdd = 3.3V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[6]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[6]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < T_A ≤ 85 °C, analog power = off.

DC General Purpose IO Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 9. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 200 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Full Speed USB Specifications

Table 10 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -10°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -10°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 10. DC Full-Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential Input Sensitivity	0.2	–	–	V	| (D+) - (D-) |
V_{CM}	Differential Input Common Mode Range	0.8	–	2.5	V	
V_{SE}	Single Ended Receiver Threshold	0.8	–	2.0	V	
C_{IN}	Transceiver Capacitance	–	–	20	pF	
I_{IO}	High-Z State Data Line Leakage	-10	–	10	μA	0V < V_{IN} < 3.3V.
R_{EXT}	External USB Series Resistor	23	–	25	W	In series with each USB pin.
V_{UOH}	Static Output High, Driven	2.8	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull up enabled.
V_{UOHI}	Static Output High, Idle	2.7	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull up enabled.
V_{UOL}	Static Output Low	–	–	0.3	V	15 kΩ ± 5% to Ground. Internal pull up enabled.
Z_O	USB Driver Output Impedance	28	–	44	W	Including R_{EXT} Resistor.
V_{CRS}	D+/D- Crossover Voltage	1.3	–	2.0	V	

Note
6. Standby current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This must be compared with devices that have similar

DC Operational Amplifier Specifications

Table 11 and Table 12 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 11. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	–	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 60 60 80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 μA μA μA μA μA μA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

Table 12. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5V Only	 – –	 1.65 1.32	 10 8	 mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 60 60 80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

DC Low Power Comparator Specifications

Table 13 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 13. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

DC IDAC Resolution

Table 14 lists IDAC typical resolution. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 14. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DAC}	Current output of 1 LSB (1x Setting)	-	75	-	nA	

DC Analog Output Buffer Specifications

Table 15 and Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 15. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	μV/°C	
V_{CMOB}	Common Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 0.6 0.6	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	53	64	–	dB	(0.5 x Vdd - 1.3) $\leq V_{OUT} \leq$ (Vdd - 2.3).

Table 16. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	34	64	–	dB	$(0.5 \times Vdd - 1.0) \leq V_{OUT} \leq (0.5 \times Vdd + 0.9)$.

DC Analog Reference Specifications

Table 17 and Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 17. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[7]	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[7]	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[7]	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[7]	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[7]	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[7]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V

Table 17. 5V DC Analog Reference Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

Table 18. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[7]	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[7]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[7]	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[7]	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[7]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

DC Analog PSoC Block Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 19. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

Note

7. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

DC POR and LVD Specifications

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register.

Table 20. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
 V_{PPOR0R} V_{PPOR1R} V_{PPOR2R}	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	 2.91 4.39 4.55	–	 V V V	
 V_{PPOR0} V_{PPOR1} V_{PPOR2}	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	 2.82 4.39 4.55	–	 V V V	
 V_{PH0} V_{PH1} V_{PH2}	PPOR Hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – – –	 92 0 0	 – – –	 mV mV mV	
 V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	 2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	 2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	 2.98[8] 3.08 3.20 4.08 4.57 4.74[9] 4.82 4.91	 V V V V V V V V	

Notes
8. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
9. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 21 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\le T_A \le$ 85°C, or 3.0V to 3.6V and -40°C $\le T_A \le$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 21. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[10]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note

10. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

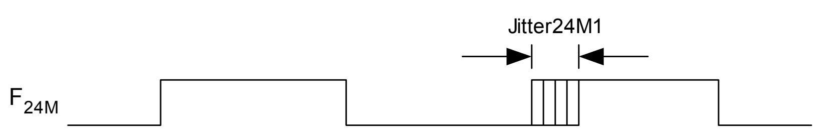
AC Chip Level Specifications

Table 22 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 22. AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[11,12]	MHz	Trimmed for 5V operation using factory trim values.
$F_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[12,13]	MHz	Trimmed for 3.3V operation using factory trim values.
$F_{IMOUSB5V}$	Internal Main Oscillator Frequency with USB (5V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[12]	MHz	-10°C ≤ T_A ≤ 85°C 4.35 ≤ Vdd ≤ 5.15
$F_{IMOUSB3V}$	Internal Main Oscillator Frequency with USB (3.3V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[12]	MHz	-0°C ≤ T_A ≤ 70°C 3.15 ≤ Vdd ≤ 3.45
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.96[11,12]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.96[12,13]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[11,12,14]	MHz	Refer to the AC Digital Block Specifications.
F_{BLK3}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[12, 14]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz Period Jitter	–	100		ns	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.08	48.0	49.92[11,13]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F_{MAX}	Maximum Frequency of signal on row input or row output.	–	–	12.96	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	μs	

Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram



Notes
11. 4.75V < Vdd < 5.25V.
12. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
13. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.

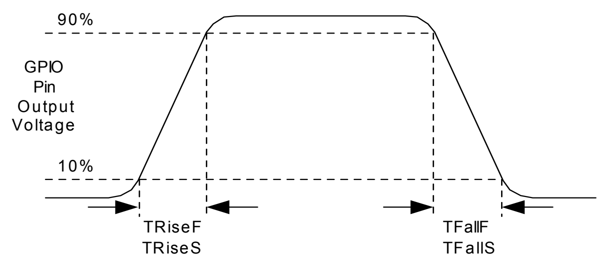
AC General Purpose IO Specifications

Table 23 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 23. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 10. GPIO Timing Diagram



AC Full Speed USB Specifications

Table 24 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -10°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -10°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 24. AC Full-Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RFS}	Transition Rise Time	4	–	20	ns	For 50 pF load.
T_{FSS}	Transition Fall Time	4	–	20	ns	For 50 pF load.
T_{RFMFS}	Rise/Fall Time Matching: (T_R/T_F)	90	–	111	%	For 50 pF load.
$T_{DRATEFS}$	Full Speed Data Rate	12 - 0.25%	12	12 + 0.25%	Mbps	

AC Operational Amplifier Specifications

Table 25 and Table 26 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 25. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 μs μs μs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 μs μs μs
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/μs V/μs V/μs
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/μs V/μs V/μs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 26. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 μs μs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 μs μs
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/μs V/μs
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/μs V/μs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

AC Low Power Comparator Specifications

Table 27 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, or 2.4V to 3.0V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 27. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

Table 28 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq$ 85°C, or 3.0V to 3.6V and -40°C $\leq T_A \leq$ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 28. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[15]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	25.92	MHz	
Counter	Enable Pulse Width	50[15]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	25.92	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[15]	–	–	ns	
	Disable Mode	50[15]	–	–	ns	
	Maximum Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[15]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

Note

15. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

Table 29 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 29. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency for USB Applications	23.94	24	24.06	MHz	
–	Duty Cycle	47	50	53	%	
–	Power up to IMO Switch	150	–	–	μs	

AC Analog Output Buffer Specifications

Table 30 and Table 31 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 30. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 2.5 2.5	 μs μs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 2.2 2.2	 μs μs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/μs V/μs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/μs V/μs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

Table 31. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 3.8 3.8	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 2.6 2.6	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100pF Load Power = Low Power = High	 0.7 0.7	 – –	 – –	 MHz MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100pF Load Power = Low Power = High	 200 200	 – –	 – –	 kHz kHz	

AC Programming Specifications

Table 32 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 32. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6

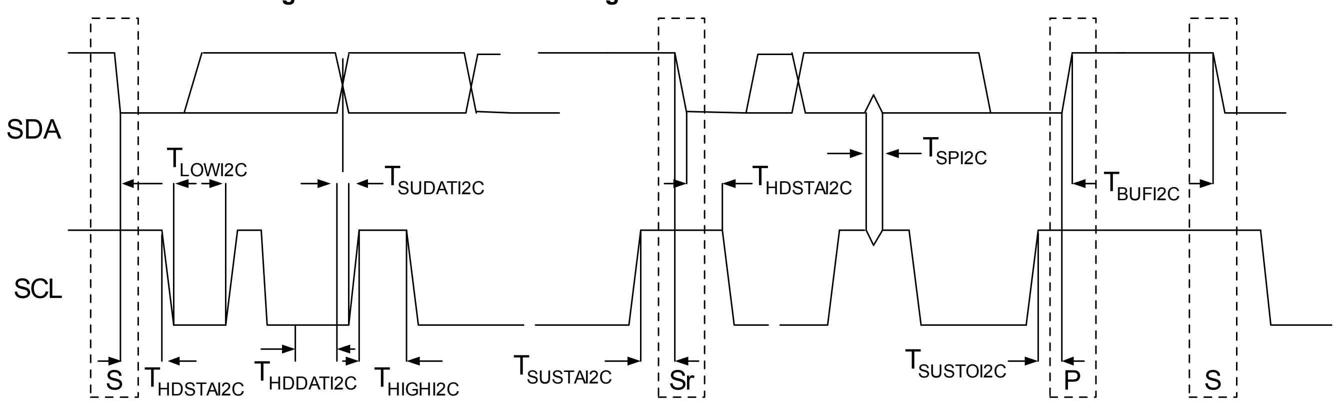
AC I²C Specifications

Table 33 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 33. AC Characteristics of the I²C SDA and SCL Pins for Vdd

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	μs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	μs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	μs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[16]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	μs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs	
T_{SPI2C}	Pulse Width of Spikes are Suppressed by the Input Filter.	–	–	0	50	ns	

Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

16. A fast-mode I2C-bus device is used in a standard mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I2C-bus specification) before the SCL line is released.

Package Dimensions

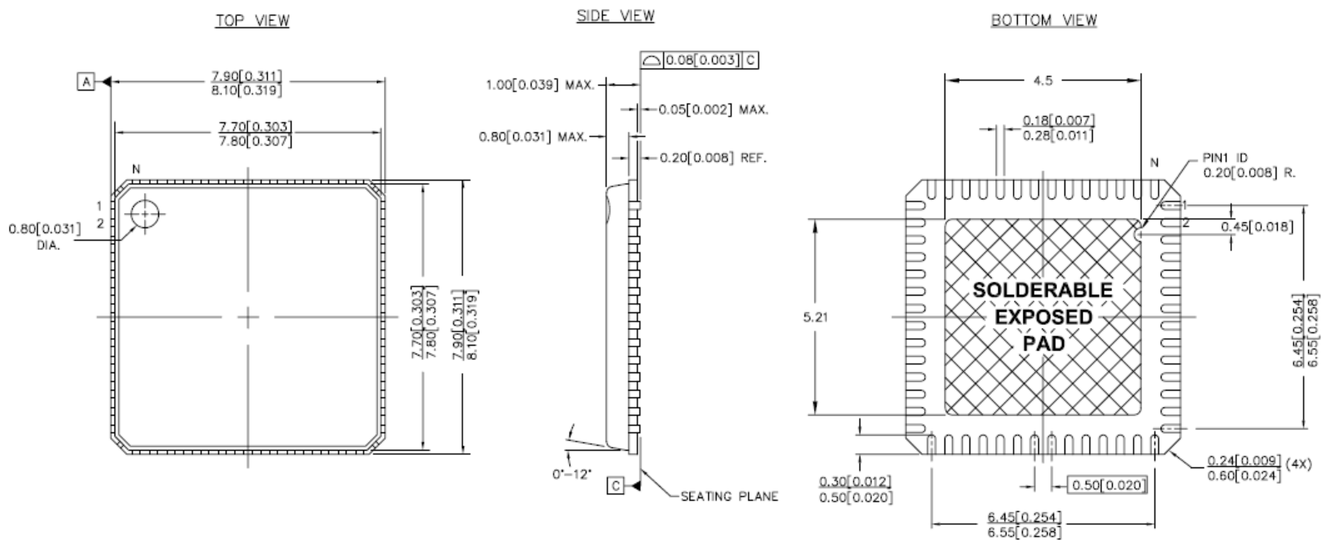
This section illustrates the package specification for the CY8CTMA120 TrueTouch devices along with the thermal impedance for the package and solder reflow peak temperatures.

It is important to note that emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Note Pinned vias for thermal conduction are not required for the low power PSoC device.

Figure 12. 56-Pin (8x8 mm) QFN



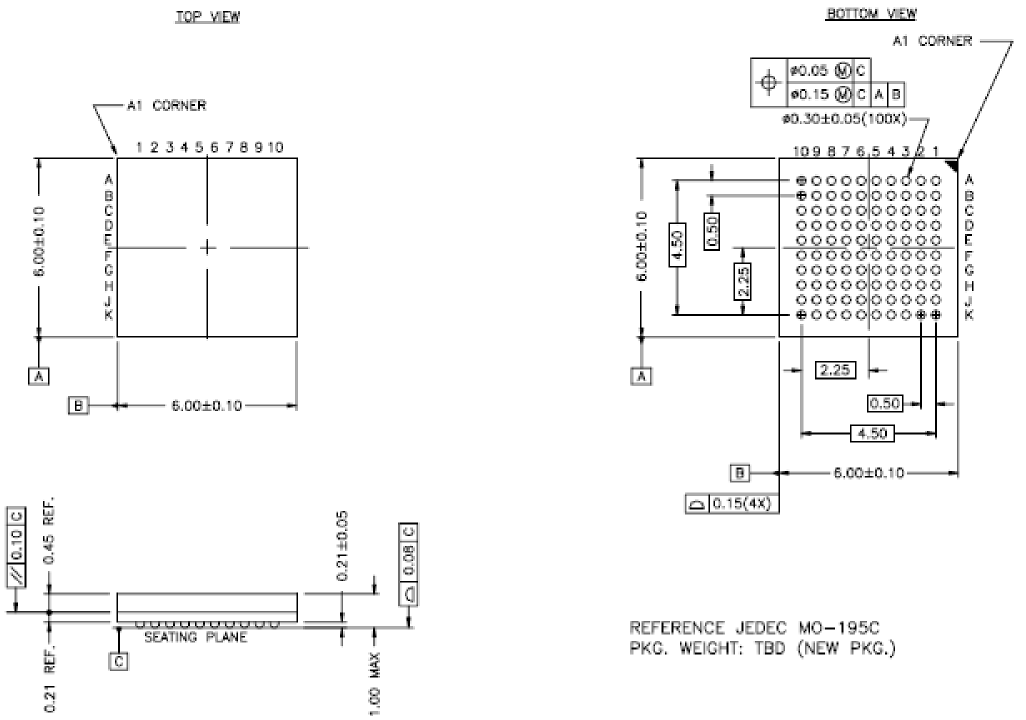
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF56A	STANDARD
LY56A	PB-FREE

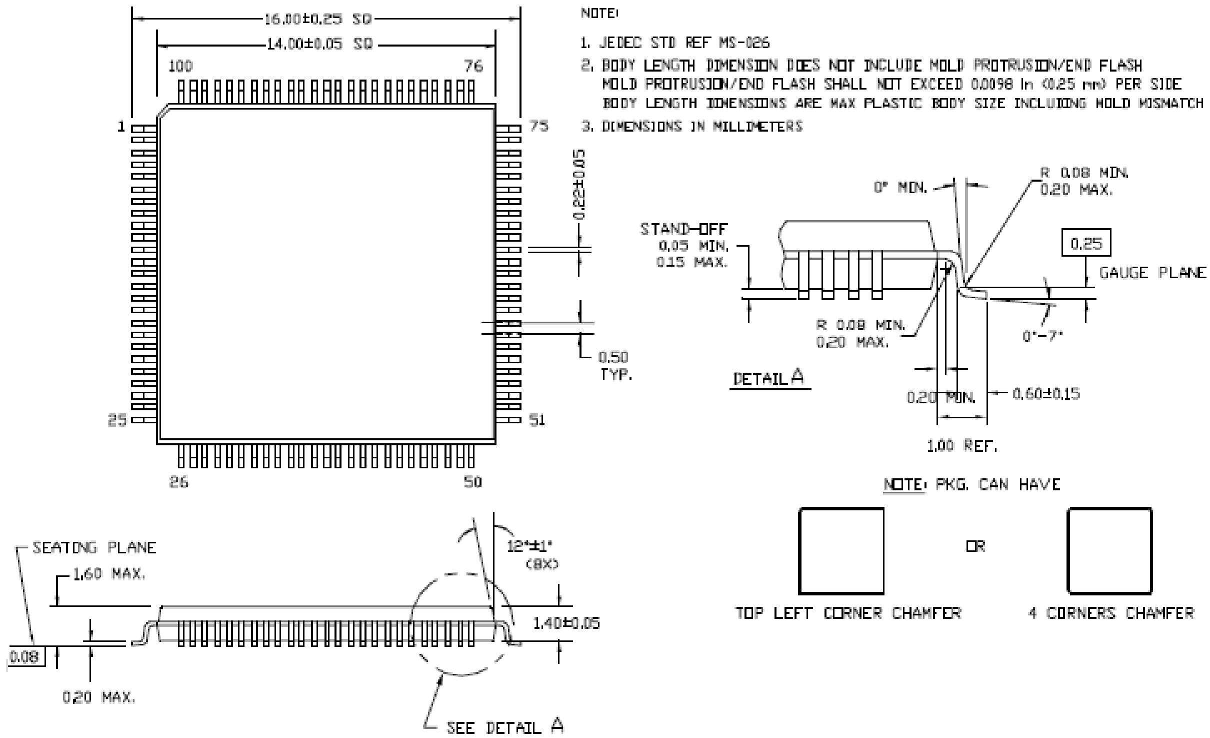
001-12921 **

Figure 13. 100-Ball (6X6 mm) VFBGA



51-85209 *B

Figure 14. 100-Pin (14x14x1.4 mm) TQFP



51-85048 *C

Thermal Impedance for the Package

Package	Typical θ_{JA} [17]
56 QFN[18]	12.93 °C/W
100 TQFP	51 °C/W
100 VFBGA	65 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature[19]	Maximum Peak Temperature
56 QFN	240°C	260°C
100 VFBGA	240°C	260°C

Notes

17. $T_J = T_A + \text{Power} \times \theta_{JA}$.
18. To achieve the thermal impedance specified for the ** package, the center thermal pad is soldered to the PCB ground plane.
19. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ± 5oC with Sn-Pb or 245 ± 5oC with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications

Development Tools

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. It is used by thousands of PSoC developers. This robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under Design Resources > Software and Drivers.

PSoC Programmer

PSoC Programmer is flexible enough to be used on the bench in development and suitable for factory programming. It works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express™. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Hi-Tech C Lite Compiler

Hi-Tech C Lite is an ANSI C compiler optimized for PSoC to deliver dense, efficient executable code for a smaller than ever footprint. Hi-Tech C Lite is available for download at http://www.cypress.htsoft.com. To install the HI-TECH Lite version, download the complier installation file from HI-TECH and choose the Lite option when prompted for a registration key. The Lite version can be upgraded to the 45-day full featured evaluation version or the PRO version at any time. However, the PRO version can only be enabled with a purchased registration key.

Hi-Tech C Pro Compiler

Hi-Tech C Pro is an optional upgrade to PSoC Designer that offers all the benefits of Hi-Tech C Lite with additional features. Hi-Tech C Pro is available for purchase either at the Cypress Online Store or at http://www.cypress.htsoft.com. Hi-Tech C Pro is recommended for touchscreen applications using the Multi-Touch All-Point CY8CTMA120 device.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Third Party Tools

Several tools are specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details for each of these tools are found at http://www.cypress.com under Design Resources > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on emulating a circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see application note AN2323 “Debugging - Build a PSoC Emulator into Your Board”.

Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Single-Touch Enabled	Multi-Touch Gesture Enabled	Multi-Touch All-Point Enabled	X/Y Sensor Inputs
56-Pin (8x8 mm) QFN	CY8CTMA120-56LFXI	16K	1K	-40C to +85C	Y	Y	Y	Up to 37
56-Pin (8x8 mm) QFN (Tape and Reel)	CY8CTMA120-56LFXIT	16K	1K	-40C to +85C	Y	Y	Y	Up to 37
100-Pin OCD TQFP	CY8CTMA120-00AXI	16K	1K	-40C to +85C	Y	Y	Y	Up to 37
100-Ball (6X6 mm) VFBGA	CY8C24994-24BVXI	16K	1K	-40C to +85C	Y	Y	Y	Up to 37

Ordering Code Definitions

CY 8 T MA XXX 56 XX

- XX — Package Type: .... Thermal Rating:
  - .... PX = PDIP Pb-Free C = Commercial
  - .... SX = SOIC Pb-Free I = Industrial
  - .... PVX = SSOP Pb-Free E = Extended
  - .... LFX/LKX = QFN Pb-Free
  - .... AX = TQFP Pb-Free
  - .... BVX = VFBGA Pb-Free
- 56 — Pin Count: 56-Pin
- XXX — Part Number
- MA — Family Code: TMA = Multi-Touch All-Point Touchscreen Controller
- T — Technology Code: C = CMOS
- 8 — Marketing Code: 8 = Cypress PSoC
- CY — Company ID: CY = Cypress

Document History Page

Document Title: CY8CTMA120 TrueTouch™ Multi-Touch All-Point Touchscreen Controller Document Number: 001-46901				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2518134	DSO/AESA	06/18/08	New data sheet
*A	2523303	DSO/PYRS	07/01/08	Updated X/Y sensor inputs to 38 and supported screen sizes to 7.3” and below
*B	2549257	YOM/PYRS	08/06/08	Added other sections based on PSoC data sheets
*C	2580296	KRY/AESA	10/07/08	Updated 56-Pin Part Pinout (QFN) table Added 100-Ball VFBGA Part Pinout Added 100-Ball (6X6 mm) VFBGA Package Diagram Updated Thermal Impedance and Solder Reflow Peak Temperature tables

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

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