8K x 8 Magnetic Nonvolatile CMOS RAM

Features

- **100% form-, fit-, and function-compatible with 8K × 8 micropower SRAM CY9C6264**
  - **Fast Read and Write access: 70 ns**
  - **Voltage range: 4.5V–5.5V operation**
  - **Low active power: 495 mW (max.)**
  - **Low standby power, CMOS: 825 µW (max.)**
  - **Data retention current: 0 µA at V_{CC} = 0V**
  - **Memory expansion with $\overline{CE1}$, CE2, and $\overline{OE}$ features**
  - **TTL-compatible inputs and outputs**
  - **Automatic power-down when deselected**
- **Replaces 8K × 8 battery backed (BB) SRAM, EEPROM, FeRAM, or Flash memory**
  - **Data is automatically protected during power loss**
  - **Write cycle endurance: >10^{15} Cycles**
  - **Data Retention: >10 Years**
  - **Shielded from external magnetic fields**
  - **Extra 16-bytes for device identification and tracking**
- **Optional industrial temperature range: –40°C to +85°C**
- **JEDEC STD 28-pin DIP (600-mil), 28-pin (300-mil) SOIC and TSOP packages**

Description

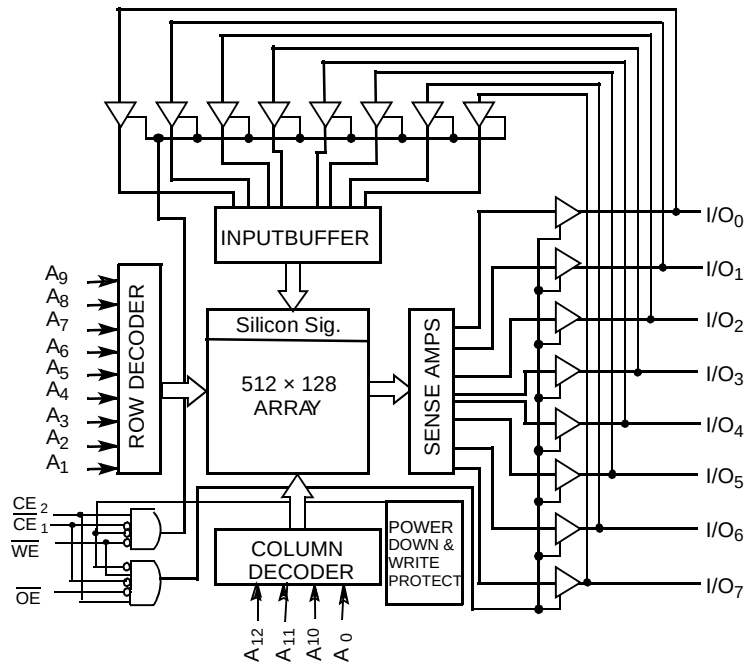
The CY9C6264 is a high-performance CMOS nonvolatile RAM employing an advanced magnetic RAM (MRAM) process. An MRAM is nonvolatile memory that operates as a RAM. It provides data retention for more than 10 years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM, EEPROM, Flash and FeRAM. Its fast writes and high write cycle endurance makes it superior to other types of nonvolatile memory.

The CY9C6264 operates very similar to other SRAM devices. Memory read and write cycles require equal times. The MRAM memory is nonvolatile due to its unique magnetic process. Unlike BBSRAM, the CY9C6264 is truly a monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the serious disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the CY9C6264 ideal for nonvolatile memory applications requiring frequent or rapid writes in a byte wide environment.

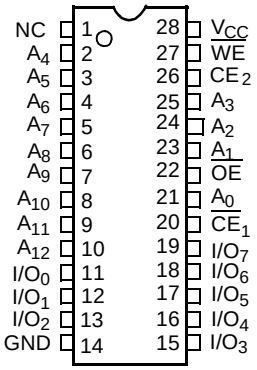
The CY9C6264 is offered in both commercial and industrial temperature ranges.

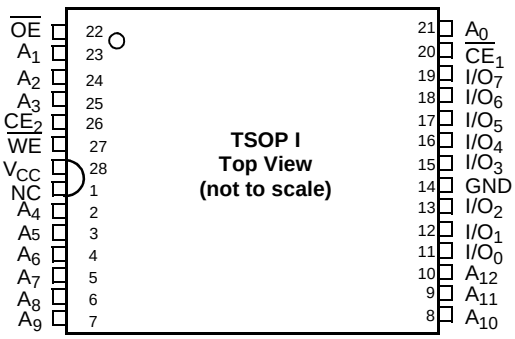
Logic Block Diagram



Pin Configurations

SOIC/DIP
Top View





TSOP I
Top View
(not to scale)

Overview

The CY9C6264 is a byte-wide MRAM memory. The memory array is logically organized as 8,192 × 8 and is accessed using an industry standard parallel asynchronous SRAM-like interface. The CY9C6264 is inherently nonvolatile and offers write protect during sudden power loss. Functional operation of the MRAM is similar to SRAM-type devices, otherwise.

Memory Architecture

Users access 8,192 memory locations each with eight data bits through a parallel interface. Internally, the memory array is organized into 1 block of 512 rows × 128 columns each.

The access and cycle time are the same for Read and Write memory operations. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

Memory Operation

The CY9C6264 is designed to operate in a manner similar to other bytewide memory products. For users familiar with BBSRAM, the MRAM performance is superior. For users familiar with EEPROM, Flash and FeRAM, the obvious differences result from higher write performance of MRAM technology and much higher write endurance.

All memory array bits are set to logic “1” at the time of shipment.

Read Operation

A read cycle begins whenever $\overline{WE}$ (Write Enable) is inactive (HIGH) and $\overline{CE_1}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active LOW while CE_2 active HIGH. The unique address specified by the 12 address inputs (A0–A12) defines which of the 8,192 bytes of data is to be accessed. Valid data will be available at the eight output pins within tAA (access time) after the last address input is stable, providing that $\overline{CE_1}$ or CE_2 and $\overline{OE}$ access times are also satisfied. If $\overline{CE_1}$ or CE_2 and $\overline{OE}$ access times are not satisfied, the data access must be measured from the later-occurring signal ($\overline{CE_1}$, CE_2 or $\overline{OE}$) and the limiting parameter is either t_{ACE1} for $\overline{CE_1}$, t_{ACE2} for CE_2, or t_{DOE} for the $\overline{OE}$ rather than address access.

Write Cycle

The CY9C6264 initiates a Write cycle whenever the $\overline{WE}$ and $\overline{CE_1}$ signals are active (LOW) or $\overline{WE}$ low and CE_2 HIGH, after address inputs are stable. The later occurring falling edge of $\overline{CE_1}$ (rising in case of CE_2) or $\overline{WE}$ will determine the start of the Write cycle. The Write cycle is terminated by the earlier rising edge of $\overline{CE_1}$ (falling edge in case of CE_2) or $\overline{WE}$. All address inputs must be kept valid throughout the Write cycle. The $\overline{OE}$ control signal should be kept inactive (HIGH) during Write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE_1}$ or CE_2 and $\overline{OE}$ active), $\overline{WE}$ will disable the outputs in t_{HZWE} from the $\overline{WE}$ falling edge.

Unlike other nonvolatile memory technologies, there is no Write delay with MRAM. The entire memory operation occurs in a single bus cycle. Therefore, any operation including Read or Write can occur immediately following a Write. Data Polling, a technique used with EEPROMs to determine if the Write is complete, is unnecessary. Page Write, a technique used to enhance EEPROM Write performance, is also unnecessary because of inherently fast Write cycle time for MRAM.

Write Inhibit and Data Retention Mode

This feature protects against the inadvertent Write. The CY9C6264 provides full functional capability for V_{CC} greater than 4.5V and Write-protects the device below 4.0V. Data is maintained in the absence of V_{CC}. During the power-up, normal operation can resume 20 µS after V_{PFD} is reached. Refer to page 8 for details.

Sudden Power Loss—“Brown out”

The nonvolatile RAM constantly monitors V_{CC}. Should the supply voltage decay below the operating range, the CY9C6264 automatically write-protects itself, all inputs become “don’t care,” and all outputs become high impedance. Refer to page 8 for details.

Silicon Signature/Device ID

An extra 16 bytes of MRAM are available to the user for Device ID. By raising A7 to V_{CC} + 2.0V and by using address locations 00 (Hex) to F (Hex) on address pins A12, A11, A10, and A0 (MSB to LSB) respectively, the additional bytes may be accessed in the same manner as the regular memory array with 140-ns access time. Dropping A7 from input high (V_{CC} + 2.0V) to $\leq$ V_{CC} + 0.5V max. returns the device to normal operation after 140-ns delay.

Address (MSB to LSB) A12 A11 A10 A0	Description	ID
00h	Manufacturer ID	34h
01h	Device ID	41h
02h–Fh	User Space	14 bytes

User Space bits are set to logic “1” at the time of shipment.

Magnetic Shielding

CY9C6264 is protected from external magnetic fields through the application of a “magnetic shield” that covers the entire memory device.

Applications

Battery-backed SRAM (BBSRAM) Replacement

CY9C6264 is designed to replace (plug and play) existing BBSRAM while eliminating the need for battery and V_{CC} monitor IC, reducing cost and board space and improving system reliability.

The cost associated with multiple components, assemblies, and manufacturing overhead associated with battery-backed SRAM is eliminated by using monolithic MRAM. CY9C6264 eliminates multiple assemblies, connectors, modules, field maintenance, and environmental issues common with BB SRAM. MRAM is a true nonvolatile RAM with high performance, high endurance, and data retention.

Battery-backed SRAMs are forced to monitor V_{CC} in order to switch to the backup battery. Users that are modifying existing designs to use MRAM in place of BBSRAM, can eliminate the V_{CC} controller IC along with the battery. MRAM performs this function on-chip.

Cost

The cost of both the component and manufacturing overhead of battery-backed SRAM is high. In addition, there is a built-in rework step required for battery attachment in case of surface

mount assembly. This can be eliminated with MRAM. In the case of DIP battery-backed modules, the assembly techniques are constrained to through-hole assembly and board wash using no water.

System Reliability

Battery-backed SRAM is inherently vulnerable to shock and vibration. In addition, a negative voltage on any pin of a battery-backed SRAM, even a momentary undershoot, can cause data loss. The negative voltage causes current to be drawn directly from the battery, weakens the battery, and reduces its capacity over time. In general, there is no way to monitor the lost battery capacity. MRAM guarantees reliable operation across the voltage range with inherent nonvolatility.

Space

Battery-backed SRAM in DIP modules takes up board space height and dictates through-hole assembly. MRAM is offered in surface mount packages.

Field Maintenance

Batteries must eventually be replaced, which creates an inherent maintenance problem. Despite projections of long life, it is difficult to know how long a battery will last, considering all the factors that degrade them.

Environmental

Lithium batteries are a potential disposal burden and are considered a fire hazard. MRAM eliminates all such issues through a truly monolithic nonvolatile solution.

Users replacing battery-backed SRAMs with an integrated Real-time Clock (RTC) in the same package may need to move the RTC function to a different location within the system.

EEPROM Replacement

CY9C6264 can also replace EEPROM in current applications. CY9C6264 is pinout- and functionally-compatible to byte-wide EEPROM, but it does not need data-bar polling, page Write, and hardware Write protect due to its fast Write and inadvertent Write-protect features.

Users replacing EEPROMs with MRAM can eliminate the page mode operation and simplify to standard asynchronous write. Additionally, data-bar polling can be eliminated, since every byte Write is completed within same cycle. All Writes are completed within 70 ns.

FeRAM Replacement

FeRAM requires addresses to be latched on falling edge of $\overline{CE}$, which adds to system overhead in managing the $\overline{CE}$ and latching function. MRAM eliminates this overhead by offering a simple asynchronous SRAM interface.

Users replacing FeRAM can simplify their address decoding since you do not need to drive $\overline{CE}$ active and then inactive for each address. This overhead is eliminated when using MRAM.

Secondly, MRAM Read is nondestructive and no precharge cycle is required like the one used with FeRAM.This has no apparent impact to the design, but the Read cycle time can now see immediate improvement equal to the precharge time.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–40°C to +85°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[1].....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1].....–0.5V to V_{CC} + 0.5V except in case of super voltage pin (A7) while accessing 16 device ID and silicon signature bytes.....–0.5V to V_{CC} + 2.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

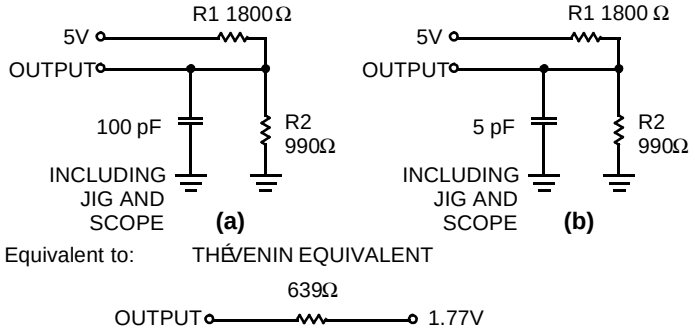
Electrical Characteristics Over the Operating Range

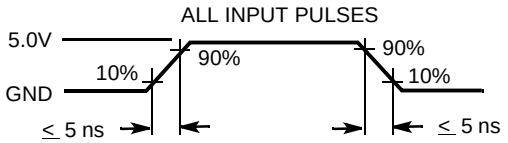
Parameter	Description	Test Conditions	CY9C62256-70			Unit
			Min.	Typ.[3]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage		2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		–0.5[1]		0.8	V
I_{IX}[2]	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–0.5		+0.5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–0.5		+0.5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			90	mA
I_{SB1}	Automatic CE Power-down Current— TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			600	µA
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V or CE_2 ≤ 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0			150	µA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms





Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Iix during access to 16 device ID and silicon signature bytes with super voltage pin at V_{CC} + 2.0V will be 100 µA maxV_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
3. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5]

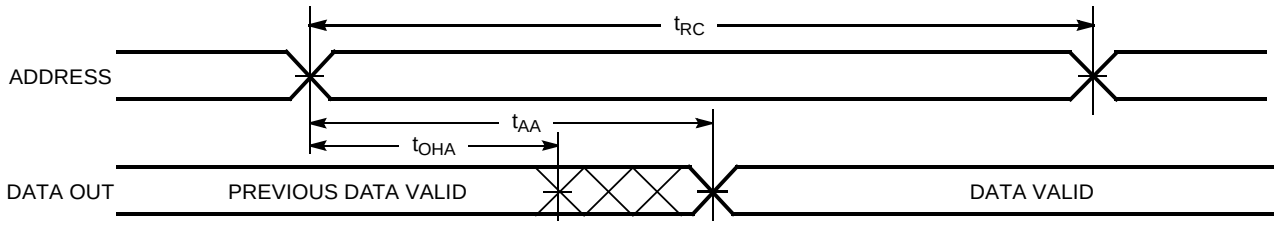
Parameter	Description	CY9C6264-70		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		70	ns
t_{ACE2}	CE_2 HIGH to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[6]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		25	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low-Z[6]	5		ns
t_{LZCE2}	CE_2 HIGH to Low-Z [6]	5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High-Z[6, 7] CE_2 LOW to High-Z [6, 7]		25	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-up CE_2 HIGH to Power-up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-down CE_2 LOW to Power-down		70	ns
Write Cycle[8, 9]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	60		ns
t_{SCE2}	CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	5		ns

Notes:

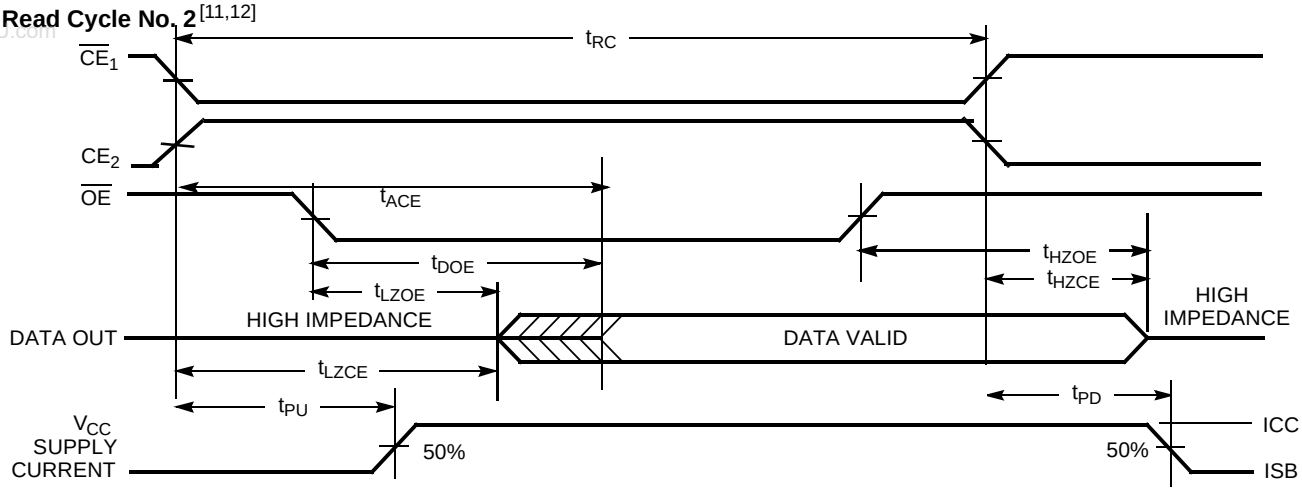
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE1} is less than t_{LZCE1}, t_{HZCE2} is less than t_{LZCE2}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal Write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW or CE_2 HIGH and $\overline{WE}$ LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the Write.
9. The minimum write pulse width for Write cycle #3 ($\overline{WE}$-controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

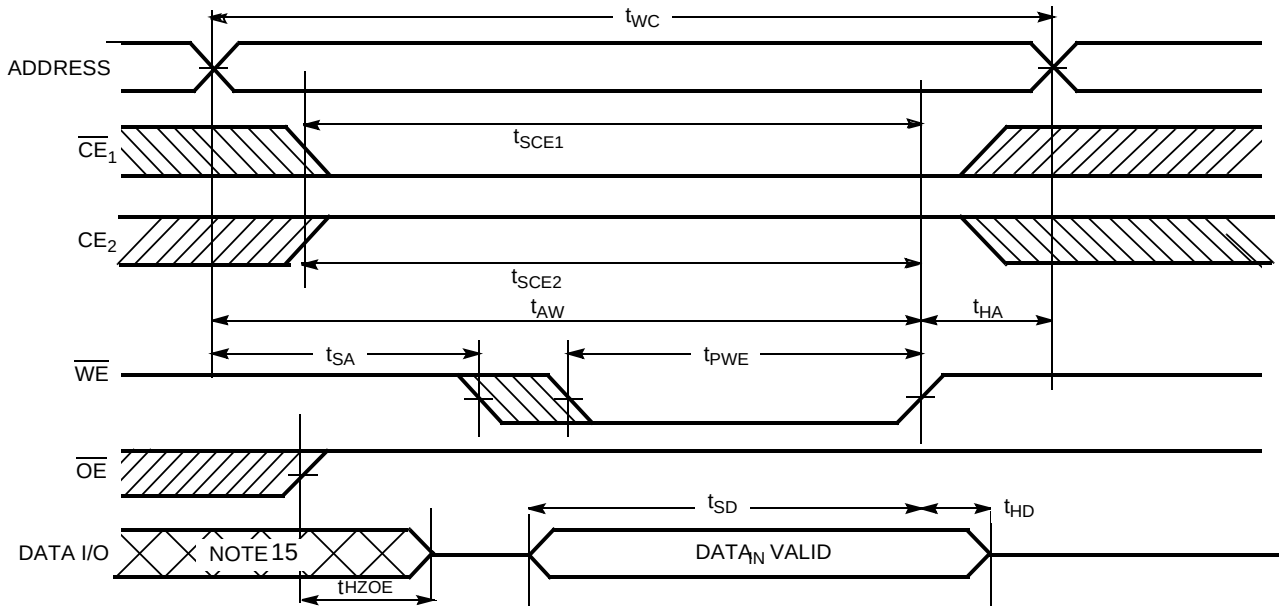
Read Cycle No. 1 [10, 11]



Read Cycle No. 2 [11,12]



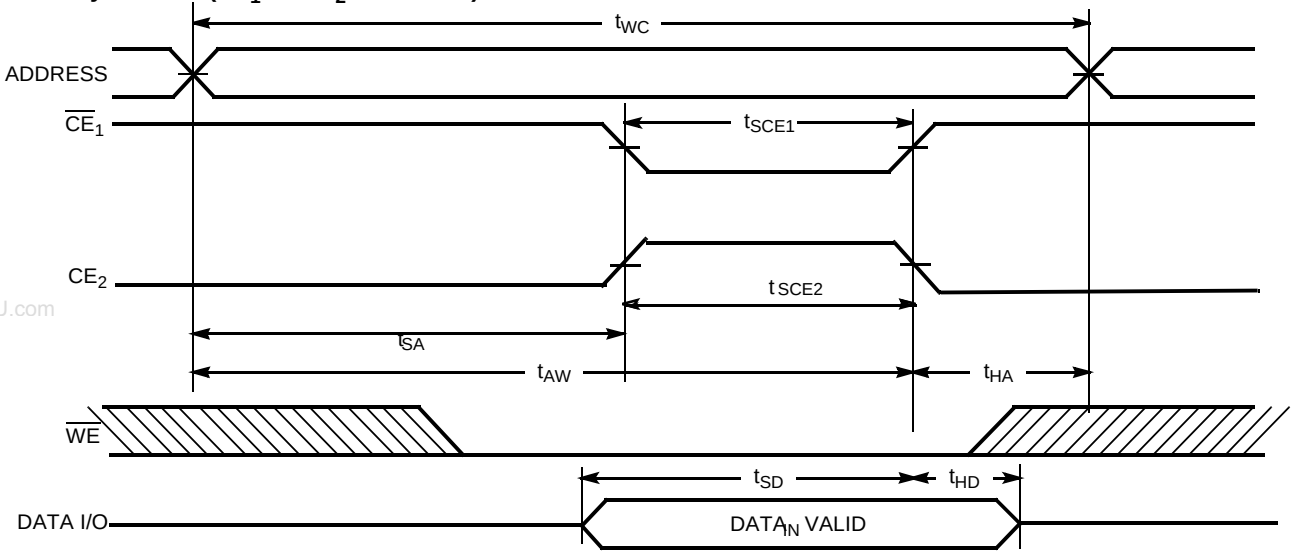
Write Cycle No. 1 ($\overline{WE}$ Controlled) [8,13,14]



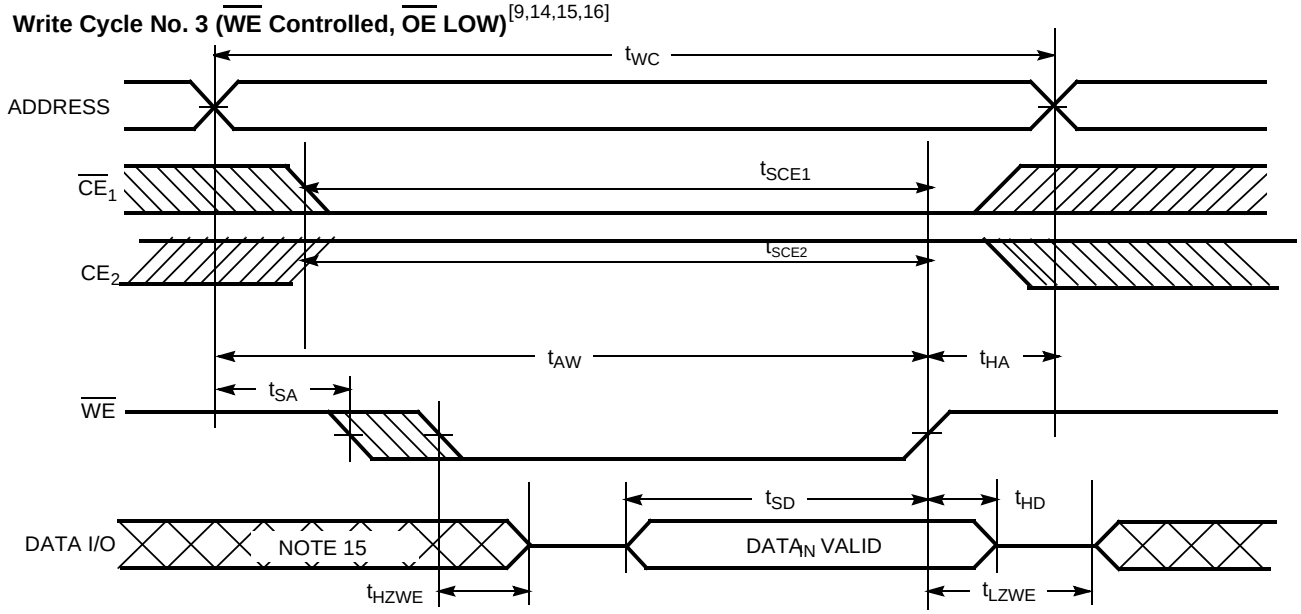
10. Device is continuously selected. $\overline{OE} = V_{IL}$ $\overline{CE_1} = V_{iL}$ Or $\overline{OE} = V_{IL}$ $CE_2 = V_{IH}$.
11. $\overline{WE}$ is HIGH for Read cycle.
12. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW Or CE_2 transition to HIGH.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE_1}$ Or CE_2 Controlled)[8,13,14]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9,14,15,16]



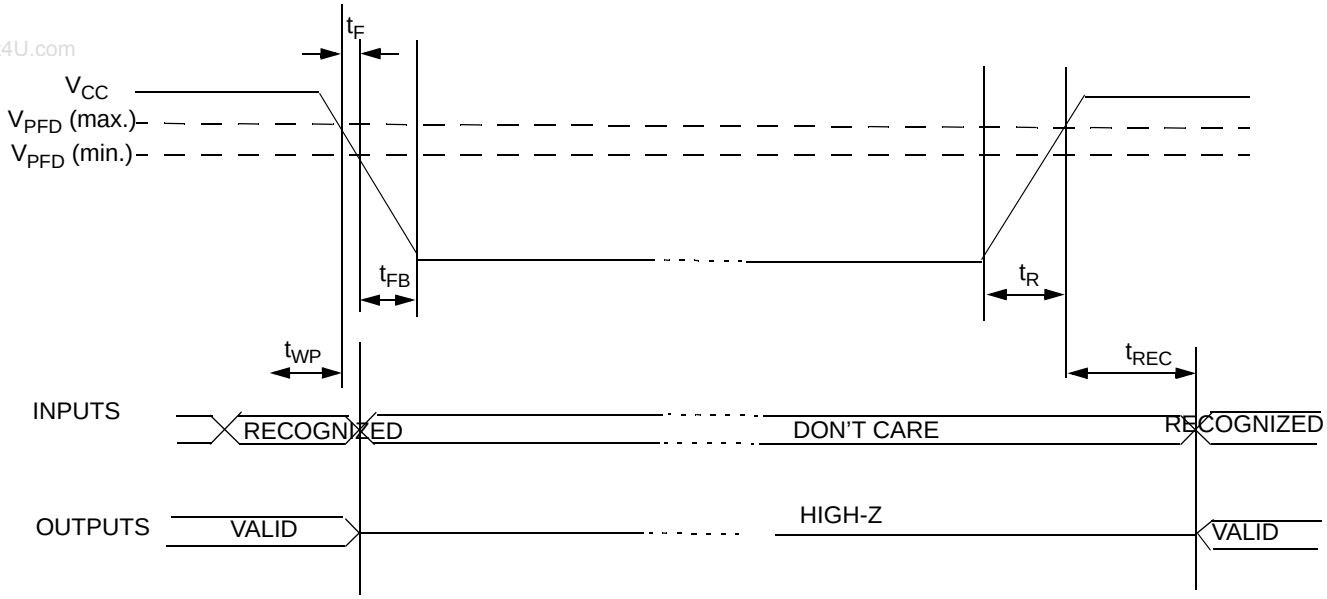
Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	V_{CC}	Inputs/Outputs	Mode	Power
H	L	X	X	4.5–5.5V	High-Z	Deselect/Power-down	Standby (I_{SB})
H	H	X	X	4.5–5.5V	High-Z	Deselect/Power-down	Standby (I_{SB})
L	L	X	X	4.5–5.5V	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	4.5–5.5V	Data Out	Read	Active (I_{CC})
L	H	L	X	4.5–5.5V	Data In	Write	Active (I_{CC})
L	H	H	H	4.5–5.5V	High-Z	Deselect, Output Disabled	Active (I_{CC})
X	X	X	X	< 4.0V	Inputs = X, Outputs = High-Z	Write Inhibit	Active (I_{CC})

Note:
16. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the outputs remain in high-impedance state.

Power-down/Power-up Mode AC Waveforms

Parameter	Description	Min.	Typ.	Max.	Unit
V_{PFD}	Power-fail Deselect Voltage	4.0	4.25	4.5	V
t_F [17]	V_{PFD} (max.) to V_{PFD} (min.) Vcc Fall Time	100			µs
t_{FB}	V_{PFD} (min.) to V_{SS} Vcc Fall Time	50			µs
t_R	V_{SS} to V_{PFD} (max.) Rise Time	20			µs
t_{WP}	Write Protect Time On V_{CC} = V_{PFD}			20	µs
t_{REC}	V_{PFD} (max.) to Inputs Recognized			20	µs



Note:

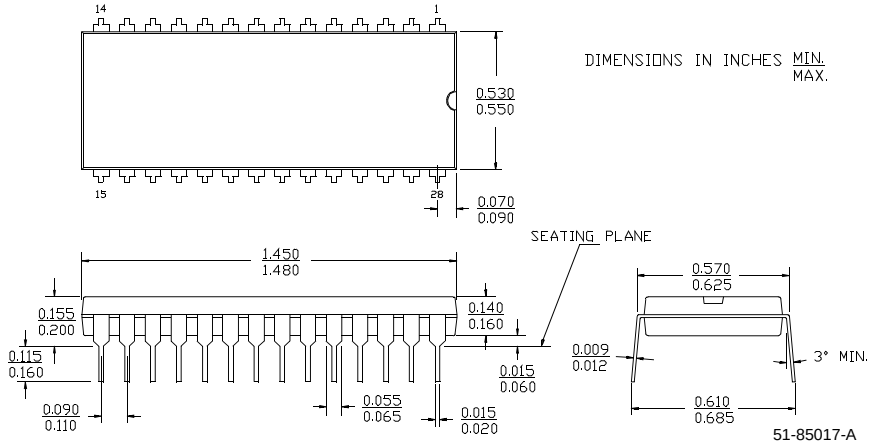
17. 16. V_{PFD} (max.) to V_{PFD} (min.) fall time of less than t_F may result in deselection/write protection not occurring until 20 µs after V_{CC} passes V_{PFD} (min.).

Ordering Information

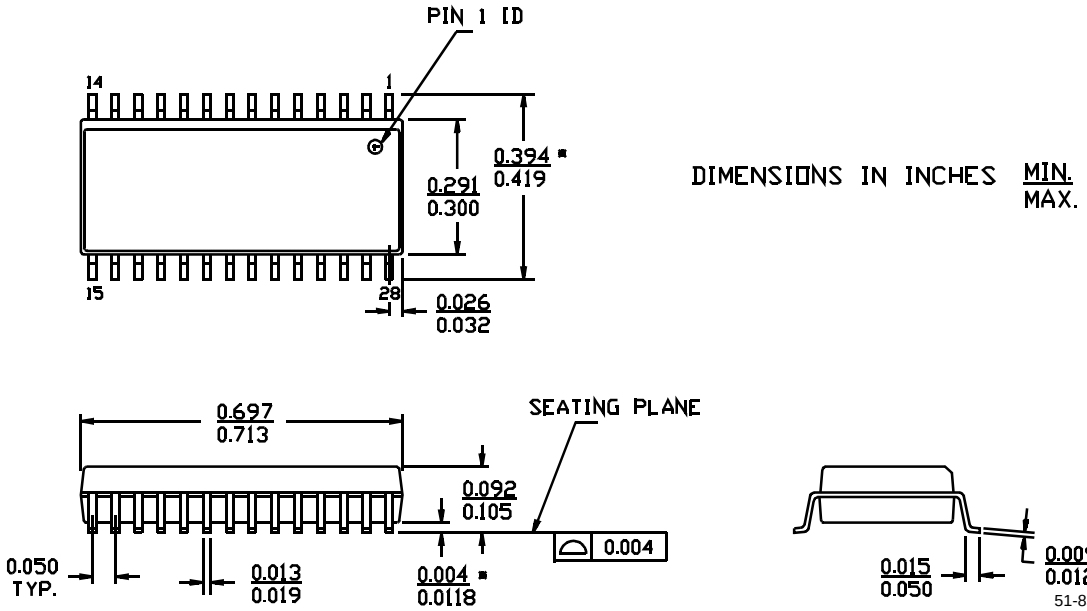
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY9C6264–70SC	S21	28-pin (300-mil) Molded SOIC	Commercial
	CY9C6264-70SI	S21	28-pin (300-mil) Molded SOIC	Industrial
	CY9C6264–70ZC	Z28	28-pin Thin Small Outline Package	Commercial
	CY9C6264–70ZI	Z28	28-pin Thin Small Outline Package	Industrial
	CY9C6264–70PC	P15	28-pin (600-mil) Molded DIP	Commercial
	CY9C6264-70PI	P15	28-pin (600-mil) Molded DIP	Industrial

Package Diagrams

28-pin (600-Mil) Molded DIP P15

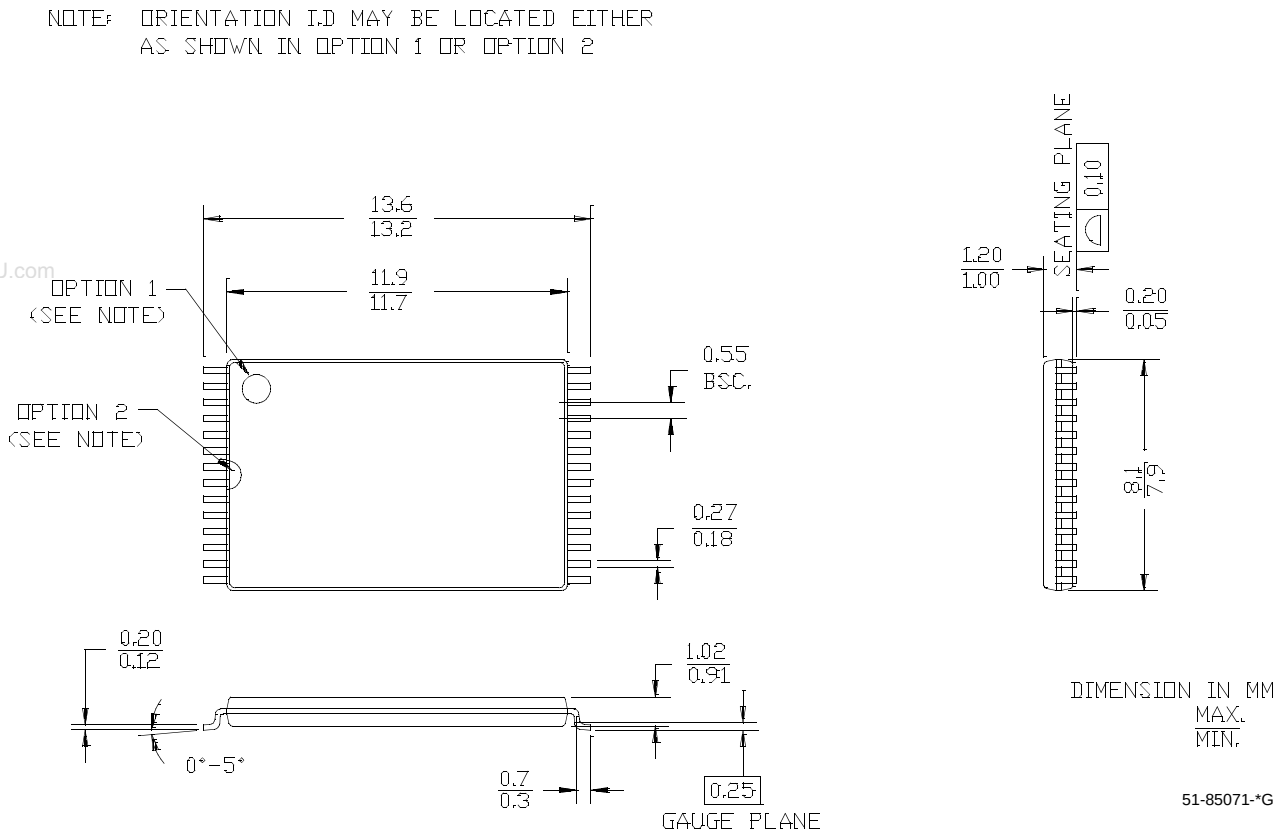


28-pin (300-mil) Molded SOIC S21



Package Diagrams (continued)

28-pin Thin Small Outline Package Type 1 (8 × 13.4 mm) Z28



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Document Title: CY9C6264 8K x 8 Magnetic Nonvolatile CMOS RAM Document Number: 38-15003				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116317	06/11/02	NBP	New Data Sheet
*A	116771	07/25/02	NBP	Add state of memory bits at the time of shipment