CYBT-3330xx-02

EZ-BT™ WICED® Module

General Description

The CYBT-3330xx-02 is a fully integrated Bluetooth® Smart Ready wireless module. The CYBT-3330xx-02 includes an onboard crystal oscillator, passive components, flash memory, and the Cypress CYW20706 silicon device. Refer to the CYW20706 datasheet for additional details on the capabilities of the silicon device used in this module.

The CYBT-3330xx-02 supports peripheral functions (ADC and PWM), UART, I2C, and SPI communication, and a PCM/I2S audio interface. The CYBT-3330xx-02 includes a royalty-free Bluetooth stack compatible with Bluetooth 5.0 in a 12.0 × 13.5 × 1.95 mm package.

The CYBT-3330xx-02 includes 512 KB of onboard serial flash memory and is designed for standalone operation. The CYBT-3330xx-02 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYBT-3330xx-02 is offered in two certified versions. The CYBT-333032-02 supports an external antenna through an RF solder pad output. The CYBT-333047-02 supports an external antenna via a u-FL connector.

Module Description

- Module size: 12.00 mm × 13.50 mm × 1.95 mm
- Bluetooth 5.0 Qualified Smart Ready module
  - QDID: 131625
  - Declaration ID: D041935
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 512-KB on-module serial flash memory
- Up to 11 GPIOs
- Temperature range: –30 °C to +85 °C
- Arm® Cortex®-M3 32-bit processor
- Maximum TX output power
  - +12 dbm for Bluetooth Classic
  - +9 dBm for Bluetooth Low Energy
    - BLE connection range of up to 250 meters at 9 dBm[1]
- RX Receive Sensitivity:
  - Bluetooth Classic:
    - –93.5 dBm at 1 Mbps, GFSK
    - –95.5 dBm at 2 Mbps, π/4-DQPSK
    - –89.5 dBm at 3 Mbps, 8-DPSK
  - –96.5 dBm for Bluetooth Low Energy

Power Consumption

- Enhanced Data Rate (EDR) at 8 dBm
  - Peak TX current: 52.5 mA
  - Peak RX current consumption: 26.4 mA
- Bluetooth Low Energy (BLE) at 0 dBm
  - 1-second interval BLE ADV average current consumption: 315 µA
- Low power mode support
  - Deep Sleep: 2.69 µA

Functional Capabilities

- Σ-Δ ADC for audio (12 bits) and DC measurement (10 bits)
- Serial Communications Interface compatible with I^2C slaves
- SPI support for both master and slave modes
- HCI interface through UART
- PCM/I2S Audio interface
- Two-wire Global Coexistence Interface (GCI)
- Integrated peripherals such as PWM, ADC
- Programmable output power control
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Bluetooth wideband speech support

Benefits

CYBT-3330xx-02 provides all necessary components required to operate BLE and/or BR/EDR communication standards.

- Proven hardware design ready to use
- Dual-mode operation eliminates the need for multiple modules
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation and Over-the-air (OTA) updates
- Bluetooth SIG Listed with QDID and Declaration ID
- Fully certified module eliminates the time needed for design, development and certification processes
- WICED® STUDIO provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a Bluetooth application

Note

1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +9.0 dBm. Actual range will vary based on end product design, environment, receive sensitity and transmit output power of the central deivce.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: EZ-BLE/BT Module Portfolio, Module Roadmap
- CYW20706 BT Silicon Datasheet
- Development Kits:
  - CYBT-333047-EVAL, CYBT-3330xx-02 Evaluation Board
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Files for EZ-BLE/EZ-BT Modules
  - KBA223428 - Programming an EZ-BT WICED Module

Development Environment

Wireless Connectivity for Embedded Devices (WICED) Studio Software Development Kit (SDK)

Cypress' WICED® (Wireless Connectivity for Embedded Devices) is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth® connectivity in system design.

WICED Studio is the only SDK for the Internet of Things (IoT) that combines Wi-Fi and Bluetooth into a single integrated development environment. In addition to providing WICED APIs and an application framework designed to abstract complexity, WICED Studio also leverages many common industry standards.

Technical Support

- Cypress Community: Whether you're a customer, partner or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share and engage with both Cypress experts and other embedded engineers around the world.
- Frequently Asked Questions (FAQs): Learn more about our Bluetooth ecosystem.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

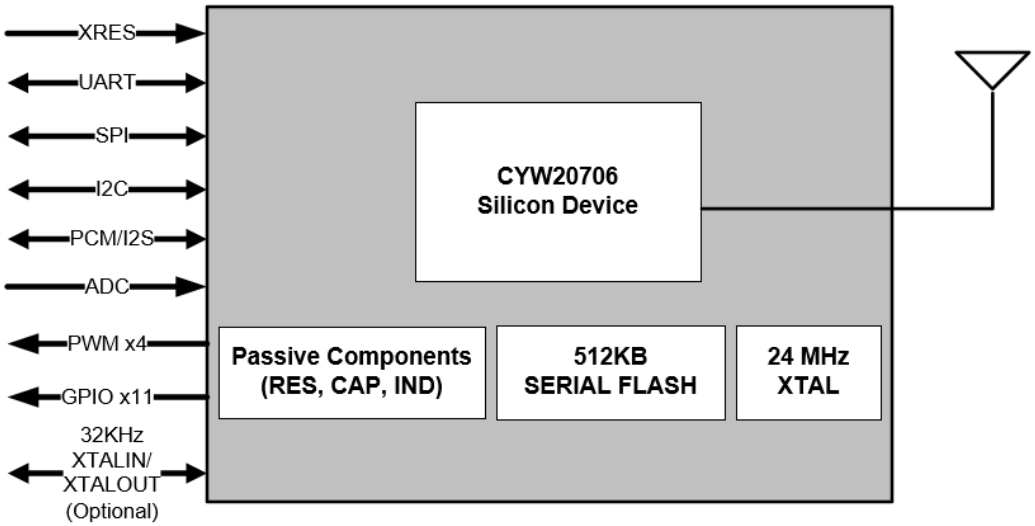
Contents

Overview

Functional Block Diagram

Figure 1 illustrates the CYBT-3330xx-02 functional block diagram.

Figure 1. Functional Block Diagram



Module Description

The CYBT-3330xx-02 module is a complete module designed to be soldered to the application's main board.

Module Dimensions and Drawing

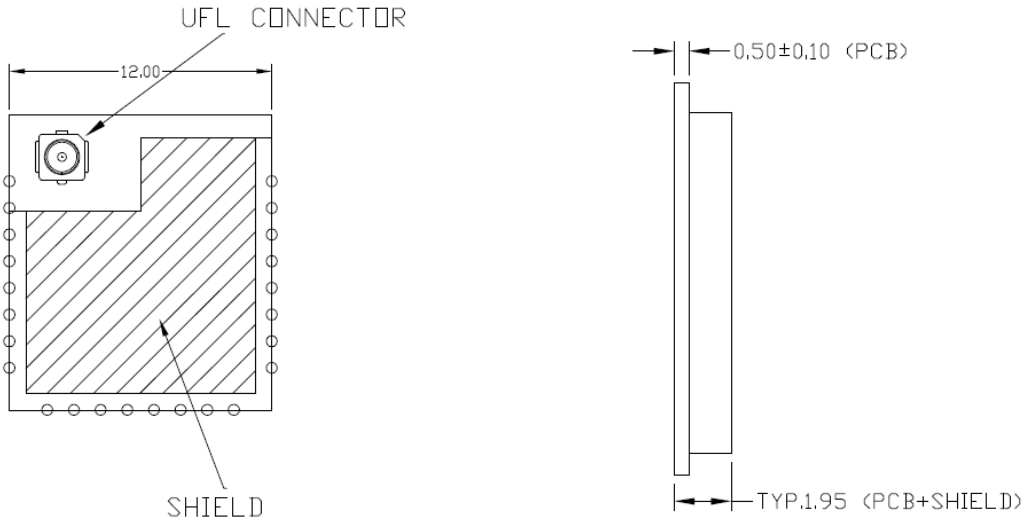
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	12.00 ± 0.15 mm
	Width (Y)	13.50 ± 0.15 mm
PCB thickness	Height (H)	0.50 ± 0.05 mm
Shield height	Height (H)	1.45 mm typical
Maximum component height	Height (H)	1.45 mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.95 mm typical

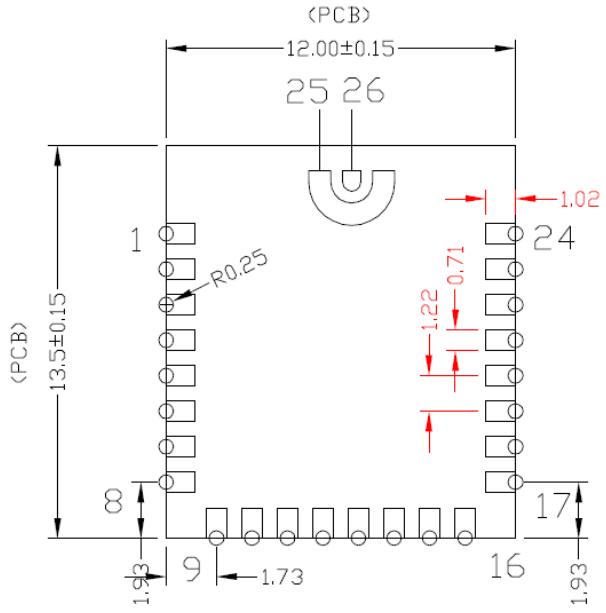
See Figure 2 for the mechanical reference drawing for CYBT-3330xx-02.

Figure 2. Module Mechanical Drawing



Top View (Seen from Top)

Side View



Bottom View (Seen from Bottom)

PAD1:P0/P34
PAD2:I2C_SCL
PAD3:XRES
PAD4:I2C_SDA
PAD5:P2/P37/P28
PAD6:SPI2_CS_N
PAD7:GND
PAD8:SPI2_MISO
PAD9:SPI2_MOSI
PAD10:SPI2_CLK
PAD11:GPIO_0
PAD12:GPIO_1
PAD13:GND
PAD14:GPIO_4
PAD15:P4/P24
PAD16:UART_TXD
PAD17:UART_CTS
PAD18:UART_RTS
PAD19:GPIO_7
PAD20:UART_RXD
PAD21:VDDIN
PAD22:GPIO_3
PAD23:GPIO_6
PAD24:GND
PAD25:GND-for 333032 only
PAD26:ANT-for 333032 only

Notes

2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.
3. The CYBT-3330xx-02 includes castellated pad connections, denoted as the circular openings at the pad location above.

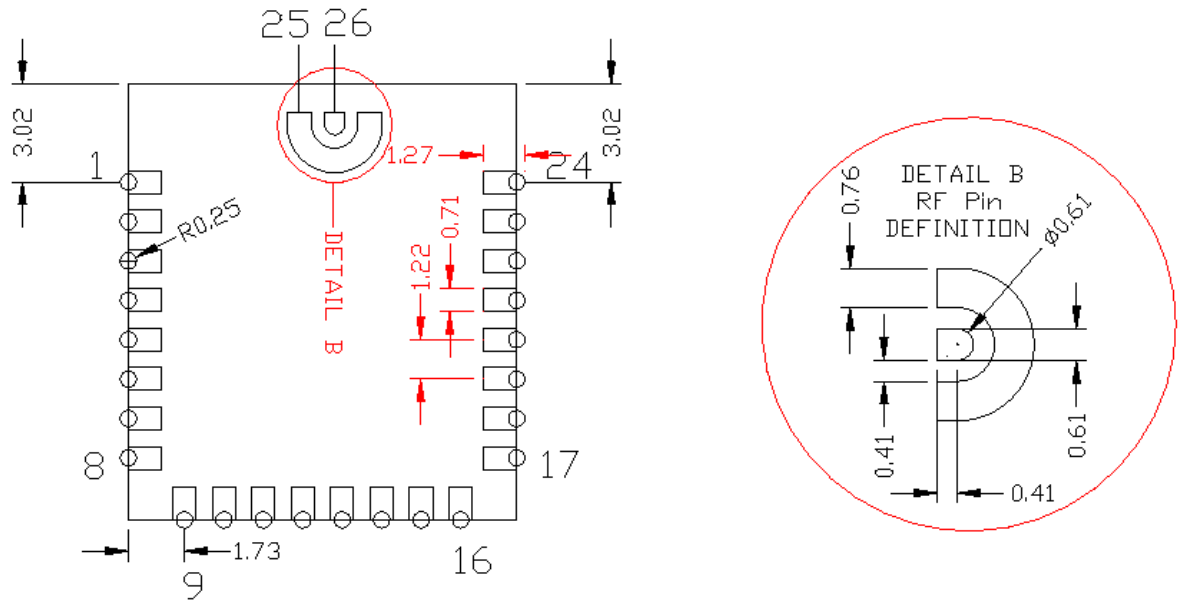
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBT-3330xx-02 connects to the host board via solder pads on the backside of the module. Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBT-3330xx-02 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	26	Solder Pads	1.27 mm	0.71 mm	1.22 mm

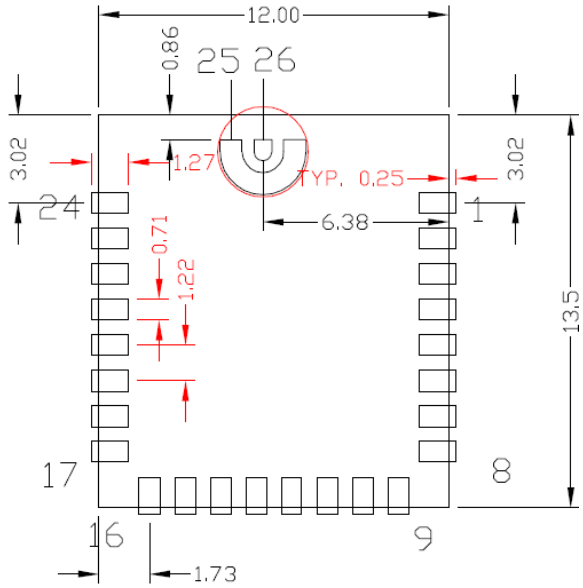
Figure 3. Solder Pad Dimensions (Seen from Bottom)



Recommended Host PCB Layout

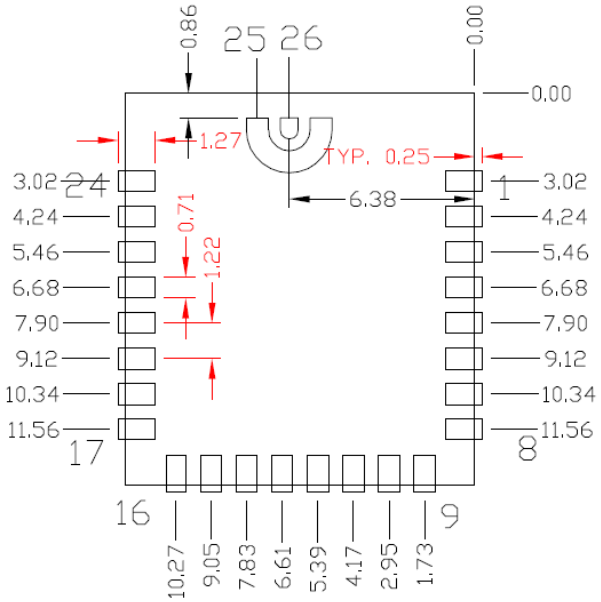
Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBT-3330xx-02. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 4. CYBT-3330xx-02 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 5. CYBT-3330xx-02 Host Layout (Relative to Origin)



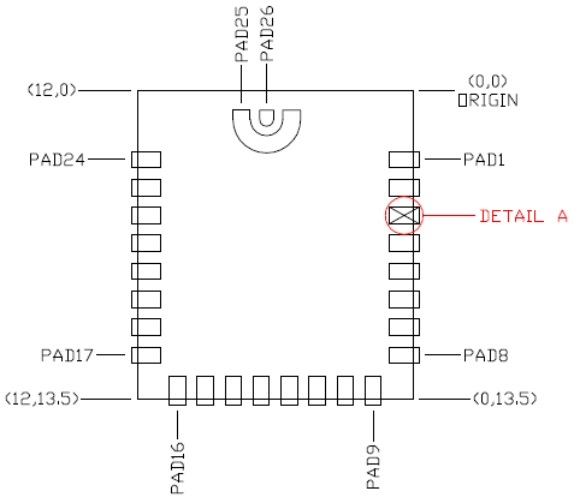
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-3330xx-02. All dimensions are referenced to the center of the solder pad. Figure 6 shows the location of each module solder pad.

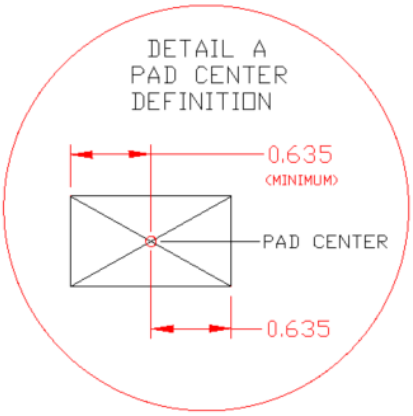
Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.38, 3.02)	(14.96, 118.90)
2	(0.38, 4.24)	(14.96, 166.93)
3	(0.38, 5.46)	(14.96, 214.96)
4	(0.38, 6.68)	(14.96, 262.99)
5	(0.38, 7.90)	(14.96, 311.02)
6	(0.38, 9.12)	(14.96, 359.05)
7	(0.38, 10.34)	(14.96, 407.09)
8	(0.38, 11.56)	(14.96, 455.12)
9	(1.73, 13.09)	(68.11, 515.35)
10	(2.95, 13.09)	(116.14, 515.35)
11	(4.17, 13.09)	(164.17, 515.35)
12	(5.39, 13.09)	(212.20, 515.35)
13	(6.61, 13.09)	(260.24, 515.35)
14	(7.83, 13.09)	(308.27, 515.35)
15	(9.05, 13.09)	(356.30, 515.35)
16	(10.27, 13.09)	(404.33, 515.35)
17	(11.62, 11.56)	(457.48, 455.12)
18	(11.62, 10.34)	(457.48, 407.09)
19	(11.62, 9.12)	(457.48, 359.05)
20	(11.62, 7.90)	(457.48, 311.02)
21	(11.62, 6.68)	(457.48, 262.99)
22	(11.62, 5.46)	(457.48, 214.96)
23	(11.62, 4.24)	(457.48, 166.93)
24	(11.62, 3.02)	(457.48, 118.90)

Figure 6. Solder Pad Reference Location



Top View (Seen on Host PCB)



Module Connections

Table 4 details the solder pad connection definitions and available functions for the pad connections for the CYBT-3330xx-02 module. Table 4 lists the CYBT-3330xx-02 solder pads, the silicon device pin, and denotes what functions are available for each solder pad.

Table 4. CYBT-3330xx-02 Solder Pad Connection Definitions

Pad	Pad Name	Silicon Pin Name	Silicon Port-Pin Name	UART	SPI[4, 5]	I2C	ADC	COEX	CLK/ XTAL	GPIO	Other
1	P0/P34	C8	PCM_Sync/ I2S_WS/P0/P34	PUART_TX/P0 PUART_RX/P34	SPI1_MOSI/P0 (master/slave)		IN29/P0 IN5/P34			✓	PCM_Sync I2S_WS
2	I2C_SCL	A8	I2S_DO/ PCM_Out/P3/ P29/P35	PUART_CTS/ P3 or P35	SPI1_CLK/P3 (master/slave)	SCL SDA/ P35	IN4/P35 IN10/29			✓ (P3/P29/P35)	I2S_DO PCM_Out PWM3 (P29)
3	XRES	RESET_N	RESET_N	External Reset (Active Low)							
4	I2C_SDA	C7	PCM_IN/ I2S_DI/P12			SDA	IN23/P12			✓ (P12)	PCM_IN I2S_DI
5	P2/P37/P28	B7	PCM_CLK/ I2S_CLK/P2/ P28/P37	PUART_RX/P2	SPI1_CS(slave)/P2 SPI1_MOSI(master)/P2 SPI1_MISO(slave)/ P37	SCL/ P37	IN11/P28 IN2/P37		ACLK1/P3 7	✓	PWM2 (P28) I2S_CLK PCM_CLK
6	SPI2_CS_N	D7	N/A	No Connect (Used for on-module memory SPI interface for CYBT-3330xx-02)							
7	GND	GND	GND	Ground							
8	SPI2_MISO	D8	N/A	No Connect (Used for on-module memory SPI interface for CYBT-3330xx-02)							
9	SPI2_MOSI	E8	N/A	No Connect (Used for on-module memory SPI interface for CYBT-3330xx-02)							
10	SPI2_CLK	E7	N/A	No Connect (Used for on-module memory SPI interface for CYBT-3330xx-02)							
11	GPIO_0	F8	BT_GPIO_0/ P36/P38		SPI1_CLK/P36 SPI1_MOSI/P38 (master/slave)		IN3/P36 IN1/P38		ACLK0/P3 6	✓ (DevWake)	
12	GPIO_1	F7	BT_GPIO_1/ P25/P32	PUART_RX/P25 PUART_TX/P32	SPI1_MISO/P25 (master/slave) SPI1_CS/P32 (slave)		IN7/P32		ACLK0/P3 2	✓ (HostWake)	
13	GND	GND	GND	Ground							
14	GPIO_4	D6	BT_GPIO_4/P6/ P31/LPO_IN	PUART_RTS/P6 PUART_TX/P31	SPI1_CS/P6 (slave)		IN8/P31			✓	Ext LPO In
15	P4/P24	G8	BT_CLK_REQ/P 4/P24	PUART_RX/P4 PUART_TX/P24	SPI1_MOSI/P4 (master/slave) SPI1_CLK/P24 (master/slave)					✓ (CLK_REQ)	
16	UART_TXD	F4	BT_UART_TXD	HCI UART Transmit Data							
17	UART_CTS	G4	BT_UART_CTS	HCI UART Clear To Send Input							
18	UART_RTS	F3	BT_UART_RTS	HCI UART Request To Send Output							
19	GPIO_7	C6	BT_GPIO_7/ P30	PUART_RTS/ P30			IN9/P30	✓(GCI_SECI _OUT)		✓	
20	UART_RXD	F5	BT_UART_RXD	HCI UART Receive Data							
21	VDDIN	G1	VDDIN	VDDIN (2.3V ~ 3.6V)							
22	GPIO_3	C5	BT_GPIO_3/ P27/P33	PUART_RX/P33	SPI1_MOSI/P27 (master/slave) SPI1_MOSI/P33 (slave)		IN6/P33		ACLK1/P3 3	✓	PWM1 (P27)
23	GPIO_6	B6	BT_GPIO_6/ P11/P26		SPI1_CS/P26 (slave)		IN24/P11	✓(GCI_SECI _IN)		✓	PWM0 (P26)
24	GND	GND	GND	Ground							
25	GND	GND	GND	Ground - Only functional for CYBT-333032-02; No Connect for CYBT-333047-02							

Notes

4. The CYBT-3330xx-02 contains a single SPI (SPI1) peripheral supporting both master or slave configurations. SPI2 is used for on-module serial memory interface.
5. In Master mode, any available GPIO can be configured as SPI1_CS. This function is not explicitly shown in Table 4.

Table 4. CYBT-3330xx-02 Solder Pad Connection Definitions (continued)

Pad	Pad Name	Silicon Pin Name	Silicon Port-Pin Name	UART	SPI[4, 5]	I2C	ADC	COEX	CLK/ XTAL	GPIO	Other
26	ANT	A2	RFOP	RF Antenna Port Input/Output - Only functional for CYBT-333032-02; No Connect for CYBT-333047-02							

Notes
4. The CYBT-3330xx-02 contains a single SPI (SPI1) peripheral supporting both master or slave configurations. SPI2 is used for on-module serial memory interface.
5. In Master mode, any available GPIO can be configured as SPI1_CS. This function is not explicitly shown in Table 4.

Connections and Optional External Components

Power Connections (VDDIN)

The CYBT-3330xx-02 contains one power supply connection, VDDIN. VDDIN accepts a supply input range of 2.3 V to 3.6 V for CYBT-3330xx-02. Table 11 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 11.

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection and the recommended ferrite bead value is 330 Ω, 100 MHz.

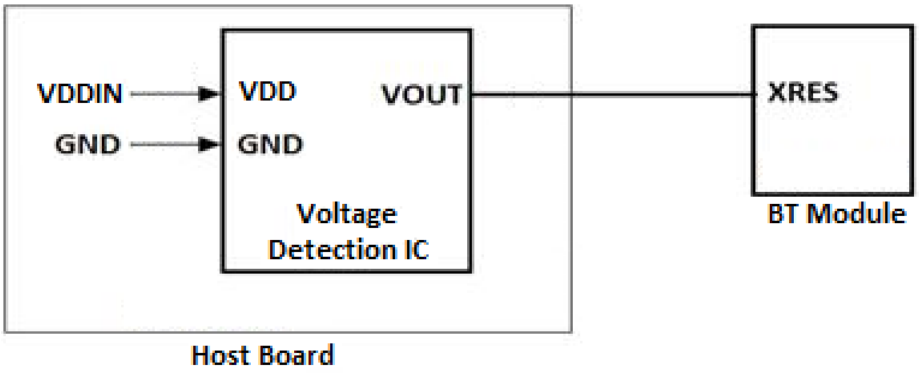
Considerations and Optional Components for Brown Out (BO) Conditions

Power supply design must be completed to ensure that the CYBT-3330xx-02 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the following range: $V_{IL} \leq VDDIN \leq V_{IH}$.

Refer to Table 12 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (that is, battery installation, high-value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Refer to Figure 7 for the recommended circuit design when using an external voltage detection IC.

Figure 7. Reference Circuit Block Diagram for External Voltage Detection IC



In the event that the module does encounter a Brown Out condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

External Reset (XRES)

The CYBT-3330xx-02 has an integrated power-on reset circuit, which completely resets all circuits to a known power-on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBT-3330xx-02 module (solder pad 3). The CYBT-3330xx-02 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYBT-3330xx-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of the Cypress CYBT-3330xx-02 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDDIN is stable.
- If the XRES connection of the CYBT-3330xx-02 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-3330xx-02 in order to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDDIN power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDDIN stability.
- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after VDD is stable.

Refer to Figure 11 on page 17 for XRES operating and timing requirements during power-on events.

Multiple-Bonded GPIO Connections

The CYBT-3330xx-02 contains GPIOs, which are multiple-bonded at the silicon level. If any of these dual-bonded GPIOs are used, only the functionality and features for one of these port pins may be used. The desired port pin should be configured in the WICED Studio SDK. For details on the features and functions that each of these multiple-bonded GPIOs provide, refer to Table 4.

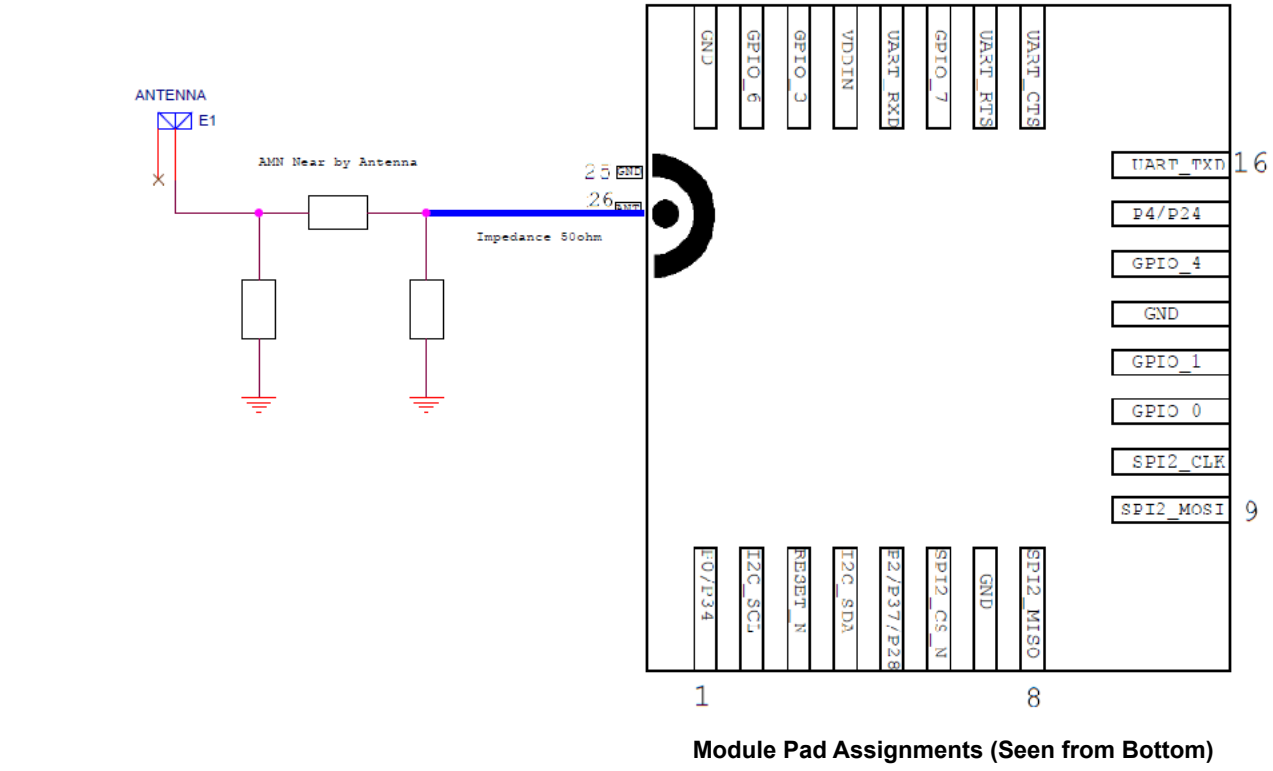
The list below details the multiple-bonded GPIOs available on the CYBT-3330xx-02 module:

- PAD 1 P0/34: I2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of four is available)
- PAD 2 I2C_SCL: I2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- PAD 4 I2C_SDA: I2S_PCM_IN/P12 (dual bonded; only one of two is available)
- PAD 5 P2/P37/P28: I2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- PAD 11 GPIO_0: GPIO_0/P36/P38 (triple bonded; only one of three is available)
- PAD 12 GPIO_1: GPIO_1/P25/P32 (triple bonded; only one of three is available)
- PAD 14 GPIO_4: GPIO_4/LPO_IN/P6/P31 (quadruple bonded; only of four is available)
- PAD 15 P4/P24: BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- PAD 19 GPIO_7: GPIO_7/P30 (dual bonded; only one of two is available)
- PAD 22 GPIO_3: GPIO_3/P27/P33 (triple bonded; only one of three is available)
- PAD 23 GPIO_6: GPIO_6/P11/P26 (triple bonded; only one of three is available)

Antenna Matching Network Requirements

The CYBT-333032-02 module requires ANT and GND connections to an external antenna via the RF pad connections on the module (Pads 25 and 26). In order to optimize RF performance, an Antenna Matching Network (AMN) is required to be placed between the ANT connection (Pad 26) and the antenna used in the final design. Figure 8 details the recommeded Pi topology circuit footprint to use for the Antenna Matching Network.

Figure 8. Recommended Antenna Matching Network for CYBT-3330xx-02 Module



Module Pad Assignments (Seen from Bottom)

Denotes a component footprint representing either a capacitor, inductor, or 0 Ohm resistor.

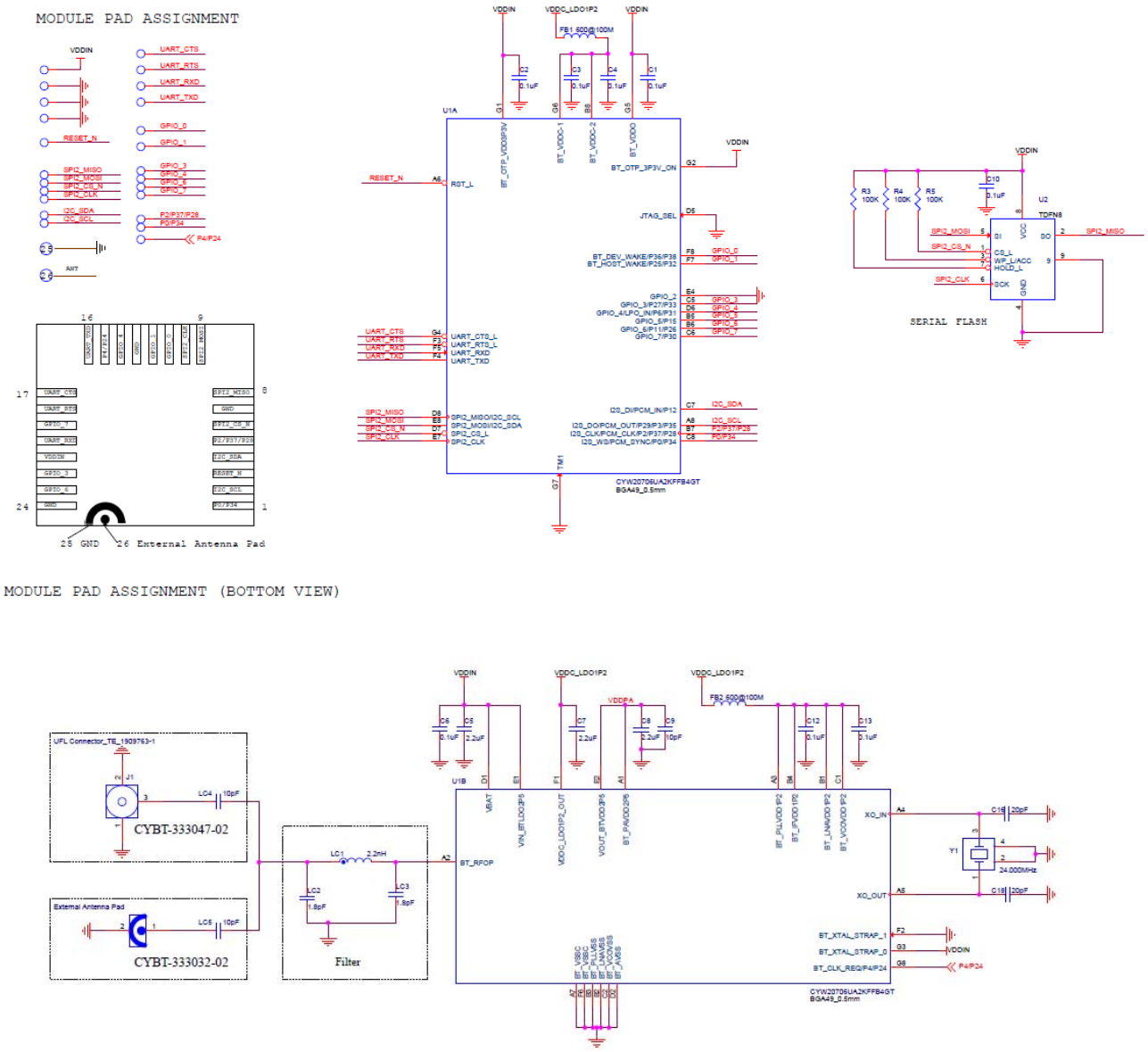
The design guidelines that should be followed when completing the Antenna Matching Network are as follows:

- The AMN should be placed close to the antenna on the main board.
- Routing to the AMN from the ANT pad on the module must be controlled to an imedance of 50 Ω.

The final AMN circuit may contain only a single component, or all three components shown above. The final number and type of components will be determined based on the actual design of the system, and the final values for each component can be determined through tuning the AMN. For details on how to properly tune an AMN, please refer to Application Note AN91445.

Figure 9 illustrates the CYBT-3330xx-02 schematic.

Figure 9. CYBT-3330xx-02 Schematic Diagram



Critical Components List

Table 5 details the critical components used in the CYBT-3330xx-02 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	49-pin FBGA BT/BLE Silicon Device - CYW20706
Silicon	U2	8-pin TDF8N, 512K Serial Flash
Crystal	Y1	24.000 MHz, 12PF

Qualified Antenna for CYBT-3330xx-02

The CYBT-3330xx-02 module has been designed to work with a standard 2.2 dBi dipole antenna. Any antenna of equivalent or less gain can be used without additional application and testing for FCC regulations. Table 5 details the approved antennas for the CYBT-3330xx-02 module for Bluetooth operation.

Table 6. Qualified Antennas

Manufacturer	Part Number	Gain
Antenova	B4844-01	2.2 dBi
Pulse	W1030	2.0 dBi

Functional Description

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types. The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Table 7. Bluetooth Features

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive Frequency Hopping	–
Paging and Inquiry	eSCO	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	**Bluetooth 3.0**	**Bluetooth 4.0**
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	eSCO	–
Bluetooth 4.1	**Bluetooth 4.2**	
Low Duty Cycle Advertising	Data Packet Length Extension	–
Dual Mode	LE Secure Connection	–
LE Link Layer Topology	Link Layer Privacy	–

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state in the Bluetooth Link Controller.

- States:
  - Standby
  - Connection
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - Advertising
  - Scanning

Test Mode Support

The CYBT-3330xx-02 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYBT-3330xx-02 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment.

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

Microcontroller Unit

The microprocessor unit in CYBT-3330xx-02 runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYBT-3330xx-02 uses SPI Serial Flash for NVRAM storage.

One-Time Programmable Memory

The microprocessor unit in CYBT-3330xx-02 includes 2 KB of one-time programmable (OTP) memory that allows manufacturing customization and avoids the need for an onboard NVRAM. If customization is not required, then OTP does not need to be programmed. Whether the OTP is programmed or not, to save power it is disabled when the boot process is complete. The OTP is designed to store minimal amount of information. Aside from OTP data, most user configuration information will be downloaded to RAM after the CYBT-3330xx-02 boots and is ready for host transport communication.

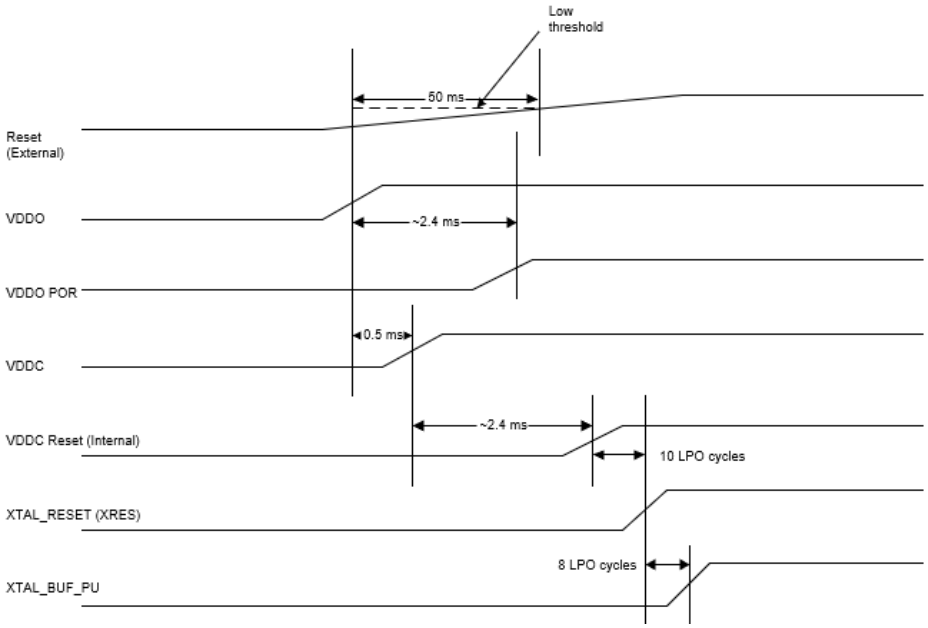
The OTP contents are limited to:

- Parameters required prior to downloading the user configuration to RAM.
- Parameters unique to each part and each customer (for example, the Bluetooth device address and/or the software license key).
- VDDIN for the module must be kept to 3.0 V to 3.6 V power supply range if OTP is used in the application.

External Reset (XRES)

The CYBT-3330xx-02 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, XRES, can be used to put the CYBT-3330xx-02 in the reset state. The XRES pin has an internal pull-up resistor and, in most applications, it does not require anything to be connected to it.

Figure 10. External Reset Internal Timing

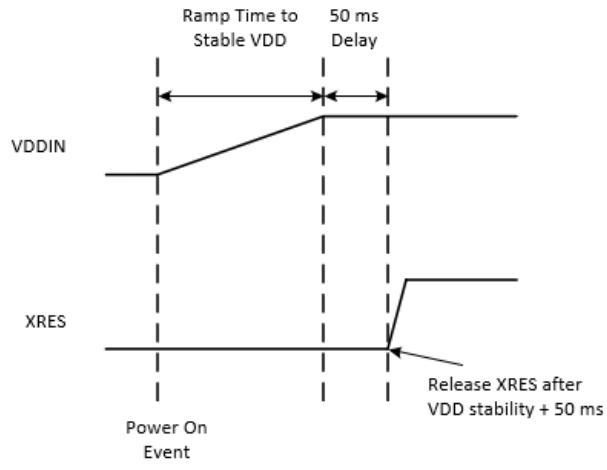


External Reset (XRES) Recommended External Components and Proper Operation

During a power-on event, the XRES line of the CYBT-3330xx-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. Refer to Figure 11 for the Power-On XRES timing operation. This power-on operation can be accomplished in the following ways:

- A host device should connect a GPIO to the XRES of the Cypress CYBT-3330xx-02 module and pull XRES low until VDD is stable. XRES can be released after VDD is stable.
- If the XRES connection of the CYBT-3330xx-02 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-3330xx-02.
- The XRES release timing can also be controlled via an external voltage detection circuit.

Figure 11. Power-On External Reset (XRES) Operation



Integrated Radio Transceiver

The CYBT-3330xx-02 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. The CYBT-3330xx-02 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The CYBT-3330xx-02 a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4-GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the BLE specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYBT-3330xx-02 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBT-3330xx-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. The CYBT-3330xx-02 uses an internal loop filter.

Calibration

The CYBT-3330xx-02 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Internal LDO

The microprocessor in CYBT-3330xx-02 uses two LDOs – one for 1.2 V and the other for 2.5 V. The 1.2-V LDO provides power to the baseband and radio and the 2.5-V LDO powers the PA.

Collaborative Coexistence

The CYBT-3330xx-02 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

Global Coexistence Interface

The CYBT-3330xx-02 supports the proprietary Cypress Global Coexistence Interface (GCI) which is a 2-wire interface.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over GCI_SECI_IN and GCI_SECI_OUT a 2-wire interface, one serial input (GCI_SECI_IN), and one serial output (GCI_SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI_SECI_IN and GCI_SECI_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

SECI I/O

The microprocessor in CYBT-3330xx-02 has dedicated GCI_SECI_IN (PAD 23/GPIO_6) and GCI_SECI_OUT (PAD19/GPIO_7) pins. Refer to Table 4, which detail the module solder pad number used for SECI I/O.

Peripheral and Communication Interfaces

I²C Communication Interface

The CYBT-3330xx-02 provides a 2-pin master I²C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. This interface is compatible with I²C slave devices. I²C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by the I²C:

- 100 kHz
- 400 kHz
- 800 kHz (not a standard I²C-compatible speed.)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed.)

The following transfer types are supported by the I²C:

- Read (up to 127 bytes can be read)
- Write (up to 127 bytes can be written)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written)
- Write-then-Read (Up to127 bytes can be written and up to 127 bytes can be read)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pad (I2C_SCL) and data pad 2 (I2C_SDA) are both open-drain I/O pins. Pull-up resistors, external to the CYBT-3330xx-02, are required on both the SCL and SDA pad for proper operation.

HCI UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 4 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYBT-3330xx-02 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 4 Mbps. The baud rate of the CYBT-3330xx-02UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 8 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 8. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
4M	0xFF	0xF4	High rate	0.00
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYBT-3330xx-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Peripheral UART Interface

The CYBT-3330xx-02 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each signal as shown in Table 9.

Table 9. CYBT-3330xx-02 Peripheral UART

Signal Name	PUART_TX	PUART_RX	PUART_CTS_N	PUART_RTS_N
PUART Port Configuration #1	P0	P2	P3	P6
PUART Port Configuration #2	P31	P33	P35	P30

Serial Peripheral Interface

The CYBT-3330xx-02 has two independent SPI interfaces. One is a master-only interface (SPI2) and the other (SPI1) can be either a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYBT-3330xx-02 has optional I/O ports that can be configured individually and separately for each functional pin. The CYBT-3330xx-02 acts as an SPI master device that supports 3.3 V SPI slaves. In master mode, refer to Table 4 to identify the solder pads avialable for SPI1_MISO, SPI1_MOSI, and SPI1_CLK connections. NOTE: In master mode, any available GPIO can be assigned as SPI1_CS.

The CYBT-3330xx-02 can also act as an SPI slave device that supports a 3.3 V SPI master. For SPI1 slave mode, refer to Table 4 to identify the solder pads available for SPI1 slave mode connections.

SPI voltage depends on V_{DDIN}; therefore, V_{DDIN} should be set to 3.3 V for SPI communication.

PCM Interface

The CYBT-3330xx-02 includes a PCM interface that shares pins with the I^2S interface. The PCM Interface on the CYBT-3330xx-02 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYBT-3330xx-02 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYBT-3330xx-02.

Slot Mapping

The CYBT-3330xx-02 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The CYBT-3330xx-02 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The CYBT-3330xx-02 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYBT-3330xx-02 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

Clock Frequencies

The CYBT-3330xx-02 has an integrated 24 MHz crystal on the module. There is no need to add an additional crystal oscillator.

GPIO Port

The CYBT-3330xx-02 has a maximum of 11 GPIOs. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3 V or 4 mA at 1.8 V, except chips P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3 V.

The following GPIOs are available on the module pads:

- PAD 1 P0/34: I2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of four is available)
- PAD 2 I2C_SCL: I2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- PAD 4 I2C_SDA: I2S_PCM_IN/P12 (dual bonded; only one of two is available)
- PAD 5 P2/P37/P28: I2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- PAD 11 GPIO_0: GPIO_0/P36/P38 (triple bonded; only one of three is available)
- PAD 12 GPIO_1: GPIO_1/P25/P32 (triple bonded; only one of three is available)
- PAD 14 GPIO_4: GPIO_4/LPO_IN/P6/P31 (quadruple bonded; only of four is available)
- PAD 15 P4/P24: BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- PAD 19 GPIO_7: GPIO_7/P30 (Dual bonded; only one of two is available)
- PAD 22 GPIO_3: GPIO_3/P27/P33 (triple bonded; only one of three is available)
- PAD 23 GPIO_6: GPIO_6/P11/P26 (triple bonded; only one of three is available)

Refer to Table to determine what GPIOs can be configured as ADC Inputs.

Note Any available GPIO can be used for SPI1_CS when in master mode.

Port 26–Port 29 in PAD 23/PAD 22/PAD 5/PAD 2

P[26:29] in PAD 23/PAD 22/PAD 5/PAD 2 consists of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have PWM functionality, which can be used for LED dimming. For a description of the capabilities of all GPIOs, see Table 4.

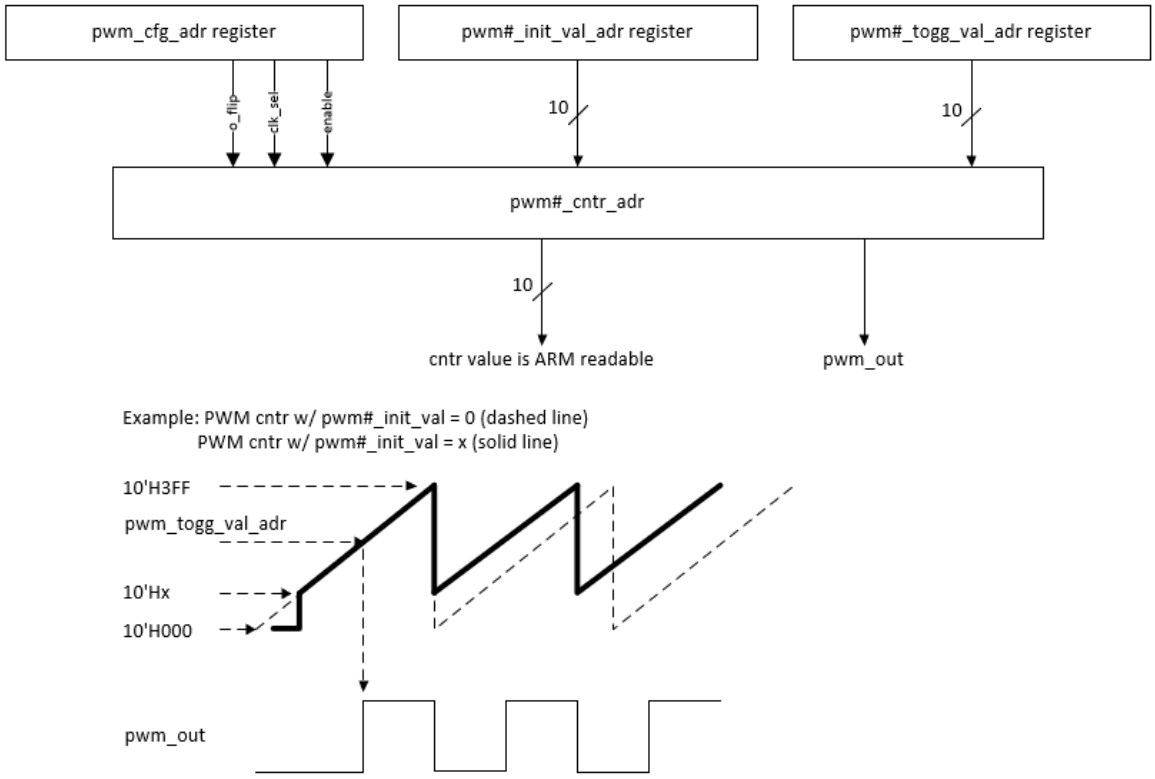
PWM

The CYBT-3330xx-02 has four PWMs (PWM0-3). The PWM module consists of the following:

- The following GPIOs can be mapped as PWMs, module pad shown in [ ]:
  - PWM0: P26 on P11/P26 [Pad 23]
  - PWM1: P27 on P33/P27 [Pad 22]
  - PWM2: P28 on P2/P37/P28 [Pad 5]
  - PWM3: P29 on P3/P35/P29/I2C_SCL [Pad 2]
- PWM1-4: Each of the four PWM channels contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1-4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 12 shows the structure of one PWM.

Figure 12. PWM Block Diagram



Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in deep sleep (HIDOFF) mode.

BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYBT-3330xx-02 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYBT-3330xx-02 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode

The CYBT-3330xx-02 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF (Deep Sleep) mode, the CYBT-3330xx-02 baseband and core are powered off by disabling power to LDOOUT. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

Electrical Characteristics

Table 10 shows the maximum electrical rating for voltages referenced to VDDIN pad.

Table 10. Maximum Electrical Rating

Rating	Symbol	Value	Unit
V_{DDIN}	–	3.795	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating ambient temperature range	T_{opr}	–30 to +85	°C
Storage temperature range	T_{stg}	–40 to +85	°C

Table 11 shows the power supply characteristics for the range T_J = 0 to 125 °C.

Table 11. Power Supply

Parameter	Description	Min[6]	Typ	Max[6]	Unit
V_{DDIN}	Power Supply Input (CYBT-3330xx-02)	2.3	–	3.6	V
V_{DDIN_RIPPLE}	Maximum Power Supply Ripple for V_{DDIN} input voltage	–	–	100	mV

Table 12 shows the specifications for the digital voltage levels.

Table 12. Digital Voltage Levels

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.8	V
Input high voltage	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	V_{DDIN} – 0.4	–	–	V
Input capacitance (V_{DDMEM} domain)	C_{IN}	–	–	0.4	pF

Table 13 shows the current consumption measurements

Table 13. Bluetooth, BLE, BR and EDR Current Consumption

Parameter	Description	Silicon or Module Parameter	Output Power Level/Class	Typ	Unit
Bluetooth Classic (BR, EDR)					
3DM5/3DH5	HCI control mode	Silicon	Class 1	37.1	mA
DM1/DH1	HCI control mode	Silicon	Class 1	32.2	mA
DM3/DH3	HCI control mode	Silicon	Class 1	38.2	mA
DM5/DH5	HCI control mode	Silicon	Class 1	38.5	mA
RX_{1M_BR}	Peak receive (1 Mbps) current level when receiving a basic rate packet (radio only)	Silicon	Class 1	26.4	mA
TX_{1M_BR}	Peak transmit (1 Mbps) current level when transmitting a basic rate packet (radio only)	Silicon	10 dBm	60.3	mA
RX_{23M_EDR}	Peak receive (EDR) current level when receiving a 2 or 3 Mbps rate packet (radio only)	Silicon	Class 1	26.4	mA
TX_{23M_EDR}	Peak transmit (EDR) current level when transmitting a 2 or 3 Mbps rate packet (radio only)	Silicon	8 dBm	52.5	mA

Note
6. Overall performance degrades beyond minimum and maximum supply voltages.The voltage range specified is determined by the minimum and maximum operating voltage of the SPI Serial Flash included on the module.

Table 13. Bluetooth, BLE, BR and EDR Current Consumption

Parameter	Description	Silicon or Module Parameter	Output Power Level/Class	Typ	Unit
Bluetooth Classic (BR, EDR)					
Deep Sleep	Deep Sleep (HIDOFF) current	Module	All	2.69	µA
IDLE	Module is idle, non-discoverable and non-connectable	Module	Class 1	0.11	mA
I_{Scan}	Inquiry Scan (1.28 seconds)	Module	Class 1	0.65	mA
P_{Scan}	Page scan (1.28 seconds)	Module	Class 1	0.65	mA
I_{Scan} + P_{Scan}	Inquiry scan + Page Scan (1.28 seconds)	Module	Class 1	1.2	mA
Connected	Connected with no data transfer	Module	Class 1	2.6	mA
Connected + P_{Scan}	Connected with no data transfer + Page Scan (1.28 seconds)	Module	Class 1	3.3	mA
Connected + I_{Scan} + P_{Scan}	Connected with no data transfer + Inquiry Scan(1.28 seconds) + Page Scan (1.28 seconds)	Module	Class 1	3.6	mA
Connected + SNIFF	Connected with no data transfer + SNIFF (500 ms)	Module	Class 1	0.95	mA
Connected + SNIFF + I_{Scan} + P_{Scan}	Connected with no data transfer + SNIFF (500 ms) + Inquiry Scan and Page Scan 1.28 seconds	Module	Class 1	1.9	mA
TX_BR	Data transfer @ 115200 baud rate	Module	Class 1	22	mA
TX+SNIFF_BR	Data transfer @ 115200 baud rate + Sniff (500 ms)	Module	Class 1	5.5	mA
Bluetooth Low Energy (BLE)					
TX_{Peak}	Peak TX current	Module	-2.5dBm +6.5 dBm +9.0 dBm	42 54 56	mA
RX_{Peak}	Peak RX current	Module	-2.5dBm +6.5 dBm +9.0 dBm	28 28 28	mA
Deep Sleep	Deep Sleep (HIDOFF) current	Module	All	2.69	µA
Connection_1s	Connection - 1-second interval	Module	-2.5dBm +6.5 dBm +9.0 dBm	970 980 1000	µA
Connection_4s	Connection - 4-second interval	Module	-2.5dBm +6.5 dBm +9.0 dBm	900 945 950	µA
Adv_640	Advertisement (low duty cycle) - 640 ms	Module	-2.5dBm +6.5 dBm +9.0 dBm	0.4 0.5 0.5	mA
Adv_30	Advertisement (high duty cycle) - 30 ms	Module	-2.5dBm +6.5 dBm +9.0 dBm	3.8 4.2 4.3	mA
Adv_1s	1-second non-connectable advertisement (Beacon)	Module	-2.5dBm +6.5 dBm +9.0 dBm	315 350 350	µA

Chipset RF Specifications

All specifications in Table 14 are for industrial temperatures and are single-ended. Unused inputs are left open.

Table 14. Chipset Receiver RF Specifications

Parameter	Conditions	Min	Typ[7]	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[8]	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	LE GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference Performance					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–40	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB
Out-of-Band Blocking Performance (CW)[9]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Notes
7. Typical operating conditions are 1.22-V operating voltage and 25°C ambient temperature.
8. The receiver sensitivity is measured at BER of 0.1% on the device interface.
9. Meets this specification using front-end band pass filter.

Table 14. Chipset Receiver RF Specifications (continued)

Parameter	Conditions	Min	Typ[7]	Max	Unit
Out-of-Band Blocking Performance, Modulated Interferer					
776–764 MHz	CDMA	–	–10[10]	–	dBm
824–849 MHz	CDMA	–	–10[10]	–	dBm
1850–1910 MHz	CDMA	–	–23[10]	–	dBm
824–849 MHz	EDGE/GSM	–	–10[10]	–	dBm
880–915 MHz	EDGE/GSM	–	–10[10]	–	dBm
1710–1785 MHz	EDGE/GSM	–	–23[10]	–	dBm
1850–1910 MHz	EDGE/GSM	–	–23[10]	–	dBm
1850–1910 MHz	WCDMA	–	–23[10]	–	dBm
1920–1980 MHz	WCDMA	–	–23[10]	–	dBm
Intermodulation Performance[11]					
BT, Df = 5 MHz	–	–39.0	–	–	dBm
Spurious Emissions[12]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM Rx	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

Notes
10. Numbers are referred to the pin output with an external BPF filter.
11. f0 = –64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n * 1 MHz, where n = 3, 4, or 5. For the typical case, n = 4.
12. Includes baseband radiated emissions.

Table 15. Chipset Transmitter RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
General					
Frequency Range	–	2402	–	2480	MHz
Class1: GFSK Tx Power[13]	–	–	12	–	dBm
Class1: EDR Tx Power[14]	–	–	9	–	dBm
Class 2: GFSK Tx Power	–	–	2	–	dBm
Power Control Step	–	2	4	8	dB
Modulation Accuracy					
π/4-DQPSK Frequency Stability	–	–10	–	10	kHz
π/4-DQPSK RMS DEVM	–	–	–	20	%
π/4-QPSK Peak DEVM	–	–	–	35	%
π/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK Frequency Stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[15]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[15, 16]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

Table 16. Chipset BLE RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	N/A	2402	–	2480	MHz
Rx Sense[17]	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
Tx Power[18]	N/A	–	–	9	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[19]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

Notes
13. TBD dBm output for GFSK measured with PAVDD = 2.5 V.
14. TBD dBm output for EDR measured with PAVDD = 2.5 V.
15. Maximum value is the value required for Bluetooth qualification.
16. Meets this spec using a front-end band-pass filter.
17. Dirty Tx is Off.
18. The BLE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc. The output is capped at 12 dBm out. The BLE Tx power at the antenna port cannot exceed the 10 dBm EIRP specification limit.
19. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Timing and AC Characteristics

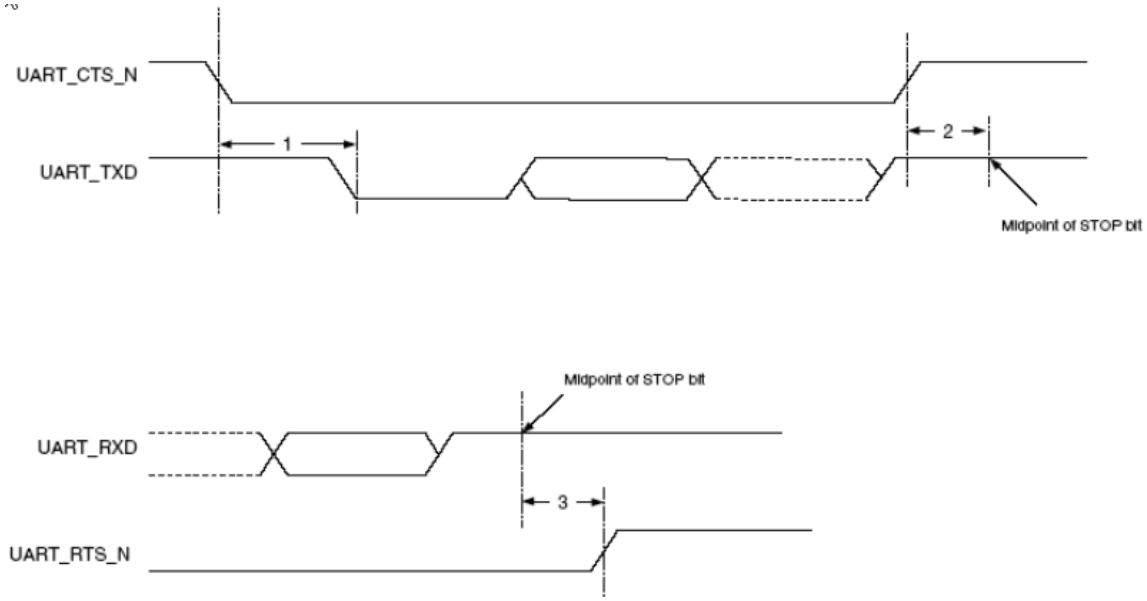
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 17. UART Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

Figure 13. UART Timing



SPI Timing

The SPI interface supports clock speeds up to 12 MHz.

Table 18 and Figure 14 show the timing requirements when operating in SPI Mode 0 and 2, and SPI Mode 1 and 3, respectively.

Table 18. SPI Mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	ns
3	Time from master assert SPI_CSN to first clock edge	20	∞	ns
4	Setup time for MOSI data lines	8	½ SCK	ns
5	Hold time for MOSI data lines	8	½ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	ns
8	Idle time between subsequent SPI transactions	1 SCK	∞	ns

Figure 14. SPI Timing – Mode 0 and 2

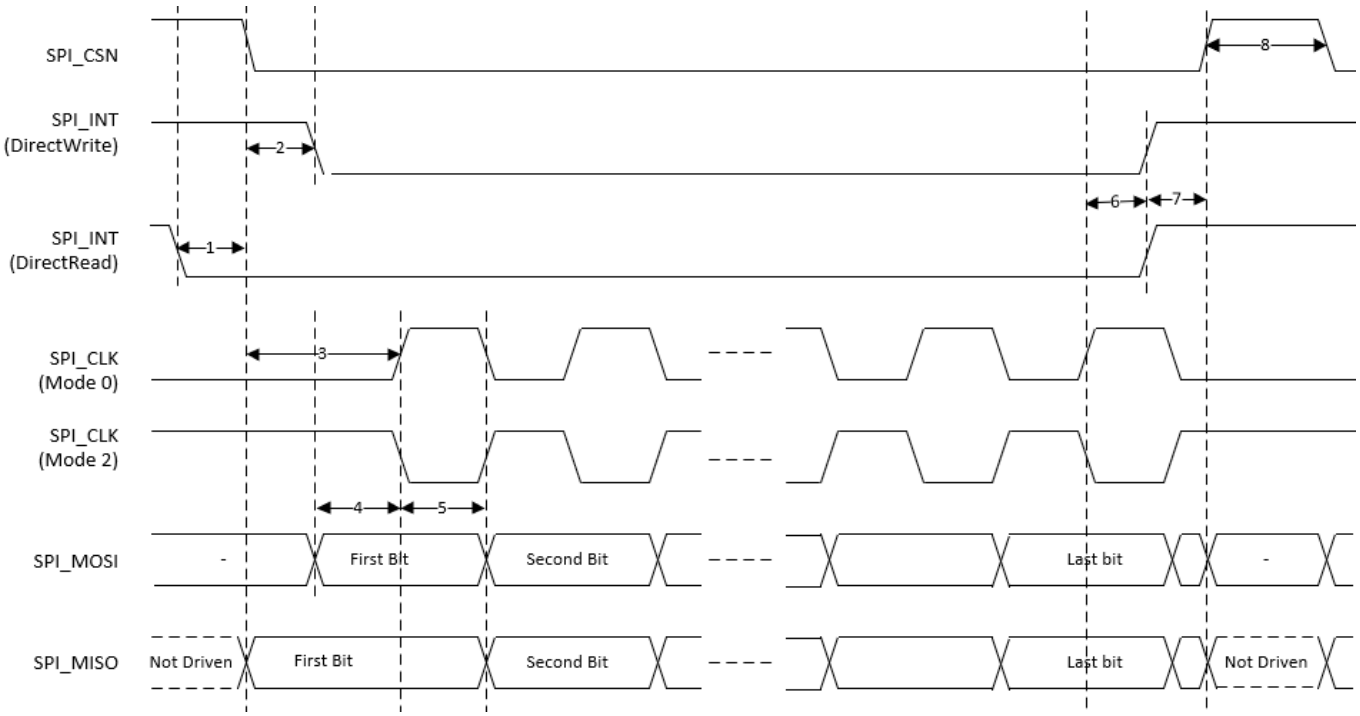
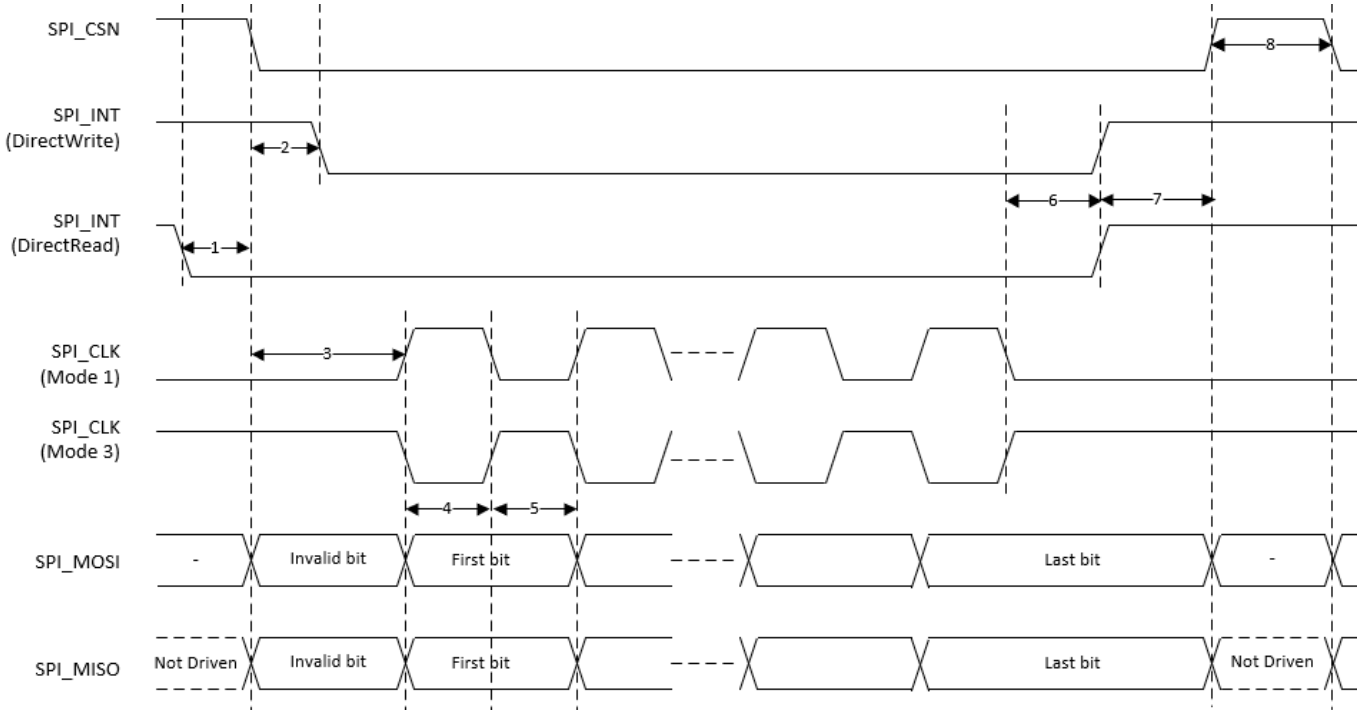


Table 19 and Figure 15 show the timing requirements when operating in SPI Mode 1 and 3.

Table 19. SPI Mode 1 and 3

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	ns
3	Time from master assert SPI_CSN to first clock edge	20	∞	ns
4	Setup time for MOSI data lines	8	½ SCK	ns
5	Hold time for MOSI data lines	8	½ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	ns
8	Idle time between subsequent SPI transactions	1 SCK	∞	ns

Figure 15. SPI Timing – Mode 1 and 3



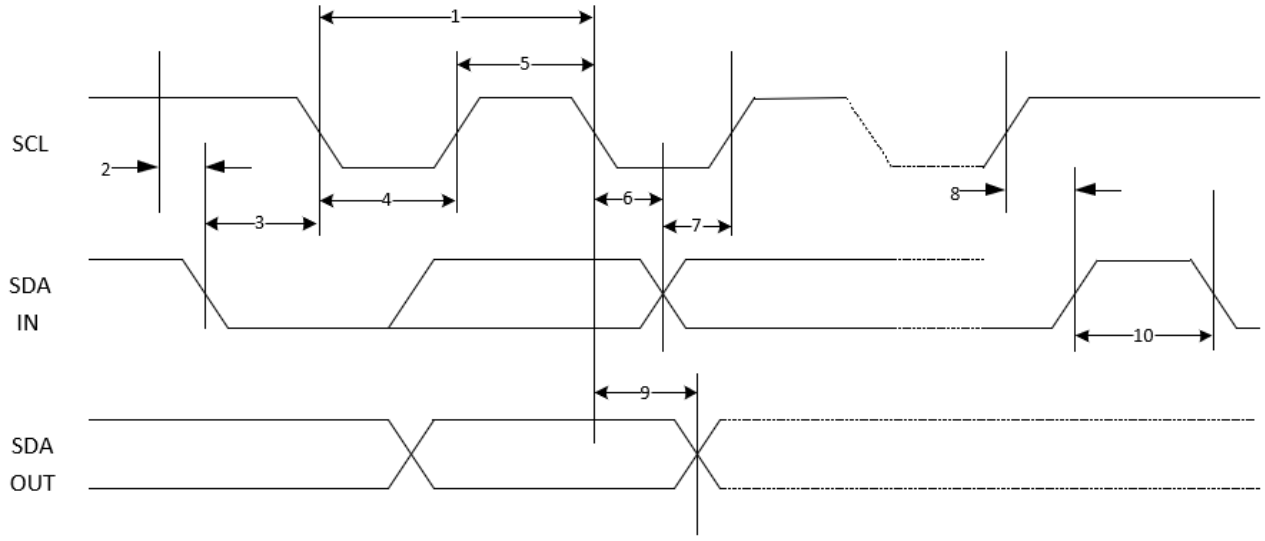
I2C Interface Timing

Table 20. I2C Interface Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[20]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[21]	650	–	ns

Notes
20. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
21. Time that the cbus must be free before a new transaction can start.

Figure 16. I2C Interface Timing Diagram



PCM Interface Timing

Short Frame Sync, Master Mode

Figure 17. PCM Timing Diagram (Short Frame Sync, Master Mode)

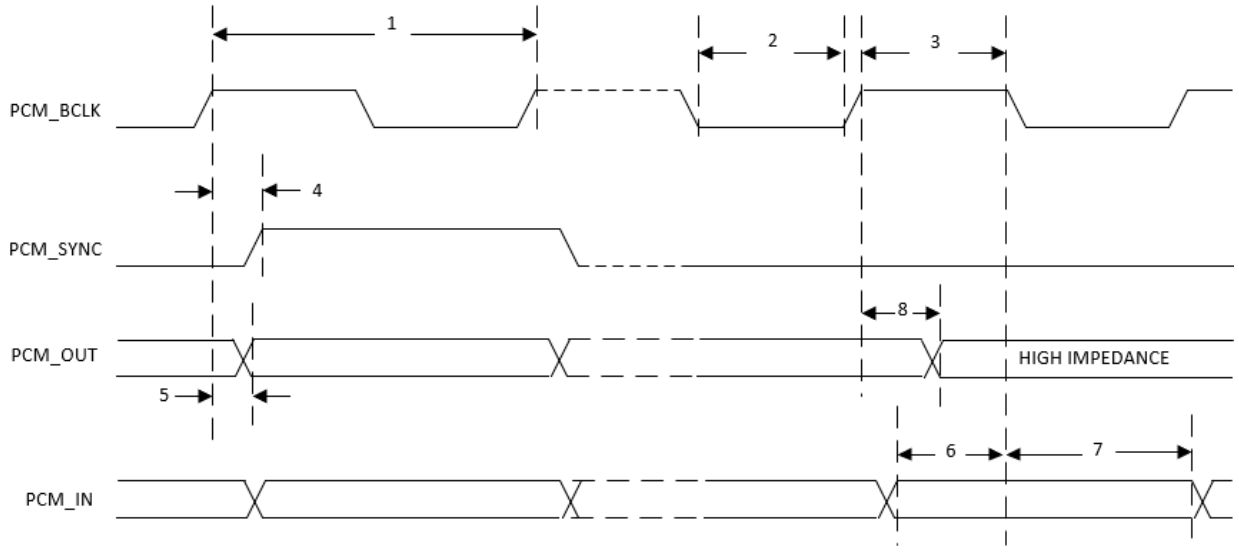


Table 21. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC delay	0	–	25.0	ns
5	PCM_OUT delay	0	–	25.0	ns
6	PCM_IN setup	8.0	–	–	ns
7	PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

Short Frame Sync, Slave Mode

Figure 18. PCM Timing Diagram (Short Frame Sync, Slave Mode)

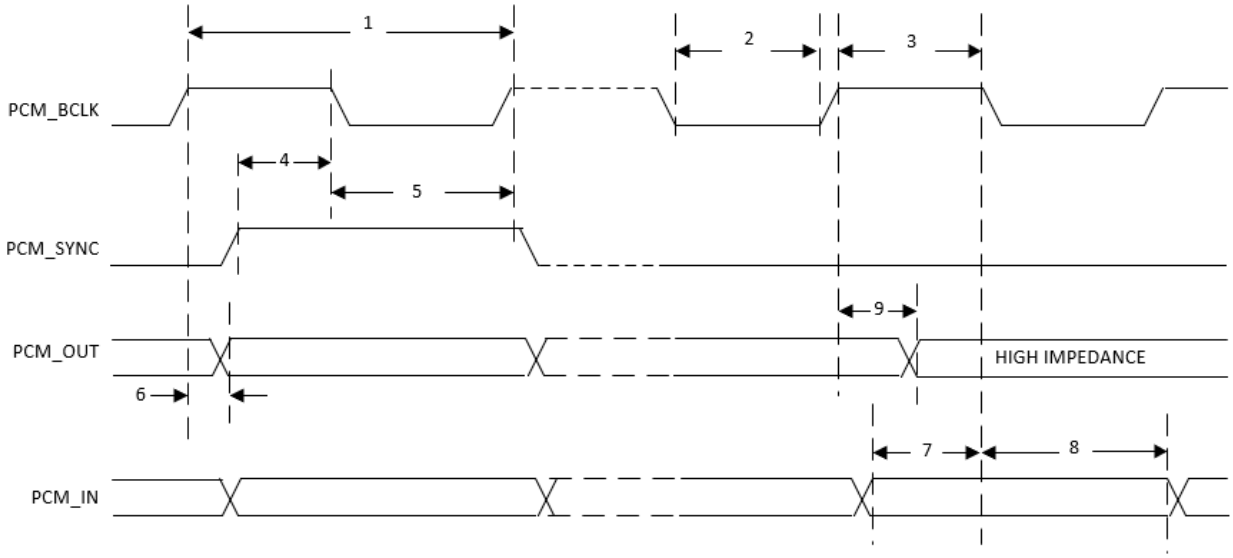


Table 22. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC setup	8.0	–	–	ns
5	PCM_SYNC hold	8.0	–	–	ns
6	PCM_OUT delay	0	–	25.0	ns
7	PCM_IN setup	8.0	–	–	ns
8	PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

Long Frame Sync, Master Mode

Figure 19. PCM Timing Diagram (Long Frame Sync, Master Mode)

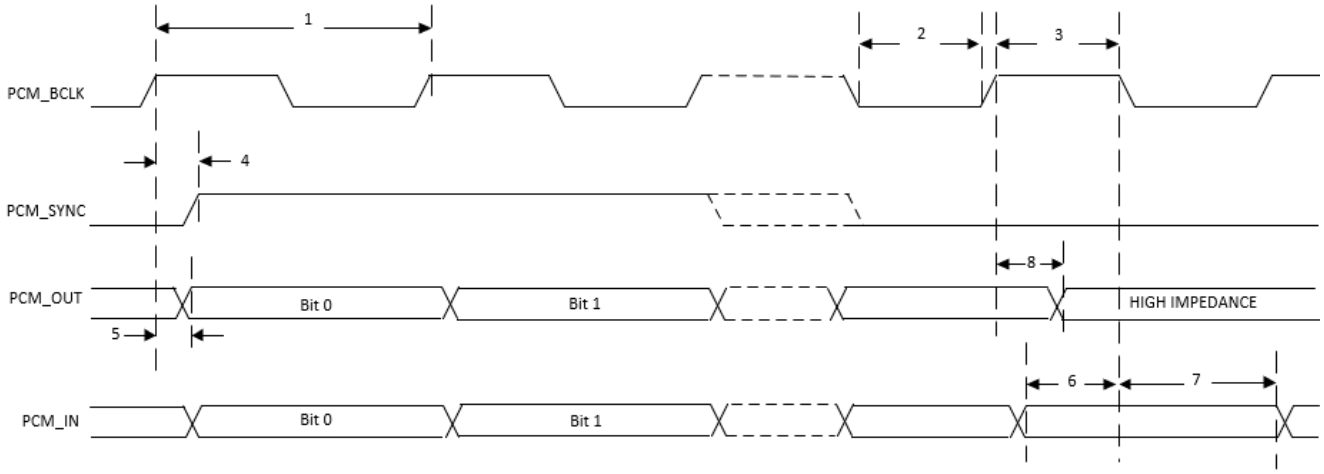


Table 23. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC delay	0	–	25.0	ns
5	PCM_OUT delay	0	–	25.0	ns
6	PCM_IN setup	8.0	–	–	ns
7	PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

Long Frame Sync, Slave Mode

Figure 20. PCM Timing Diagram (Long Frame Sync, Slave Mode)

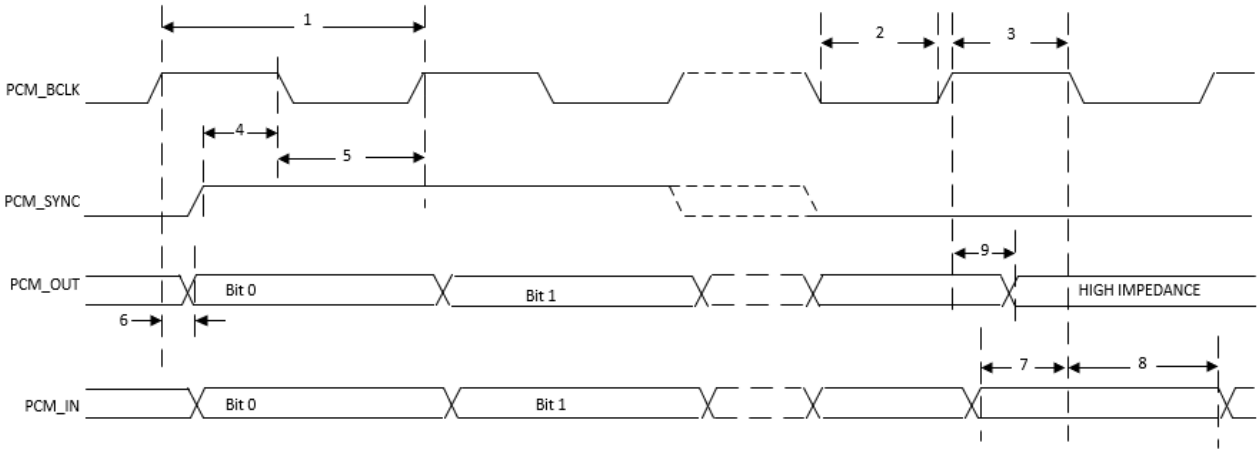


Table 24. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC setup	8.0	–	–	ns
5	PCM_SYNC hold	8.0	–	–	ns
6	PCM_OUT delay	0	–	25.0	ns
7	PCM_IN setup	8.0	–	–	ns
8	PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

I^2S Interface Timing

The I^2S interface supports both master and slave modes. The I^2S signals are:

- I^2S clock: I^2S SCK
- I^2S Word Select: I^2S WS
- I^2S Data Out: I^2S SDO
- I^2S Data In: I^2S SDI

I^2S SCK and I^2S WS become outputs in master mode and inputs in slave mode, while I^2S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I^2S bus, per the I^2S specification. The MSB of each data word is transmitted one bit clock cycle after the I^2S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I^2S WS is low, and right-channel data is transmitted when I^2S WS is high. Data bits sent by the CYBT-3330xx-02 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider. In the slave mode, any clock rate is supported to a maximum of 3.072 MHz. Timing values specified in Table 25 are relative to high and low threshold levels.

Table 25. Timing for I^2S Transmitters and Receivers

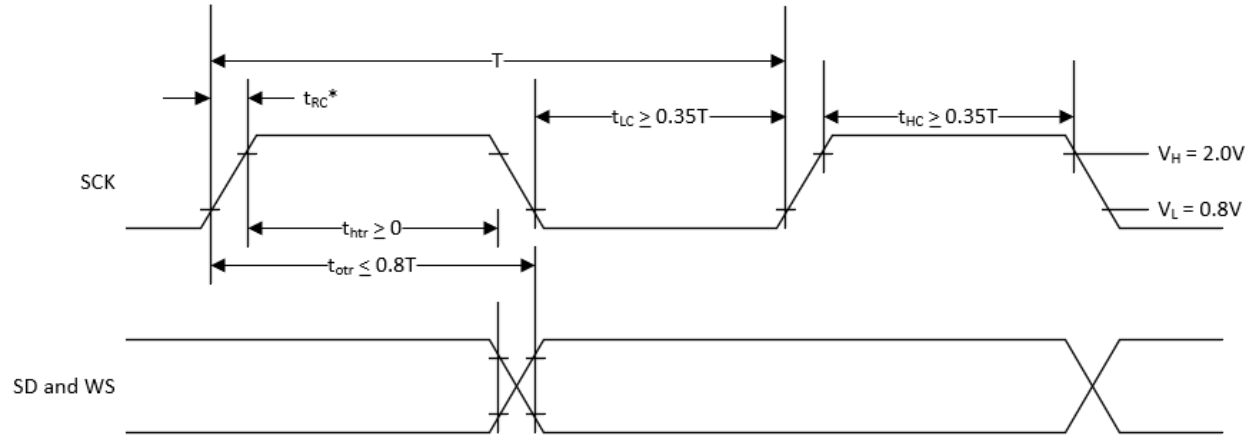
	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	Note 22
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	Note 23
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	Note 23
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	Note 24
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	Note 24
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	Note 25
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	Note 26
Hold time t_{htr}	0	–	–	–	–	–	–	–	Note 26
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	Note 27
Hold time t_{hr}	–	–	–	–	–	0	–	–	Note 27

Note The time periods specified in Figure 21 and Figure 22 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Notes

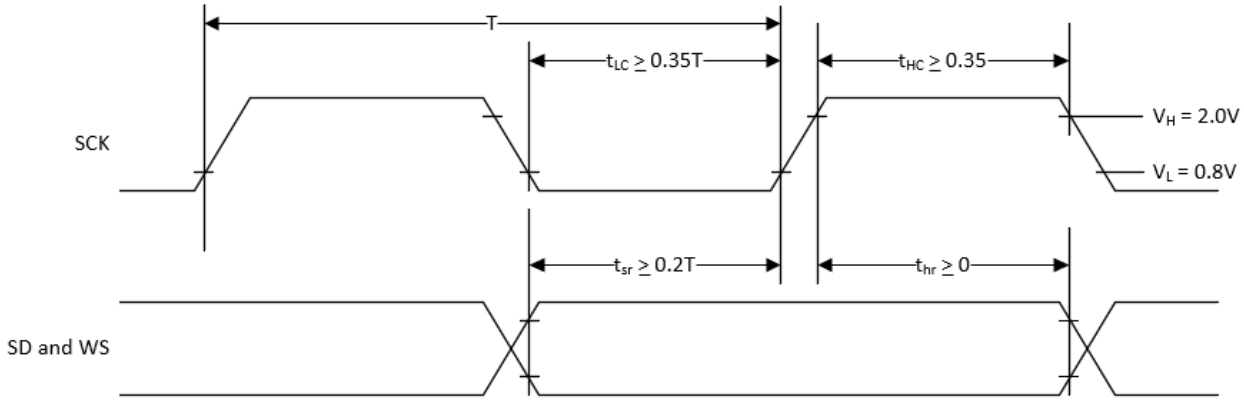
22. The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver have to be able to handle the data transfer rate.
23. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.
24. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.
25. Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter has to guarantee that thtr is greater than or equal to zero, so long as the clock rise-time tRC is not more than tRCmax, where tRCmax is not less than 0.15Ttr.
26. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
27. The data setup and hold time must not be less than the specified receiver setup and hold time.

Figure 21. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 22. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Environmental Specifications

Environmental Compliance

This CYBT-333032-02 BLE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

This CYBT-3330347-02 BLE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) directives. The Cypress module and components used to produce this module are RoHS.

RF Certification

The CYBT-3330xx-02 module will be certified under the following RF certification standards at production release.

- FCC: WAP3047
- CE
- IC: 7922A-3047
- MIC: 201-180688

Safety Certification

The CYBT-3330xx-02 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

Environmental Conditions

Table 26 describes the operating and storage conditions for the Cypress BLE module.

Table 26. Environmental Conditions for CYBT-3330xx-02

Description	Minimum Specification	Maximum Specification
Operating temperature	–30 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	–40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into end system Components[28]	–	15 kV Air 2.0 kV Contact

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note
28. This does not apply to the RF pins (ANT).

Regulatory Information

FCC

FCC NOTICE:

The device CYBT-3330xx-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. Transmitter operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: **WAP3047**.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP3047".

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in Table 6 on page 14. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antenna in Table 6, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBT-3330xx-02 with the dipole antenna (Antenova_B4844 and Pulse_W1030) is far below the FCC radio frequency exposure limits.

Nevertheless, use CYBT-3330xx-02 in such a manner that it minimizes the potential for human contact during normal operation.End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance. SAR is not required for this module as long as the distance is higher than 9 mm away from the user since the maximum output power is below FCC threshold.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

ISED

Innovation, Science and Economic Development Canada (ISED) Certification

CYBT-3330xx-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development Canada (ISED),

License: IC: **7922A-3047**

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 6 on page 14, having a maximum gain of 2.2 dBi. Antennas not included in this list or having a gain greater than 2.2 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 Ω. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBT-3330xx-02 including the specified antennas comply with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBT-3330xx-02, y compris les antennes spÈcifiÈes, sont conformes aux RËgles RSS-GEN de Canada. L'appareil rÈpond aux exigences d'approbation de l'Ëmetteur modulaire tel que dÈcrit dans RSS-GEN. L'opÈration est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interfÈrences nuisibles, et (2) Cet appareil doit accepter toute interfÈrence reÁue, y compris les interfÈrences pouvant entraÓner un fonctionnement indÈsirable.

ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 10 mm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé. Cet équipement doit être installé et utilisé avec un minimum de 10 mm de distance entre la source de rayonnement et votre corps.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notices above. The IC identifier is **7922A-3047**. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-3047".

European Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBT-3330xx-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

CE

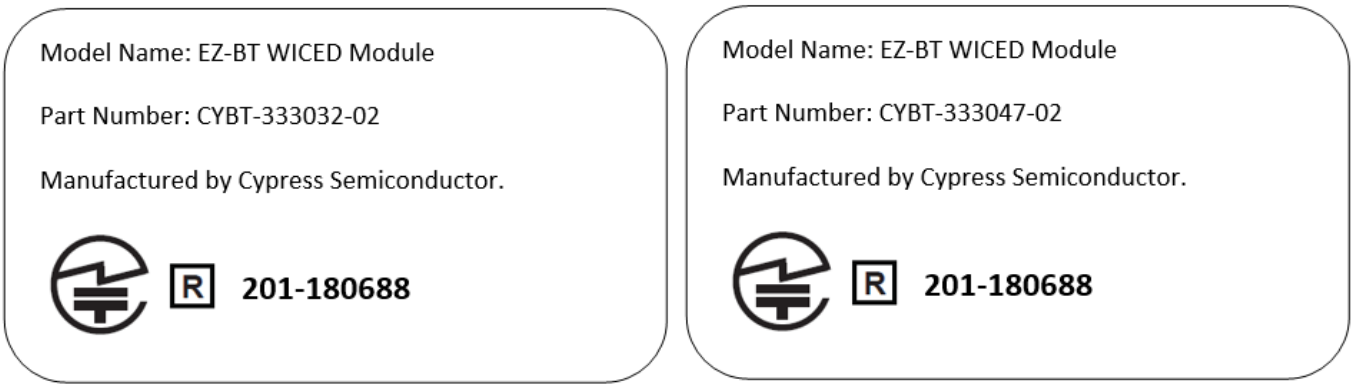
All versions of the CYBT-3330xx-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC Japan

CYBT-3330xx-02 is certified as a module with certification number **201-180688**. End products that integrate CYBT-3330xx-02 do not need additional MIC Japan certification for the end product.

The end product can display the certification label of the embedded module.

Figure 23. MIC Labels for CYBT-333032-02 and CYBT-333047-02



Packaging

Table 27. Solder Reflow Peak Temperature

Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBT-333043-02	24-pad SMT	260 °C	30 seconds	2
CYBT-333047-02	24-pad SMT	260 °C	30 seconds	2

Table 28. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module Part Number	Package	MSL
CYBT-333043-02	26-pad SMT	MSL 3
CYBT-333047-02	26-pad SMT	MSL 3

The CYBT-3330xx-02 is offered in tape and reel packaging. Figure 24 details the tape dimensions used for the CYBT-3330xx-02.

Figure 24. CYBT-3330xx-02 Tape Dimensions

Mesurement	
E	1.75±0.10
F	11.50±0.10
P2	2.00±0.10
∅Do	$1.50^{+0.10}_{-0.00}$
ØD1	$1.50^{+0.10}_{-0.00}$
Po	4.00±0.10
10Po	40.00±0.20
W	24.00±0.30
P	16.00±0.10
Ao	12.40±0.10
B0	13.90±0.10
K0	2.45±0.10
t	0.30±0.05

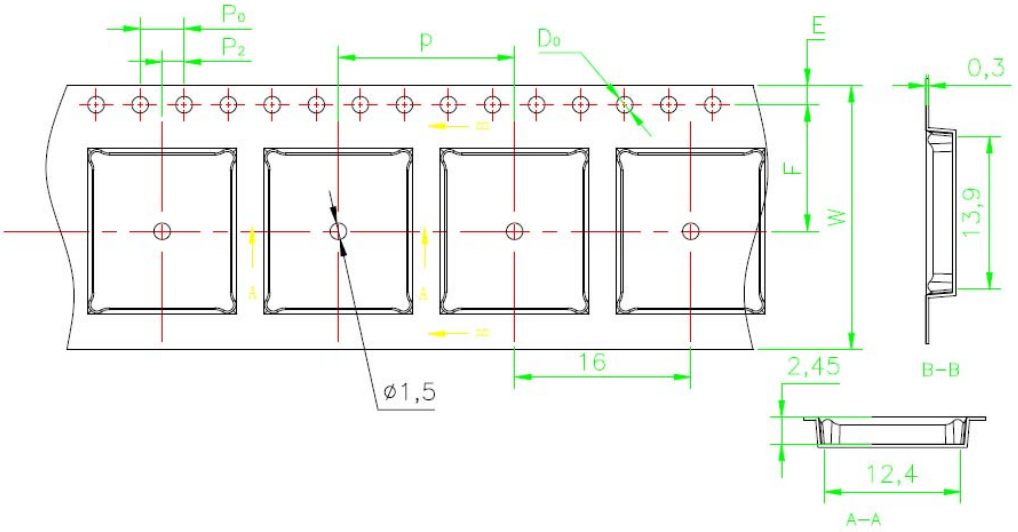


Figure 25 details the orientation of the CYBT-3330xx-02 in the tape as well as the direction for unreeling.

Figure 25. Component Orientation in Tape and Unreeling Direction

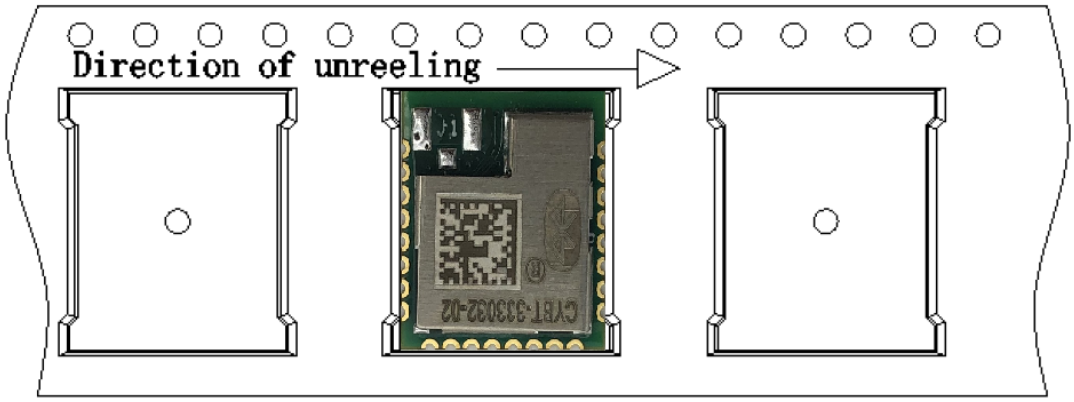
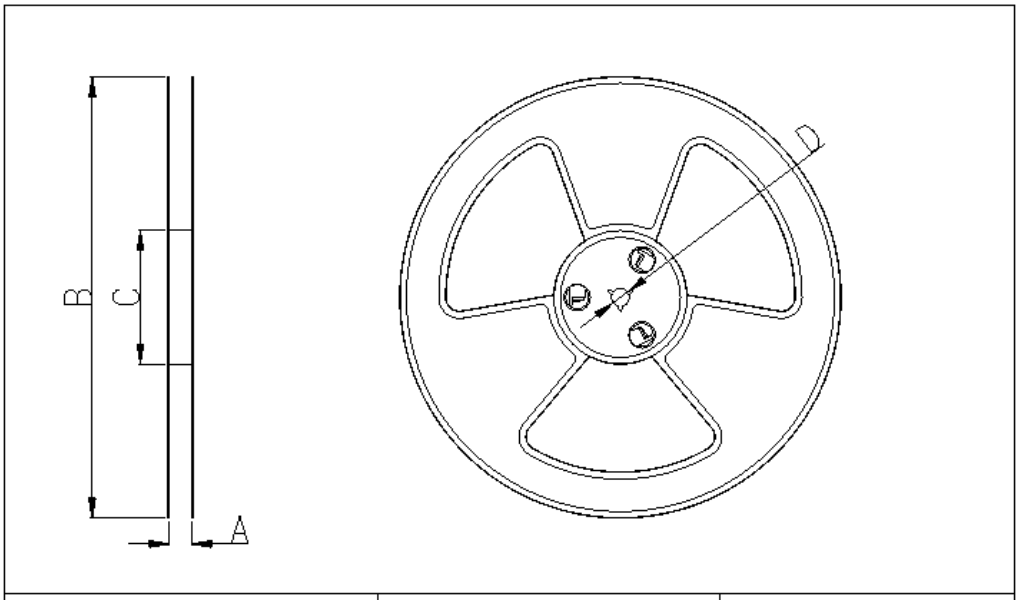


Figure 26 details reel dimensions used for the CYBT-3330xx-02.

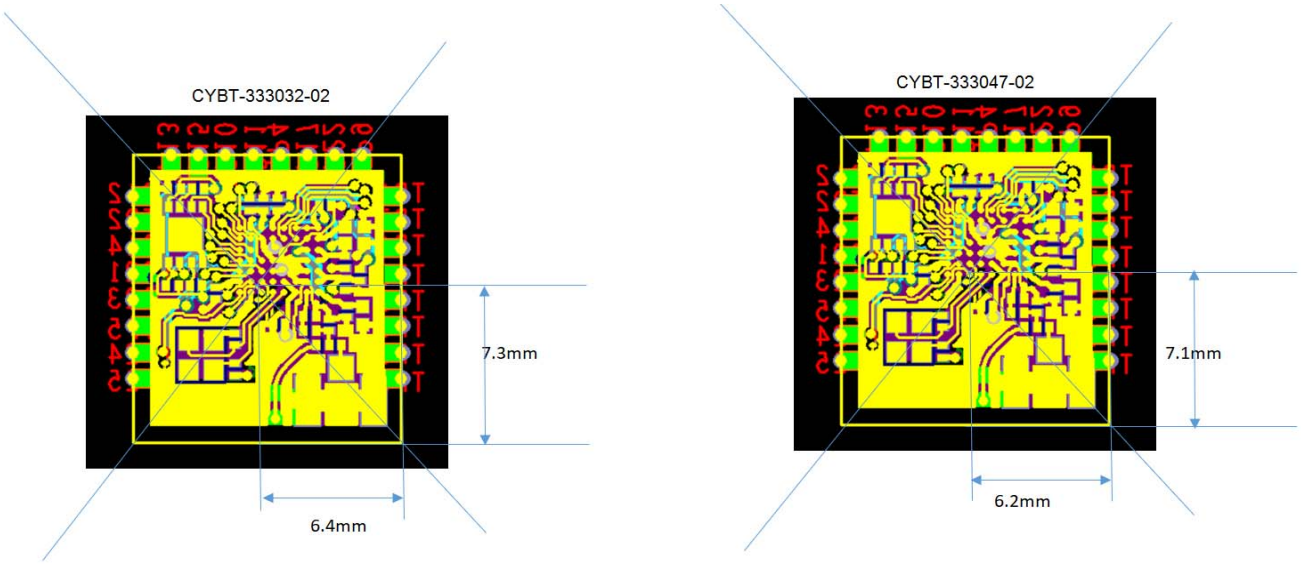
Figure 26. Reel Dimensions



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.4	+2.0mm	−0.0mm
B	Reel Diameter	254.00	+2.0mm	−2.0mm
C	Outer Axis Diameter	100.00	+2.0mm	−2.0mm
D	Inner Axis Diameter	13.20	+0.3mm	−0.2mm

The CYBT-3330xx-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBT-3330xx-02 is detailed in Figure 27.

Figure 27. CYBT-3330xx-02 Center of Mass



Ordering Information

Table 29 lists the CYBT-3330xx-02 part number and features. Table 30 lists the reel shipment quantities for the CYBT-3330xx-02.

Table 29. Ordering Information

Part Number	CPU Speed (MHz)	Flash Size (KB)	RAM Size (KB)	UART	I^2C (BSC)	PWM	Package	Packaging
CYBT-333043-02	24	512	352	Yes	Yes	4	26-SMT	Tape and Reel
CYBT-333047-02	24	512	352	Yes	Yes	4	26-SMT	Tape and Reel

Table 30. Tape and Reel Package Quantity and Minimum Order Amount

Description	Minimum Reel Quantity	Maximum Reel Quantity	Comments
Reel Quantity	500	500	Ships in 500 unit reel quantities.
Minimum Order Quantity (MOQ)	500	–	–
Order Increment (OI)	500	–	–

The CYBT-3330xx-02 is offered in tape and reel packaging. The CYBT-3330xx-02 ships in a reel size of 500.

For additional information and a complete list of Cypress Semiconductor Wireless products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

U.S. Cypress Headquarters Address	198 Champion Court, San Jose, CA 95134
U.S. Cypress Headquarter Contact Info	(408) 943-2600
Cypress website address	http://www.cypress.com

Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
ALU	arithmetic logic unit
AMN	Antenna Matching Network
AMUXBUS	analog multiplexer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CE	European Conformity
CSA	Canadian Standards Association
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
ESD	electrostatic discharge
FCC	Federal Communications Commission
FET	field-effect transistor
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HCI	host controller interface
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
PAL	programmable array logic, see also PLD

Acronym	Description
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QDID	qualification design ID
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
SOC	start of conversion
SOF	start of frame
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.

Table 31. Acronyms Used in this Document

Acronym	Description
PC	program counter
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
STN	super twisted nematic
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TN	twisted nematic
TRM	technical reference manual
TTL	transistor-transistor logic

Acronym	Description
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 32. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Document History Page

Document Title: CYBT-3330xx-02, EZ-BT™ WICED® Module Document Number: 002-25196				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	6480010	SHNG	02/26/2019	Preliminary datasheet for CYBT-3330xx-02 module.
*A	6604799	SHNG	07/09/2019	Updated QDID and Declaration ID in Module Description. Updated MPNs in Packaging and Ordering Information.

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