512 Mb radiation tolerant NOR flash

Serial (QSPI), 3.3 V

General description

The CYEL17B family devices are flash non-volatile memory products using:

- Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) charge trap gate technology
- 40-nm process lithography

The CYEL17B family connects to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single-bit serial input and output is supported as well as optional four-bit wide Quad I/O (QIO) and Quad Peripheral Interface (QPI) commands.

The architecture features a page programming buffer that allows up to 2 KB to be programmed in one operation and provides individual 1 MB sector, 8 MB block, or entire 64 MB chip erase.

By using CYEL17B family devices at the higher clock rates supported, with Quad commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous NOR flash memories while reducing signal count dramatically.

The CYEL17B family products offer high densities coupled with the flexibility and fast performance required by a variety of mobile or embedded applications. Provides an ideal storage solution for systems with limited space, signal connections, and power. These memories offer flexibility and performance well beyond ordinary serial flash devices. They are ideal for FPGA configuration boot memory, code shadowing to RAM, and storing re-programmable data.

Features

- Serial Peripheral Interface (SPI) with multi-I/O
  - Clock polarity and phase modes 0 and 3
  - Quad peripheral interface (QPI) option
  - Extended addressing: 24- or 32-bit address options
- Read
  - Commands: SPI, Quad I/O
  - Modes: Quad Data, Quad I/O, QPI, Continuous (XIP)
  - Serial flash discoverable parameters (SFDP) for configuration information
- Program architecture
  - 2K bytes page programming buffer
- Erase architecture
  - Uniform 1 MB sector erase
  - Uniform 8 MB block erase
  - Chip erase
  - Erase suspend and resume mode for block and sector erase
- 10,000 program/erase cycles (T = 85°C)
- 10 year data retention (T = 125°C)
- Security features
  - Block protection: flexible block range
- Technology
  - 40 nm SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) charge trap memory technology
- Single supply voltage
  - V_{DD} = 2.97 V to 3.63 V

Features

- CMOS I/O support
  - V_{DDIO} = 1.8 V and 3.3 V support
- Temperature range/grade
  - Military (–55°C to +125°C)
- Package
  - 100-lead thin quad flatpack (100-TQFP)
- Radiation data
  - Total dose = > 100 krad
  - Heavy ion single event effects
    - SEU immune
    - SEFI < 2.77×10^{-5} upsets/dev-day
    - Latch up immunity > 81 MeV.cm^2/mg (125°C)

Performance summary

Table 1. Maximum read rates

Command	Clock rate (MHz)	MBps
Read	33	4.125
Quad I/O and QPI Read	133	66.5

Table 2. Maximum program and erase rates

Operation	Rate
2 KB Page Programming	64 KBps (32 ms)
1 MB Sector Erase	47.5 MBps (22 ms)
8 MB Block Erase	47.5 MBps (176 ms)
Full Chip Erase	47.5 MBps (1.5 s)

Table 3. Typical current consumption, –55°C to +125°C

Operation	Typical current	Unit
Quad I/O and QPI Read	50	mA
Program	50	mA
Erase	50	mA
Page/Chip Scrub Flash	50	mA
Page/Chip Scrub SRAM	25	mA
POR (in rush)	15	mA
Standby	5	mA

Table of contents

Table of contents

1 Product overview

1.1 Key features

Table 4 512M CYEL17B512 key features

Parameter	CYEL17B512
Technology node	40-nm
Architecture	SONOS charge trap memory
Release date	Q3'24
Density	512 Mb
Bus width	×1, ×4
Supply voltage	2.97 V–3.63 V
I/O voltage support	2.97 V–3.63 V
	1.71 V–1.89 V
Read speed	4.1 MBps (33 MHz)
Fast read speed	16.5 MBps (133 MHz)
Quad read speed	66 MBps (133 MHz)
Program buffer size	2 KB
Erase sector/block size	1 MB / 8 MB / 64 MB
Sector / block erase time (typ)	47.5 MBps (1 MB)
	47.5 MBps (8 MB)
	47.5 MBps (64 MB)
Page programming rate (typ)	64 KBps (2 KB)
Page scrub time	32 ms
Chip scrub time	1024 s
Block protection	Yes
Erase suspend/resume	Yes
Operating temperature	–55°C to +125°C

2 Connection diagrams

2.1 100-lead thin quad flatpack (100-TQFP)[1]

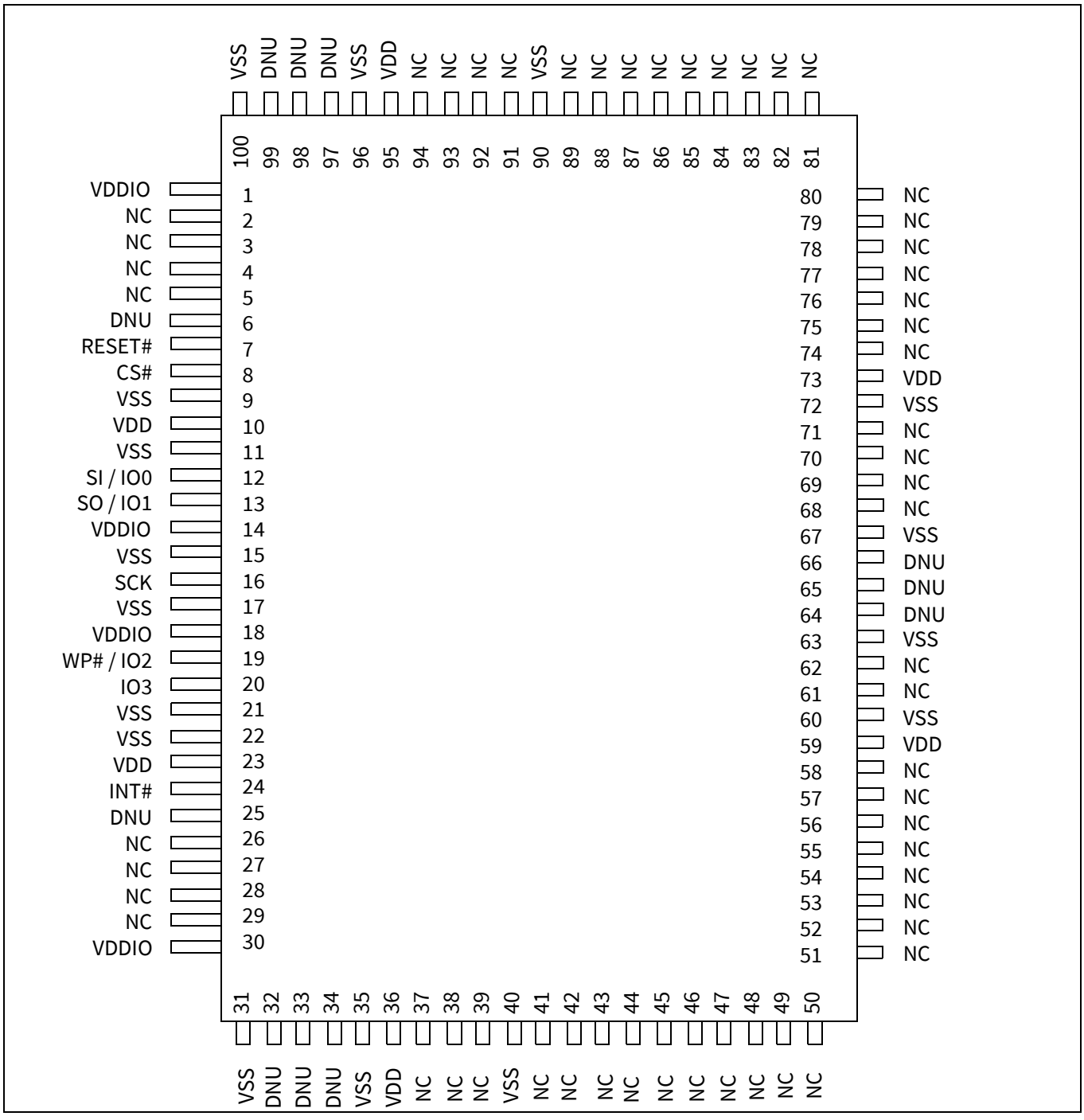


Figure 1 100-lead thin quad flatpack (100TQFP), top view

Note
1. The RESET# input has an internal pull-up and may be left unconnected if hardware reset is not in use.

3 Signal descriptions

3.1 Serial Peripheral Interface with multiple input / output (SPI-QIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The CYEL17B family reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 7 signals. The CYEL17B family uses the industry standard single bit SPI and four bit (Quad) wide serial transfers.

3.2 Input/output summary quad input / output (QIO)

Table 5 Signal list

Signal name	Type	Description
RESET#	Input	Hardware Reset: LOW = Device resets and returns to standby state, ready to receive a command.
SCK	Input	Serial Clock
CS#	Input	Chip Select
SI / IO0	I/O	Serial Input for single bit data commands or IO0 for Quad commands.
SO / IO1	I/O	Serial Output for single bit data commands. IO1 for Quad commands.
WP# / IO2	I/O	Write Protect when not in Quad mode (CR1V[1] = 0 and SR1NV[7] = 1). IO2 when in Quad mode (CR1V[1] = 1). If write protection is enabled by SR1NV[7] = 1 and CR1V[1] = 0, the host system is required to drive WP# HIGH or LOW during a WRR or WRAR command.
IO3	I/O	IO3 in Quad-I/O mode, when Configuration Register 1 QUAD bit, CR1V[1] = 1, or in QPI mode, when Configuration Register 2 QPI bit, CR2V[3] = 1 and CS# is LOW.
INT#	Output (Open Drain)	System Interrupt (INT#). When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.
V_{DD}	Supply	Core Power Supply
V_{SS}	Supply	Core Ground
V_{DDIO}	Supply	I/O Supply
NC	Unused	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a printed circuit board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{DD}.
DNU	Reserved	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the serial input (SI) signal. Data may be sent back to the host serially on the serial output (SO) signal.

Quad input / output (I/O) commands send instructions to the memory only on the SI/IO0 signal. Address or data is sent from the host to the memory as four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as four bit (nibble) groups on IO0, IO1, IO2, and IO3.

QPI mode transfers all instructions, addresses, and data from the host to the memory as four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as four bit (nibble) groups on IO0, IO1, IO2, and IO3.

3.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in commands.

3.4 Chip Select (CS#)

The chip select signal indicates when a command is transferring information to or from the device and the other signals are relevant for the memory device.

When the CS# signal is at the logic HIGH state, the device is not selected and all input signals are ignored and all output signals are high impedance. The device will be in the Standby Power mode, unless an internal embedded operation is in progress. An embedded operation is indicated by the Status Register 1 Work-in-progress bit (SR1V[0]) set to '1', until the operation is completed. Some example embedded operations are: Program, Erase, or Write Registers (WRR) operations.

Driving the CS# input to the logic LOW state enables the device, placing it in the Active power mode. After power-up, a falling edge on CS# is required prior to the start of any command.

3.5 Serial Input (SI) / IO0

This input signals used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal. SI becomes IO0 - an input and output during Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK in commands).

3.6 Serial Output (SO) / IO1

This output signals used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal. SO becomes IO1 - an input and output during Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK in commands).

3.7 Write Protect (WP#) / IO2

When WP# is driven LOW (V_{IL}), when the Status Register Protect 0 (SRP0_NV) or (SRP0) bit of Status Register 1 (SR1NV[7]) or (SR1V[7]) is set to a '1', it is not possible to write to Status Registers, Configuration Registers. In this situation, the command selecting SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV is ignored, and no error is set.

This prevents any alteration of the Block Protection settings. As a consequence, all the data bytes in the memory area that are protected by the Block Protection feature are also hardware protected against data modification if WP# is LOW during commands changing Status Registers, Configuration Registers with SRP0_NV set to '1'.

The WP# function is not available when the Quad mode is enabled (CR1V[1] = 1) or QPI mode is enabled (CR2V[3] = 1). The WP# function is replaced by IO2 for input and output during Quad mode or QPI mode is enabled (CR2V[3] = 1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data on the falling edge of SCK, in commands).

When the WP# function is available when the Quad mode is disabled (CR1V[1] = 0), the pin acts as an input only with no pull up. So it is recommend that the system drive the input high when not using the WP# function.

3.8 IO3

IO3 is used for input and output during Quad mode (CR1V[1] = 1) or QPI mode is enabled (CR2V[3] = 1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in commands). The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.

3.9 RESET#

The RESET# input provides a hardware method of resetting the device to standby state, ready for receiving a command. When RESET# is driven to logic LOW (V_{IL}) for at least a period of t_{RP}, the device starts the hardware reset process.

RESET# causes the same initialization process as is performed when power comes up and requires t_{PU} time.

RESET# may be asserted LOW at any time. To ensure data integrity any operation that was interrupted by a hardware reset should be re-initiated once the device is ready to accept a command sequence. If a page program is interrupted by a reset, the data being programmed as well as the remaining page data may be lost and won't be recovered by re-initiating the page program.

RESET# has an internal pull-up resistor and may be left unconnected in the host system if not used. The internal pull-up will hold Reset HIGH after the host system has actively driven the signal HIGH and then stops driving the signal.

3.10 INT#

The INT# output will transition from HIGH to LOW if an internal interrupt event has occurred and was enabled within the Interrupt Status Register (ISR). The Interrupt Status Register indicates what enabled internal event(s) have occurred since the last time the ISR was cleared. If enabled, the INT# output pin will then transition from HIGH to LOW upon the occurrence of an enabled event. Once the host recognizes that INT# has transitioned to the LOW state the Interrupt Status Register can be read to determine which internal event was responsible. The ISR can be accessed through RDAR/WRAR from the SPI and QPI interfaces. Possible events are 1-bit ECC detection, 2-bit ECC detection, or Ready/Busy signals. This feature can also be disabled/enabled in the ISR.

3.11 Core Voltage Supply (V_{DD})

V_{DD} is the core voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase.

3.12 Versatile I/O Voltage Supply (V_{DDIO})

The versatile I/O (V_{DDIO}) supply is the voltage source for all device input receivers and output drivers and allows the host system to set the voltage levels that the device tolerates on all inputs and drives on outputs (address, control, and I/O signals). The V_{DDIO} range is 1.71 V to 1.89 V or 2.97 V to 3.63 V. V_{DDIO} cannot be greater than V_{DD}. V_{DDIO} may be tied to V_{DD} so that interface signals operate at the same voltage as the core of the device. During the rise of power supplies the V_{DDIO} supply voltage must remain less than or equal to the V_{DD} supply voltage.

3.13 Supply (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, I/Os, and output drivers. It is recommended to connect them to the same ground.

3.14 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a printed circuit board (PCB).

3.15 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

4 Block diagrams

4.1 Logic block diagram

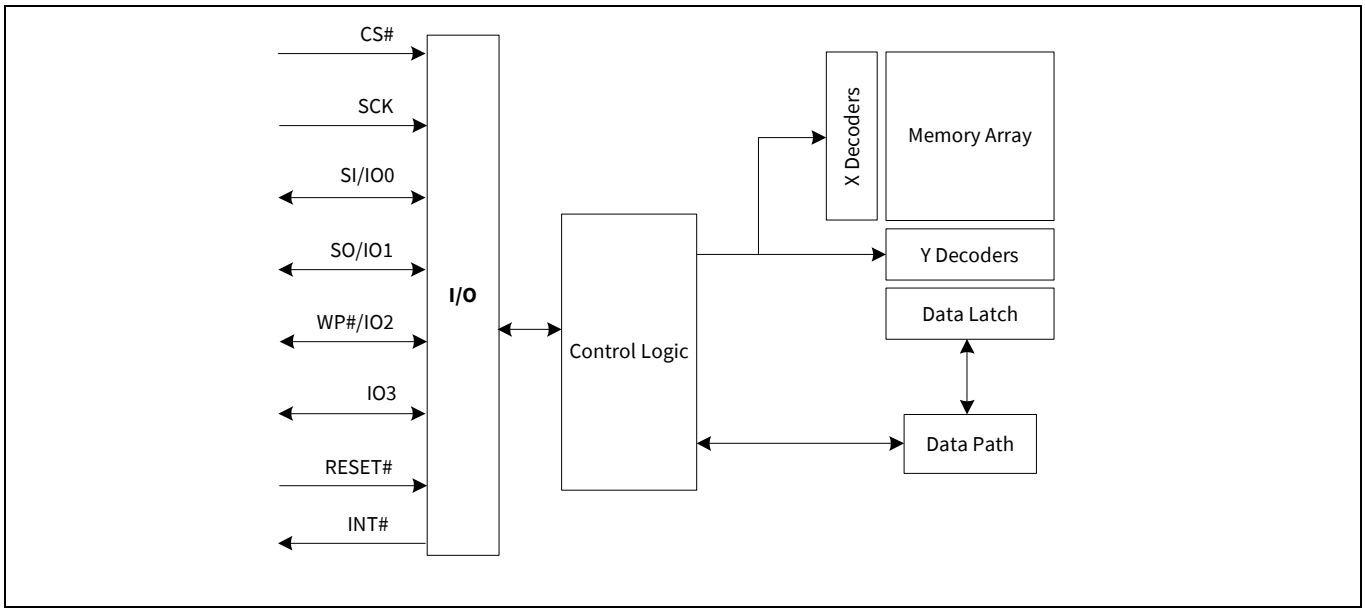


Figure 2 Logic block diagram Quad-SPI

4.2 System block diagram

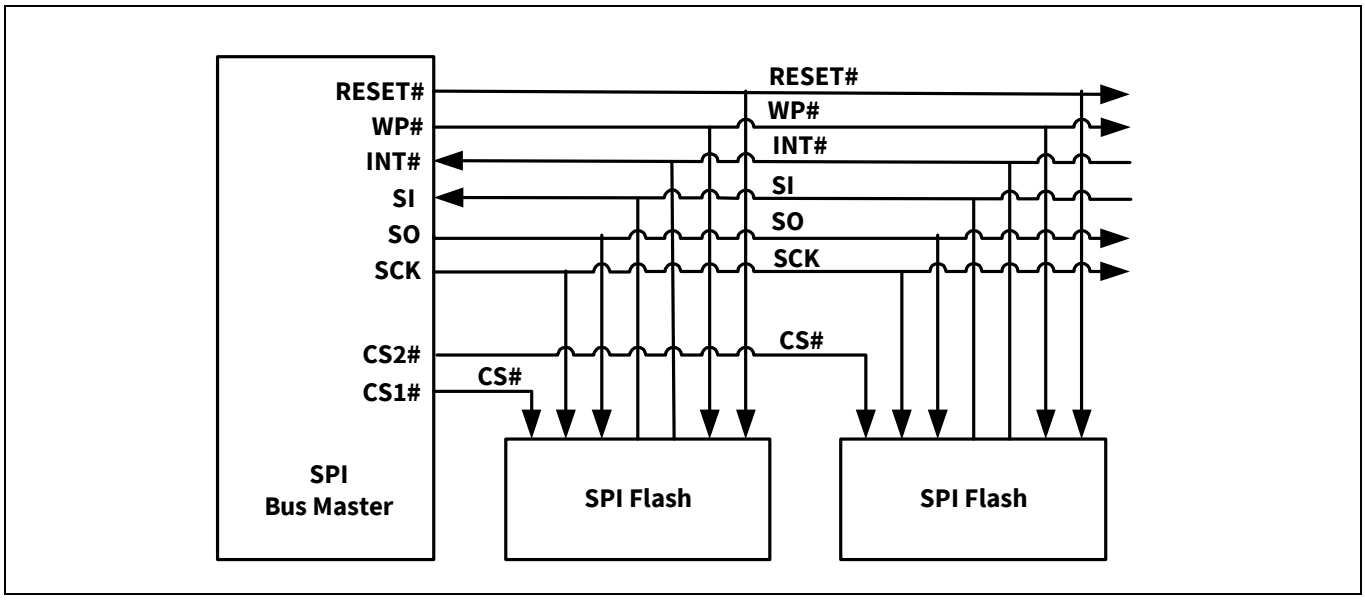


Figure 3 Bus master and memory devices on the SPI bus - Single bit data path

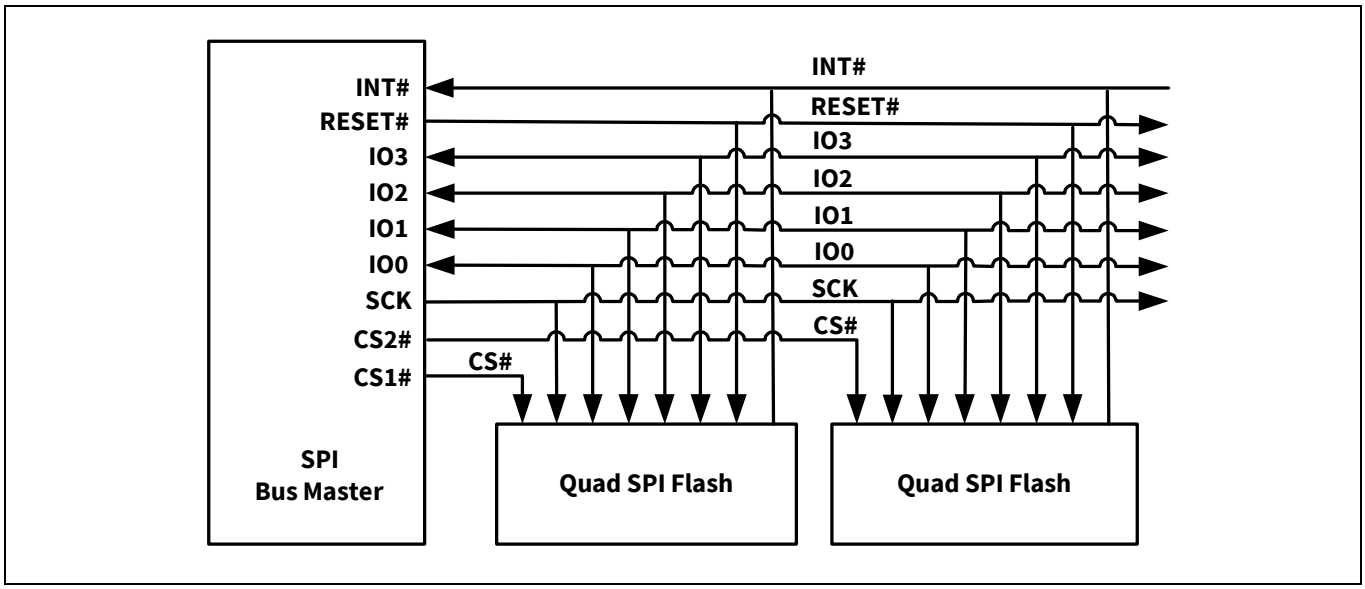


Figure 4 Bus master and memory devices on the SPI bus - Quad bit data path

5 Signal protocols

5.1 SPI clock modes

5.1.1 Single data rate

The CYEL17B family can be driven by an embedded micro-controller (bus master) in either of the two following clocking modes.

- **Mode 0** with clock polarity (CPOL) = 0 and clock phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in Standby mode and not transferring any data.

- SCK will stay at logic LOW state with CPOL = 0, CPHA = 0
- SCK will stay at logic HIGH state with CPOL = 1, CPHA = 1

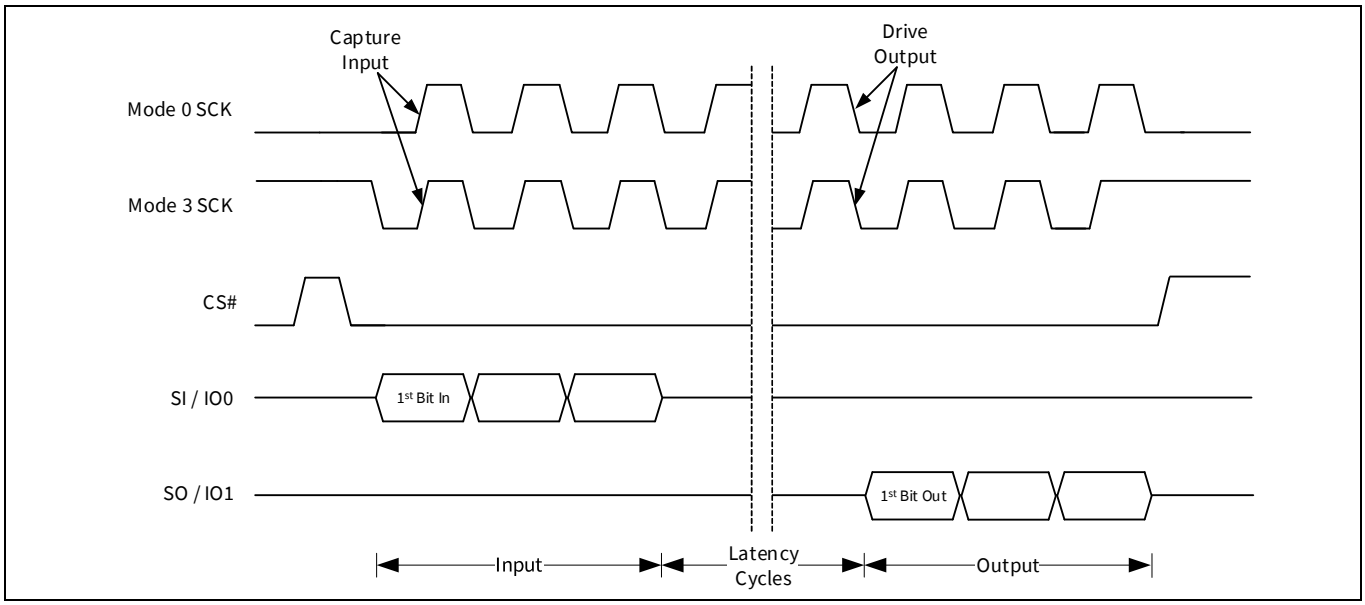


Figure 5 SPI modes supported

The timing diagrams throughout the remainder of the document are generally shown as both Mode 0 and 3 by showing SCK as both HIGH and LOW at the fall of CS#. In some cases a timing diagram may show only Mode 0 with SCK LOW at the fall of CS#. In such a case, Mode 3 timing simply means clock is HIGH at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for Mode 3.

The SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In Mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already LOW at the beginning of a command.

5.2 Command protocol

All communication between the host system and CYEL17B family memory devices is in the form of units called commands. See **"Commands"** on page 39 for definition and details for all commands.

All commands begin with an 8-bit instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory or data transfer from the memory. All instruction, address and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction
- address and instruction modifier (continuous read mode bits)
- data

Single bit wide commands start with an instruction and may provide an address or data, all sent only on the SI signal. Data may be sent back to the host serially on the SO signal. This is referenced as a 1-1-1 command protocol for single bit width instruction-single bit width address and modifier-single bit data.

Quad-O commands provide an address sent from the host as serial on SI (IO0) then followed by dummy-cycles. Data is returned to the host as four-bit (nibble) groups on IO0, IO1, IO2 and IO3. This is referenced as 1-1-4 for Quad-O command protocols.

Quad Input / Output (I/O) commands provide an address sent from the host as four bit (nibble) groups on IO0, IO1, IO2, and IO3 then followed by dummy-cycles. Data is returned to the host similarly as four bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-4-4 for Quad I/O command protocols.

The CYEL17B family also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier and data. This is referenced as a 4-4-4 command protocol.

Commands are structured as follows:

- Each command begins with CS# going LOW and ends with CS# returning HIGH. The memory device is selected by the host driving the Chip Select (CS#) signal LOW throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction selects the type of information transfer or device operation to be performed. The instruction transfers occur on SCK rising edges. However, some read commands are modified by a prior read command, such that the instruction is implied from the earlier command. This is called Continuous Read Mode. When the device is in continuous read mode, the instruction bits are not transmitted at the beginning of the command because the instruction is the same as the read command that initiated the Continuous Read Mode. In Continuous Read mode the command will begin with the read address. Thus, Continuous Read Mode removes eight instruction bits from each read command in a series of same type read commands.
- The instruction may be standalone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit byte boundary address. The address transfers occur on SCK rising edge, in commands.
- In legacy SPI mode, the width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals or they may be done in 4-bit groups per (quad) transfer on the IO0–IO3 signals. Within the quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.
- In QPI mode, the width of all transfers is a 4-bit wide (quad) transfer on the IO0–IO3 signals.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge in commands.

- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy-cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge in commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal HIGH. The CS# signal can be driven HIGH after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input HIGH. The CS# signal must go HIGH after the eighth bit, of a stand-alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven HIGH when the number of bits after the CS# signal was driven LOW is an exact multiple of eight bits. If the CS# signal does not go HIGH exactly at the eight bit boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address and mode bits are shifted into the device with the most significant bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

5.2.1 Command sequence examples

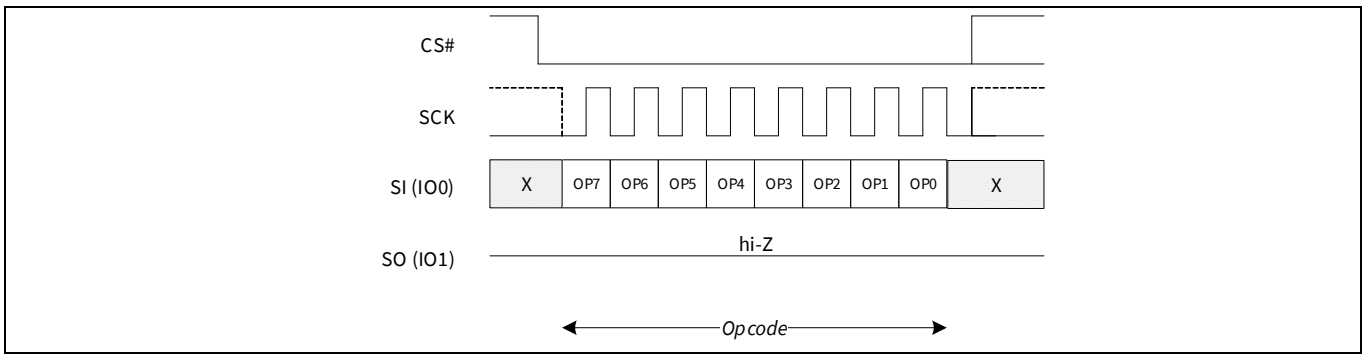


Figure 6 Standalone Instruction command

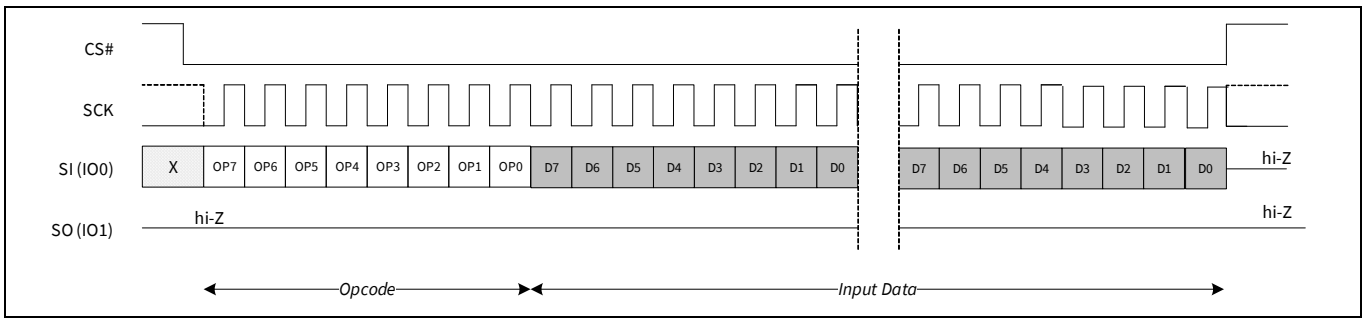


Figure 7 Single Bit Wide Input command

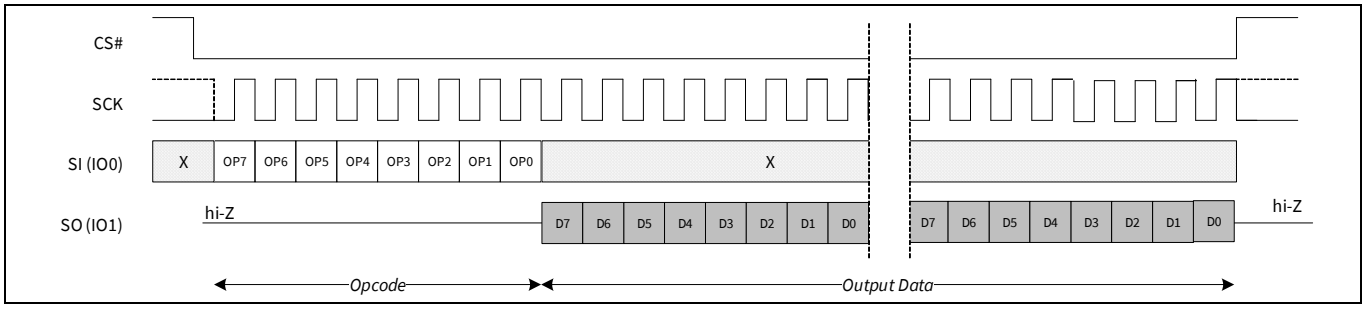


Figure 8 Single Bit Wide Output command without latency

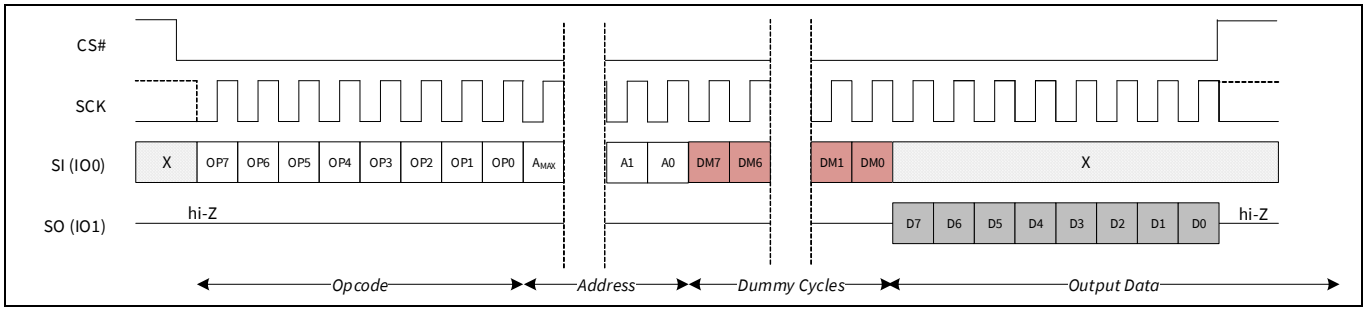


Figure 9 Single Bit Wide I/O command with latency

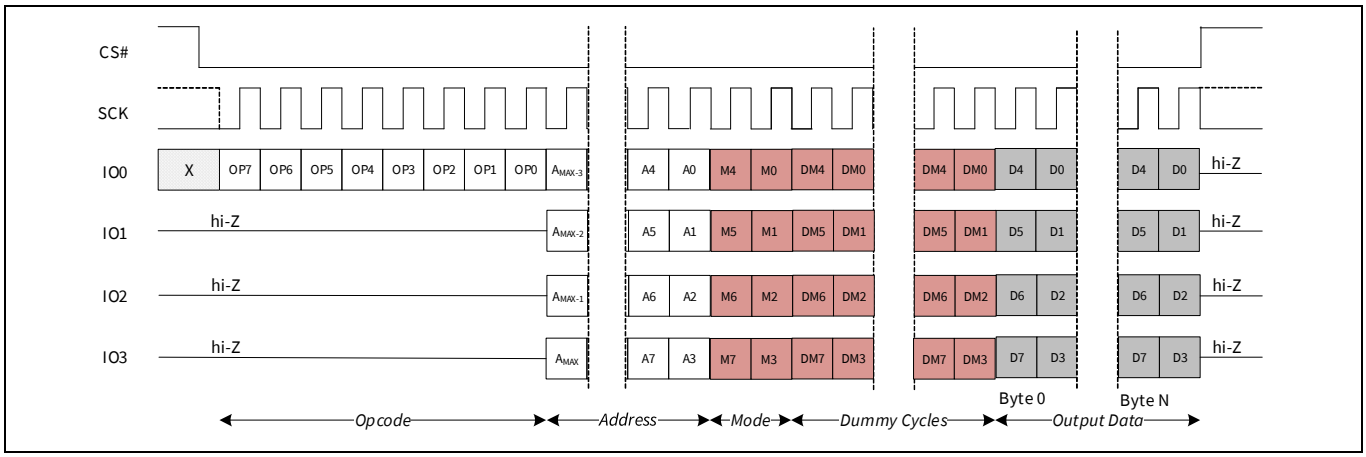


Figure 10 Quad I/O command

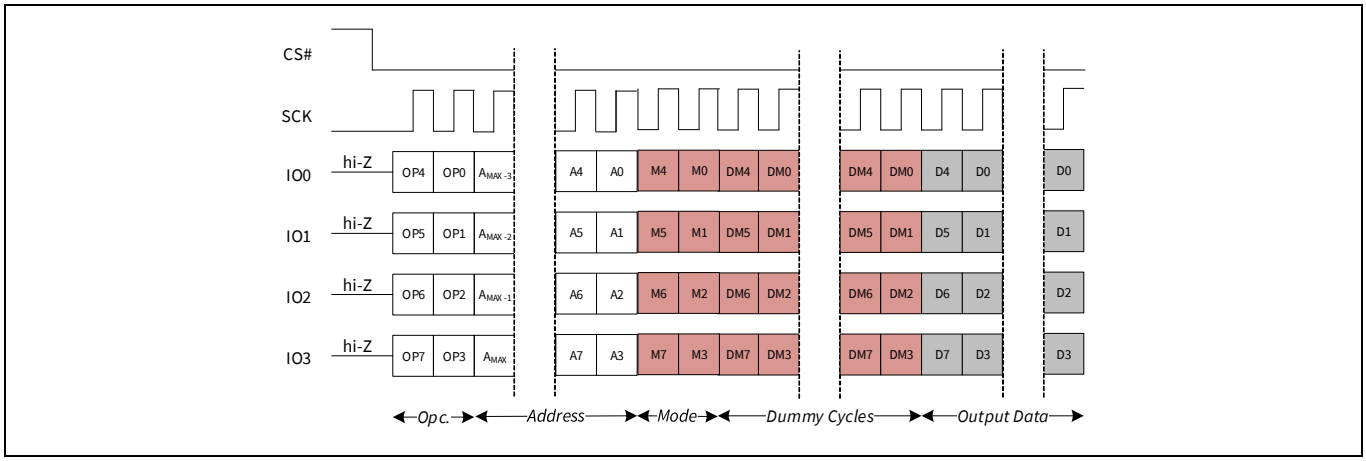


Figure 11 Quad I/O Read command in QPI mode

Additional sequence diagrams, specific to each command, are provided in **"Commands"** on page 39.

6 Address space map

6.1 Overview

6.1.1 Extended address

The CYEL17B family supports 32-bit (4-byte) addresses to enable higher density devices than allowed by previous generation (legacy) SPI devices that supported only 24-bit (3-byte) addresses. A 24-bit, byte resolution, address can access only 16 MB (128 Mb) maximum density. A 32-bit, byte resolution, address allows direct addressing of up to a 4 GB (32 Gb) address space.

Legacy commands continue to support 24-bit addresses for backward software compatibility. Extended 32-bit addresses are enabled in two ways:

- Extended address mode — a volatile configuration register bit that changes all legacy commands to expect 32-bits of address supplied from the host system.
- 4-byte address commands — that perform both legacy and new functions, which always expect 32-bit address.

The default condition for extended address mode, after power-up or reset, is controlled by a non-volatile configuration bit. The default extended address mode may be set for 24- or 32-bit addresses. This enables legacy software compatible access to the first 128 Mb of a device or for the device to start directly in 32-bit address mode.

6.1.2 Multiple address spaces

Many commands operate on the main Flash memory array. Some commands operate on address spaces separate from the main Flash array. Each separate address space uses the full 24-or 32-bit address but may only define a small portion of the available address space.

6.2 Flash memory array

The main flash array is divided into uniform erase units called physical blocks (8 MB) sectors (1 MB) and page (2 KB).

Table 6 CYEL17B512 sector address map

Block size (MB)	Block count	Block range	Sector size (MB)	Sector count	Sector range	Page size (KB)	Page count	Address range (byte address)	Notes
8	1	BA00	1	1	SA00	2	1	0000000h–00007FFh	Starting Address — Ending Address
						:	:	:	
			1	8	SA07	2	4096	07FF800h–07FFFFFh	
:	:	:	:	:	:	:	:	:	
8	8	BA07	1	56	SA55	2	28672	3800000h–38007FFh	
						:	:	:	
			1	64	SA63	2	32768	3FFF800h–3FFFFFFh	

6.3 ID address space

6.3.1 Device ID

The RDID command (9Fh) reads information from a separate Flash memory address space for device identification (ID). See **"Device ID address map"** on page 116 for the tables defining the contents of the ID address space. The ID address space is programmed by Infineon and read-only for the host system. The RDID command operates on the lowest address die only.

6.3.2 Device unique ID

A 64-bit unique number is located in 8 bytes of the Unique Device ID address space, see **Table 44**. This unique ID may be used as a software readable serial number that is unique for each device.

6.4 JEDEC JESD216 serial flash discoverable parameters (SFDP) space

The RSFDP command (5Ah) reads information from a separate Flash memory address space for device identification, feature and configuration information in accordance with the JEDEC JESD216 standard for Serial Flash Discoverable Parameters. The ID address space is incorporated as one of the SFDP parameters. See **"JEDEC JESD216D serial flash discoverable parameters"** on page 98 for the tables defining the contents of the SFDP address space. The SFDP address space is programmed by Infineon and read-only for the host system.

6.5 Registers

The registers are small groups of memory cells used to configure how the CYEL17B family memory device operates or to report the status of device operations. The registers are accessed by specific commands. The commands (and hexadecimal instruction codes) used for each register are noted in each register description.

In legacy SPI memory devices the individual register bits could be a mixture of volatile, non-volatile or one-time programmable (OTP) bits within the same register. In some configuration options the type of a register bit could change e.g. from non-volatile to volatile.

The CYEL17B family uses separate non-volatile or volatile memory cell groups (areas) to implement the different register bit types. However, the legacy registers and commands continue to appear and behave as they always have for legacy software compatibility. There is a non-volatile and a volatile version of each legacy register when that legacy register has volatile bits or when the command to read the legacy register has zero read latency. During power-on reset (POR), hardware reset or software reset the non-volatile version of a register is copied to the volatile version to provide the default state of the volatile register. When non-volatile register bits are written, the non-volatile version of the register is erased and programmed with the new bit values and the volatile version of the register is updated with the new contents of the non-volatile version. When volatile register bits are written, only the volatile version of the register has the appropriate bits updated.

The type for each bit is noted in each register description. The default state shown for each bit refers to the state after power-on reset, hardware reset or software reset if the bit is volatile. If the bit is non-volatile the default state is the value of the bit when the device is shipped from Infineon.

6.5.1 Status Register 1

6.5.1.1 Status Register 1 Non-volatile (SR1NV)

Related commands: Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 7 Status Register 1 Non-volatile (SR1NV)

Bits	Field name	Function	Type	Default state	Description
7	SRP0_NV	Status Register Protect 0	Non-volatile	0	Provides the default state for SRP0.
6	RFU	Reserved	Non-volatile	0	Reserved for Future Use.
5	TBPROT_NV	TBPROT	Non-volatile	0	Provides the default state for TBPROT.
4	BP_NV2	Block Protection	Non-volatile	000b	Provides the default state for BP bits.
3	BP_NV1				
2	BP_NV0				
1	WEL_D	WEL	Non-volatile read-only	0	Provides the default state for the WEL Status. Not user programmable.
0	WIP_D	WIP	Non-volatile read-only	0	Provides the default state for the WIP Status. Not user programmable.

- **Status Register Protect Non-volatile (SRP0_NV) SR1NV[7]:** Provides the default state for SRP0. See **"Status Register Protect (SRP0)"** on page 37.
- **Top or Bottom Protection (TBPROT_NV) SR1NV[5]:** Provides the default state for TBPROT.
- **Block Protection (BP_NV2, BP_NV1, BP_NV0) SR1NV[4:2]:** Provides the default state for BP_2 to BP_0 bits.
- **Write Enable Latch Default (WEL_D) SR1NV[1]:** Provides the default state for the WEL Status in SR1V[1]. This bit is programmed by Infineon and is not user programmable.
- **Write In Progress Default (WIP_D) SR1NV[0]:** Provides the default state for the WIP Status in SR1V[0]. This bit is programmed by Infineon and is not user programmable.

6.5.1.2 Status Register 1 Volatile (SR1V)

Related commands: Read Status Register 1 (RDSR1 05h), Write Enable (WREN 06h), Write Registers (WRR 01h), Clear Status Register (CLSR 30h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDSR1 command.

Table 8 CYEL17B512 Status Register 1 Volatile (SR1V)

Bits	Field name	Function	Type	Default state	Description
7	SRP0	Status Register Protect 0	Volatile	SR1NV	1 = Locks state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV when WP# is LOW, by not executing any command that would affect SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV. 0 = No register protection, even when WP# is LOW.
6	RFU	Reserved	Non-volatile		Reserved for Future Use
5	TBPROT	Top or Bottom Relative Protection	Volatile		1 = BP starts at bottom (Low address). 0 = BP starts at top (High address).
4	BP2	Block Protection Volatile	Volatile		Protects the selected range of sectors (Blocks) from Program or Erase.
3	BP1				
2	BP0				
1	WEL	Write Enable Latch	Volatile read-only		0 = Not write enabled, no embedded operation can start. 1 = Write Enable, embedded operation can start. This bit is not affected by WRR or WRAR, only WREN, WRDI and CLSR commands affect this bit.
0	WIP	Write in Progress	Volatile read-only		1 = Device Busy, an embedded operation is in progress such as program or erase. 0 = Ready Device is in standby mode and can accept commands. This bit is not affected by WRR or WRAR, it only provides WIP status.

- **Status Register Protect 0 (SRP0) SR1V[7]:** Places the device in the Hardware Protected mode when this bit is set to '1' and the WP# input is driven LOW. In this mode, any commands that change status registers or configuration registers are ignored and not accepted for execution, effectively locking the state of the Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV bits, by making the registers read-only. If WP# is HIGH, Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV may be changed.
  If SRP0 is '0', WP# has no effect, the Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV may be changed. WP# has no effect on the writing of any other registers. SRP0 tracks any changes to the non-volatile version of this bit (SRP0_NV). When QPI or QIO mode is enabled (CR2V[3] or CR1V[1] = '1') the internal WP# signal level is = 1 because the WP# external input is used as IO2 when either mode is active. This effectively turns off hardware protection. The Register SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V and CR3NV are unlocked and can be written. See **"Status Register Protect (SRP0)"** on page 37.

- **TBPROT SR1V[5]:** This bit defines the reference point of the Block Protection bits BP3, BP2, BP1 and BP0 in the Status Register. As described in the status register section, the BP3–0 bits allow the user to optionally protect a portion of the array, ranging from 1/64, ¼, ½, etc., up to the entire array. When TBPROT is set to a '0' the Block Protection is defined to start from the top (maximum address) of the array. When TBPROT is set to a '1' the Block Protection is defined to start from the bottom (zero address) of the array. TBPROT tracks any changes to the non-volatile version of this bit (TBPROT_NV).
- **Block Protection (BP2, BP1, BP0) SR1V[4:2]:** These bits define the main Flash array area to be protected against program and erase commands. See **"Block protection"** on page 38 for a description of how the BP bit values select the memory array area protected.
- **Write Enable Latch (WEL) SR1V[1]:** The WEL bit must be set to '1' to enable program, write or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to a '1' to allow any program, erase or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to a '0' to prevent all program, erase and write commands from execution. The WEL bit is cleared to '0' at the end of any successful program, write or erase operation. Following a failed operation the WEL bit may remain set and should be cleared with a WRDI command. After a power-down / power-up sequence, hardware-reset or software-reset, the Write Enable Latch is set to a WEL_D. The WRR or WRAR command does not affect this bit.
- **Work In Progress (WIP) SR1V[0]:** Indicates whether the device is performing a program, write, erase operation or any other operation during which a new operation command will be ignored. When the bit is set to a '1' the device is busy performing an operation. While WIP is '1', only Read Status Registers (RDSR1, RDSR2), Read Any Register (RDAR), Erase Suspend (EPS), Clear Status Register (CLSR), Read Configuration Registers (RDCR1, RDCR2, RDCR3) and Software Reset (RSTEN 66h followed by RST 99h) commands are accepted. EPS command will only be accepted if memory array erase or program operations are in progress. The status register E_ERR and P_ERR bits are updated while WIP = 1. When P_ERR or E_ERR bits are set to '1', the WIP bit will remain set to '1' indicating the device remains busy and unable to receive new operation commands. A Clear Status Register (CLSR) command must be received to return the device to standby mode. When the WIP bit is cleared to '0' no operation is in progress. This is a read-only bit.

6.5.2 Status Register 2 Volatile (SR2V)

Related commands: Read Status Register 2 (RDSR2 07h), Read Any Register (RDAR 65h). Status Register 2 does not have user programmable non-volatile bits, all defined bits are volatile read-only status. The default state of these bits are set by hardware.

Table 9 Status Register 2 Volatile (SR2V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	–	0	Reserved for Future Use
6	E_ERR	Erase error occurred	Volatile read-only	0	1= Error occurred 0 = No Error
5	P_ERR	Programming error occurred	Volatile read-only	0	1 = Error occurred 0 = No Error
4	RFU	Reserved	–	0	Reserved for Future Use
3	RFU	Reserved	–	0	Reserved for Future Use
2	RFU	Reserved	–	0	Reserved for Future Use
1	ES	Erase Suspend	Volatile read-only	0	1 = In Erase Suspend mode 0 = Not in Erase Suspend mode
0	RFU	Reserved	–	0	Reserved for Future Use

- **Erase Error (E_ERR) SR2V[6]:** The erase error bit is used as an erase operation success or failure indication. When the Erase Error bit is set to a '1' it indicates that there was an error in the last erase operation. This bit will also be set when the user attempts to erase an individual protected main memory sector. The Chip Erase command will not set E_ERR if a protected sector is found during the command execution. When the erase error bit is set to a '1' this bit can be cleared to zero with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.
- **Program Error (P_ERR) SR2V[5]:** The Program Error bit is used as a program operation success or failure indication. When the program error bit is set to a '1' it indicates that there was an error in the last program operation. This bit will also be set when the user attempts to program within a protected main memory sector. When the Program Error bit is set to a '1' this bit can be cleared to zero with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.
- **Erase Suspend (ES) SR2V[1]:** The Erase Suspend bit is used to determine when the device is in Erase Suspend mode. This is a status bit that cannot be written by the user. When Erase Suspend bit is set to '1', the device is in Erase Suspend mode. When Erase Suspend bit is cleared to '0', the device is not in Erase Suspend mode. Refer to **"Erase Suspend (EPS 75h)"** on page 90 for details about the Erase Suspend/Resume commands.

6.5.3 Configuration Register 1

Configuration Register 1 controls certain interface and data protection functions. The register bits can be changed using the WRR command with sixteen input cycles or with the WRAR command.

6.5.3.1 Configuration Register 1 Non-volatile (CR1NV)

Related commands: Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 10 Configuration Register 1 Non-volatile (CR1NV)

Bits	Field name	Function	Type	Default state	Description
7	CSCRBT_NV	Chip Scrub Target Selection	Non-volatile	0	Target device for Chip Scrub: 0 = Flash 1 = MCU SRAM
6	WL_NV	Wrap Length		00	00 = 8-byte wrap 01 = 16-byte wrap 10 = 32-byte wrap 11 = 64-byte wrap
5					
4	WE_NV	Wrap Enable		0	1 = Wrap Enabled 0 = Wrap Disabled
3	RFU	Reserved		0	Reserved for Future Use
2	RFU	Reserved		0	Reserved for Future Use
1	QUAD_NV	Quad Default		0	Provides the default state for QUAD.
0	AD34_NV	Address Length at Power-up		0	Provides the default state for Address Length 1 = 4-byte address 0 = 3-byte address

- **Chip Scrub Target Selection Non-volatile CR1NV[7]:** This bit controls the target of the Chip Scrub command. When set to '0', the Chip Scrub command (CSCRB) will operate on the Flash memory. When set to '1', the Chip Scrub command (CSCRB) will operate on the MCU SRAMs.
- **Wrap Length Non-volatile CR1NV[6:5]:** These bits controls the POR, hardware reset or software reset state of the wrapped read length and alignment.
- **Wrap Enable Non-volatile CR1NV[4]:** This bit controls the POR, hardware reset or software reset state of the wrap enable. The commands affected by Wrap Enable are: Read, Read (4-byte), Fast Read, Fast Read (4-byte), Quad Output Read, Quad Output Read (4-byte), Read Quad I/O, and read Quad I/O (4-byte). This configuration bit enables the device to start immediately (boot) in wrapped burst read mode rather than the legacy sequential read mode.
- **Quad Data Width Non-volatile (QUAD_NV) CR1NV[1]:** Provides the default state for the QUAD bit in CR1V[1]. The WRR or WRAR command affects this bit. Programming CR1NV[1] = 1 will default operation to allow Quad-data-width commands at Power-on or Reset.
- **Address Length at Power-up Non-volatile CR1NV[0]:** This bit controls the POR, hardware reset or software reset state of the expected address length for all commands that require address and are not fixed 3-byte or 4-byte only address. Most commands that need an address are legacy SPI commands that traditionally used 3-byte (24-bit) address. For device densities greater than 128 Mb, a 4-byte (32-bit) address is required to access the entire memory array. The address length configuration bit is used to change all 3-byte address commands to expect 4-byte address. This non-volatile Address Length configuration bit enables the device to start immediately (boot) in 4-byte address mode rather than the legacy 3-byte address mode.

6.5.3.2 Configuration Register 1 Volatile (CR1V)

Related commands: Read Configuration Register 1 (RDCR1 35h), Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDCR1 command. The register can also be written by the Set Wrap Length (SWL 77h) command.

Table 11 Configuration Register 1 Volatile (CR1V)

Bits	Field name	Function	Type	Default state	Description
7	CSCRBT	Chip Scrub Target Selection	Volatile	CR1NV	Target device for Chip Scrub: 0 = Flash 1 = MCU SRAM
6	WL	Wrap Length			00 = 8-byte wrap 01 = 16-byte wrap 10 = 32-byte wrap 11 = 64-byte wrap
5					
4	WE	Wrap Enable			1 = Wrap Enabled 0 = Wrap Disabled
3	RFU	Reserved			Reserved for Future Use
2	RFU	Reserved			Reserved for Future Use
1	QUAD	Quad Default			The QUADIT bit selects the I/O width of the device. When configured to 4-bits (QUAD), WP# becomes IO2 and IO3 becomes active I/O signal. Selection options: 0 = Data Width set to 1 bit wide 1 = Data Width set to 4 wide (Quad)
0	AD34	Address Length at Power-up			Read Status Only Bit 1 = 4-byte address 0 = 3-byte address

- **Chip Scrub Target Selection CR1V[7]:** This bit controls the target of the Chip Scrub command. When set to '0', the Chip Scrub command (CSCRB) will operate on the Flash memory. When set to '1', the Chip Scrub command (CSCRB) will operate on the MCU SRAMs.
- **Wrap Length CR1V[6:5]:** These bits control the wrapped read length and alignment during normal operation. These volatile configuration bits enable the user to adjust the burst wrapped read length during normal operation.
- **Wrap Enable CR1V[4]:** This bit controls the burst wrap feature. This volatile configuration bit enables the device to enter and exit burst wrapped read mode during normal operation. When CR1V[4] = 0, the wrap mode is not enabled and unlimited length sequential read is performed. When CR1V[4] = 1, the wrap mode is enabled and a fixed length and aligned group of 8, 16, 32 or 64 bytes is read starting at the byte address provided by the read command and wrapping around at the group alignment boundary.
- **Quad Data Width (QUAD) CR1V[1]:** When set to '1', this bit switches the data width of the device to 4-bit - Quad mode. That is, WP# becomes IO2 and IO3 becomes an active I/O signal. The WP# input is not monitored for its normal function and is internally set to HIGH (inactive). The commands for Serial Reads still function normally but, there is no need to drive the WP# input for those commands when switching between commands using different data path widths. The QUAD bit must be set to one when using the Quad Output Read, Quad I/O Read.

- **Address Length (AD34) CR1V[0]:** This bit shows what the address length will be after power-on reset, hardware reset or software reset for all commands that require address and are not fixed 3-byte or 4-byte address. This volatile register bit is also updated when the 4BAM or 4BEX opcodes are issued.
  - It is not legal to use WRAR to address 0x00800002 to set and clear the AD34 volatile bit. It may only be changed using 4BAM/4BEX or in conjunction with a write to the corresponding non-volatile bit.
  - Is it not legal to use WRAR to address 0x00800002 to set and clear the QUAD volatile bit. It may only be changed in conjunction with a write to the corresponding nonvolatile bit.

6.5.4 Configuration Register 2

Configuration Register 2 controls certain interface functions. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The non-volatile version of the register provides the ability to set the POR, hardware reset or software reset state of the controls. The volatile version of the register controls the feature behavior during normal operation.

6.5.4.1 Configuration Register 2 Non-volatile (CR2NV)

Related commands: Non-volatile Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 12 Configuration Register 2 Non-volatile (CR2NV)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	Non-volatile	0	Reserved for Future Use
6	ODS_NV	Drive Strength		0	Provides the default output drive strength. See **Table 13**.
5				0	
4				0	
3	QPI_NV	QPI		0	1 = Enabled -- QPI (4-4-4) protocol in use 0 = Disabled -- Legacy SPI protocols in use, instruction is always serial on SI Provides the default state for QPI mode.
2	RFU	Reserved		0	Reserved for Future Use
1	RFU	Reserved		0	Reserved for Future Use
0	RFU	Reserved		0	Reserved for Future Use

- **Output Drive Strength Non-volatile CR2NV[6:4]:** These bits control the POR, hardware reset, or software reset state of the IO signal output drive strength. Multiple drive strengths are available to help match the output impedance with the system printed circuit board environment to minimize overshoot and ringing. These non-volatile output drive strength configuration bits enable the device to start immediately (boot) with the appropriate drive strength.

Table 13 Output impedance control

CR2NV[6:5] Impedance selection	Drive strength (mA)	Notes
X00	12	12 mA is the factory default configuration. Other drive strengths can be programmed by writing into impedance selection bits in CR2[6:4].
X01	8	
X10	4	
X11	2	

- **QPI Non-volatile CR2NV[3]:** This bit controls the POR, hardware reset or software reset state of the expected instruction width for all commands. Legacy SPI commands always send the instruction one bit wide (serial I/O) on the SI (IO0) signal. The CYEL17B family also supports the QPI mode in which all transfers between the host system and memory are 4 bits wide on IO0 to IO3, including all instructions. This non-volatile QPI configuration bit enables the device to start immediately (boot) in QPI mode rather than the legacy serial instruction mode. The recommended procedure for moving to QPI mode is to first use the QPIEN (38h) command, the WRR or WRAR command can also set CR2V[3] = 1, QPI mode. Following commands can then be immediately sent in QPI protocol. The WRAR command can be used to program CR2NV[3] = 1, followed by polling of SR1V[0] to know when the programming operation is completed. Similarly, to exit QPI mode use the QPIEX (F5h) command. The WRR or WRAR command can also be used to clear CR2V[3] = 0.

6.5.4.2 Configuration Register 2 Volatile (CR2V)

Related commands: Read Configuration Register 2 (RDCR2 15h), Read Any Register (RDAR 65h), Write Enable (WREN 06h), Write Register (WRR 01h), Write Any Register (WRAR 71h), Enter 4-byte Address Mode (4BAM B7h), Exit 4-byte Address Mode (4BEX E9h), Enter QPI (QPIEN 38h), Exit QPI (SPIEN F5h). This is the register displayed by the RDCR2 command.

Table 14 Configuration Register 2 Volatile (CR2V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	Volatile	0	Reserved for Future Use
6	ODS	Drive Strength		CR2NV	See **Table 13**.
5					
4					
3	QPI	QPI			1 = Enabled -- QPI (4-4-4) protocol in use 0 = Disabled -- Legacy SPI protocols in use
2	RFU	Reserved		0	Reserved for Future Use
1	RFU	Reserved		0	Reserved for Future Use
0	RFU	Reserved		0	Reserved for Future Use

- **Output Drive Strength CR2V[6:5]:** These bits control the IO signal output impedance (drive-strength). This volatile output impedance configuration bit enables the user to adjust the drive-strength during normal operation.
- **QPI CR2V[3]:** This bit controls the expected instruction width for all commands. This volatile QPI configuration bit enables the device to enter and exit QPI mode during normal operation. When this bit is set to QPI mode, the QUAD mode is active, independent of the setting of QIO mode (CR1V[1]). When this bit is cleared to legacy SPI mode the QUAD bit is not affected. The QPI CR2V[3] bit can also be set to '1' by the QPIEN (38h) command and set to '0' by the QPIEX (F5h) command.

Table 15 QPI and QIO mode control bits

QPI CR2V[3]	QUAD CR1V[1]	Description
0	0	SIO mode: Single Read, WP#/IO2 input is in use as WP# pin.
0	1	QIO mode: Single, and Quad Read, WP#/IO2 input is in use as IO2.
1	X	QPI mode: Quad Read, WP#/IO2 input is in use as IO2.

6.5.5 Configuration Register 3

The register bits can be read and changed using the, Read Configuration 3 (RDCR3 33h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

6.5.5.1 Configuration Register 3 Non-volatile (CR3NV)

Related commands: Non-volatile Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 16 Configuration Register 3 Non-volatile (CR3NV)

Bits	Field name	Function	Type	Default state	Description
7	ECCS_NV	ECC Error Selection	Non-volatile	0	1 = 1-bit/2-bit Error Detection & Correction Enabled 0 = 2-bit Error Detection & Correction Enabled (DECDED ECC always enabled; register only controls what is stored in the ADDTRAP)
6	RFU	Reserved		0	Reserved for future use.
5	RLC1_NV	Register Latency Default	Non-volatile	0	Selects # of register read latency cycles 0 to 3 latency (dummy) cycles following opcode or register address.
4	RLC0_NV			0	
3	MRL_NV	Read Latency Default		1	0 to 15 latency (dummy) cycles following read address or continuous mode bits.
2				0	
1				0	
0				0	

- **ECC Error Selection (ECCS) CR3NV[7]:** This bit selects between 2-bit ECC error detection and correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection and correction.
  Note: DECDEC ECC is always enabled. This register only controls what is stored in the Address Trap Register register. The Address Trap Register captures either 2-bit or both 1-bit and 2-bit ECC errors based on ECCS selection.
- **Register Latency Code (RLC[1:0]) CR3NV[5:4]:** These bits control the read latency (dummy cycle) delay in all variable latency register read instructions. It enables the user to adjust the read latency during normal operation to optimize the latency for different register read instructions at different operating frequencies.

Table 17 Latency code (cycles) versus frequency for Volatile Registers

Latency code	Type 1		Type 4		Type 5		Type 9	
	RDAR (1-1-1) (4-4-4)		RDSN (1-1-1) (4-4-4)		RDSR1 (1-1-1) (4-4-4) RDSR2 (1-1-1) (4-4-4) RDCR1 (1-1-1) (4-4-4) RDCR2 (1-1-1) (4-4-4) RDCR3 (1-1-1) (4-4-4)		RUID (1-1-1) (4-4-4) RDID2 (1-1-1) (4-4-4) RDQID (1-1-1) (4-4-4)	
	Latency cycles	Max frequency	Latency cycles	Max frequency	Latency cycles	Max frequency	Latency cycles	Max frequency
00	0	66 MHz	0	66 MHz	0	66 MHz	8	133 MHz
01	1	66 MHz	1	66 MHz	0	66 MHz	8	133 MHz
10	1	66 MHz	2	133 MHz	1	66 MHz	8	133 MHz
11	2	133 MHz	3	133 MHz	2	133 MHz	8	133 MHz

- **Memory Read Latency Non-volatile CR3NV[3:0]:** These bits control the POR, hardware reset or software reset state of the read latency (dummy cycle) delay in all variable latency read commands. The following read commands have a variable latency period between the end of address or mode and the beginning of read data returning to the host.
  The non-volatile read latency configuration bits set the number of read latency (dummy-cycles) in use so the device can start immediately (boot) with an appropriate read latency for the host system.

Table 18 Latency code (cycles) versus frequency

Latency code 0	Read command maximum frequency (MHz)					
	Read (1-1-1)	Fast Read (1-1-1)	Fast Read (4-4-4)	Quad O Read (1-1-4)	Quad I/O Read (1-4-4)	Quad I/O Read QPI (4-4-4)
	Mode cycles = 0	Mode cycles = 8	Mode cycles = 2	Mode cycles = 0	Mode cycles = 2	Mode cycles = 2
0	33	110	20	33	20	20
1	33	120	33	40	33	33
2	33	125	40	50	40	40
3	33	133	50	60	50	50
4	33	133	60	70	60	60
5	33	133	70	80	70	70
6	33	133	80	90	80	80
7	33	133	90	100	90	90
8 (default)	33	133	100	110	100	100
9	33	133	110	120	110	110
10	33	133	120	125	120	120
11	33	133	125	133	125	125
12	33	133	133	133	133	133
13	33	133	133	133	133	133
14	33	133	133	133	133	133
15	33	133	133	133	133	133

Table 19 Latency code (cycles) versus frequency for NV Registers

Latency code	Read command maximum frequency (MHz)			
	Read Any Register (1-1-1)	Read Any Register QPI (4-4-4)	Read SFDP RSFDP (1-1-1)	Read SFDP RSFDP QPI (4-4-4)
	Mode cycles = 0	Mode cycles = 0	Mode cycles = 0	Mode cycles = 0
0	33	4	110	80
1	40	10	110	80
2	50	20	110	80
3	60	33	110	80
4	70	40	110	80
5	80	50	110	80
6	90	60	110	80
7	100	70	110	80
8	110	80	110	80
9	120	90	110	80
10	133	100	110	80
11	133	110	110	80
12	133	120	110	80
13	133	125	110	80
14	133	133	110	80
15	133	133	110	80

The Read SFDP command always have a dummy cycle of eight and the maximum frequencies for different interfaces related to eight dummy-cycles. Read Unique ID has eight cycles of latency.

6.5.5.2 Configuration Register 3 Volatile (CR3V)

Related commands: Read Configuration 3 (RDCR3 33h), Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), and Write Any Register (WRAR 71h). This is the register displayed by the RDCR3 command.

Table 20 Configuration Register 3 Volatile (CR3V)

Bits	Field name	Function	Type	Default state	Description
7	ECCS_NV	ECC Error Selection	Volatile	CR3NV	1 = 1-bit/2-bit Error Detection & Correction Enabled 0 = 2-bit Error Detection & Correction Enabled (DECDED ECC always enabled; register only controls what is stored in the ADDTRAP)
6	ECCDI_NV	ECC Disable			1 = ECC Disabled 0 = ECC Enabled
5	RLC1_NV	Register Latency Default			Selects # of register read latency cycles 0 to 3 latency (dummy) cycles following opcode or register address
4	RLC0_NV				
3	MRL_NV	Read Latency Default			0 to 15 latency (dummy) cycles following read address or continuous mode bits.
2					
1					
0					

- **ECC Error Selection (ECCS) CR3NV[7]:** This bit selects between 2-bit ECC error detection and correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection and correction.
  Note: DECDEC ECC is always enabled. This register only controls what is stored in the Address Trap Register register. The Address Trap Register captures either 2-bit or both 1-bit and 2-bit ECC errors based on ECCS selection.
- **Error Correction Disable (ECCDI) CR3NV[6]:** Disables the programming of the ECC syndrome bits during user program and will turn off the ECC correction/detection during user read, always indicating no ECC events are occurring. When ECCDI has ECC enabled, the normal ECC behavior of the device is active for both program and read modes. ECCDI is a volatile bit and will always be reset to '0' at POR, hardware reset or software reset. This bit does not affect reads of Serial Flash Discovery Parameter data, and neither reads nor writes of nonvolatile register, which always keep ECC protection enabled.
- **Register Latency CR3V[3:0]:** These bits control the read latency (dummy cycle) delay in all variable latency register read instructions. It enables the user to adjust the read latency during normal operation to optimize the latency for different register read instructions at different operating frequencies.
- **Memory Read Latency CR3V[3:0]:** These bits set the read latency (dummy cycle) delay in variable latency read commands. These volatile configuration bits enable the user to adjust the memory read latency during normal operation to optimize the latency for different commands or, at different operating frequencies, as needed.

6.5.6 ECC Detection Counter Register (ECCDC)

The ECC Detection Count register (ECCDC) stores the number of times ECC 1-bit detections/corrections and ECC 2-bit detections/corrections have occurred during read operations since the last CLECC, POR, hardware or software reset. ECCDC register is only updated during Read Instruction. ECC Status Read Instruction does not affect the ECCDC Register. Only one ECC error is counted for each data unit. If multiple read command access the same unit data containing an ECC error, the applicable field (ECCDC1 or ECCDC2) will increment each time the unit data is read. Once the count reaches 0xFFFF, the ECCDC will stop incrementing.

Table 21 ECC Count Register

Volatile - Flip-Flops					Description
Bits	**Name**	**Function**	**Read / Write**	**Default state**	
15:0	ECCDC1	ECC Detection Count	R	0000h	Count of 1-bit ECC corrections since the last POR or hardware/software reset
31:16	ECCDC2	ECC Detection Count	R	0000h	Count of 2-bit ECC corrections since the last POR or hardware/software reset

6.5.7 Address Trap Register (ADDTRAPR)

The Address Trap register (ADDTRAPR) stores the ECC unit data byte address where a 1-bit/2-bit correction or only a 2-bit correction occurred during a read operation (configuration option). ADDTRAPR stores the ECC unit address of the first ECC correction captured during a memory read operation since the last Clear ECC instruction. Address Trap register is only updated during Read Instructions. ECC Status Read Instruction does not affect the Address Trap Register. Clear ECC (CLECC 0x1B) instruction clears the Address Trap register 0x00000000. The value in the ADDTRAPR register is only meaningful when the ECCDC register contains a non-zero value.

Table 22 Address Trap Register

Volatile - Flip-Flops					Description
Bits	**Name**	**Function**	**Read / Write**	**Default state**	
31:0	ADDTRAP	Store ECC Address	R	0000h	Store the byte address of unit data where 1-bit or 2-bit ECC detection/correction occurred. Address captured is dependent on ECCS register setting.

6.5.8 Interrupt Configuration Register (ICR)

The INT_N pin is an open-drain output used to indicate to the host system that an event has occurred within the memory device. The Interrupt Configuration Register determines when an internal event is enabled to trigger a HIGH to LOW transition on the INT_N output pin. The ICR can be accessed through RDAR/WRAR from the SPI and QPI interfaces. Clearing a bit within ICR has no effect on the ISR and it is a system responsibility to independently clear the ISR as required.

Table 23 Interrupt Configuration Register Volatile

Bits	Field name	Function	Type	Default state	Description
7	INT_N_EN	INT_N Output Enable	R/W	1	1 = INT_N output disabled (HIGH or Open-Drain) 0 = INT_N output enabled, internal events will cause a HIGH to LOW transition
6	RFU	Reserved		1	Reserved for Future Use
5	RFU	Reserved		1	Reserved for Future Use
4	RDY_EN	Ready/Busy Transition Enable	R/W	1	1 = Ready/Busy transitions will not transition the INT_N output 0 = A Busy to Ready transition will cause a HIGH to LOW transition on the INT_N output
3	RFU	Reserved		1	Reserved for Future Use
2	RFU	Reserved		1	Reserved for Future Use
1	2BED_EN	2BED Enable	R/W	1	1 = 2-bit ECC detection/correction will not transition the INT_N output 0 = 2-bit ECC detection/correction will cause a HIGH to LOW transition the INT_N output
0	1BEC_EN	1BED Enable	R/W	1	1 = 1-bit ECC correction/detection will not transition the INT_N output 0 = 1-bit ECC correction/detection will cause a HIGH to LOW transition the INT_N output

- **INT_N_EN:** Enables the operation of the INT_N pin upon any of the enabled interrupt sources setting within Interrupt Status Register.
- **RDY_EN:** Enables propagation of the setting of the RDY bit within the Interrupt Status Register to the INT_N pin when set to ‘0’.
- **2BED_EN:** Enables propagation of the setting of the 2BED bit within the Interrupt Status Register to the INT_N pin when set to ‘0’.
- **1BEC_EN:** Enables propagation of the setting of the 1BEC bit within the Interrupt Status Register to the INT_N pin when set to ‘0’.

6.5.9 Interrupt Status Register (ISR)

The Interrupt Status Register indicates what internal event(s) have occurred since the last time the ISR was cleared. If enabled, the INT_N output pin will then transition from HIGH to LOW upon the occurrence of an enabled event. Once the host recognizes that INT_N has transitioned to the LOW state the Interrupt Status Register can be read to determine which internal event was responsible. The ISR can be accessed through RDAR/WRAR from the SPI and QPI interfaces. These bits set when the associated event occurs. The corresponding bit in the ICR must be set for the INT to propagate out of the device.

Table 24 Interrupt Status Register Volatile

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved		1	Reserved for Future Use
6	RFU	Reserved		1	Reserved for Future Use
5	RFU	Reserved		1	Reserved for Future Use
4	RDY	Ready/Busy Transition	R/W	1	1 = A Busy to Ready transition has not occurred 0 = A Busy to Ready transition has occurred
3	RFU	Reserved		1	Reserved for Future Use
2	RFU	Reserved		1	Reserved for Future Use
1	2BED	2-bit ECC Error Detected	R/W	1	1 = 2-bit error detection/correction has not occurred 0 = 2-bit error detection/correction has occurred
0	1BEC	1-bit ECC Error Corrected	R/W	1	1 = 1-bit error detection/correction has not occurred 0 = 1-bit error detection/correction has occurred

- **2BED:** A correctable 2-bit error occurred while accessing the Flash array via a user read operation. ECC errors during program/scrub routines are not captured in the ISR.
- **1BEC:** A correctable 1-bit error occurred while accessing the Flash array via a user read operation. ECC errors during program/scrub routines are not captured in the ISR.

Notes:

ISR bits stay low till they are disabled by the host.

Interrupt Status Bits are “sticky” bits. Once enabled, they can only be disabled by:

- Disable the INT_N output by loading a ‘1’ into bit 7 of the Interrupt Configuration Register.
- Reset the appropriate bit (by writing a ‘1’) in the ISR bit that indicates which internal event occurred to cause the output to go LOW. All ISR bits that are LOW and are also enabled in the ICR must be reset before the INT_N output will return HIGH.
- Clear ECC Status Instruction (CLECC 1Bh) – if the error was ECC related.
- Hardware Reset, Power-On Reset or Software Reset.

6.5.10 ECC Status Register (ECCSR)

The status of ECC unit data is presented in the ECC Status Register. The functionality of ECC Status Register is described in table below and can be accessed through the Read Any Register (RDAR) instruction. The ECCSR contains the ECC status of any error correction action of the unit data whose byte was addressed during memory reads. The correct sequence for RDAR based ECCSR read is as follows:

- Read data from memory array using any of the Read instructions.
- ECCSR is updated by the device.
- RDAR of ECCSR will provide the status of any ECC event since the last clear.

Note: ECCSR is cleared by POR, Hardware/Software reset or a Clear ECC instruction.

Table 25 ECC Status Register Volatile

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved		0	Reserved for Future Use
6	RFU	Reserved		0	Reserved for Future Use
5	RFU	Reserved		0	Reserved for Future Use
4	2BC	2-bit ECC Correction / Detection	R	0	1 = 2-bit Error detection/correction occurred since last ECCSR Clear 0 = No 2-bit Error detection/correction occurred since last ECCSR Clear
3	1BC	1-bit ECC Correction / Detection	R	0	1 = 1-bit Error detection/correction occurred since last ECCSR Clear 0 = No 1-bit Error detection/correction occurred since last ECCSR Clear
2	RFU	Reserved		0	Reserved for Future Use
1	RFU	Reserved		0	Reserved for Future Use
0	RFU	Reserved		0	Reserved for Future Use

- **2-Bit ECC Correction (2BC) ECCSR:** This bit indicates that a 2-bit ECC detection/correction has occurred on any addressed data unit during memory reads since the last Clear ECC instruction.
  Note: The address associated with 2BC is placed in the ECC Address Trap Register. Only the first error address is captured. The Address Trap Register can be accessed using RDAR instruction. The Address Trap Register size is 4 bytes. The Address Trap register is reset upon POR or Hardware reset or Clear ECC instruction.
  Note: The ECC errors are kept in an ECCDC register. Each time an ECC correction is detected in the ECC Unit, the ECCDC register is incremented. The count is enabled for both 1b and 2b corrections. The ECCDC register is reset upon CLECC, POR or Hardware/Software reset. It can be read using RDAR instruction.
- **1-Bit ECC Correction (1BC) ECCSR:** This bit indicates that a 1-bit ECC detection/correction error has occurred on any addressed unit data during memory reads since the last Clear ECC instruction.
  Note: The address associated with 1BC may be placed in the ECC Address Trap Register dependent on the ECC Error Selection (ECCS) setting. Only the first error address is captured. The Address Trap Register can be accessed using RDAR instruction. The Address Trap Register size is 4 bytes. The Address Trap register is reset upon POR or Hardware reset or Clear ECC Status Register instruction.
  Note: The ECC errors are kept in an ECCDC register. Each time an ECC correction is detected in the ECC Unit, the ECCDC register is incremented. The count is enabled for both 1b and 2b corrections. The ECCDC register is reset upon CLECC, POR or Hardware/Software reset. It can be read using RDAR instruction.

7 Data protection

Data protection is required to safeguard against unintended changes to stored data. This includes inadvertent writing to, erasing or programming the device. Legacy Block Protection is a combination of hardware and software based non-volatile data protection schemes. In software based protection, the memory array is configured as read-only based on an address range using a combination of Block Protect (BP2, BP1 and BP0) and TBPROT (Top/Bottom Protection) bits in the status register. Furthermore, Status Register Protection Bit 0 (SRP0), places all Status & Configuration registers in read-only mode as well (WP# must be LOW). Hardware data protection is implemented using the Write Protect (WP#) pin where applying the write protect signal freezes the Status and Configuration registers in read-only mode (Status Register Protection bits must be set to '1'). In the 1Gb dual-die device, each die has its own set of Block Protection configuration bits that affect only the address space of the die, but the WP# signal is common to both die.

Both of these mechanisms combined ensure that Write, Erase and Program instructions are checked before they are accepted for execution.

If the protection mechanisms are in place and a program or erase instruction is issued to the protected areas, the device returns an ERROR flag.

7.1 Write Enable commands

7.1.1 Write Enable (WREN)

The Write Enable (WREN) command must be written prior to any command that modifies non-volatile data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit is cleared to '0' (disables writes) during power-up, hardware and software reset or after the device completes the following commands:

- Page Program (PP or 4PP)
- Quad Page Program (QPP or 4QPP)
- Page Scrub (PSCRB, 4PSCRB)
- Chip Scrub (CSCRB)
- Sector Erase (SE or 4SE)
- Block Erase (BE or 4BE)
- Chip Erase (CE)
- Write Disable (WRDI)
- Write Registers (WRR)
- Write Any Register (WRAR)

7.2 Write Protect Signal

When not in Quad mode (CR1V[1] = 0) or QPI mode (CR2V[3] = 0), the Write Protect (WP#) input in combination with the Status Register Protect 0 (SRP0) bit (SR1NV[7]) provide hardware input signal controlled protection. When WP# is LOW and SRP0 is set to '1' Status Register 1 (SR1NV and SR1V), Configuration register (CR1NV, CR1V, CR2NV, CR2V, CR2NV and CR3NV) are protected from alteration. This prevents disabling or changing the protection defined by the Block Protect bits. See **"Status Register 1"** on page 20.

7.3 Status Register Protect (SRP0)

The Status Register Protect bits (SRP0) are volatile bits in the configuration and status registers (CR1V[0] and SR1V[7]). The SRP bits control the method of write protection for SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV: software protection, hardware protection.

Table 26 Status Register Protection bits

SRP0 SR1V[7]	WP#	Status Register	Description
0	X	Software Protection	WP# pin has no control. SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV can be written [Factory Default]
1	0	Hardware Protected	When WP# pin is low SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV are locked and can not be written
1	1	Hardware Unprotected	When WP# pin is high SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV are unlocked and can be written

Notes:

- SRP0 is reloaded from SRP0_NV (SR1NV[7]) default state after a power-down, power-up cycle, software or hardware reset. To enable hardware protection mode by the WP# pin at power-up set the SRP0_NV bit to '1'.
- When QPI or QIO mode is enabled (CR2V[3] or CR1V[1] = '1') the internal WP# signal level is = 1 because the WP# external input is used as IO2 when either mode is active. This effectively turns off hardware protection when SRP1–SRP0 = 01b. The Register SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV are unlocked and can be written.
- WIP, WEL, and SUS (SR1[1:0] and CR1[7]) are volatile read only status bits that are never affected by the Write Status Registers command.
- The non-volatile version of SR1NV, CR1NV, CR2NV and CR3NV are not writable when protected by the SRP bits and WP# as shown in the table. The non-volatile version of these status register bits are selected for writing when the Write Enable (06h) command precedes the Write Status Registers (01h) command or the Write Any Register (71h) command.
- The volatile version of registers SR1V, CR1V and CR2V are not writable when protected by the SRP bits and WP# as shown in the table. The volatile version of these status register bits are selected for writing when the Write Enable for volatile Status Register (50h) command precedes the Write Status Registers (01h) command or the Write Enable (06h) command precedes the Write Any Register (71h) command.

7.4 Block protection

The Block Protect bits (Status Register bits BP2, BP1, BP0) in combination with the Configuration Register TBPROT bit can be used to protect an address range of the main flash array from program and erase operations. The size of the range is determined by the value of the BP bits and the upper or lower starting-point of the range is selected by the TBPROT bit of the configuration register (CR1NV[5]).

Table 27 Upper array start of protection (TBPROT = 0)

Status Register content			Protected fraction of memory array	Protected memory (KB)
BP2	BP1	BP0		
0	0	0	None	0
0	0	1	Upper 64th	1024
0	1	0	Upper 32nd	2048
0	1	1	Upper 16th	4096
1	0	0	Upper 8th	8192
1	0	1	Upper 4th	16384
1	1	0	Upper Half	32768
1	1	1	All Sectors	65536

Table 28 Lower array start of protection (TBPROT = 1)

Status Register content			Protected fraction of memory array	Protected memory (KB)
BP2	BP1	BP0		
0	0	0	None	0
0	0	1	Lower 64th	1024
0	1	0	Lower 32nd	2048
0	1	1	Lower 16th	4096
1	0	0	Lower 8th	8192
1	0	1	Lower 4th	16384
1	1	0	Lower Half	32768
1	1	1	All Sectors	65536

When TBPROT is set to a ‘0’ the Legacy Block Protection is defined to start from the top (maximum address) of the array. When TBPROT is set to a ‘1’ the Legacy Block Protection is defined to start from the bottom (zero address) of the array. TBPROT tracks any changes to the non-volatile version of this bit (TBPROT_NV).

8 Commands

All communication between the host system and CYEL17B family memory devices is in the form of units called commands. See **“Command protocol”** on page 14 for details on command protocols.

Although host software in some cases is used to directly control the SPI interface signals, the hardware interfaces of the host system and the memory device generally handle the details of signal relationships and timing. For this reason, signal relationships and timing are not covered in detail within this software interface focused section of the document. Instead, the focus is on the logical sequence of bits transferred in each command rather than the signal timing and relationships. Following are some general signal relationship descriptions to keep in mind. For additional information on the bit-level format and signal timing relationships of commands, see **“Command protocol”** on page 14.

- The host always controls the Chip Select (CS#), Serial Clock (SCK) and Serial Input (SI) - SI for single bit wide transfers. The memory drives Serial Output (SO) for single bit read transfers. The host and memory alternately drive the IO0–IO3 signals during Quad transfers.
- All commands begin with the host selecting the memory by driving CS# LOW before the first rising edge of SCK. CS# is kept LOW throughout a command and when CS# is returned HIGH the command ends. Generally, CS# remains LOW for eight bit transfer multiples to transfer byte granularity information. No commands will be accepted if CS# is returned HIGH not at an 8-bit boundary.

8.1 Command set summary

8.1.1 Extended addressing

To accommodate addressing above 128 Mb, there are two options:

- Instructions that always require a 4-byte address, used to access up to 32 Gb of memory.

Table 29 Extended address 4-byte address commands

Command name	Function	Instruction (Hex)
4READ	Read	13
4FAST_READ	Read Fast	0C
4QOR	Quad Output Read	6C
4QIOR	Quad I/O Read	EC
4ECCRD	ECC Read	18
4PP	Page Program	12
4PSCRB	Page Scrub	CF
4QPP	Quad Page Program	34
4SE	Sector Erase	21
4BE	Block Erase	DC

- A 4-byte address mode for backward compatibility to the 3-byte address instructions. The standard 3-byte instructions can be used in conjunction with a 4-byte address mode controlled by the address length configuration bit (CR2V[0]). The default value of CR2V[0] is loaded from CR2NV[1] (following power up, hardware reset or software reset), to enable default 3-byte (24-bit) or 4-byte (32-bit) addressing. When the address length (CR2V[0]) set to '1', the legacy commands are changed to require 4-bytes (32-bits) for the address field. The following instructions can be used in conjunction with the 4-byte address mode configuration to switch from 3 bytes to 4 bytes of address field.

Table 30 Extended address 4-byte address mode with 3-byte address commands

Command name	Function	Instruction (hex)
READ	Read	03
FAST_READ	Read Fast	0B
QOR	Quad Output Read	6B
QIOR	Quad I/O Read	EB
PP	Page Program	02
PSCRB	Page Scrub	CE
QPP	Quad Page Program	32
SE	Sector Erase	20
BE	Block Erase	D8
RDAR	Read Any Register	65
WRAR	Write Any Register	71

8.1.2 Command summary by function

Table 31 CYEL17B family command set (sorted by function)

Function	Command name	Command description	Instruction value (hex)	Maximum frequency (MHz)	Address length (bytes)	QPI[2]
ID and Serial Number	RDID	Read ID (JEDEC Manufacturer ID)	9F	133	0	Yes
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5A	110 SPI 80 QPI	3 or 4	Yes
	RDQID	Read Quad ID	AF	133	0	Yes
	RUID	Read Unique ID	4C	133	0	Yes
	WRSN	Write Serial Number	C2	133	0	Yes
	RDSN	Read Serial Number	C3	133	0	Yes
Register Access	RDSR1	Read Status Register 1	05	133	0	Yes
	RDSR2	Read Status Register 2	07	133	0	No
	RDCR1	Read Configuration Register 1	35	133	0	No
	RDCR2	Read Configuration Register 2	15	133	0	No
	RDCR3	Read Configuration Register 3	33	133	0	No
	RDAR	Read Any Register	65	133	3 or 4	Yes
	WRR	Write Register (Status-1 and Configuration-1, 2, 3)	01	133	0	Yes
	WRDI	Write Disable	04	133	0	Yes
	WREN	Write Enable for Non-volatile data change	06	133	0	Yes
	WRAR	Write Any Register	71	133	3 or 4	Yes
	CLSR	Clear Status Register	30	133	0	Yes
	4BAM	Enter 4 Byte Address Mode	B7	133	0	Yes
	4BEX	Exit 4 Byte Address Mode	E9	133	0	Yes
	SWL	Set Wrap Length	77	133	0	Yes
	QPIEN	Enter QPI	38	133	0	No
	SPIEN	Exit QPI	F5	133	0	Yes
	ECCRD	ECC Read	19	133	3 or 4	Yes
	4ECCRD	ECC Read	18	133	4	Yes
	CLECC	Clear ECC	1B	133	0	Yes

Table 31 CYEL17B family command set (sorted by function) *(continued)*

Function	Command name	Command description	Instruction value (hex)	Maximum frequency (MHz)	Address length (bytes)	QPI[2]
Read Flash Array	READ	Read	03	33	3 or 4	No
	4READ	Read	13	33	4	No
	FAST_READ	Fast Read	0B	133	3 or 4	No
	4FAST_READ	Fast Read	0C	133	4	No
	QOR	Quad Output Read	6B	133	3 or 4	No
	4QOR	Quad Output Read	6C	133	4	No
	QIOR	Quad I/O Read (CR1V[1] = 1) or CR2V[3] = 1	EB	133	3 or 4	Yes
	4QIOR	Quad I/O Read (CR1V[1] = 1) or CR2V[3] = 1	EC	133	4	Yes
Program Flash Array	PP	Page Program	02	133	3 or 4	Yes
	4PP	Page Program	12	133	4	Yes
	QPP	Quad Page Program	32	133	3 or 4	No
	4QPP	Quad Page Program	34	133	4	No
Page Scrub	PSCRB	Page Scrub	CE	133	3 or 4	Yes
	4PSCRB	Page Scrub	CF	133	4	Yes
Chip Scrub	CSCRB	Chip Scrub	8E	133	0	Yes
Erase Flash Array	SE	Sector Erase	20	133	3 or 4	Yes
	4SE	Sector Erase	21	133	4	Yes
	BE	Block Erase	D8	133	3 or 4	Yes
	4BE	Block Erase	DC	133	4	Yes
	CE	Chip Erase	60	133	0	Yes
	CE	Chip Erase (alternate instruction)	C7	133	0	Yes
Erase/ Suspend/ Resume	EPS	Erase Suspend	75	133	0	Yes
	EPR	Erase Resume	7A	133	0	Yes
Reset	RSTEN	Software Reset Enable	66	133	0	Yes
	RST	Software Reset	99	133	0	Yes
	MBR	Mode Bit Reset	FF	133	0	Yes

8.1.3 Read device identification

There are multiple commands to read information about the device manufacturer, device type and device features. SPI memories from different vendors have used different commands and formats for reading information about the memories. The CYEL17B family supports the three device information commands.

Note
2. Commands not supported in QPI mode have undefined behavior if sent when the device is in QPI mode.

8.1.4 Register read or write

There are multiple registers for reporting embedded operation status or controlling device configuration options. There are commands for reading or writing these registers. Registers contain both volatile and non-volatile bits. Non-volatile bits in registers are automatically erased and programmed as a single (write) operation.

8.1.4.1 Monitoring operation status

The host system can determine when a write, program, erase, suspend or other embedded operation is complete by monitoring the work in progress (WIP) bit in the Status Register. The Read from Status Register 1 command or Read Any Register command provides the state of the WIP bit. The Read from Status Register 2 or Read Any Register command provides the state of the program error (P_ERR) and erase error (E_ERR) bits in the Status Register indicate whether the most recent program or erase command has not completed successfully. When P_ERR or E_ERR bits are set to '1', the WIP bit will remain set to one indicating the device remains busy and unable to receive most new operation commands. Only status reads (RDSR1 05h, RDSR2 07h), Read Any Register (RDAR 65h), Read Configuration RDCR1 and RDCR3, status clear (CLSR 30h) and software reset (RSTEN 66h followed by RST 99h) are valid commands when P_ERR or E_ERR is set to '1'. A Clear Status Register (CLSR) command must be sent to return the device to standby state. Alternatively, Hardware Reset or Software Reset (RSTEN 66h followed by RST 99h) may be used to return the device to standby state.

8.1.4.2 Configuration

There are commands to read, write and protect registers that control interface path width, interface timing, interface address length and some aspects of data protection.

8.1.5 Read flash array

The data may be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input HIGH. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

Burst Wrap read can be enabled by the Set Wrap Length (SWL 77h) command with the requested wrapped read length and alignment, see **"Set Wrap Length (SWL 77h)"** on page 64.

There are several different read commands to specify different access latency and data path widths.

- The Read command provides a single address bit per SCK rising edge on the SI/IO signal with read data returning a single bit per SCK falling edge on the SO/IO1. This command has zero latency between the address and the returning data but is limited to a maximum SCK rate of 33 MHz.
- Other read commands have a latency period between the address and returning data but can operate at higher SCK frequencies. The latency depends on a configuration register read latency value.
- The Fast Read command provides a single address bit per SCK rising edge on the SI/IO0 signal with read data returning a single bit per SCK falling edge on the SO/IO signal.
- Quad Output Read commands provide address on SI/IO0 pin on the SCK rising edge with read data returning four bits of data per SCK falling edge on the IO0–IO3 signals.
- Quad I/O Read commands provide address two bits or four bits per SCK rising edge with read data returning four bits of data per SCK falling edge on the IO0–IO3 signals. Continuous read feature is enabled if the mode bits value is Axh.

8.1.6 Program flash array

The programming data requires two commands: Write Enable (WREN) and Page Program (PP, 4PP, QPP, 4QPP). The Page Program command accepts from 1 byte up to 2048 consecutive bytes of data (page) to be programmed in one operation. For programs of less than 2048 bytes, the bytes of the addressed page that are not part of the user input data will be read from the Flash memory, ECC corrected and re-written to the Flash.

A user program command will internally initiate a page erase followed by a page program.

8.1.7 Scrub flash array

Scrubbing data requires two commands: Write Enable (WREN) and Page Scrub (PSCRB, 4PSCRB) or Chip Scrub (CSCRB).

Note All scrub commands will execute even if legacy block protection is set. The Chip Scrub (CSCRB) command will initiate a scrub operation on both die of the DDP simultaneously.

8.1.8 Erase flash array

The Sector Erase, Block Erase or Chip Erase commands set all the bits in a sector or the entire memory array to '0'. The Write Enable (WREN) command must precede an erase command. The Chip Erase (CE) command will initiate a scrub operation on both die of the DDP simultaneously.

8.1.9 Reset

There are commands to reset to the default conditions present after power on to the device. Resetting to default conditions using software requires two commands: Reset Enable (RSTEN) and Software Reset (RST1). The reset enable is only effective for the first command to follow it and returns to a disabled state immediately after that subsequent command. If the subsequent command is RST1, a software reset is performed. If the command immediately preceding RST1 is not RSTEN, no software reset is performed.

Exiting continuous mode may be accomplished using the Mode Bit Reset command (MBR). The first subsequent traffic on SI in SPI mode or on IO[3:0] in QPI mode will be interpreted as a command and not as an address.

8.2 Identification commands

8.2.1 Read Identification (RDID 9Fh)

The Read Identification (RDID) command provides read access to manufacturer identification and device identification. The manufacturer identification is assigned by JEDEC. The device identification values are assigned by Infineon.

Any RDID command issued while a program, erase or write cycle is in progress is ignored and has no effect on execution of the program, erase or write cycle that is in progress.

The RDID instruction is shifted on SI / IO0. The RDID instruction is shifted on SI followed by 8 dummy-cycles. This latency period (i.e., dummy-cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on SO/IO1 is "don't care" and may be high impedance. After the last dummy cycle a byte of manufacturer identification, two bytes of device identification and 5 bytes of RFU will be shifted sequentially out on SO / IO1. As a whole this information is referred to as ID. See **"Device ID address map"** on page 116 for the detail description of the ID contents.

Continued shifting of output beyond the end of the defined ID address space will wrap back to byte 0 of the ID. The RDID command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

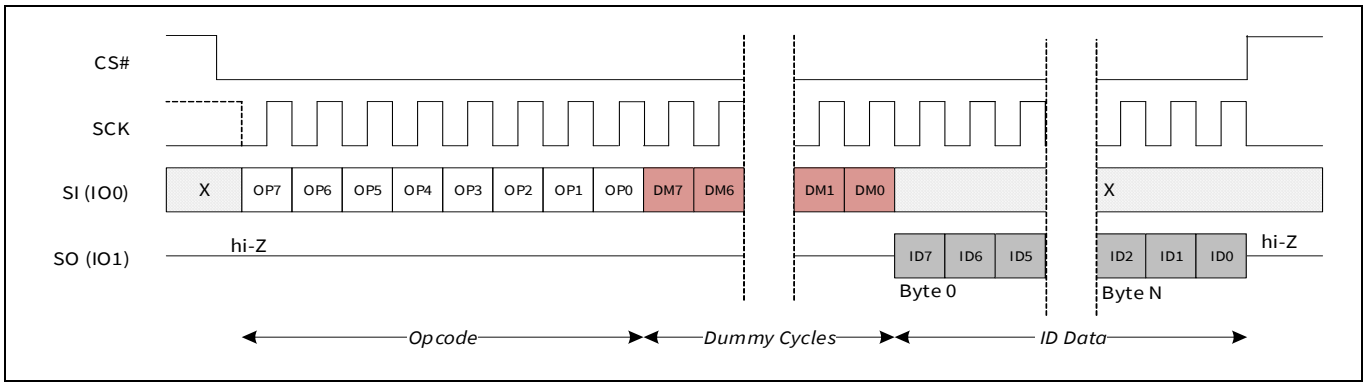


Figure 12 Read Identification (RDID) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

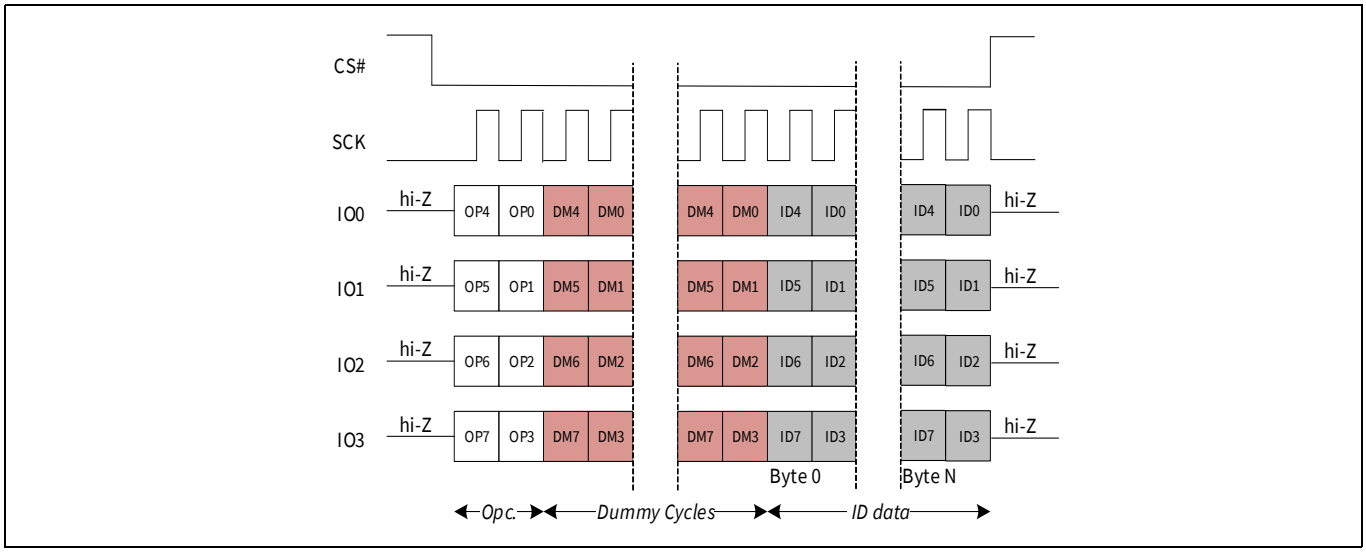


Figure 13 Read Identification (RDID) QPI Mode command

8.2.2 Read Quad Identification (RDQID AFh)

The Read Quad Identification (RDQID) command provides read access to manufacturer identification and device identification. This command is an alternate way of reading the same information provided by the RDID command while in QPI mode. In all other respects the command behaves the same as the RDID command.

The command is recognized only when the device is in QPI Mode (CR2V[3] = 1) or Quad Mode (CR1V[1] = 1). The instruction is shifted in on IO0–IO3 for QPI Mode and IO0 for Quad Mode followed by 8 dummy-cycles. This latency period (i.e., dummy-cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance. After the last bit dummy cycle, a byte of manufacturer identification, two bytes of device identification and 5 bytes of RFU will be shifted sequentially out on IO0–IO3. As a whole this information is referred to as ID. See **"Device ID address map"** on page 116 for the detail description of the ID contents.

Continued shifting of output beyond the end of the defined ID address space will wrap back to byte 0 of the ID. The command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

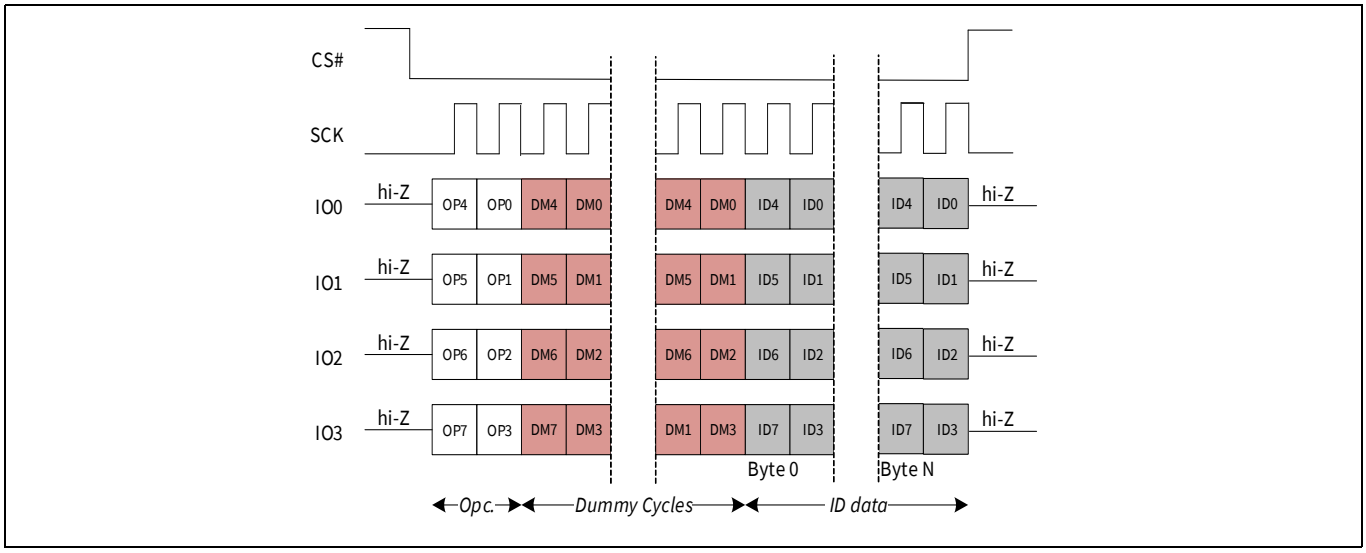


Figure 14 Read Quad Identification (RDQID) command sequence QPI mode

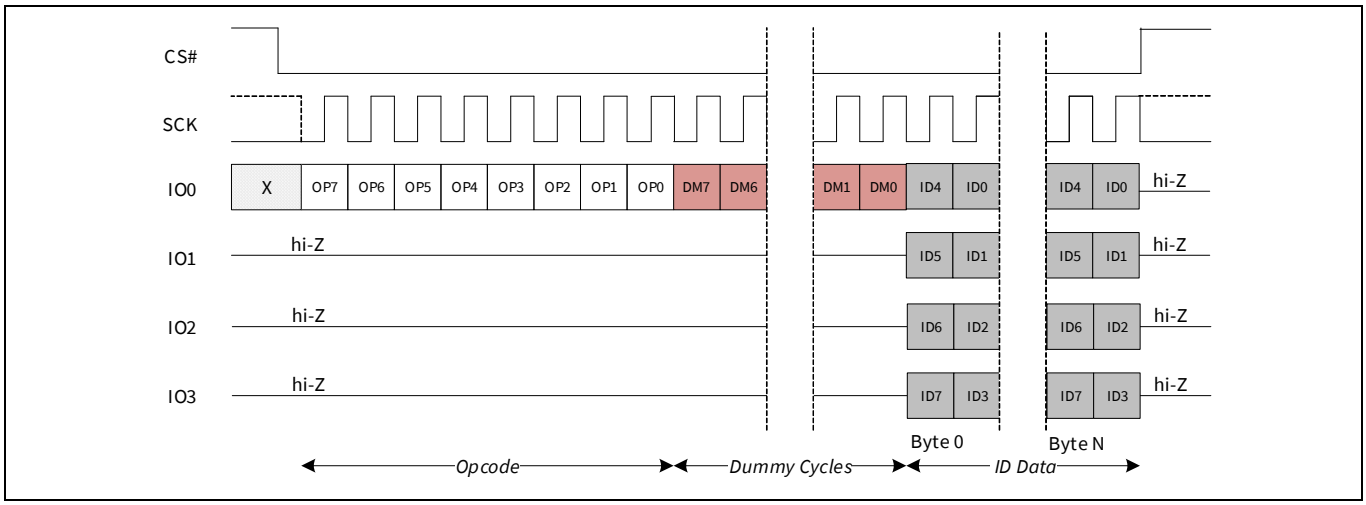


Figure 15 Read Quad Identification (RDQID) command sequence Quad mode

8.2.3 Read Serial Number (RDSN C3h)

The Read Serial Number (RDSN) command provides read access to the user programmable 8-byte serial number. A serial number read may be performed in burst mode to read all the eight bytes at once. After the last byte of serial number is read, the device loops back to the first (LSB) byte of the serial number. An RDSN instruction can be issued by shifting the opcode for RDSN after CS# goes LOW.

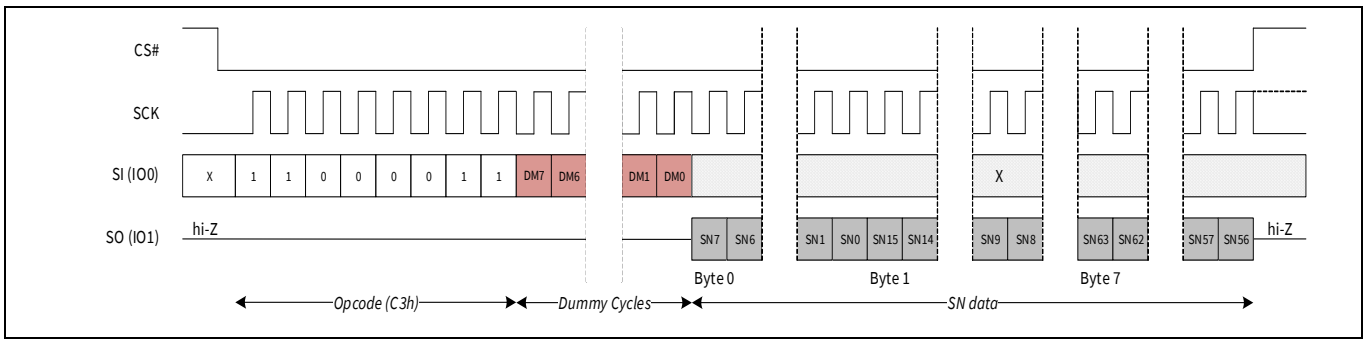


Figure 16 RDSN in SPI mode

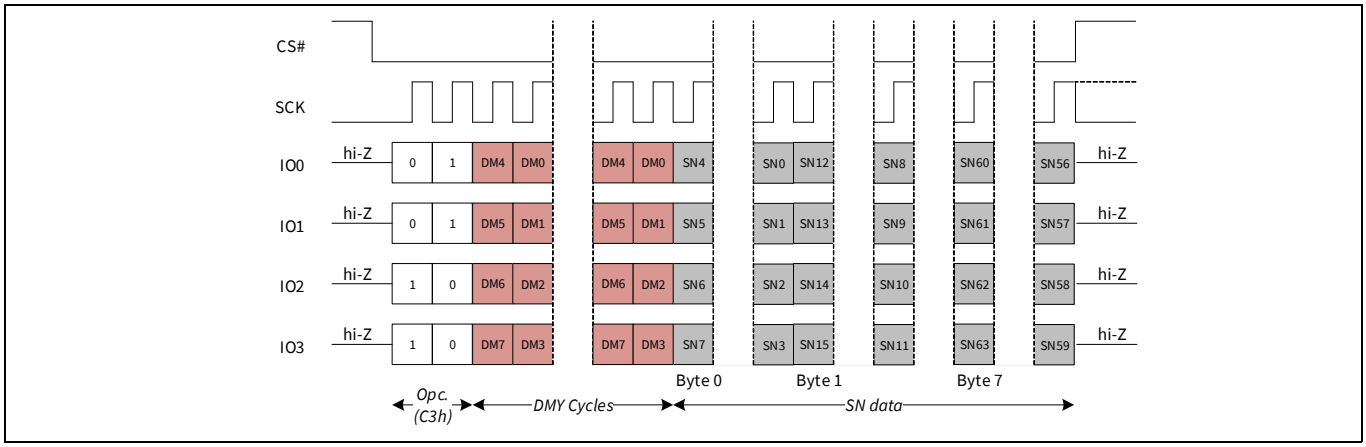


Figure 17 RDSN in QPI mode

8.2.4 Write Serial Number (WRSN C2h)

The serial number is an 8-byte memory space provided to the user to uniquely identify the device. The default value for 8 byte locations are set to '0x0000000000000000'. The serial number is written using WRSN instruction. The WRSN instruction can be used in burst mode to write all the 8 bytes of serial number. After the last byte of serial number is shifted in, CS# must be driven HIGH to complete the WRSN operation. Exactly 8 bytes must be entered or the serial number will not be written.

Notes

- The serial number is NOT defined as an OTP space.
- WRSN instruction can only be executed by the device if the Write Enable Latch (WEL) in the Status Register is set to '1' to enable write operations. When the WRSN operation is completed, the Write Enable Latch (WEL) is reset to a '0'.

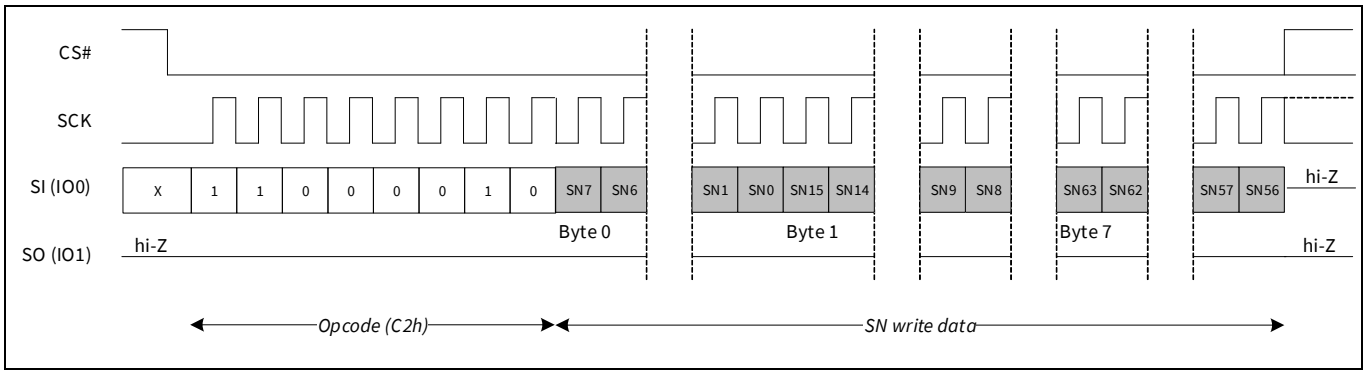


Figure 18 WRSN in SPI mode

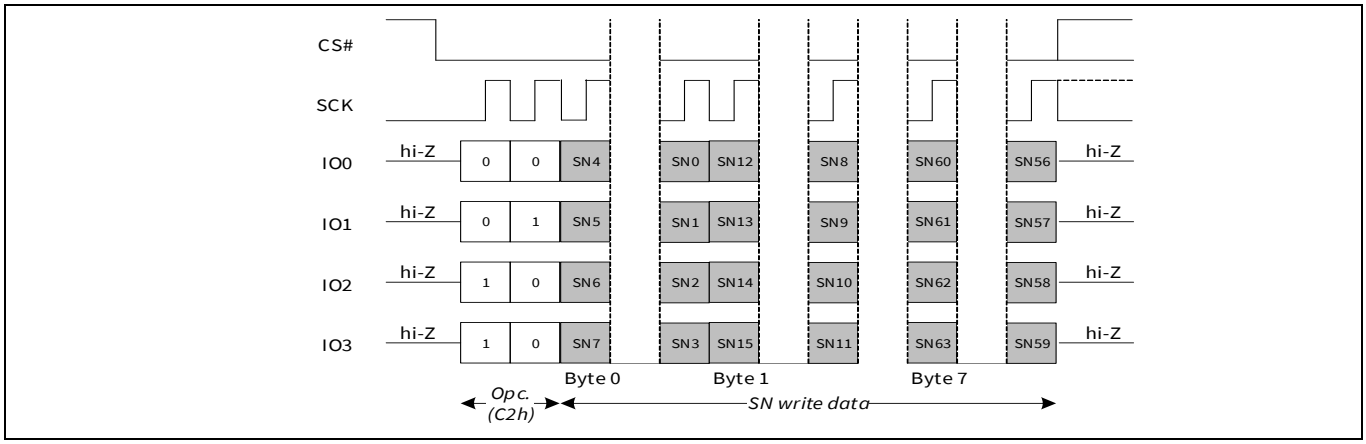


Figure 19 WRSN in QPI mode

8.2.5 Read serial flash discoverable parameters (RSFDP 5Ah)

The command is initiated by shifting on SI the instruction code “5Ah”, followed by a 24-bit (3-byte) address followed by the number of read latency (dummy-cycles) fixed at 8 cycles.

The SFDP bytes are then shifted out on SO/IO1 starting at the falling edge of SCK after the dummy-cycles. The SFDP bytes are always shifted out with the MSB first. If the 24-bit (3-byte) address is set to any non-zero value, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. In SPI mode the RSFDP command is supported up to 110 MHz in SPI and 80 MHz in QPI mode.

The read latency is fixed to eight cycles for compliance with the JEDEC JESD216 SFDP standard. Continuous (sequential) read is supported with the Read SFDP command. If the read is continued beyond the last byte of the SFDP table, the read will wrap back to the first byte.

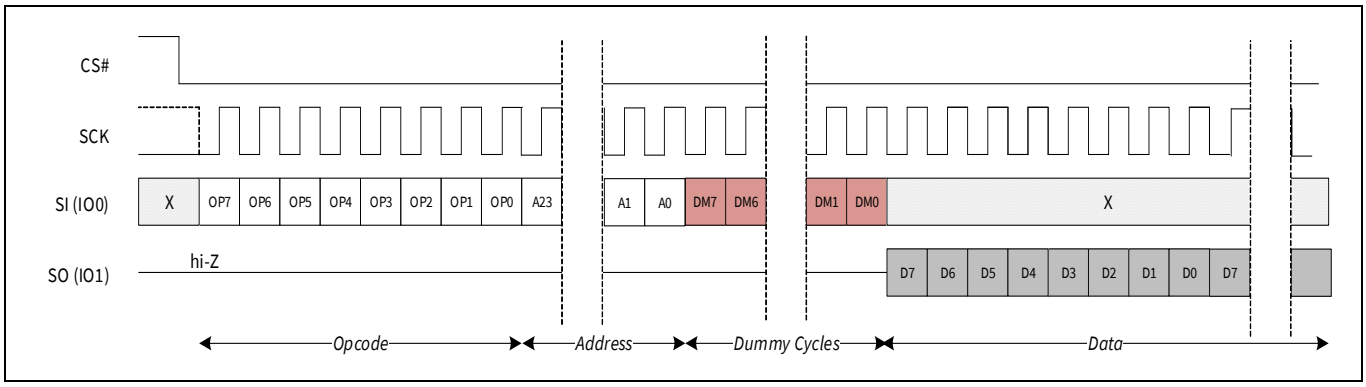


Figure 20 RSFDP command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

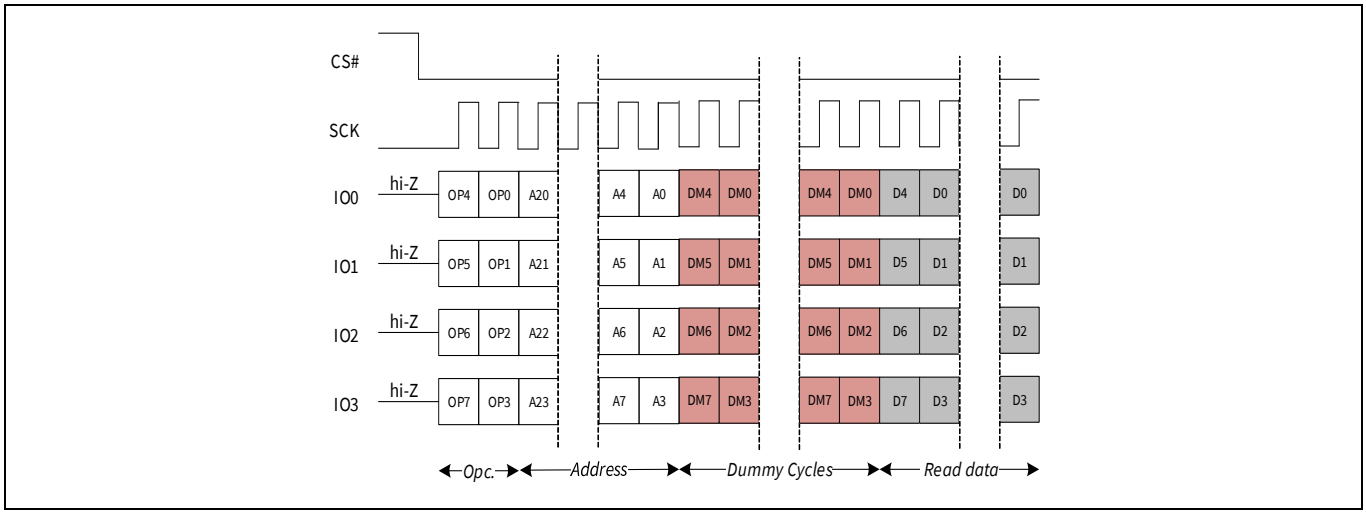


Figure 21 RSFDP QPI Mode command sequence

8.2.6 Read Unique ID (RUID 4Ch)

The Read Identification (RUID) command provides read access to factory set read only 64-bit number that is unique to each device.

The RUID instruction is shifted on SI followed by 8 dummy-cycles. This latency period (i.e., dummy-cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance. Then the 8 bytes of Unique ID will be shifted sequentially out on SO / IO1.

Continued shifting of output beyond the end of the defined Unique ID address space will wrap to byte 0 of the UID. The RUID command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

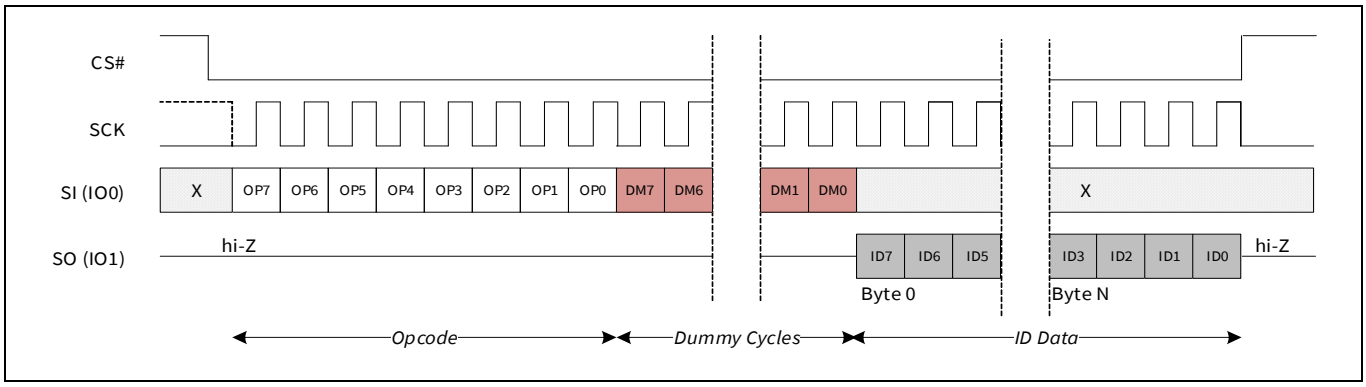


Figure 22 Read Unique ID (RUID) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

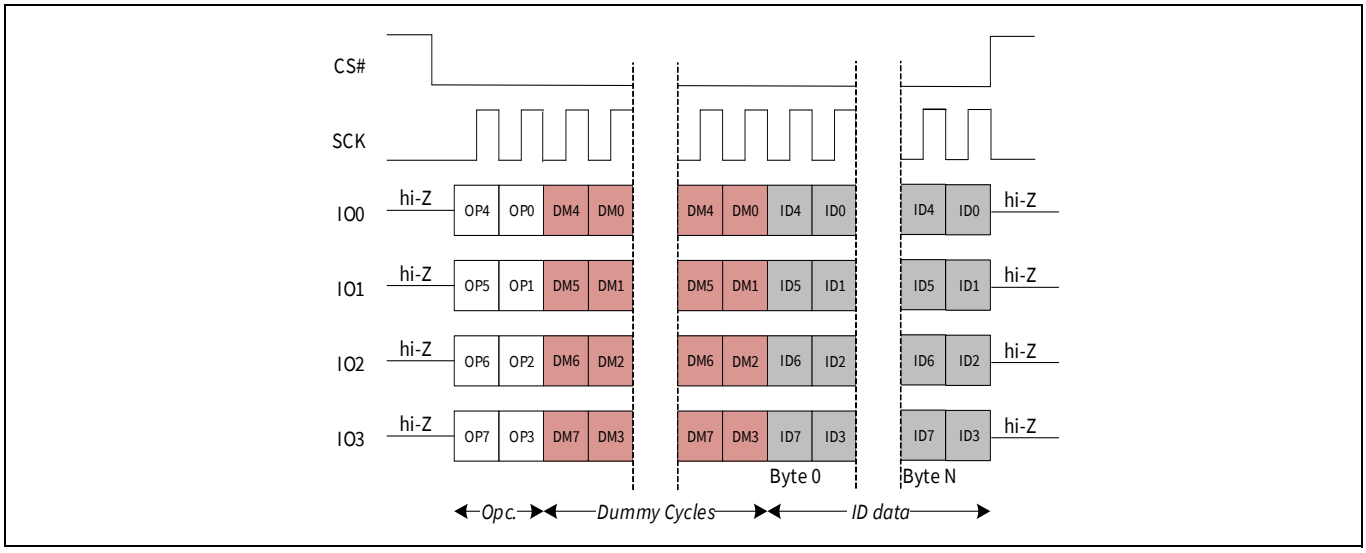


Figure 23 Read Unique ID (RUID) QPI Mode command

8.3 Register Access commands

Most registers have a dedicated instruction to read from and write to the register. E.g., the RDSR1/2 instruction reads from the SR register. The WRR instruction can burst write to the SR1, CR1, CR2 and CR3 registers. Individual registers can be written via the WRAR instruction. Dedicated register instructions do not require an address transfer.

8.3.1 Read Status Register 1 (RDSR1 05h)

The Read Status Register 1 (RDSR1) command allows the Status Register 1 contents to be read from SO/IO1.

The volatile version of Status Register 1 (SR1V) contents may be read at any time, even while a program, erase or write operation is in progress. It is possible to read Status Register 1 continuously by providing multiples of eight clock-cycles. The status is updated for each eight-cycle read.

Register access latency is determined by the Register Latency Code (RLC[1:0]) CR3NV[5:4].

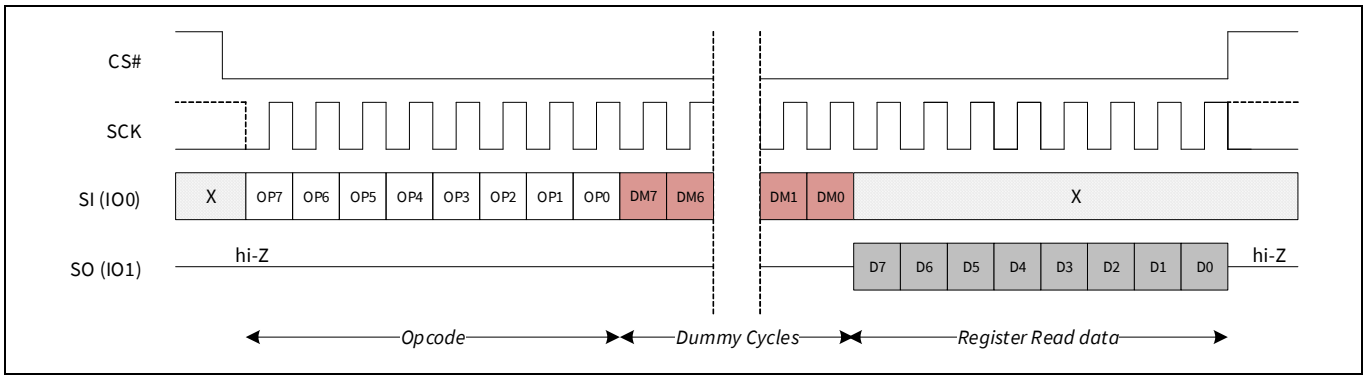


Figure 24 Read Status Register 1 (RDSR1) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

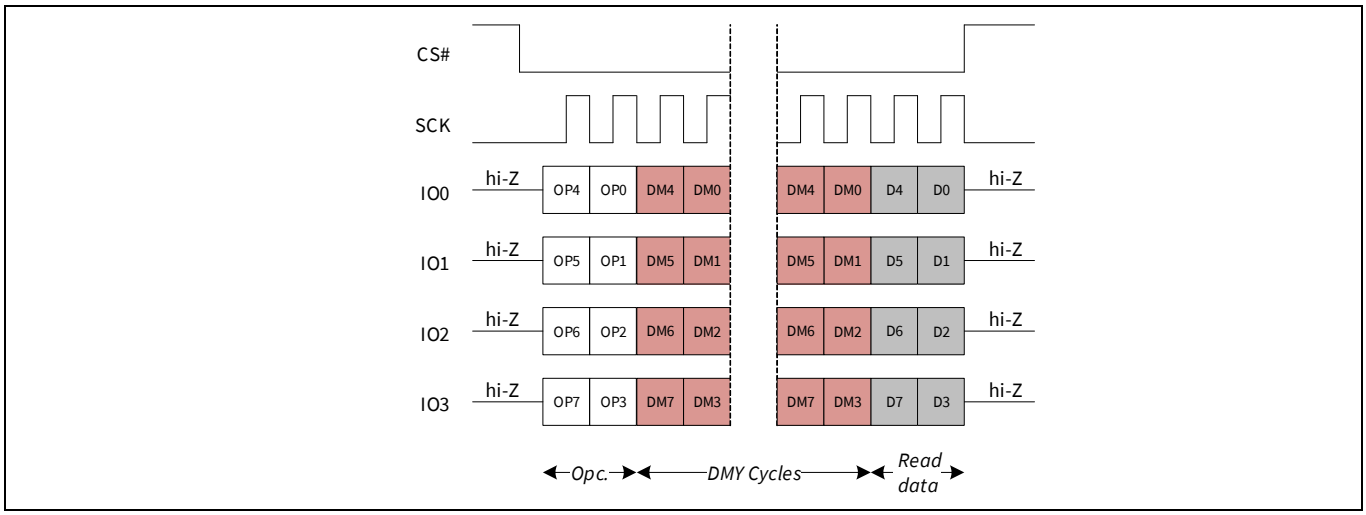


Figure 25 Read Status Register 1 (RDSR1) QPI Mode command

8.3.2 Read Status Register 2 (RDSR2 07h)

The Read Status Register 2 (RDSR2) command allows the Status Register 2 contents to be read from SO/IO1.

The volatile Status Register 2 SR2V contents may be read at any time, even while a program, erase or write operation is in progress. It is possible to read the Status Register 2 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

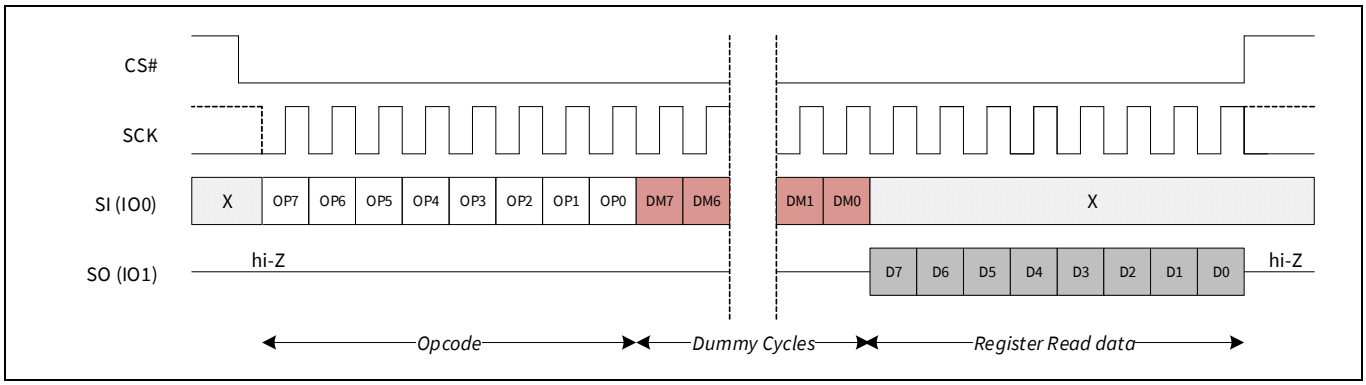


Figure 26 Read Status Register 2 (RDSR2) command

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

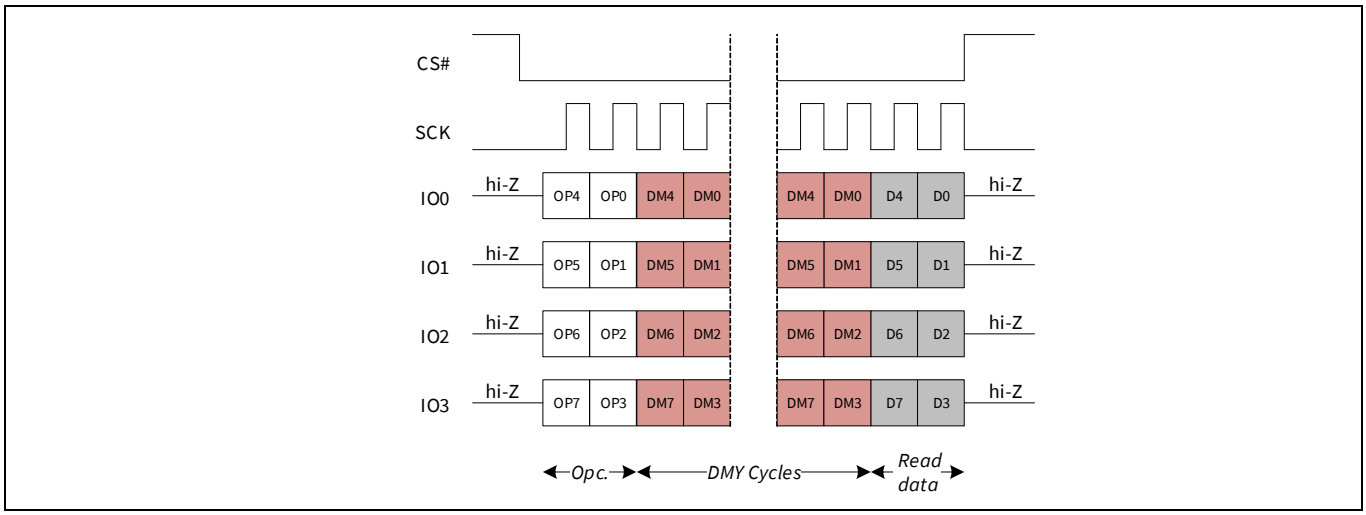


Figure 27 Read Status Register 2 (RDSR2) QPI Mode command

8.3.3 Read Configuration Registers (RDCR1 35h) (RDCR2 15h) (RDCR3 33h)

The Read Configuration Register (RDCR1, RDCR2, RDCR3) command allows the volatile Configuration Registers (CR1V, CR2V, CR3V) contents to be read from SO/IO1.

It is possible to read CR1V, CR2V and CR3V continuously by providing multiples of eight clock cycles. The Configuration Registers contents may be read at any time, even while a program, erase or write operation is in progress.

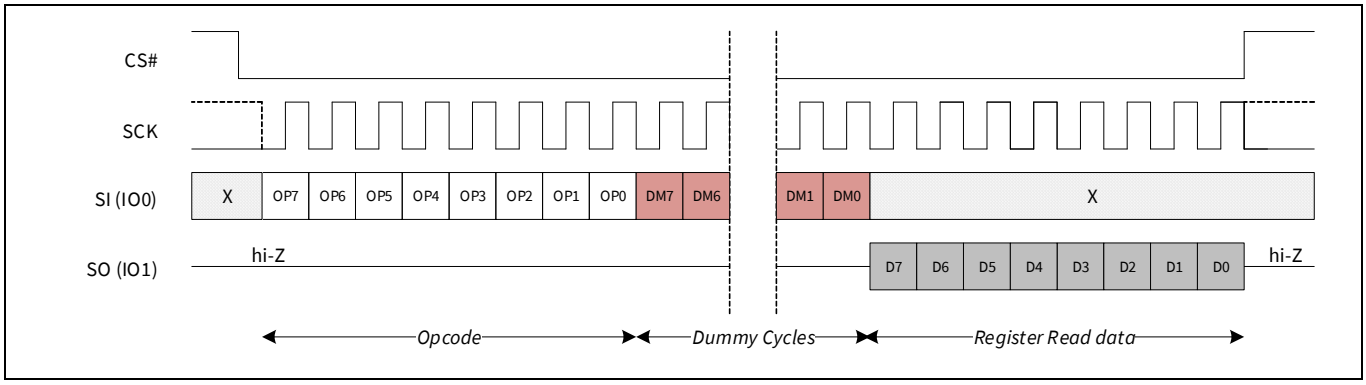


Figure 28 Read Configuration Register (RDCR1) (RDCR2) (RDCR3) command sequence

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

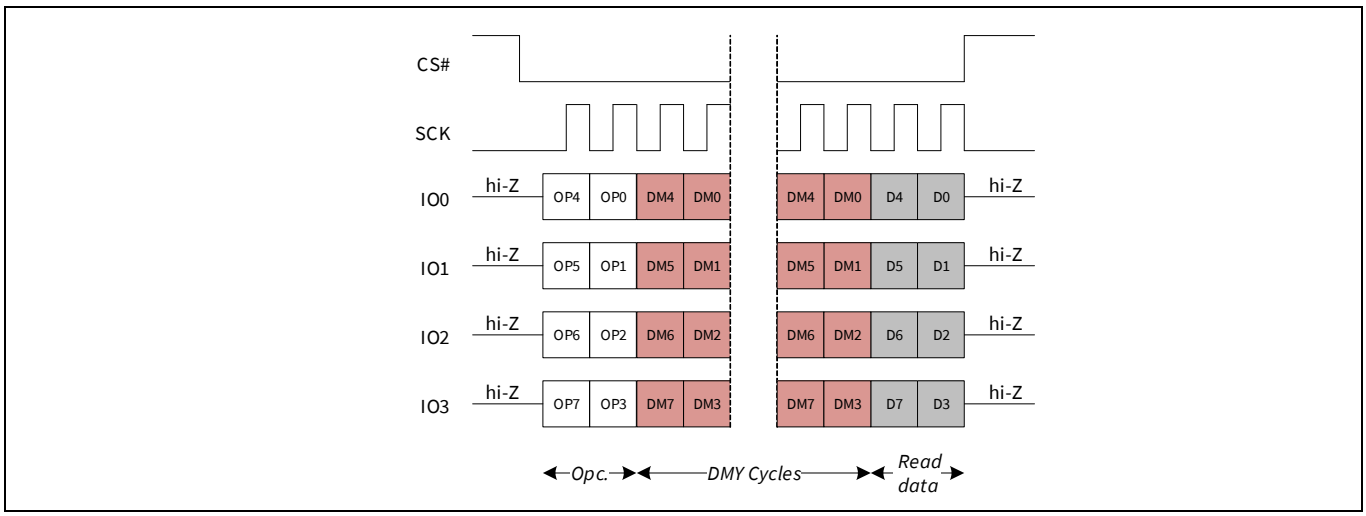


Figure 29 Read Configuration Register (RDCR1) (RDCR2) (RDCR3) QPI mode command sequence

8.3.4 Write Registers (WRR 01h)

The Write Registers (WRR) command allows new values to be written to the Status Register 1, Configuration Register 1, Configuration Register 2 and Configuration Register 3. Before the Write Registers (WRR) command can be accepted by the device, a Write Enable (WREN) command must be received. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) in the Status Register to enable non-volatile write operations and direct the values in the following WRR command to the volatile and non-volatile SR1NV, CR1NV, CR2NV and CR3NV registers.

The Write Registers (WRR) command is entered by shifting the instruction and the data-bytes on SI/IO0.

A WRR operation preceded by a WREN command, immediately writes the new value to the volatile registers then programs the new value into the non-volatile registers.

The Write Registers (WRR) command will set the P_ERR or E_ERR bits if there is a failure in the WRR operation. See **“Status Register 2 Volatile (SR2V)”** on page 23 for a description of the error bits. The device hangs busy until clear status register (CLSR) is used to clear the error and WIP for return to standby. Any Status or Configuration Register bit reserved for the future must be written as a ‘0’.

CS# must be driven to the logic HIGH state after the eighth, sixteenth, twenty-fourth or thirty-second bit of data has been latched. If not, the Write Registers (WRR) command is not executed.

If CS# is driven HIGH after the:

- eighth cycle then only the Status Register 1 is written
- sixteenth cycle both the Status 1 and Configuration 1 Registers are written;
- twenty-fourth cycle Status 1 and Configuration 1 and 2 Registers are written;
- thirty-second cycle Status 1 and Configuration 1, 2 and 3 Registers are written.

As soon as CS# is driven to the logic HIGH state, the self-timed Write Registers (WRR) operation is initiated. While the Write Registers (WRR) operation is in progress, the Status Register may still be read to check the value of the Work-in Progress (WIP) bit. The Work-in Progress (WIP) bit is a ‘1’ during the self-timed Write Registers (WRR) operation and is a ‘0’ when it is completed. The completion of the WRR command is specified by tW. When the Write Registers (WRR) operation is completed, the Write Enable Latch (WEL) is set to ‘0’.

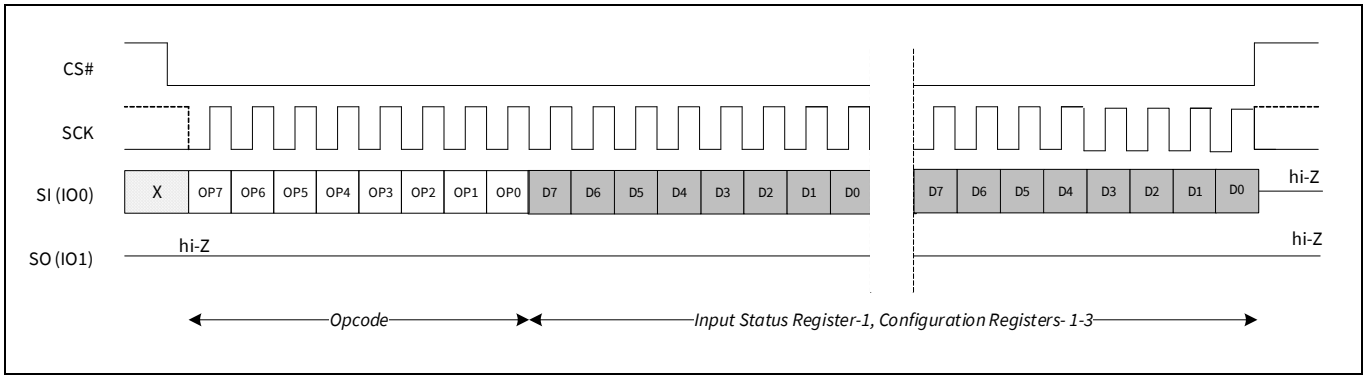


Figure 30 Write Register (WRR) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

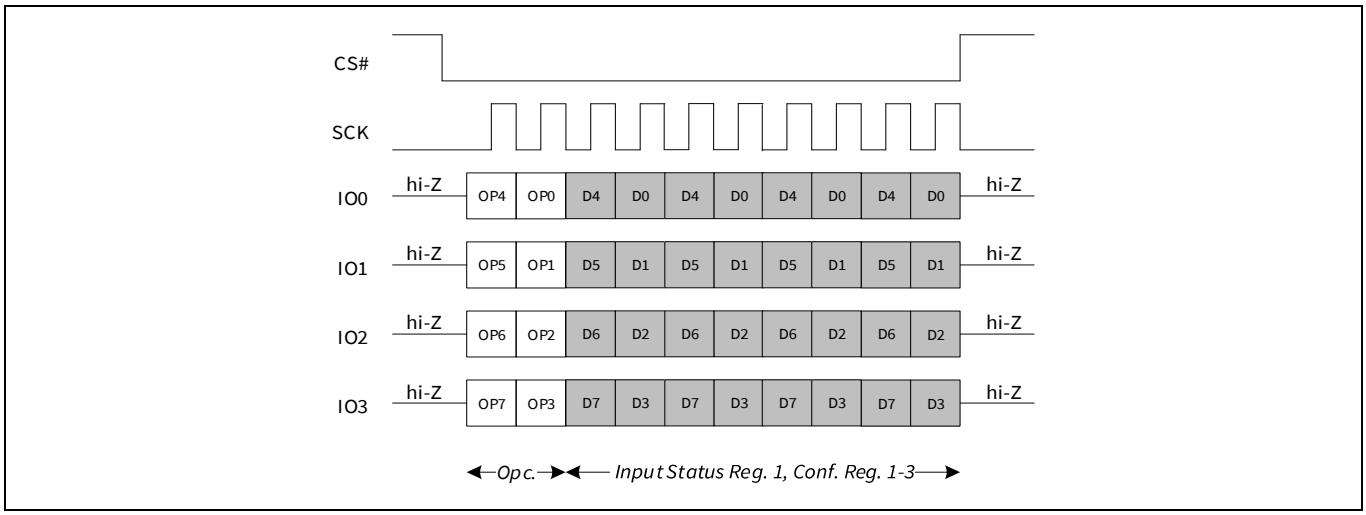


Figure 31 Write Register (WRR) command sequence QPI mode

The Write Registers (WRR) command allows the user to change the values of the Block Protection bits in either the non-volatile Status Register 1 or in the volatile Status Register 1, to define the size of the area that is to be treated as read-only.

The Write Registers (WRR) command also allows the user to set the Status Register Protect 0 (SRP0) bit to '1' or '0'. The Status Register Protect 0 (SRP0) bit and Write Protect (WP#) signal allow the BP bits to be hardware protected.

When the Status Register Protect 0 (SRP0 SR1V[7]) bit is '0', it is possible to write to the Status Register provided that the WREN command has previously been sent, regardless of whether Write Protect (WP#) signal is driven to the logic HIGH or logic LOW state.

When the Status Register Protect 0 (SRP0) bit is set to '1', two cases need to be considered, depending on the state of Write Protect (WP#):

- If Write Protect (WP#) signal is driven to the logic HIGH state, it is possible to write to the Status and Configuration Registers provided that the WREN command has previously been sent before the WRR command.
- If Write Protect (WP#) signal is driven to the logic LOW state, it is not possible to write to the Status and Configuration Registers even if the WREN command has previously been sent before the WRR command. Attempts to write to the Status and Configuration Registers are rejected, not accepted for execution and no error indication is provided. As a consequence, all the data-bytes in the memory area that are protected by the Block Protection bits of the Status Register are also hardware protected by WP#.

The WP# hardware protection can be provided:

- By setting the Status Register Protect 0 (SRP0) bit after driving Write Protect (WP#) signal to the logic LOW state.

The only way to release the hardware protection is to pull the Write Protect (WP#) signal to the logic HIGH state. If WP# is permanently tied HIGH, hardware protection of the BP bits can never be activated.

Hardware protection is disabled when Quad Mode is enabled (CR1V[1] = 1) or QPI mode is enabled (CR2V[3] = 1) because WP# becomes IO2; therefore, it cannot be utilized.

See **"Status Register Protect (SRP0)"** on page 37 for a table showing the SRP and WP# control of Status and Configuration protection.

8.3.5 Write Enable (WREN 06h)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to '1'. The Write Enable Latch (WEL) bit must be set to a '1' by issuing the Write Enable (WREN) command to enable write, program and erase commands.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI/IO0. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI/IO0, the Write Enable operation will not be executed.

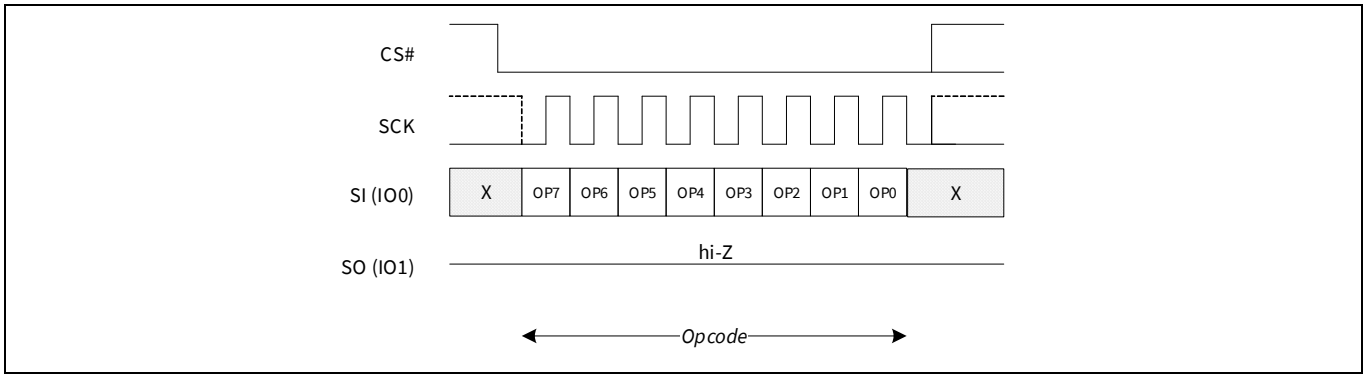


Figure 32 Write Enable (WREN) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

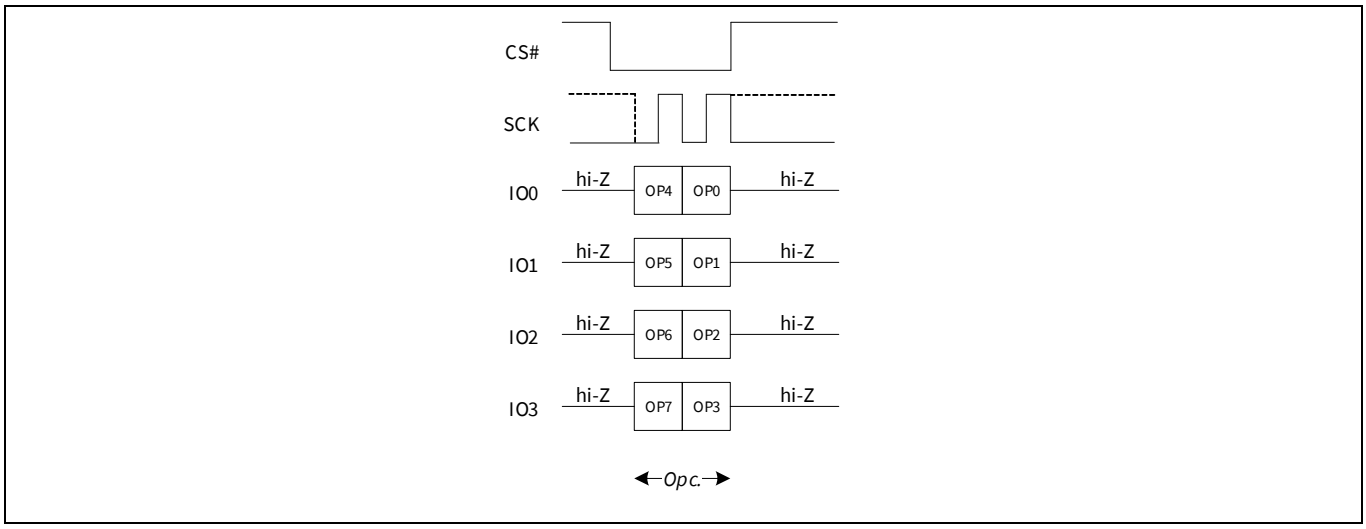


Figure 33 Write Enable (WREN) command sequence QPI mode

8.3.6 Write Disable (WRDI 04h)

The Write Disable (WRDI) command clears the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to '0'.

The Write Enable Latch (WEL) bit may be cleared to a '0' by issuing the Write Disable (WRDI) command to disable Page Program (PP, 4PP, QPP, 4QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Registers (WRR or WRAR) and other commands that require WEL be set to '1' for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit = 1.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI/IO0. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI/IO0, the write disable operation will not be executed.

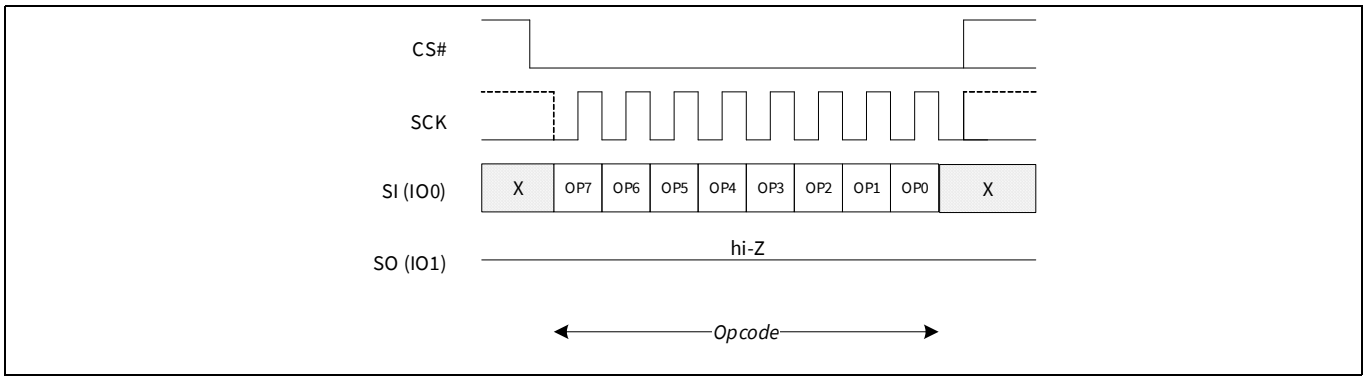


Figure 34 Write Disable (WRDI) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

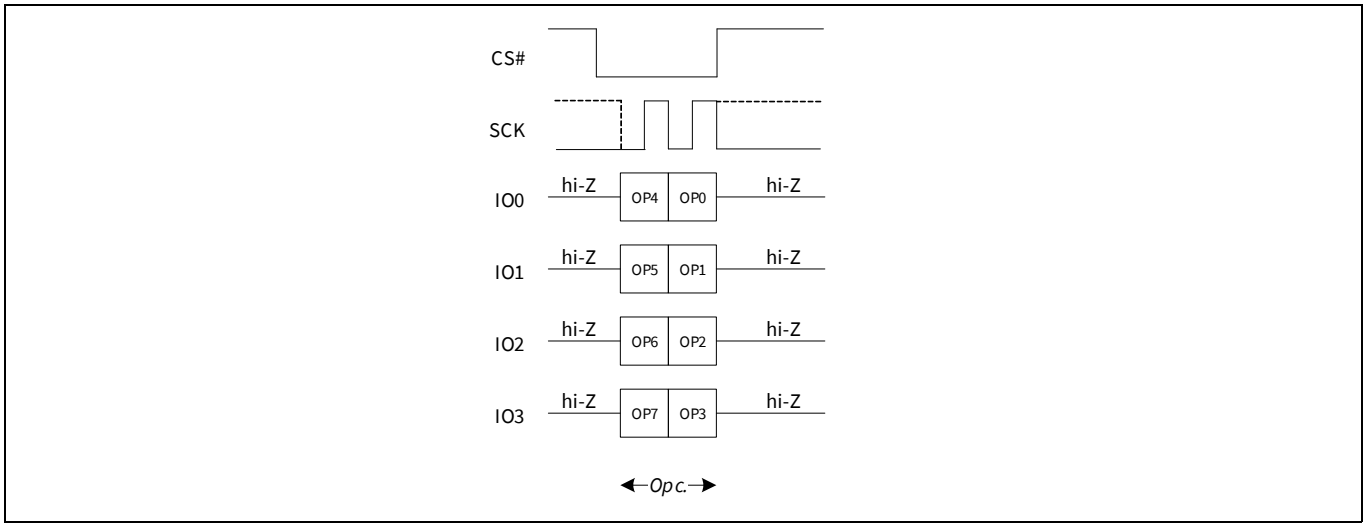


Figure 35 Write Disable (WRDI) command sequence QPI mode

8.3.7 Clear Status Register (CLSR 30h)

The Clear Status Register command clears the WIP (SR1V[0]), P_ERR (SR2V[5]) and E_ERR (SR2V[6]) bits to '0'. The WEL bit will be unchanged after this instruction is executed. It is not necessary to set the WEL bit before a Clear Status Register command is executed. The Clear Status Register command will be accepted even when the device remains busy with WIP set to '1', as the device does remain busy when either error bit is set.

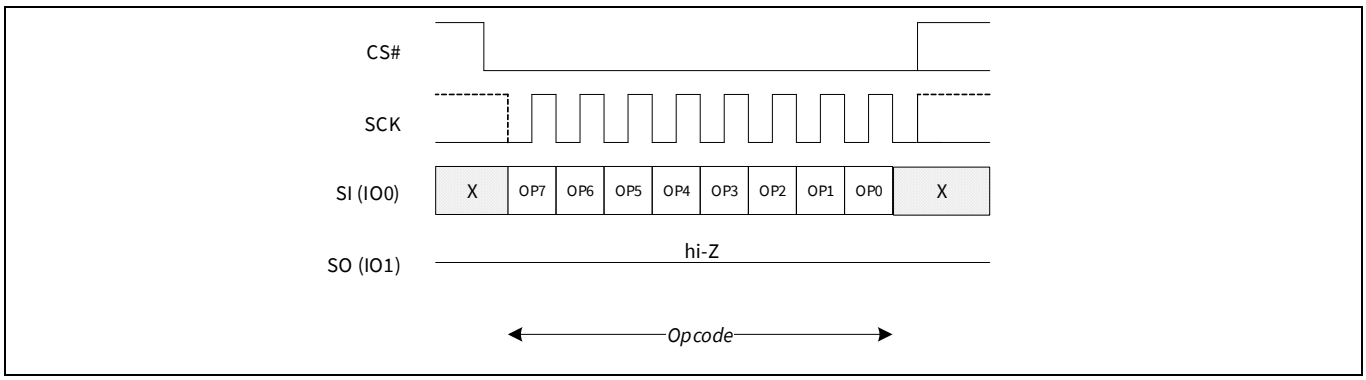


Figure 36 Clear Status Register (CLSR) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

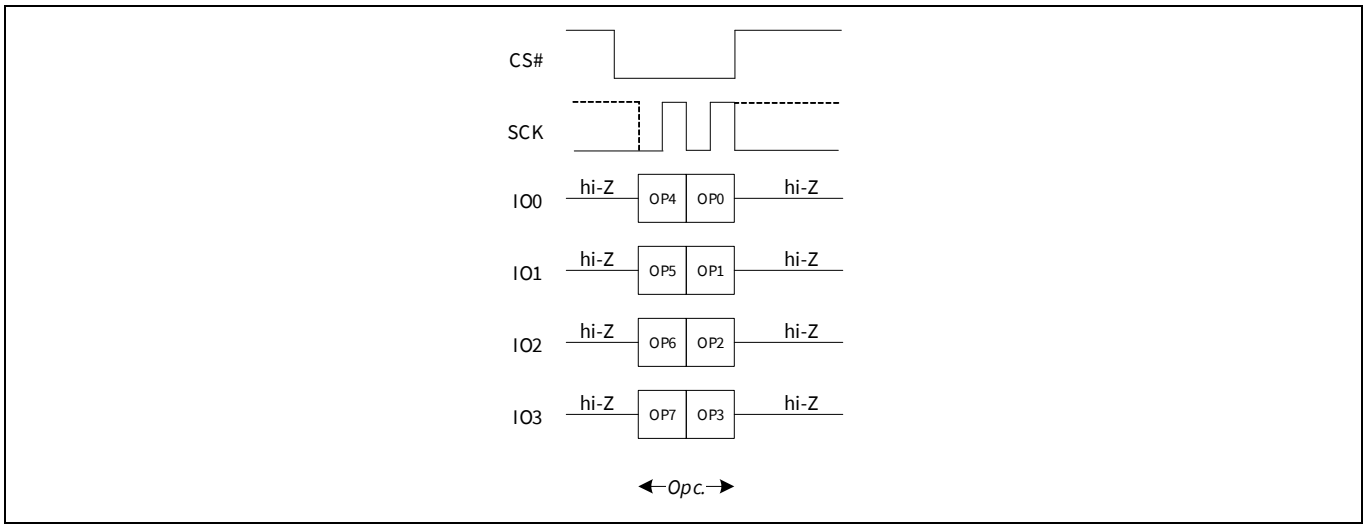


Figure 37 Clear Status Register (CLSR) QPI mode

8.3.8 Enter 4-byte address mode (4BAM B7h)

The enter 4-byte address mode (4BAM) command sets the volatile Address Length status (AD34) bit (CR1V[0]) to '1' to change all 3-byte address commands to require 4-bytes of address. This command will not affect 4-byte-only commands which will still continue to expect 4-bytes of address.

To return to 3-byte address mode the 4BEX command clears the volatile Address Length bit CR1V[0] = 0. The WRAR command can also clear the volatile Address Length bit CR1V[0] = 0. Also, a hardware or software reset may be used to return to the 3-byte address mode if the non-volatile address length bit CR1NV[0] = 1.

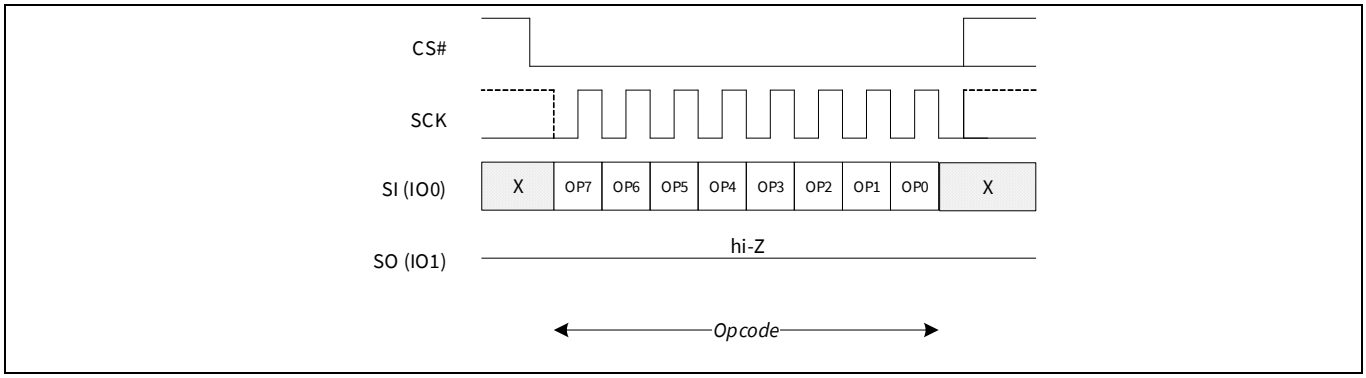


Figure 38 Enter 4-byte address mode (4BAM B7h) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

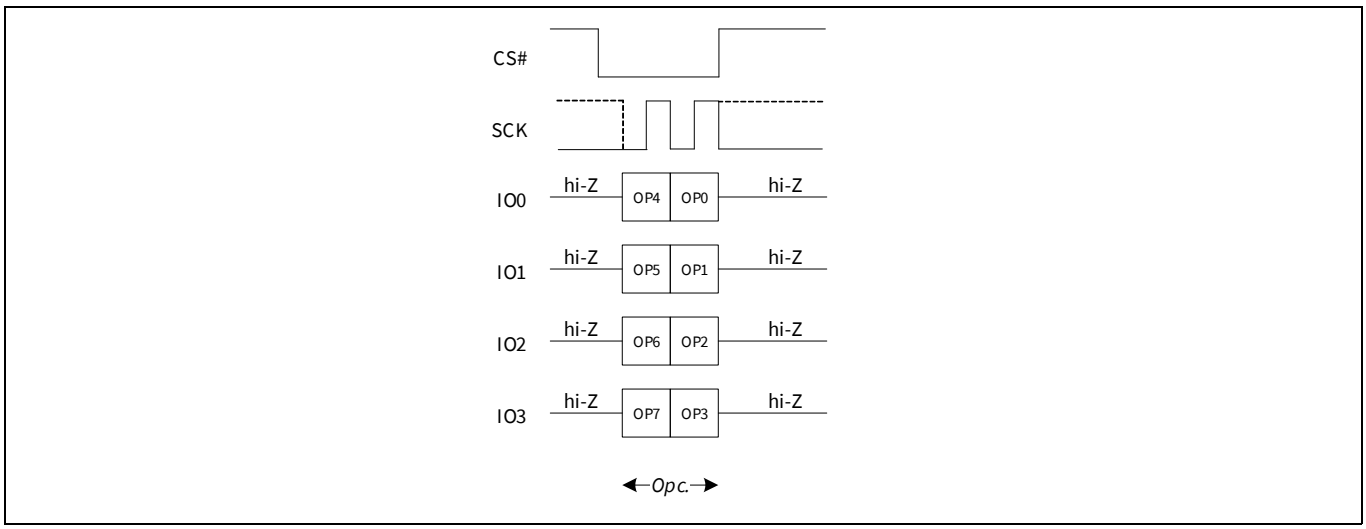


Figure 39 Enter 4-byte address QPI mode

8.3.9 Exit 4-byte address mode (4BEX E9h)

The exit 4-byte address mode (4BEX) command sets the volatile address length status (AD34) bit (CR1V[0]) to '0' to change most 4-byte address commands to require 3 bytes of address. This command will not affect 4-byte-only commands which will still continue to expect 4-bytes of address.

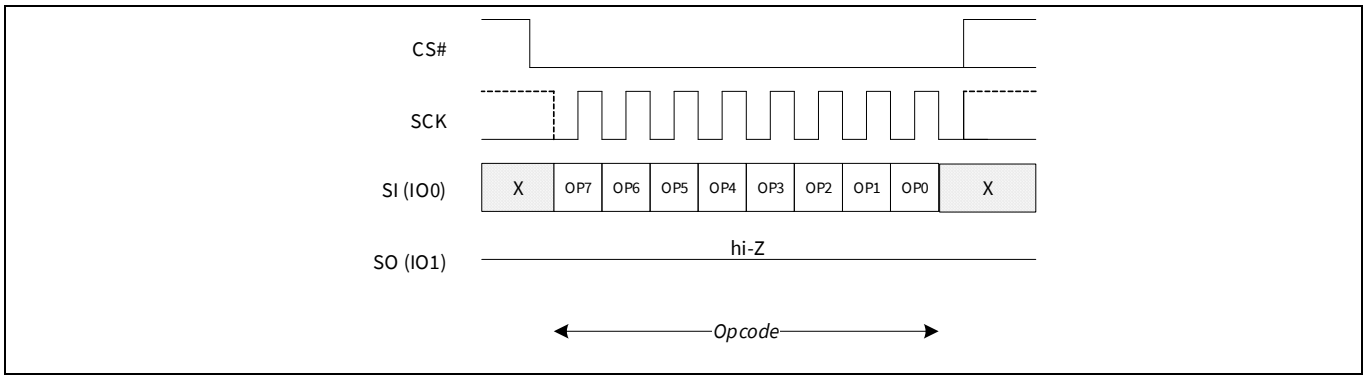


Figure 40 Exit 4-byte address mode (4BEX E9h) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

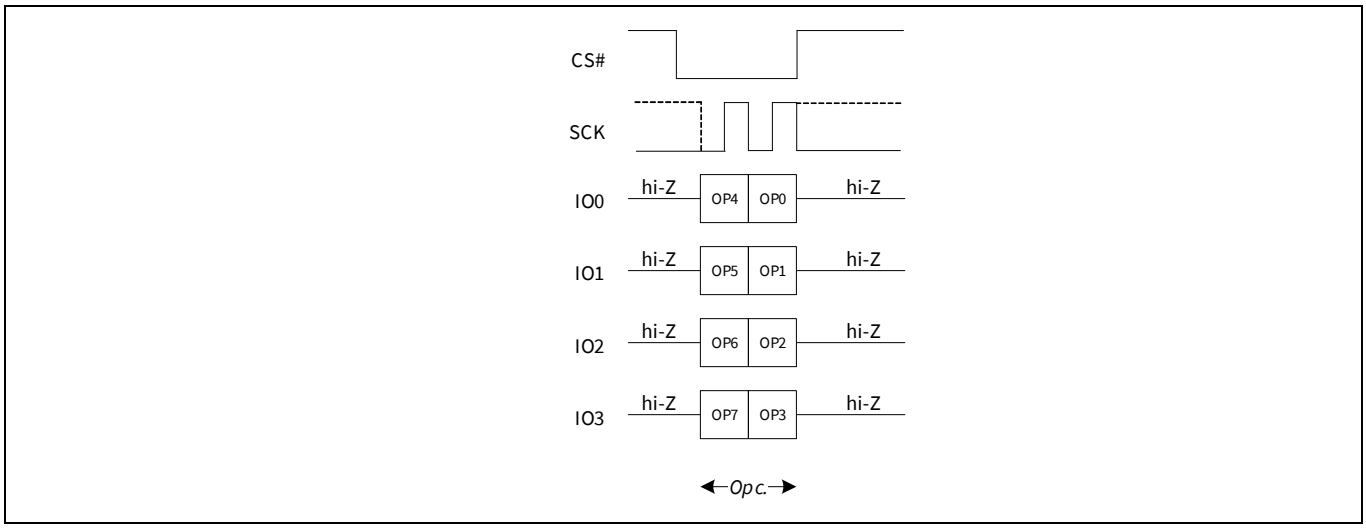


Figure 41 Exit 4-byte address QPI mode

8.3.10 Read Any Register (RDAR 65h)

The Read Any Register (RDAR) command provides a way to read all non-volatile and volatile registers. The instruction is followed by a 3- or 4-byte address (depending on the address length configuration CR1V[0]), followed by a number of latency (dummy) cycles set by CR3V[5:4] and CR3V[3:0] (depending on if volatile or non-volatile registers are addressed respectively). Then the selected register contents are returned. If the read access is continued the same addressed register contents are returned until the command is terminated - only one register is read by each RDAR command.

Reading undefined locations provides undefined data.

The RDAR command may be used during embedded operations to read Status Register 1 (SR1V).

Table 32 Register address map

Byte address (Hex)	Register name	Description
000000	SR1NV	Non-volatile Status and Configuration Registers Reading of Non-volatile Status and Configuration Registers actually reads the volatile registers.
000001	N/A	
000002	CR1NV	
000003	CR2NV	
000004	CR3NV	
...	N/A	
800000	SR1V	Volatile Status and Configuration Registers
800001	SR2V	
800002	CR1V	
800003	CR2V	
800004	CR3V	
...	N/A	
800089	ECCSR	ECC Status Register
80008A	ECCDC[7:0]	ECC Error Detection Count Register[7:0]
80008B	ECCDC[15:8]	ECC Error Detection Count Register[15:8]
80008C	ECCDC[23:16]	ECC Error Detection Count Register[23:16]
80008D	ECCDC[31:24]	ECC Error Detection Count Register[31:24]
80008E	ADDTRAPR[7:0]	ECC Address Trap Register[7:0]
80008F	ADDTRAPR[15:8]	ECC Address Trap Register[15:8]
800040	ADDTRAPR23:16]	ECC Address Trap Register[23:16]
800041	ADDTRAPR[31:24]	ECC Address Trap Register[31:24]
...	N/A	
800067	ISR	Interrupt Status Register
800068	ICR	Interrupt Configuration Registers
...	N/A	

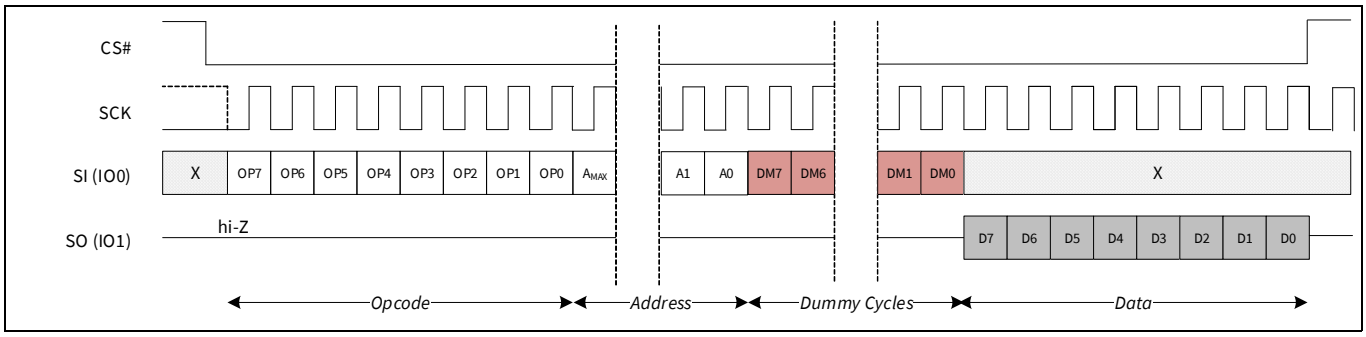


Figure 42 Read Any Register Read command sequence[3]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in and returning data out on IO0–IO3.

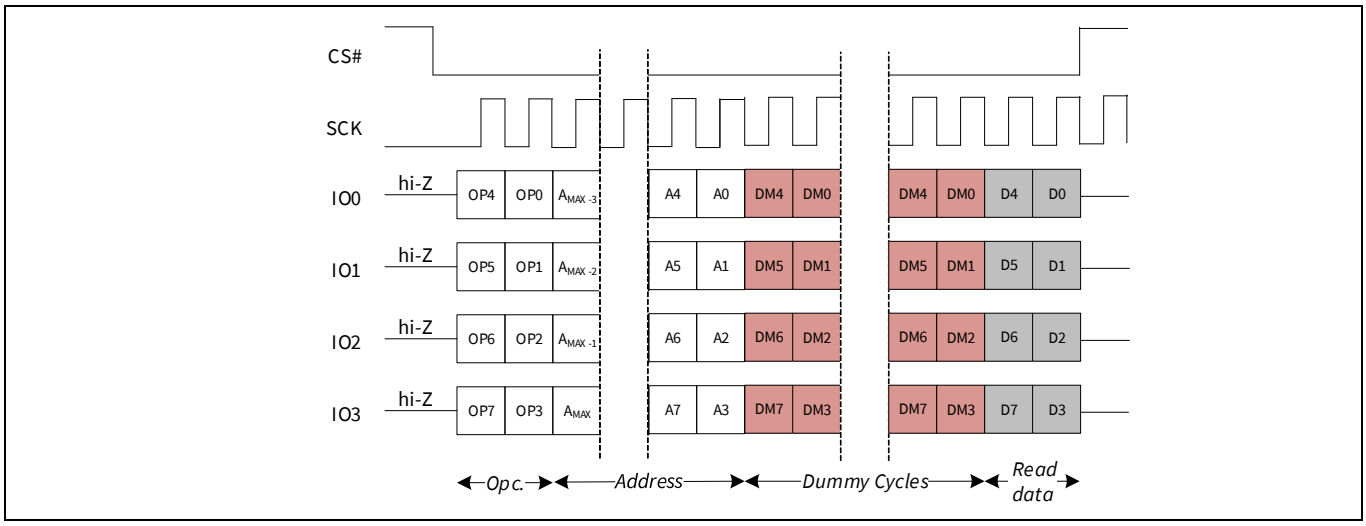


Figure 43 Read Any Register, QPI mode, command sequence[3]

Note
3. A = MSB of address = 23 for Address length CR2V[0] = 0, or 31 for CR2V[0] = 1.

8.3.11 Write Any Register (WRAR 71h)

The Write Any Register (WRAR) command provides a way to write any device register - non-volatile or volatile. The instruction is followed by a 3- or 4-byte address (depending on the address length configuration CR1V[0]), followed by one byte of data to write in the address-selected register.

Before the WRAR command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR and E_ERR bits in SR2V may be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit-types and individual rules controlling which bits may be modified. Read-only bits are never modified and the related bits in the WRAR command data-byte are ignored without setting a program or erase error indication (P_ERR or E_ERR in SR2V). Hence, the value of these bits in the WRAR data-byte do not matter.

Non-volatile bits which are changed by the WRAR command, require non-volatile register write time (tW) to be updated. The update process involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails, the related error-bit in SR2V and WIP in SR1V will be set to ‘1’.

Volatile bits which are changed by the WRAR data, require the volatile register write time (t_{CS}) to be updated.

Status Register-1 may be repeatedly read (polled) to monitor the Work-In-Progress (WIP) bit (SR1V[0]) to determine when the register write is completed and Status Register-2 for the error bits (SR2V[6, 5]) to determine if there is write failure. If there is a write failure, the clear status command is used to clear the error status and enable the device to return to standby state. When the WRAR operation is completed, the Write Enable Latch (WEL) is set to a ‘0’.

The WRAR command sequence and behavior is the same as the PP or 4PP command with only a single byte of data provided. See **“Single Byte programming”** on page 78.

The address map of the registers is the same as shown in **Table 32**.

8.3.12 Set Wrap Length (SWL 77h)

The Set Wrap Length (SWL) command is used to configure the Burst Wrap feature. Burst Wrap is used in conjunction with Read, Fast Read, Quad I/O Read in SPI, QIO or QPI modes, to access a fixed length and alignment of data. Certain applications can benefit from this feature by improving the overall system code execution performance. The Burst Wrap feature allows applications that use cache to start filling a cache line with instruction or data from a critical address first, then fill the remainder of the cache line afterwards within a fixed length (8-/16-/32-/64-bytes) of data without issuing multiple read commands.

The Set Wrap Length command is initiated by driving the CS# pin low and then shifting the instruction code “77h” and 8 “Wrap Length Bits (WL[7]–WL[0])”. Wrap Length bits WL[7] and the lower nibble WL[3:0] are not used. See Configuration Register 1 (CR1V[6:4]) for the encoding of WL[6]–WL[4] in Configuration 1 Register. Once WL[6:4] is set by a Set Wrap Length command all the following read commands will use the WL[6:4] setting to access the 8/16/32/64-byte section of data. To exit the “Wrap Around” function and return to normal read operation another Set Burst with Wrap command should be issued to set WL4 = 0. The default value of WL[6:4] upon power-on, hardware or software reset is set in the CR1NV[6:4]. Use WRR or WRAR command to set the default wrap length in CR1NV[6:4]. The Set Wrap Length (SWL) command writes only to CR1V[6:4] bits to enable or disable the wrapped read feature and set the wrap boundary. See **Table 33** for CR1V[6:5] values for wrap boundaries and start address. When enabled the wrapped read feature changes the related read commands from sequentially reading until the command ends to reading sequentially wrapped within a group of bytes.

When the wrap mode is not enabled (**Table 11**) an unlimited length sequential read is performed.

When the wrap mode is enabled (**Table 10** and **Table 11**) a fixed length and aligned group of 8-, 16-, 32- or 64-bytes is read starting at the byte address provided by the read command and wrapping around at the group alignment boundary.

The group of bytes is of length and aligned on an 8-, 16-, 32- or 64-byte boundary. CR3V[6:5] selects the boundary.

The starting address of the read command selects the group of bytes and the first data returned is the addressed byte. Bytes are then read sequentially until the end of the group boundary is reached. If the read continues the address wraps to the beginning of the group and continues to read sequentially. This wrapped read sequence continues until the command is ended by CS# returning HIGH.

Table 33 Example burst wrap sequences

CR3V value (Hex)	Wrap boundary (bytes)	Start address (Hex)	Address sequence (hex)
1X	Sequential	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...
00	8	XXXXXX00	00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02, ...
00	8	XXXXXX07	07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, ...
01	16	XXXXXX02	02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, ...
01	16	XXXXXX0C	0C, 0D, 0E, 0F, 00, 01, 02, 03, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, ...
02	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, ...
02	32	XXXXXX1E	1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, ...

Table 33 Example burst wrap sequences *(continued)*

CR3V value (Hex)	Wrap boundary (bytes)	Start address (Hex)	Address sequence (hex)
03	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, ...
03	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...

The power-on reset, hardware reset or software reset default Wrap Length can be changed by programming CR1NV with the desired value using the WRAR command.

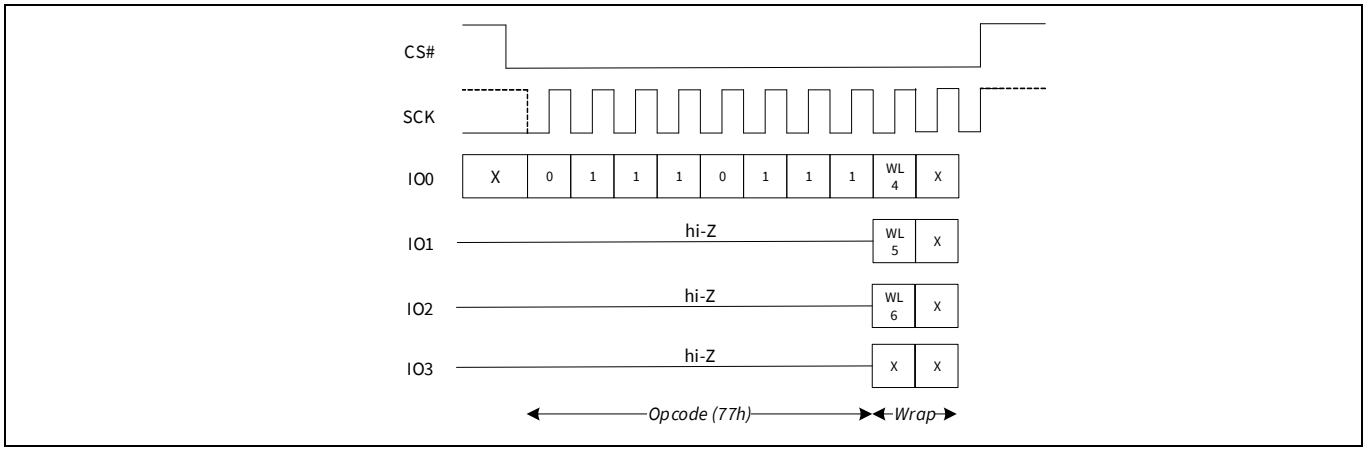


Figure 44 Set Wrap Length command sequence quad I/O mode

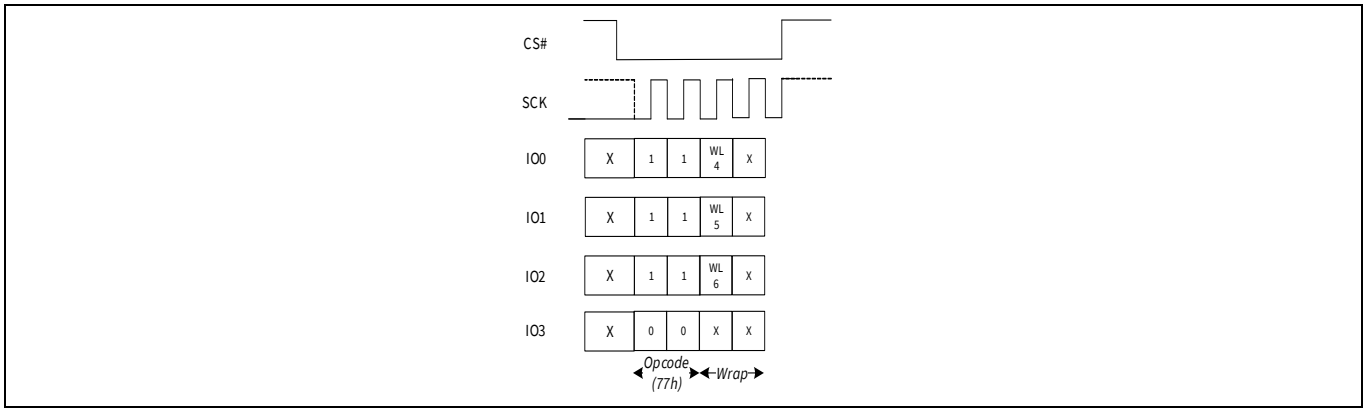


Figure 45 Set Wrap Length command sequence QPI mode

8.3.13 Enter QPI mode (QPIEN 38h)

The enter QPI mode (QPIEN) command enables the QPI mode by setting the volatile QPI bit (CR2V[3] = 1). See **Table 14**.

To return to SPI mode the SPIEX command or a write to register (CR2V[3] = 0) is required. A power-on reset, hardware or software reset will also return the part to SPI mode if the non-volatile QPI (CR2NV[3] = 0). See **Table 12**.

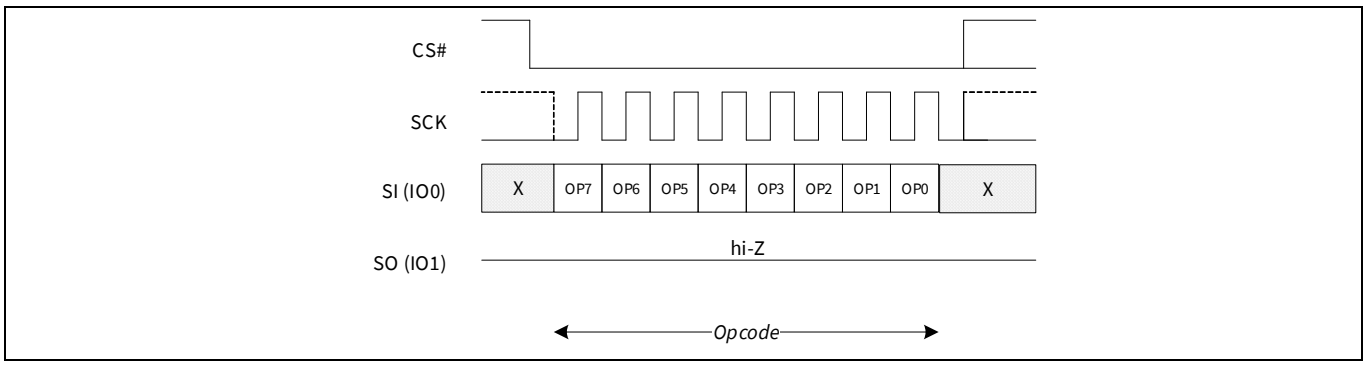


Figure 46 Enter QPI mode (QPIEN 38h) command sequence

8.3.14 Enter SPI mode (SPIEN F5h)

The enter SPI Mode (SPIEN) instruction enables the Single channel mode by resetting the QPI configuration bit to '0'. This makes SI / IO0 as input and SO/IO1 as output signals. WP# functionality is also made active.

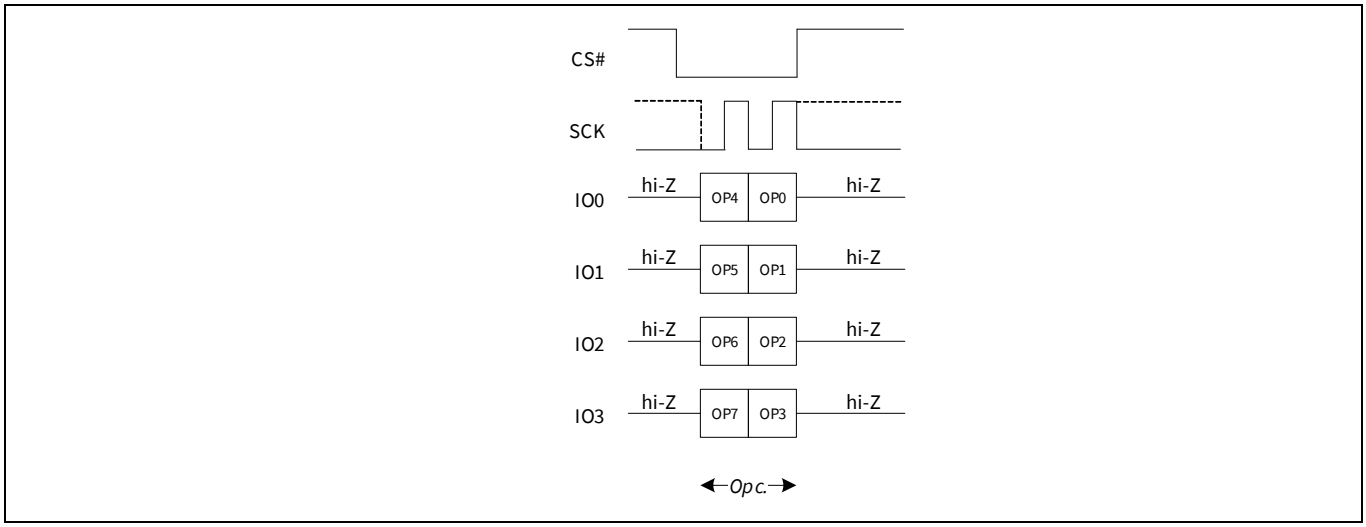


Figure 47 Enter SPI (SPIEN F5h) command sequence

8.3.15 ECC Status Read (ECCRD 19h, 4ECCRD 18h)

The ECCRD instruction is used to determine the ECC status of the addressed unit data. In ECCRD instruction the Least Significant Bits (LSB) of the address must start aligned to an ECC data unit. This is followed by the number of dummy-cycles selected by the read latency value for Read (Memory latency since the ECC data resides in the memory core). The 8-bit contents of the ECC Status are then shifted out. If CS# remains LOW the following data will be indeterminate. To read the next ECC unit status another ECCRD command should be sent out to the next address incremented by [Unit data size / 8] bytes (as an example).

Note: ECCRD latency will be the same as the memory core read latency. It will ignore the read wrap configuration registers and only operate in continuous read mode. However, 8/2 cycles will need to be added for SPI/QPI to accommodate the missing MODE byte which is present in all fast Read instructions.

Table 34 ECC Status Information

Bits	Name	Function	Read/Write	Default state	Description
7	RFU	Reserved		0	Reserved for future use
6	RFU	Reserved		0	Reserved for future use
5	RFU	Reserved		0	Reserved for future use
4	EECC2D	2-bit error in ECC unit	R	0	1 = 2-bit error detected and corrected in ECC unit 0 = No error
3	EECC1D	1-bit error in ECC unit	R	0	1 = 1-bit error detected and corrected in ECC unit 0 = No error
2	RFU	Reserved		0	Reserved for future use
1	RFU	Reserved		0	Reserved for future use
0	RFU	Reserved		0	Reserved for future use

2-Bit Error in ECC Unit (EECC2D) ECCRD: This bit indicates a 2-bit error was detected and corrected in the ECC unit. The default state of '0' for this bit indicates no failures.

Single Bit Error in ECC Unit (EECC1D) ECCRD: This bit indicates a 1-bit error was detected and corrected in the ECC unit. The default state of '0' for this bit indicates no failures.

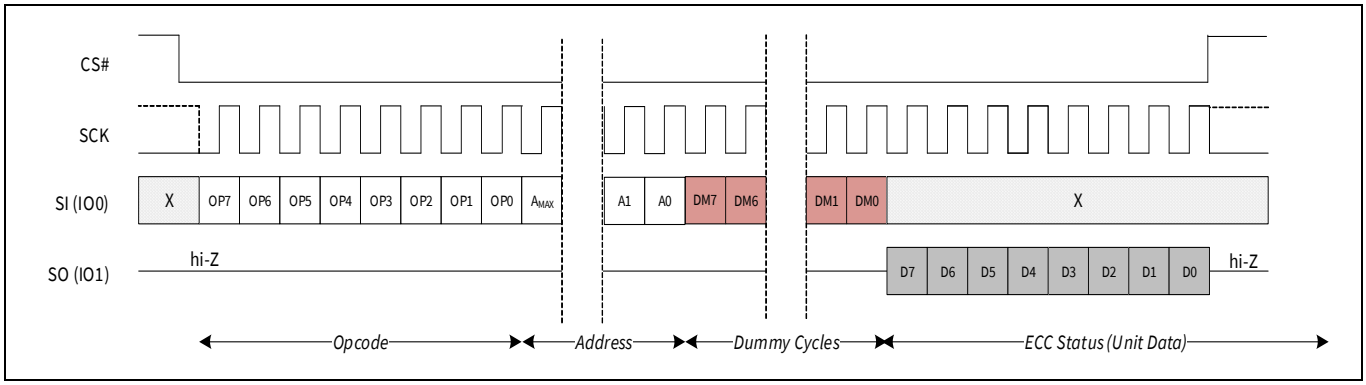


Figure 48 ECCRD in SPI mode

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

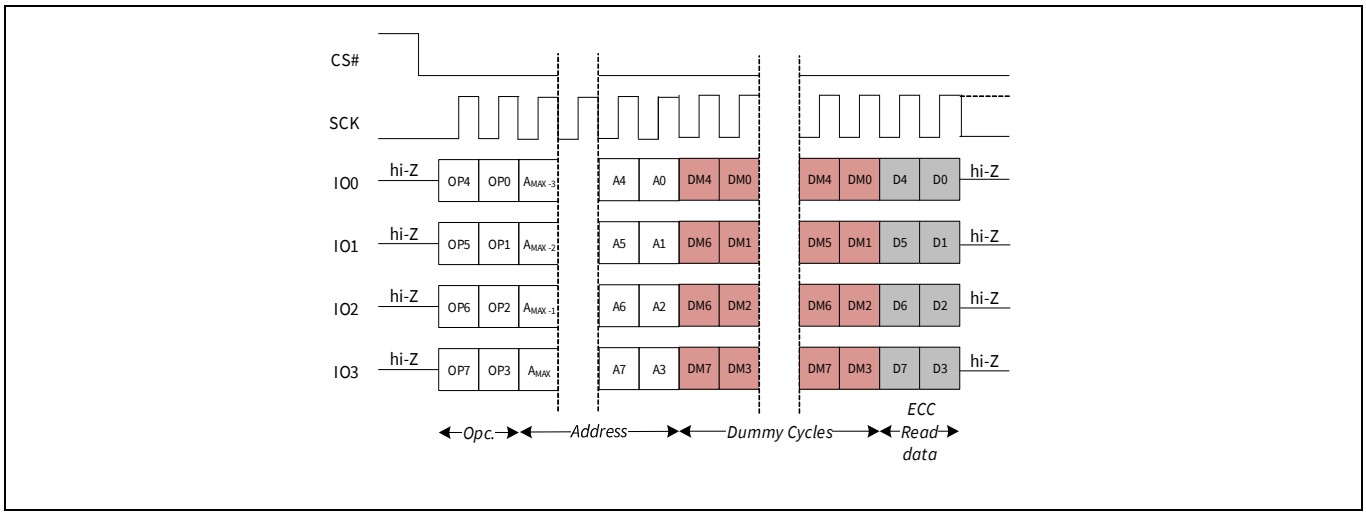


Figure 49 ECCRD in QPI mode

8.3.16 Clear ECC (CLECC 1Bh)

The Clear ECC Instruction clears all ECC flags, Address Trap and ECCDC registers. It is not necessary to set the WEL bit before a Clear Status Register instruction is executed.

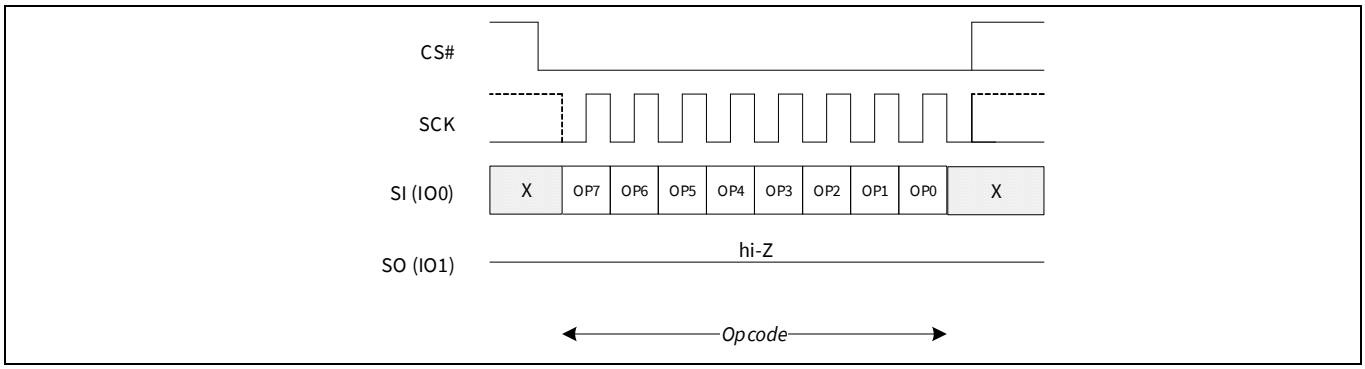


Figure 50 Clear ECC (CLECC 1Bh) in SPI mode

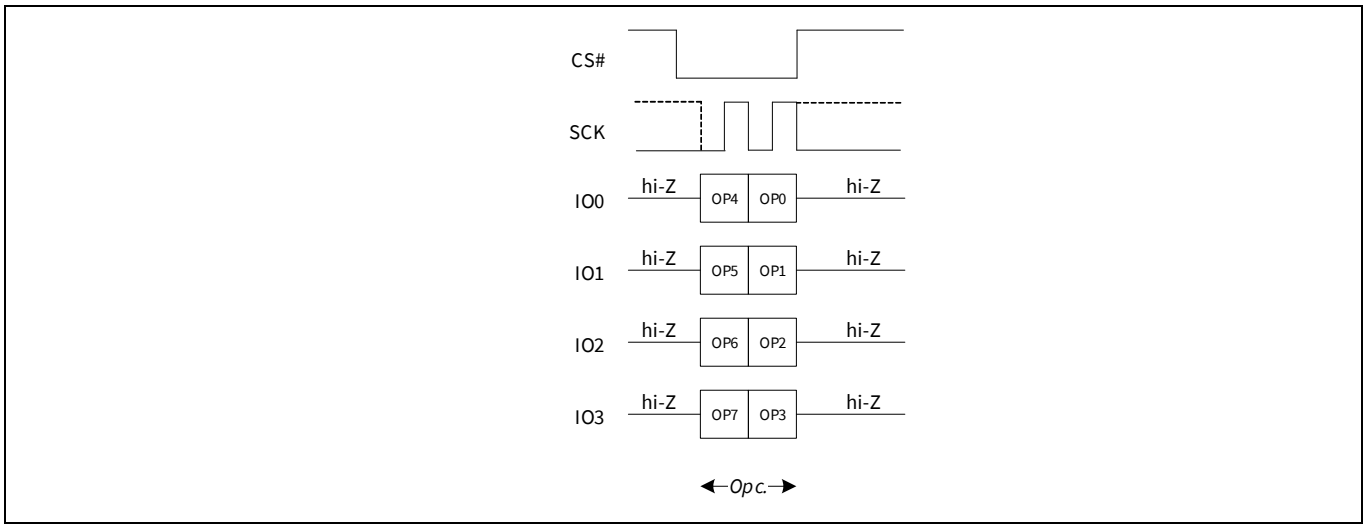


Figure 51 Clear ECC (CLECC 1Bh) in QPI mode

8.4 Read Memory Array commands

Read commands for the main Flash array provide many options for prior generation SPI compatibility or enhanced performance SPI:

- Commands transfer address or data on each rising-edge of SCK. These are called Single Data Rate commands.
- Some commands transfer address one bit per rising-edge of SCK and return data 1 bit of data per rising-edge of SCK. These are called Single width commands.
- Some commands transfer both address and data 4 bits per rising-edge of SCK. These are called Quad I/O and QPI for 4 bit. QPI also transfers instructions 4 bits per rising-edge.

All of these commands, except QPI Read, begin with an instruction code that is transferred one bit per SCK rising-edge. QPI Read transfers the instruction 4 bits per SCK rising-edge. The instruction is followed by either a 3- or 4-byte address transferred. Commands transferring address or data 4 bits per clock-edge are called Multiple I/O (MIO) commands. For CYEL17B family devices at 512 Mb or higher density, the traditional SPI 3-byte addresses are unable to directly address all locations in the memory array. Separate 4-byte address read commands are provided for access to the entire address space. These devices may be configured to take a 4-byte address from the host system with the traditional 3-byte address commands. The 4-byte address mode for traditional commands is activated by setting the Address Length bit in Configuration Register 1 to ‘1’.

The execute-in-place XIP (FAST_READ, 4FAST_READ, QIOR and 4QIOR) commands provide a performance improvement option controlled by mode bits that are sent following the address bits. The mode bits indicate whether the command following the end of the current read will be another read of the same type, without an instruction at the beginning of the read. These mode bits give the option to eliminate the instruction cycles when doing a series of XIP accesses.

Some commands require delay cycles following the address or mode bits to allow time to access the memory array - read latency. The delay or read latency cycles are traditionally called dummy-cycles. The dummy-cycles are ignored by the memory thus any data provided by the host during these cycles is “don’t care” and the host may also leave the SI signal at high impedance during the dummy-cycles. When MIO commands are used the host must stop driving the IO signals (outputs are high impedance) before the end of last dummy cycle. The number of dummy-cycles varies with the SCK frequency or performance option selected via the Configuration Register 3 (CR3V[3:0]) Latency Code. Dummy-cycles are measured from SCK falling edge to next SCK falling edge. SPI outputs are traditionally driven to a new value on the falling edge of each SCK. Zero dummy-cycles means the returning data is driven by the memory on the same falling edge of SCK that the host stops driving address or mode bits.

When using I/O commands at higher SCK frequencies (> 20 MHz), a Latency Code that provides 1 or more dummy-cycles should be selected to allow additional time for the host to stop driving before the memory starts driving data to minimize I/O driver conflict.

Each read command ends when CS# is returned HIGH at any point during data return. CS# must not be returned HIGH during the mode or dummy-cycles before data returns as this may cause mode bits to be captured incorrectly; making it indeterminate as to whether the device remains in continuous read mode. In this case, an MBR opcode must be issued to reset the mode byte to a known state.

8.4.1 Read (Read 03h or 4READ 13h)

The instructions are

- 03h (CR1V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 03h (CR1V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 13h is followed by a 4-byte address (A31–A0)

Then the memory contents, at the address given, are shifted out on SO/IO1.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached the address counter will wrap around and roll back to 000000h allowing the read sequence to be continued indefinitely.

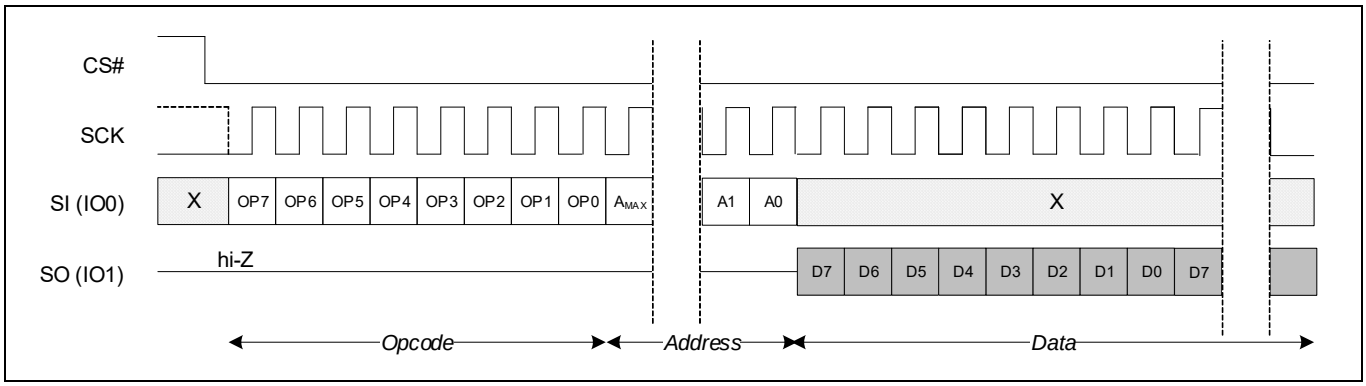


Figure 52 Read command sequence[4]

Note

4. A = MSB of address = 23 for CR1V[0] = 0, or 31 for CR1V[0] = 1 or command 13h.

8.4.2 Fast Read (FAST_READ 0Bh or 4FAST_READ 0Ch)

The instructions are

- 0Bh (CR1V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 0Bh (CR1V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 0Ch is followed by a 4-byte address (A31–A0)

For the Fast Read command, there is a latency required after the mode bits (described below) before data begins shifting out. This latency period (i.e., dummy-cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles the data values on the IO's are "don't care" and may be high impedance. The number of dummy-cycles required is determined by the frequency of SCK. The latency is configured in CR3V[3:0].

Following the latency period the memory contents at the address given is shifted out one bit at a time (SPI) through SO_IO1 or four bits at a time (Quad mode, QPI mode) through IO0–IO3. Data is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

Address jumps can be done without the need for additional Read instructions. This is controlled through the setting of the Mode bits after the address sequence. This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7–4) of the Mode bits control the length of the next read instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3–0) of the Mode bits are "don't care" ("x"). If the Mode bits equal Axh, then the device remains in XIP Mode and the next address can be entered (after CS# is raised HIGH and then asserted LOW) without requiring the read opcode, thus, eliminating cycles for the command sequence. The following sequences will release the device from XIP mode; after which, the device can accept standard SPI commands:

- During the Fast Read Command Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised HIGH the device will be released from XIP mode.
- Send the Mode Reset command.

Note that the mode bit clock cycles and additional wait-states (i.e., dummy-cycles) allow the device's internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0–IO3.

It is important that the IO signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn around) is diminished. It is allowed and may be helpful in preventing IO signal contention, for the host system to turn off the IO signal outputs (make them high-impedance) during the last "don't care" mode cycle or during any dummy-cycles.

CS# should not be driven HIGH during mode or dummy bits as this may make the mode bits indeterminate.

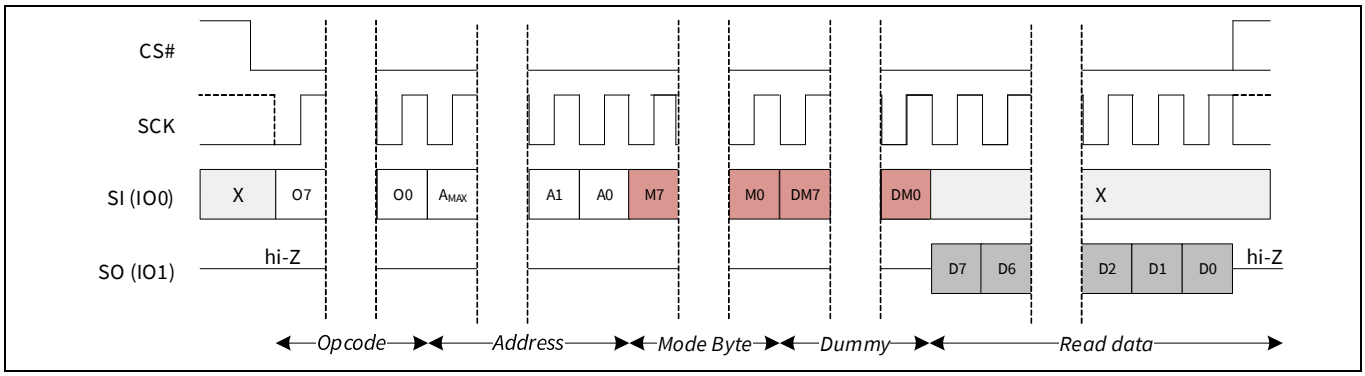


Figure 53 Fast Read (FAST_READ) command sequence[5]

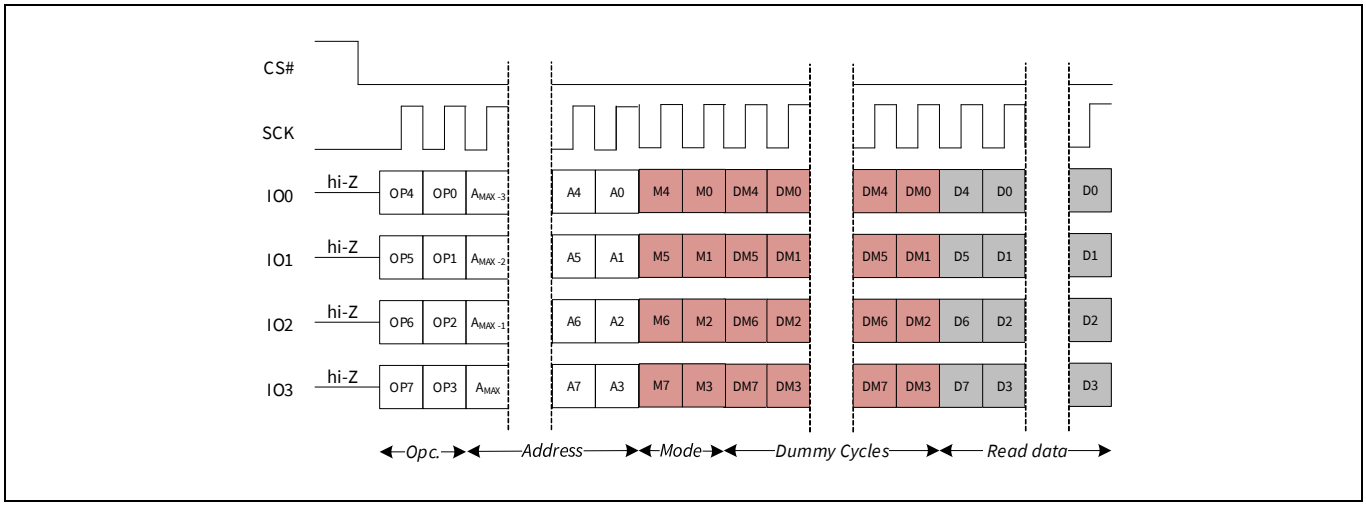


Figure 54 Fast Read (FAST_READ) command sequence in QPI mode

Note
5. A = MSB of address = 23 for CR1V[0] = 0, or 31 for CR1V[0] = 1 or command 6Ch.

8.4.3 Quad Output Read (QOR 6Bh or 4QOR 6Ch)

The instructions are

- 6Bh (CR1V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 6Bh (CR1V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 6Ch is followed by a 4-byte address (A31–A0)

Note QOR and 4QOR are only available if the QUAD bit is set. QOR and 4QOR are NOT available in QPI mode.

The address is followed by dummy-cycles depending on the latency code set in the Configuration Register CR3V[3:0]. The dummy-cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy-cycles the data value on IO0–IO3 is “don’t care” and may be high impedance.

After the dummy-cycles the memory content at the address given is shifted out four bits at a time through IO0–IO3. Each nibble (4 bits) is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached the address counter will wrap around and roll back to 000000h - allowing the read sequence to be continued indefinitely.

For Quad Output Read commands, there are dummy-cycles required after the last address bit are shifted into IO0 before data begins shifting out of IO0–IO3.

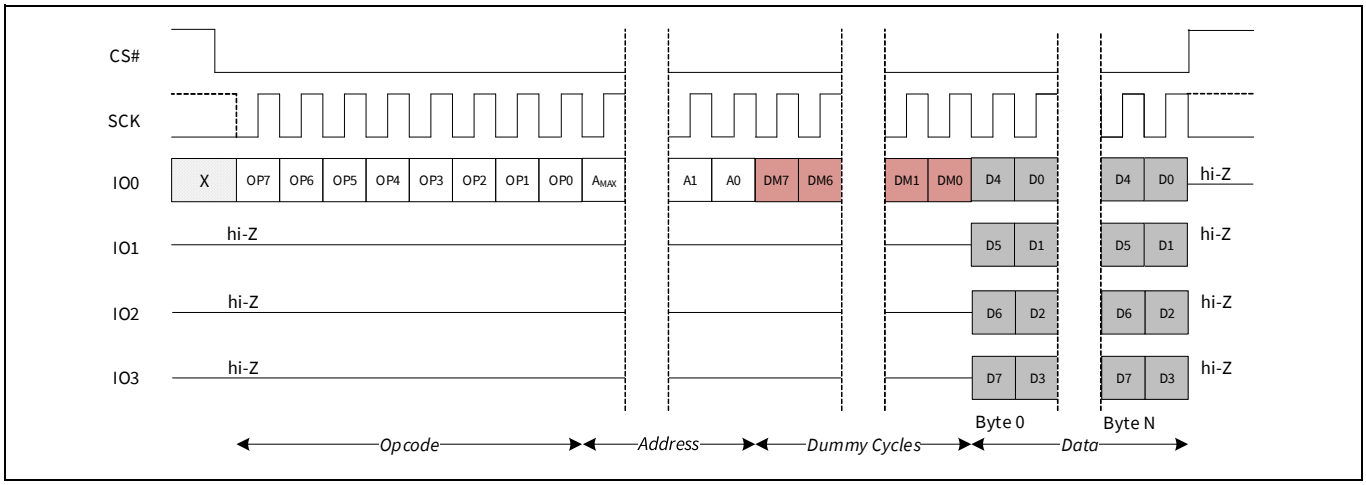


Figure 55 Quad Output Read command sequence[6]

Note
6. A = MSB of address = 23 for CR1V[0] = 0, or 31 for CR1V[0] = 1 or command 6Ch.

8.4.4 Quad I/O Read (QIOR EBh or 4QIOR ECh)

The instructions are

- EBh (CR1V[0] = 0) is followed by a 3-byte address (A23–A0) or
- EBh (CR1V[0] = 1) is followed by a 4-byte address (A31–A0) or
- ECh is followed by a 4-byte address (A31–A0)

The Quad I/O Read command improves throughput with four I/O signals IO0–IO3. It allows input of the address bits four bits per serial SCK clock. In some applications the reduced instruction overhead might allow for code execution (XIP) directly from the NOR Flash device. The QUAD bit of the Configuration Register 1 must be set (CR1V[1] = 1) or the QPI bit of Configuration Register 2 must be set (CR2V[1] = 1 to enable the Quad capability of the NOR Flash devices.

For the Quad I/O Read command there is a latency required after the mode bits (described below) before data begins shifting out of IO0–IO3. This latency period (i.e., dummy-cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles the data values on IO0–IO3 are "don't care" and may be high impedance. The number of dummy-cycles is determined by the frequency of SCK. The latency is configured in CR3V[3:0].

Following the latency period the memory contents at the address given is shifted out four bits at a time through IO0–IO3. Each nibble (4 bits) is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached the address counter will wrap around and roll back to 000000h - allowing the read sequence to be continued indefinitely.

Address jumps can be done without the need for additional Read instructions. This is controlled through the setting of the Mode bits after the address sequence. This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7–4) of the Mode bits control the length of the next read instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3–0) of the Mode bits are "don't care" ("x"). If the Mode bits equal Axh then the device remains in XIP Mode and the next address can be entered (after CS# is raised HIGH and then asserted LOW) without requiring the read opcode, thus, eliminating eight cycles for the command sequence. The following sequences will release the device from XIP mode; after which, the device can accept standard SPI commands:

During the Quad I/O Read Command Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high the device will be released from XIP mode.

Send the Mode Reset command.

Note that the two mode bit clock-cycles and additional wait states (i.e., dummy-cycles) allow the device's internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0–IO3.

It is important that the IO0–IO3 signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn-around) is diminished. It is allowed and may be helpful in preventing IO0–IO3 signal contention, for the host system to turn off the IO0–IO3 signal outputs (make them high-impedance) during the last "don't care" mode cycle or during any dummy-cycles.

CS# should not be driven HIGH during mode or dummy bits as this may make the mode bits indeterminate.

In QPI mode (CR2V[3] = 1) the Quad I/O instructions are sent 4 bits per SCK rising-edge. The remainder of the command protocol is identical to the Quad I/O commands.

In QPI mode, the QIOR instruction behaves identically to the FAST_READ instruction and the 4QIOR instruction behaves identically to the 4FAST_READ instruction.

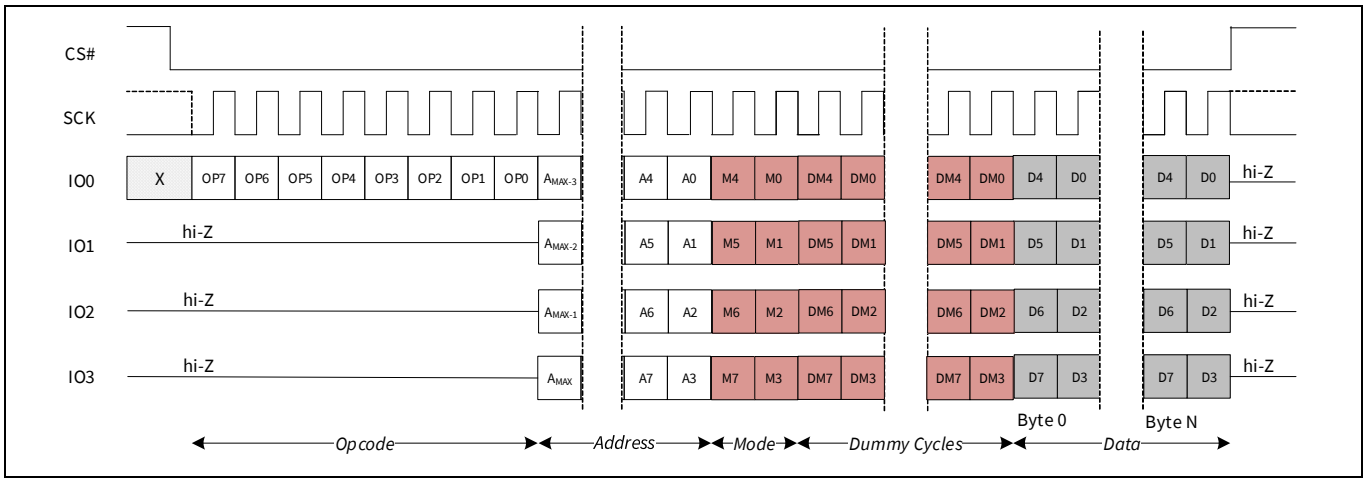


Figure 56 Quad I/O Read Initial Access command sequence[7]

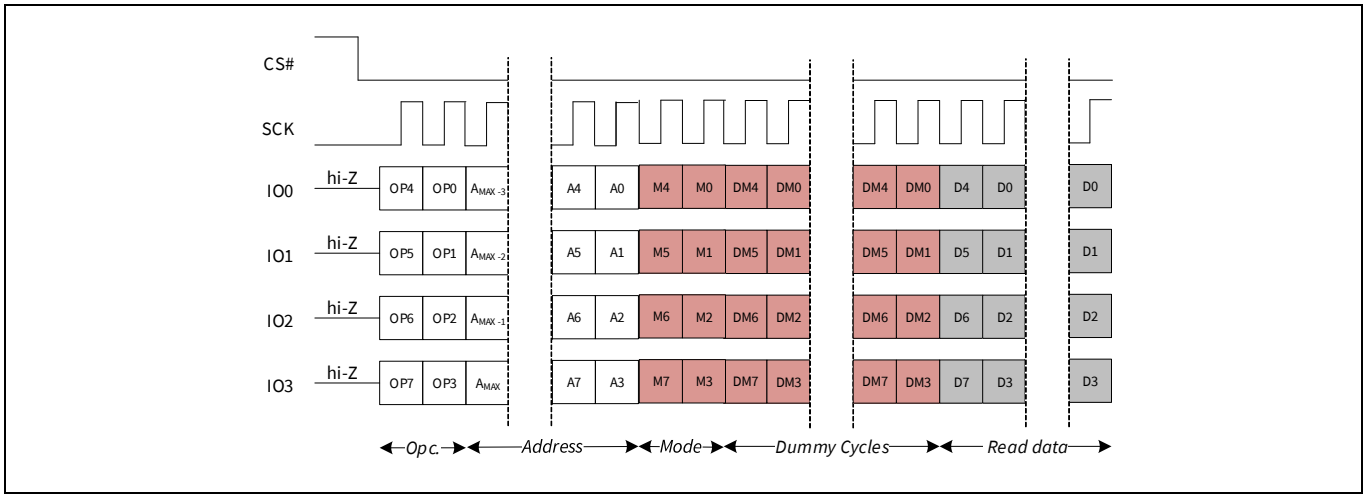


Figure 57 Quad I/O Read Initial Access command sequence QPI mode[7]

Note
7. A = MSB of address = 23 for CR1V[0] = 0, or 31 for CR1V[0] = 1 or command ECh.

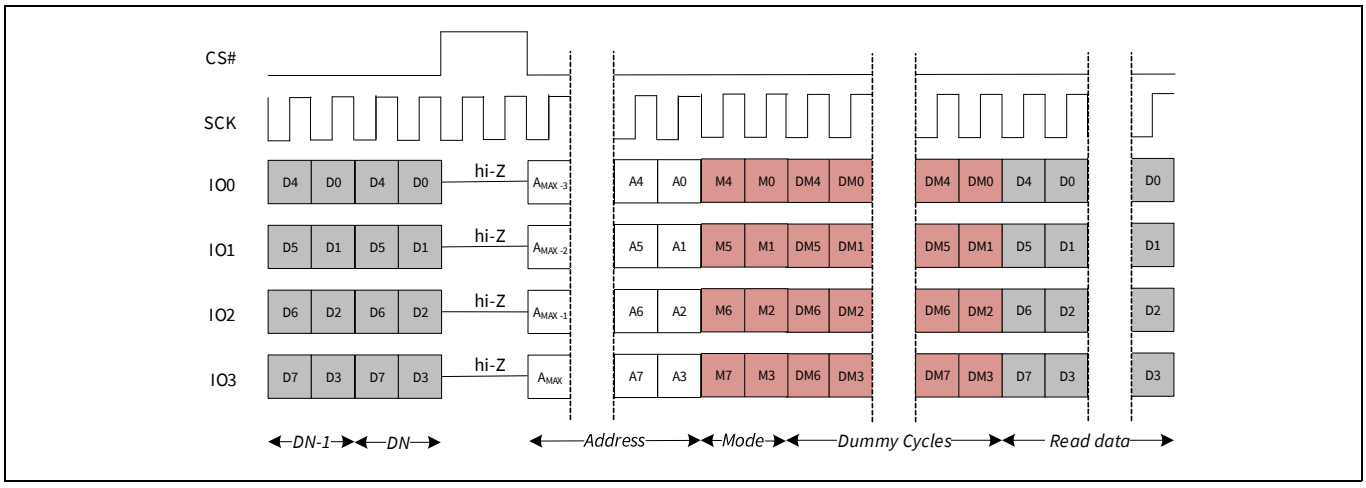


Figure 58 Continuous Quad I/O Read command sequence[8]

Note
8. The same sequence is used in QPI mode.

8.5 Program Flash Array commands

8.5.1 Program granularity

8.5.1.1 Page programming

The page programming is done by loading a page buffer with data to be programmed and issuing a programming command to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with a single programming command. Page programming allows up to a page size 2048 bytes to be programmed in one operation. The page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each Page programming operation. For the very best performance, programming should be done in full pages of 2048 bytes aligned on 2048 byte boundaries with each Page being programmed only once.

8.5.1.2 Single Byte programming

The single byte programming allows full backward compatibility to the legacy standard SPI Page Programming (PP) command by allowing a single byte to be programmed anywhere in the memory array.

8.5.2 Page Program (PP 02h or 4PP 12h)

The Page Program (PP) command allows bytes to be programmed in the memory (changing bits from ‘1’ to ‘0’ or ‘0’ to ‘1’). Before the page program (PP) commands can be accepted by the device a write enable (WREN) command must be issued and decoded by the device. After the write enable (WREN) command has been decoded successfully the device sets the write enable latch (WEL) in the Status Register to enable any write operations.

The instructions are

- 02h (CR1V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 02h (CR1V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 12h is followed by a 4-byte address (A31–A0)

and at least one data byte on SI/IO0. Up to a page can be provided on SI/IO0 after the 3-byte address with instruction 02h or 4-byte address with instruction 12h has been provided. As with the write and erase commands, the CS# pin must be driven HIGH after the eighth bit of the last byte has been latched. If this is not done the page program command will not be executed. After CS# is driven HIGH the self-timed page program command will commence for a time duration of t_{PP}.

Using the page program (PP) command to load an entire page (within the page boundary) will save overall programming time versus loading less than a page into the program buffer.

The programming process is managed by the Flash memory device internal control logic. After a programming command is issued, the programming operation status can be checked using the Read Status Register 1 command. The WIP bit (SR1V[0]) will indicate when the programming operation is completed. The P_ERR bit (SR2V[5]) will indicate if an error occurs in the programming operation that prevents successful completion of programming. This includes attempted programming of a protected area.

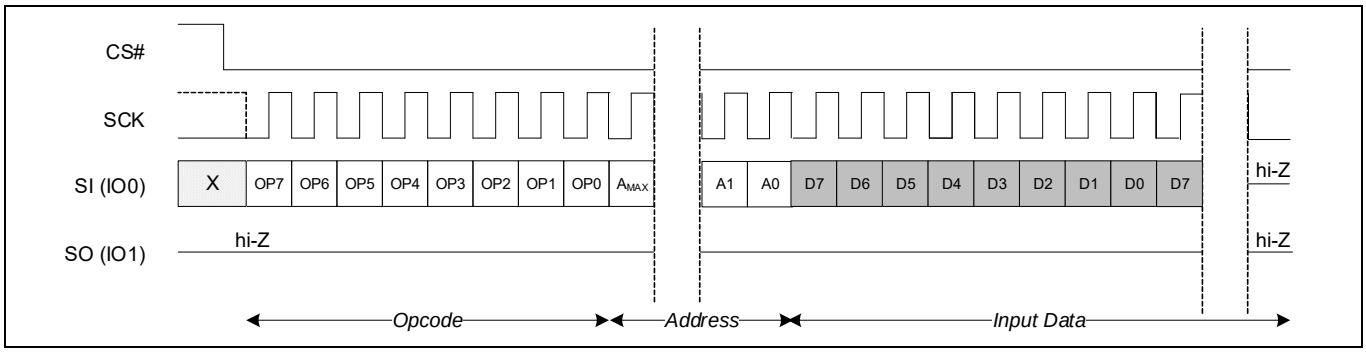


Figure 59 Page Program (PP 02h or 4PP 12h) command sequence[9]

This command is also supported in QPI mode. In QPI mode the instruction, address and data are shifted in on IO0–IO3.

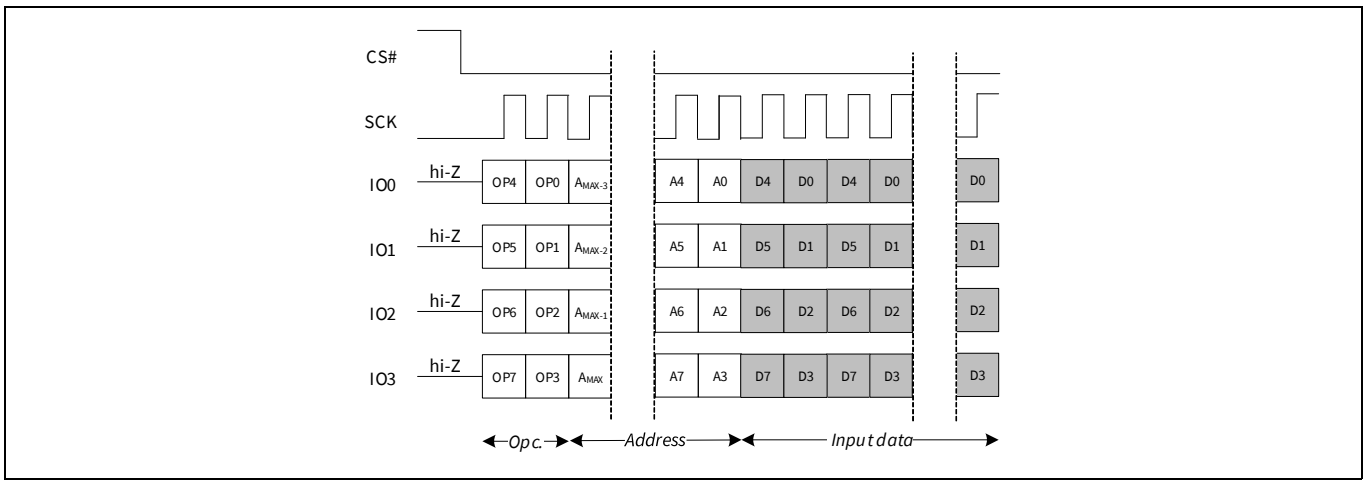


Figure 60 Page Program (PP 02h or 4PP 12h) QPI Mode command sequence[9]

Note
9. A = MSB of address = A23 for PP 02h with CR1V[0] = 0, or A31 for PP 02h with CR1V[0] = 1, or for 4PP 12h.

8.5.3 Quad Page Program (QPP 32h or 4QPP 34h)

The quad-input page program (QPP) command allows bytes to be programmed in the memory. The quad-input page program (QPP) command allows up to a page of data to be loaded into the page buffer using four signals: IO0–IO3. QPP can improve performance for PROM Programmer and applications that have slower clock speeds (< 12 MHz) by loading 4 bits of data per clock-cycle. Systems with faster clock speeds do not realize as much benefit for the QPP command since the inherent page program time becomes greater than the time it takes to clock in the data. The maximum frequency for the QPP command is 133 MHz.

To use quad page program the quad enable bit in the Configuration Register must be set (QUAD = 1). A Write Enable command must be executed before the device will accept the QPP command (Status Register 1, WEL = 1).

The instructions are

- 32h (CR1V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 32h (CR1V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 34h is followed by a 4-byte address (A31–A0)

and at least one data byte, into the IO signals. Data must be programmed at previously erased (00h) memory locations.

All other functions of QPP are identical to Page Program. The QPP command sequence is shown in the figure below.

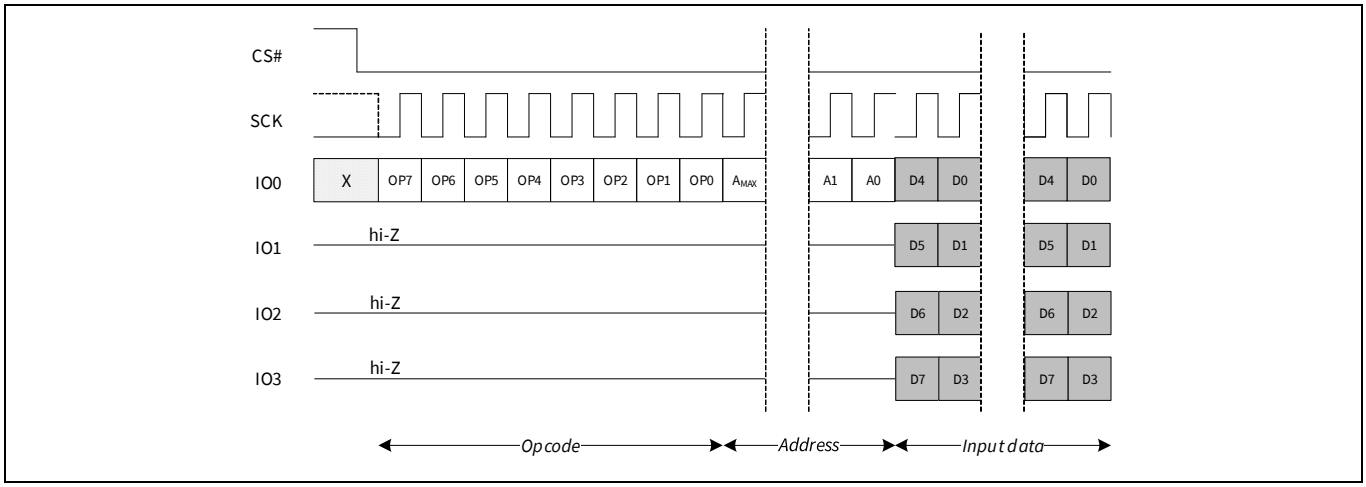


Figure 61 Quad Page Program command sequence[10]

Note
10.A = MSB of address = A23 for QPP 32h with CR1V[0] = 0, or A31 for QPP 32h with CR1V[0] = 1, or for 4QPP 34h.

8.6 Scrub Flash Array commands

8.6.1 Page Scrub (PSCRB CEh or 4PSCRB CFh)

Before the Page Scrub (PSCRB/4PSCRB) command can be accepted by the device a Write Enable (WREN) command must be issued and decoded by the device. This sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instructions are

- CEh [CR1V[0] = 0] is followed by a 3-byte address (A23–A0), or
- CEh [CR1V[0] = 1] is followed by a 4-byte address (A31–A0), or
- CFh is followed by a 4-byte address (A31–A0)

The Page Scrub command re-programs all the bits in the addressed page and applies single and double bit ECC to correction to the data in each ECC unit (128 bits) of the page. Internally this is accomplished by the following sequence:

- The page contents is read from the Flash array and transferred to RAM. During the read of the Flash data any single-bit or double-bit errors are corrected before the data is placed into the RAM.
- The contents of the RAM is then programmed back to the addressed page in the Flash array.

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of the address has been latched in on SI/IO0. This will initiate the beginning of internal scrub cycle which involves the reading and programming of the chosen page of the Flash memory array. If CS# is not driven HIGH after the last bit of address the Page Scrub operation will not be executed.

As soon as CS# is driven HIGH the internal scrub cycle will be initiated. With the internal scrub cycle in progress, the user can read the value of the Work-in Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a ‘1’ when the scrub cycle is in progress and a ‘0’ when the scrub cycle has been completed.

A PSCRB or 4PSCRB command applied to a sector that has been write protected through the Legacy Block Protection will be executed**.** A PSCRB or 4PSCRB command is applied when CR3V[7] = 1 (ECCDI) will not be executed and will set the SR2V P_ERR bit.

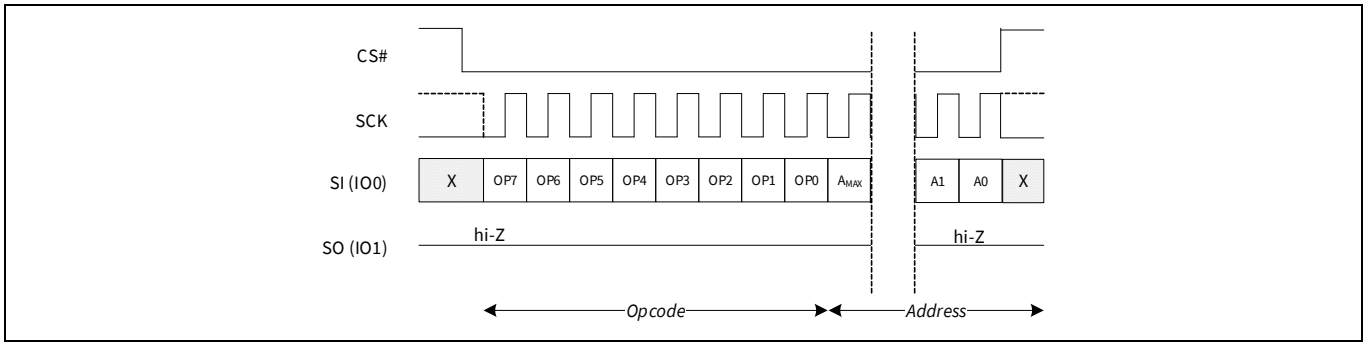


Figure 62 Page Scrub (PSCRB CEh or 4PSCRB CFh) command sequence [11]

Note
11.A = MSB of address = A23 for PSCRB CEh with CR1V[0] = 0, or A31 for PSCRB CEh with CR1V[0] = 1, or for 4PSCRB CFh.

This command is also supported in QPI mode. In QPI mode the instruction, address and data are shifted in on IO0–IO3.

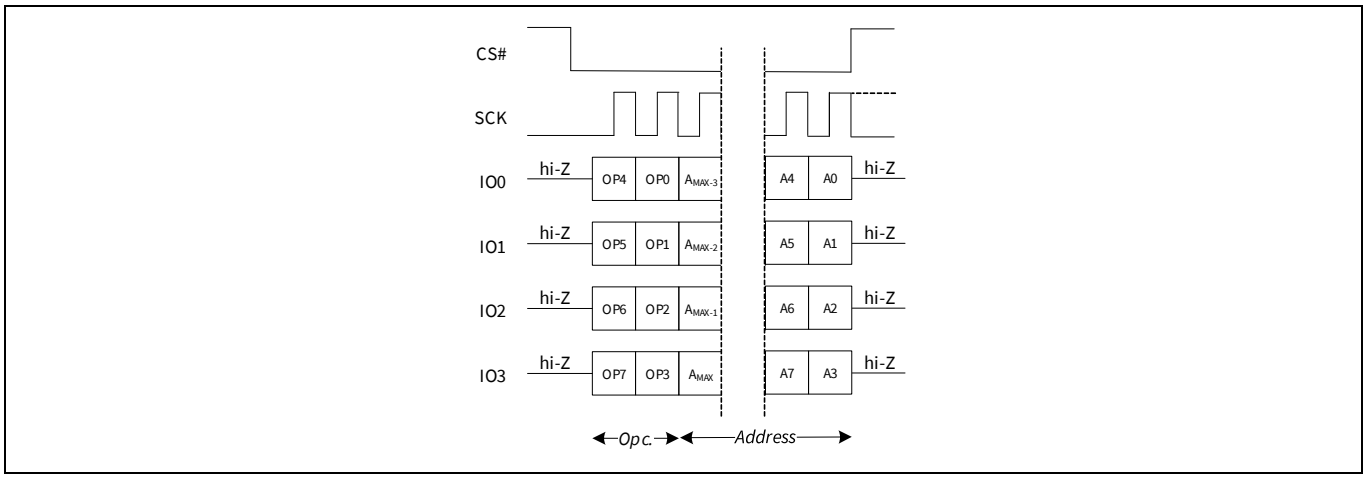


Figure 63 Page Scrub (PSCRB CEh or 4PSCRB CFh) QPI Mode command sequence[12]

Note

12.A = MSB of address = A23 for PSCRB CEh with CR1V[0] = 0, or A31 for PSCRB CEh with CR1V[0] = 1, or for 4PSCRB CFh.

8.6.2 Chip Scrub (CSCRB 8Eh)

Before the Chip Scrub (CSCRB) command can be accepted by the device a Write Enable (WREN) command must be issued and decoded by the device. This sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The Chip Scrub command, when directed at the Flash memory (CR1V[7] = 0), re-programs all the bits in the Flash memory and applies single and double bit ECC to correction to the data in each ECC unit (128 bits) of the page. Internally this is accomplished by the following sequence:

- Contents of each page are read from the Flash array and transferred to RAM. During the read of the Flash data any single-bit or double-bit errors are corrected before the data is placed in RAM.
- Contents of RAM are then programmed to the current page in the Flash array.
- Steps 1 and 2 are repeated for each page in the device.

The Chip Scrub command, when directed at the MCU SRAM memories (CR1V[7] = 1), corrects any single bit errors and re-programs all the bits in the MCU SRAMs.

CS# must be driven into the logic HIGH state after the eighth bit of the opcode has been latched in on SI/IO0. This will initiate the beginning of internal scrub cycle which involves the reading and programming all of the pages of the Flash memory array or MCU SRAMs. If CS# is not driven HIGH after the last bit of opcode the Chip Scrub operation will not be executed.

As soon as CS# is driven HIGH the internal scrub cycle will be initiated. With the internal scrub cycle in progress, the user can read the value of the Work-in Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a “1” when the scrub cycle is in progress and a “0” when the scrub cycle has been completed.

A CSCRB command is directed to the Flash memory and is applied to a device that has been write protected through the Legacy Block Protection will be executed.

A CSCRB command applied when CR3V[7] = 1 (ECCDI) will not be executed and will set the SR2 P_ERR bit.

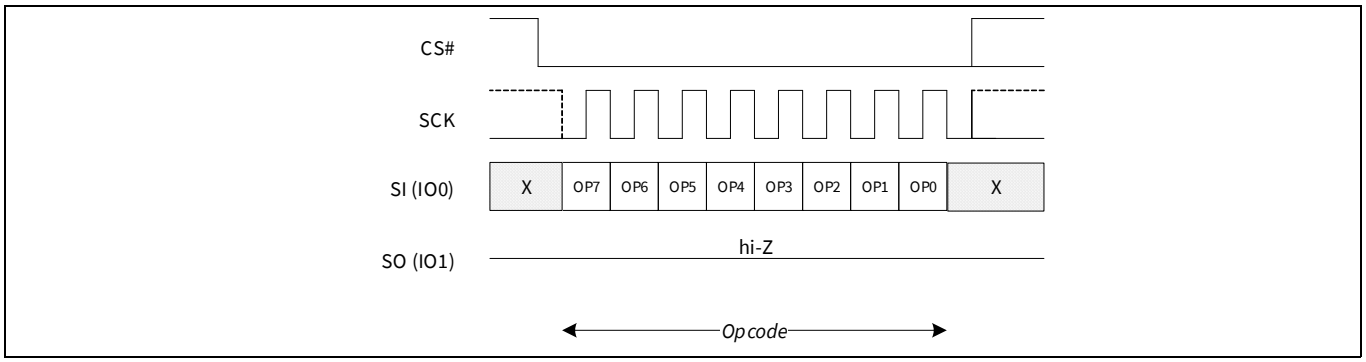


Figure 64 Chip Scrub (CSCRB 8Eh) command sequence

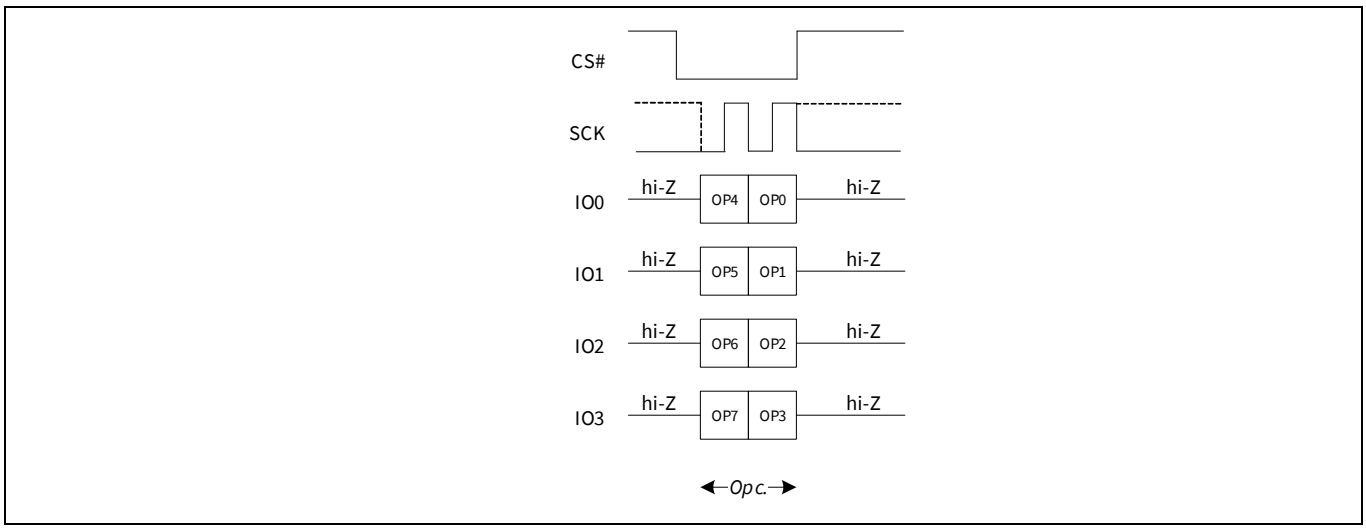


Figure 65 Chip Scrub (CSCRB 8Eh) QPI command sequence

8.7 Erase Flash Array commands

8.7.1 Sector Erase (SE 20h or 4SE 21h)

The Sector Erase (SE) command sets all bits in the addressed sector to '0' (all bytes are 00h). Before the Sector Erase (SE) command can be accepted by the device a Write Enable (WREN) command must be issued and decoded by the device. This sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instructions are

- 20h [CR1V[0] = 0] is followed by a 3-byte address (A23–A0), or
- 20h [CR1V[0] = 1] is followed by a 4-byte address (A31–A0), or
- 21h is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of the address has been latched in on SI/IO0. This will initiate the beginning of internal erase cycle which involves the pre-programming and erase of the chosen sector of the flash memory array. If CS# is not driven HIGH after the last bit of address the sector erase operation will not be executed.

As soon as CS# is driven HIGH the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Work-in Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A SE or 4SE command applied to a sector that has been write protected through the Block Protection will not be executed and will set the E_ERR status.

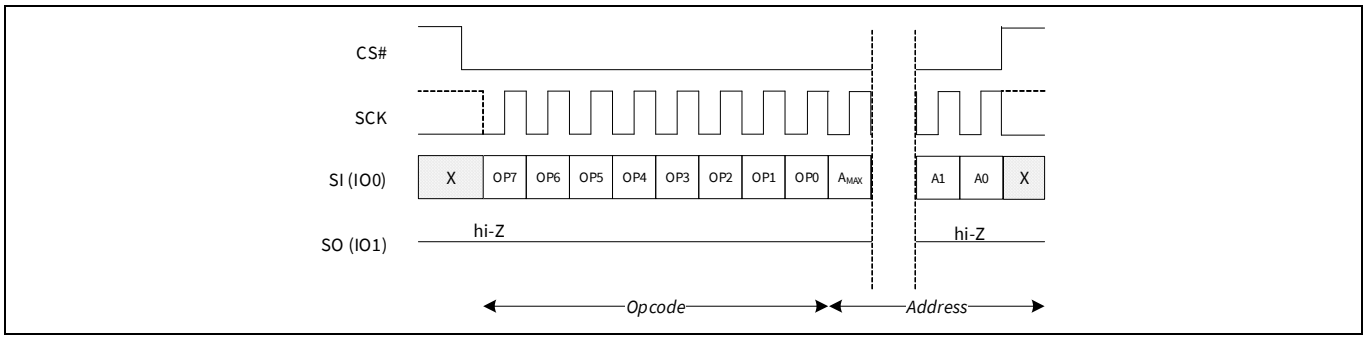


Figure 66 Sector Erase (SE 20h or 4SE 21h) command sequence[13]

Note
13.A = MSB of address = A23 for SE 20h with CR1V[0] = 0, or A31 for SE 20h with CR1V[0] = 1 or for 4SE 21h.

This command is also supported in QPI mode. In QPI mode the instruction and address is shifted in on IO0–IO3.

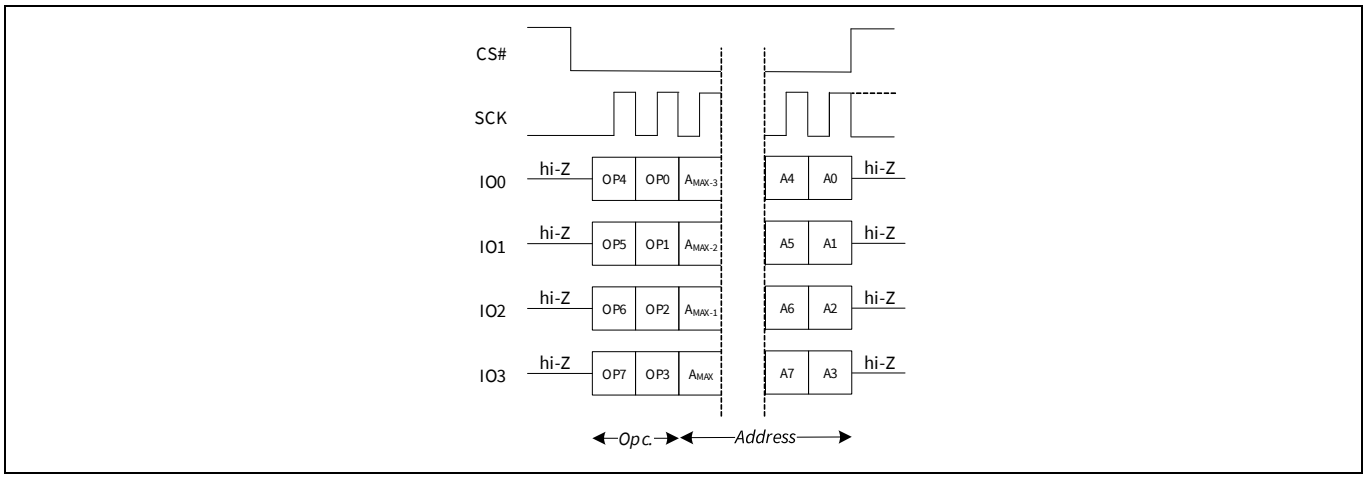


Figure 67 Sector Erase (SE 20h or 4SE 21h) QPI Mode command sequence[14]

Note
14.A = MSB of address = A23 for SE 20h with CR1V[0] = 0, or A31 for SE 20h with CR1V[0] = 1 or for 4SE 21h.

8.7.2 Block Erase (BE D8h or 4BE DCh)

The Block Erase (BE) command sets all bits in the addressed block to '0' (all bytes are 00h). Before the Block Erase (BE) command can be accepted by the device a Write Enable (WREN) command must be issued and decoded by the device. This sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instructions are

- D8h [CR1V[0] = 0] is followed by a 3-byte address (A23–A0), or
- D8h [CR1V[0] = 1] is followed by a 4-byte address (A31–A0), or
- DCh is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of address has been latched in on SI/IO0. This will initiate the erase cycle which involves the pre-programming and erase of each sector of the chosen block. If CS# is not driven HIGH after the last bit of address the block erase operation will not be executed.

As soon as CS# is driven into the logic HIGH state the internal erase cycle will be initiated. With the internal erase cycle in progress the user can read the value of the Work-in Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A Block Erase (BE) command applied to a Block that has been Write Protected through the Block Protection will not be executed and will set the E_ERR status.

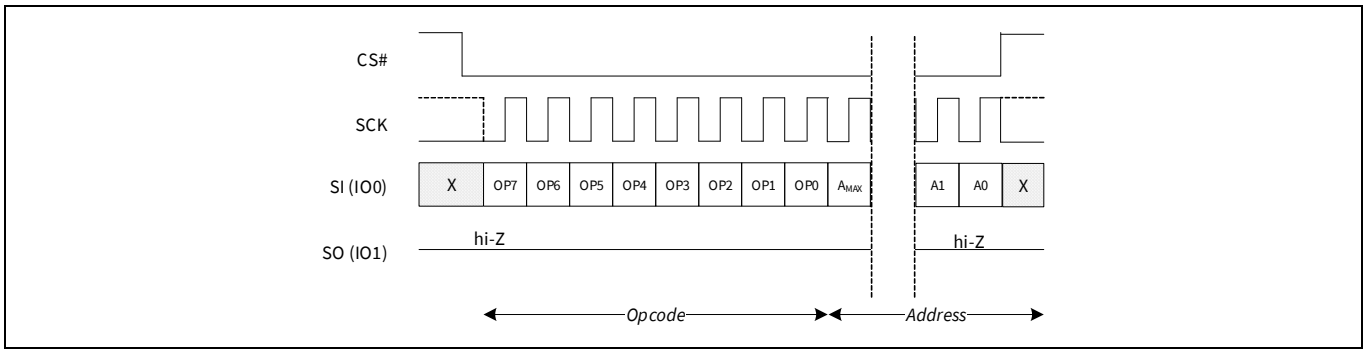


Figure 68 Block Erase (BE D8h or 4BE DCh) command sequence[15]

Note
15.A = MSB of address = A23 for BE D8h with CR1V[0] = 0, or A31 for BE D8h with CR1V[0] = 1 or 4BE DCh.

This command is also supported in QPI mode. In QPI mode the instruction and address is shifted in on IO0–IO3.

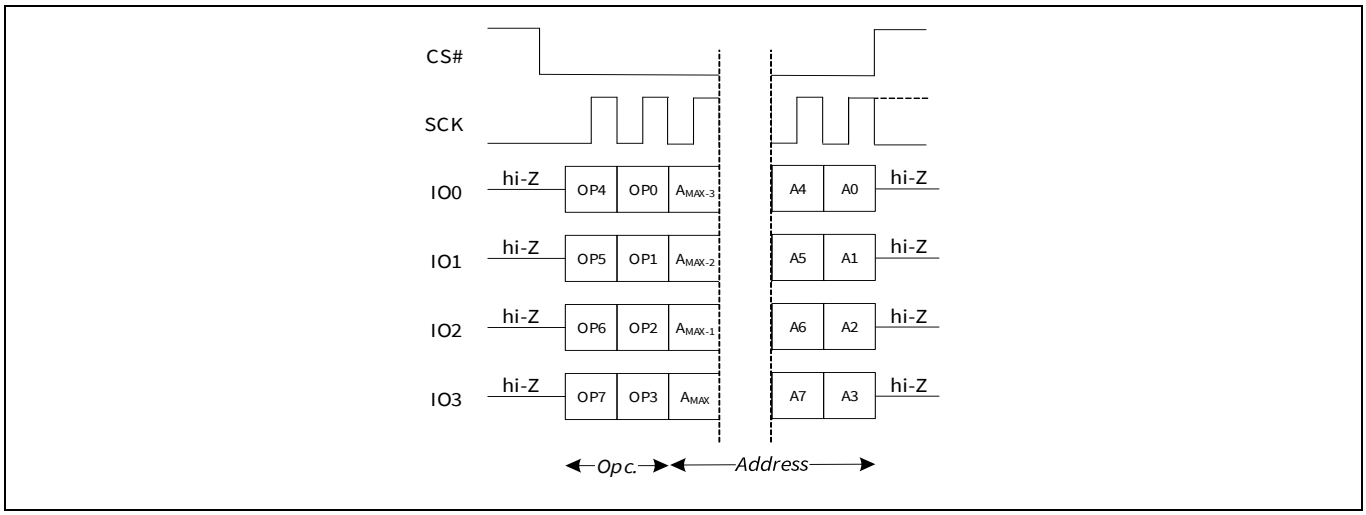


Figure 69 Block Erase (BE D8h or 4BE DCh) QPI Mode command sequence[16]

Note
16.A = MSB of address = A23 for BE D8h with CR1V[0] = 0, or A31 for BE D8h with CR1V[0] = 1 or 4BE DCh.

8.7.3 Chip Erase (CE 60h or C7h)

The Chip Erase (CE) command sets all bits to '0' (all bytes are 00h) inside the entire flash memory array. Before the CE command can be accepted by the device a Write Enable (WREN) command must be issued and decoded by the device. This sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI/IO0. This will initiate the erase cycle which involves the pre-programming and erase of the entire flash memory array. If CS# is not driven HIGH after the last bit of instruction the CE operation will not be executed.

As soon as CS# is driven into the logic HIGH state the erase cycle will be initiated. With the erase cycle in progress the user can read the value of the Work-in Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A CE command will not be executed when the Block Protection set to protect any block and this will set the E_ERR status bit.

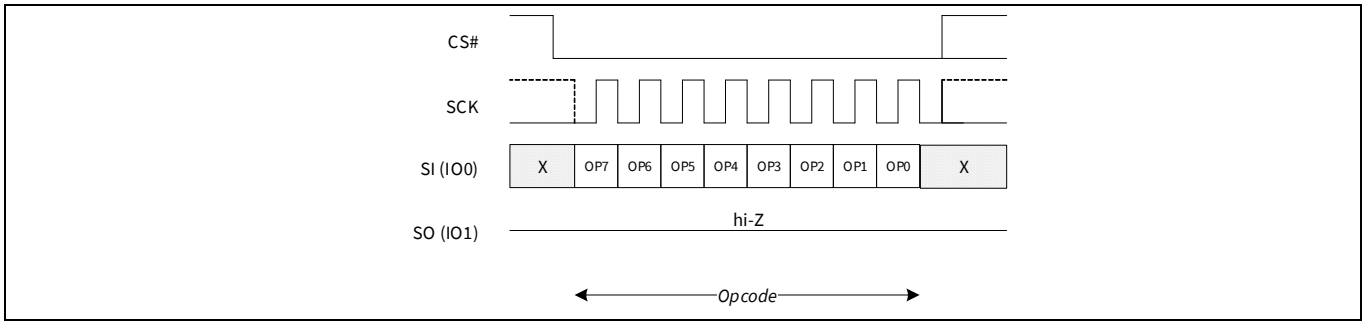


Figure 70 Chip Erase command sequence

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3.

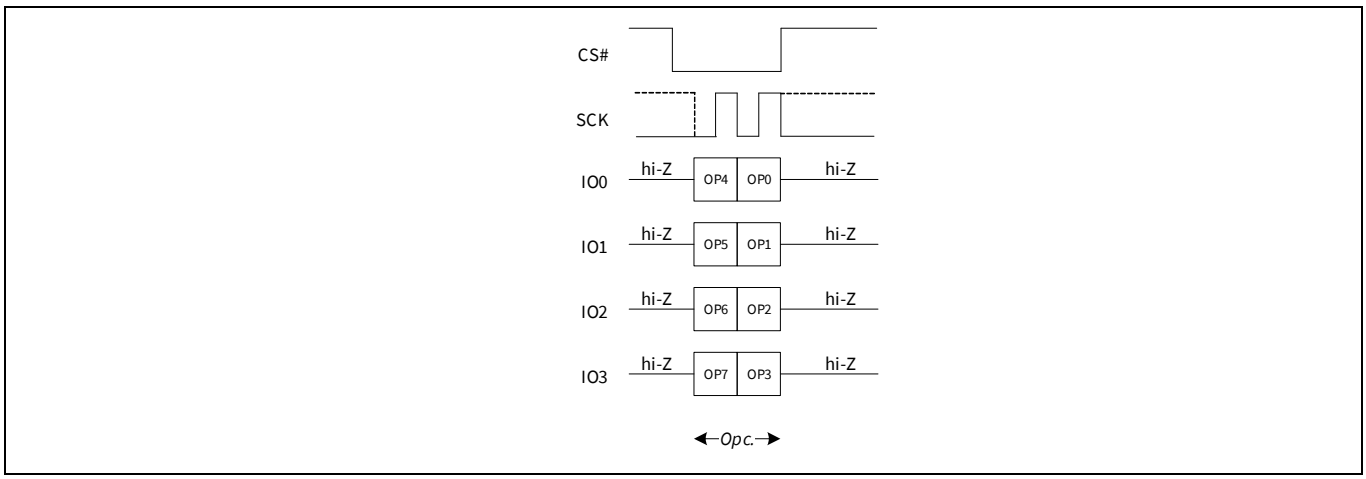


Figure 71 Chip Erase command sequence QPI mode

8.7.4 Erase Suspend (EPS 75h)

The EPS command allows the system to interrupt an erase operation and then read from any other non-erase-suspended sector or block. Erase Suspend is valid only during a sector erase or block erase operation. A Chip Erase operation cannot be suspended.

The Work in Progress (WIP) bit in Status Register 1 (SR1V[0]) must be checked to know when the erase operation has stopped. The Erase Suspend Status bit in the Status Register-2 (SR2[1]) can be used to determine if an erase operation has been suspended or was completed at the time WIP changes to '0'. The time required for the suspend operation to complete is t_{SL}.

A new suspend operation is not allowed within an already suspended erase operation. The suspend command is ignored in this situation. The WRR and WRAR commands are not allowed during Erase Suspend, therefore, it is not possible to alter the Block Protection bits during Erase Suspend.

Table 35 Summary of all cases of suspend and resume

Commands/States	IDLE	Erasing	Erase suspended	Erase suspended programming
Erase Suspend (75h)	Do nothing	Erase Suspend	Do nothing	Do nothing
Erase Resume (7Ah)	Do nothing	Do nothing	Erase Resume	Do nothing

Table 36 Commands allowed during Erase Suspend

Instruction name	Instruction code (hex)	Allowed during Erase Suspend	Comment
EPS	75	X	Suspend erase
EPR	7A	X	Required to resume from Erase Suspend
READ	03	X	All array reads allowed in suspend[17]
RDSR1	05	X	Needed to read WIP to determine end of suspend process
RDAR	65	X	Alternate way to read WIP to determine end of suspend process
RDSR2	07	X	Needed to read suspend status to determine whether the operation is suspended or complete.
RDCR1	35	X	Needed to read Configuration Register 1
RDCR2	15	X	Needed to read Configuration Register 2
RDCR3	33	X	Needed to read Configuration Register 3
ECCRD	19	X	Needed to read ECC Status[17]
4ECCRD	18	X	Needed to read ECC Status[17]
CLECC	1B	X	Needed to clear ECC Status
RUID	4C	X	Needed to read Unique Id
RDID	9F	X	Needed to read Device Id
RDQID	AF	X	Needed to read Quad Device Id
RDSN	C3	X	Needed to read Serial Number
RSFDP	5A	X	Needed to read SFDP
SWL	77	X	Needed to set Wrap Length
WREN	06	X	Required for volatile register program command within Erase Suspend
WRDI	04	X	Required for program command within Erase Suspend
PP	02	X	Required for array program during Erase Suspend. If a program command is sent for a location within an erase suspended sector or block the program operation will fail with the P_ERR bit (of the addressed die with the suspended era) set.
4PP	12	X	Required for array program during Erase Suspend. If a program command is sent for a location within an erase suspended sector or block the program operation will fail with the P_ERR bit (of the addressed die with the suspended era) set.
QPP	32	X	Required for array program during Erase Suspend. If a program command is sent for a location within an erase suspended sector or block the program operation will fail with the P_ERR bit (of the addressed die with the suspended era) set.

Note
17. Reading (READ, ECCRD, 4ECCRD, 4READ, FAST_READ, 4FAST_READ, QOR, 4QOR, QIOR and 4QIOR) at any address within an erase-suspended sector produces undetermined data.

Table 36 Commands allowed during Erase Suspend *(continued)*

Instruction name	Instruction code (hex)	Allowed during Erase Suspend	Comment
4QPP	34	X	Required for array program during Erase Suspend. If a program command is sent for a location within an erase suspended sector or block the program operation will fail with the P_ERR bit set.
PSCRB	CE	X	Required for array program during Erase Suspend. If a program command is sent for a location within an erase suspended sector or block the program operation will fail with the P_ERR bit set.
PSCRB	CF	X	Required for array program during Erase Suspend. If a program command is sent for a location within an erase suspended sector or block the program operation will fail with the P_ERR bit set.
4READ	13	X	All array reads allowed in suspend[17]
CLSR	30	X	Clear status may be used if a program operation fails during Erase Suspend.
RSTEN	66	X	Reset allowed anytime
RST	99	X	Reset allowed anytime
FAST_READ	0B	X	All array reads allowed in suspend[17]
4FAST_READ	0C	X	All array reads allowed in suspend[17]
QOR	6B	X	Read Quad Output (3-or 4-byte address)[17]
4QOR	6C	X	Read Quad Output (4-byte address)[17]
QIOR	EB	X	All array reads allowed in suspend[17]
4QIOR	EC	X	All array reads allowed in suspend[17]
MBR	FF	X	May need to reset a read operation during suspend

Note
17. Reading (READ, ECCRD, 4ECCRD, 4READ, FAST_READ, 4FAST_READ, QOR, 4QOR, QIOR and 4QIOR) at any address within an erase-suspended sector produces undetermined data.

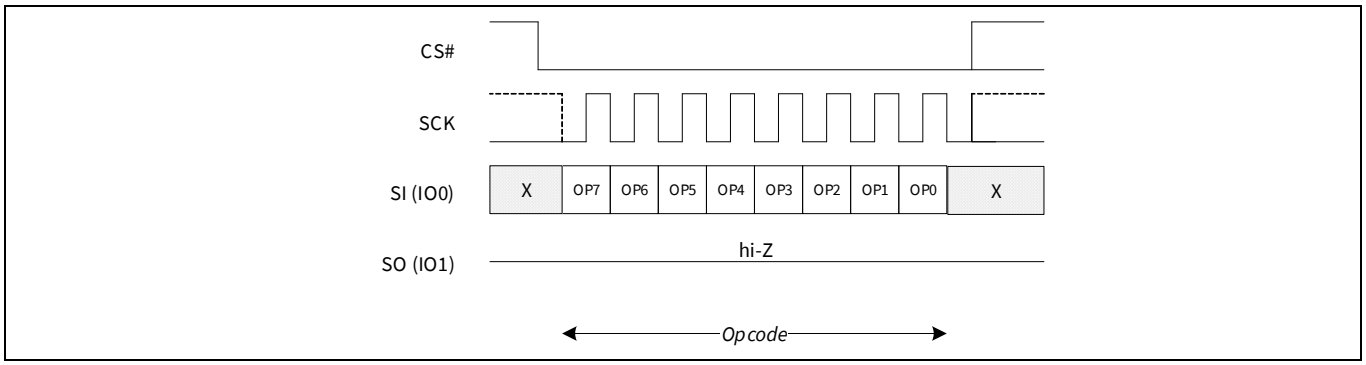


Figure 72 Erase Suspend command sequence

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3.

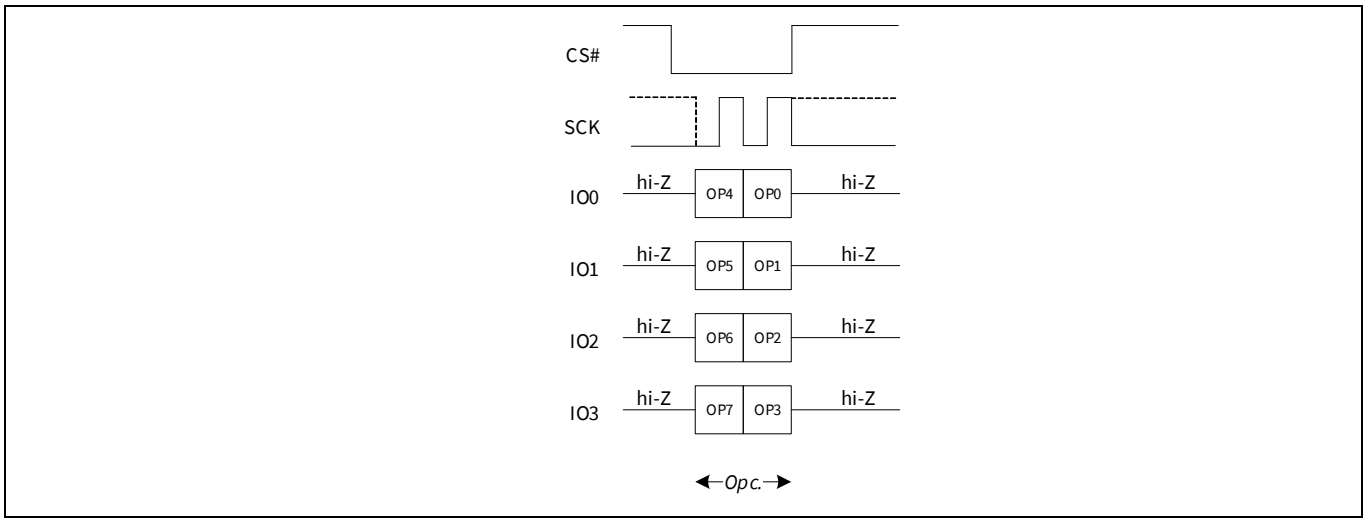


Figure 73 Erase Suspend command sequence QPI mode

8.7.5 Erase Resume (EPR 7Ah)

An Erase Resume command must be written to resume a suspended operation.

After program or read operations are completed during a program or erase suspend the Erase or Program Resume command is sent to continue the suspended operation.

After an Erase Resume command is issued the WIP bit in the Status Register 1 will be set to a '1' and the suspended operation will resume if one is suspended. If there is no suspended erase operation the resume command is ignored.

Erase operations may be interrupted as often as necessary, e.g. an Erase Suspend command could immediately follow an Erase Resume command, but in order for an erase operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{RNS}. See **Table 57**.

The Erase Suspend Status bit in the Status Register-2 (SR2[1]) can be used to determine if an erase operation has been suspended or was completed at the time WIP changes to '0'. See **Table 9**.

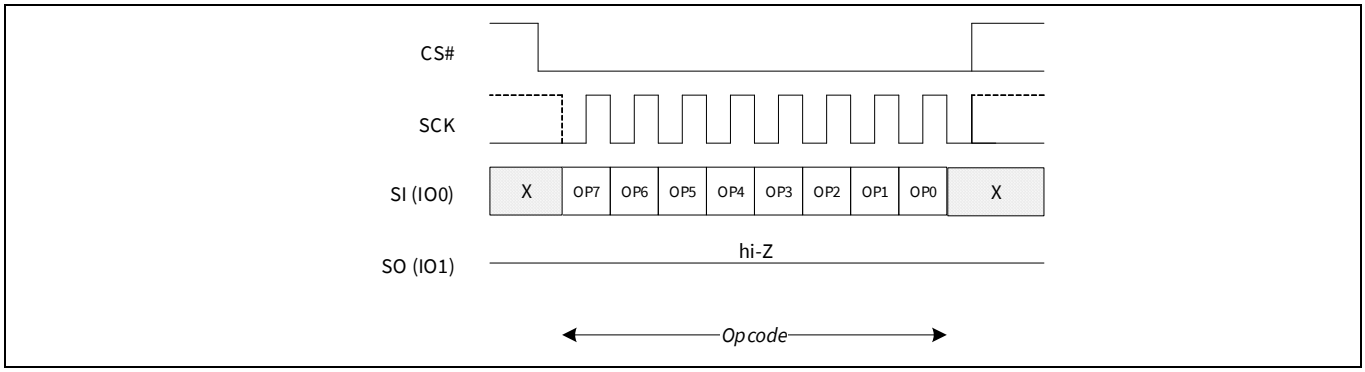


Figure 74 Erase Resume command sequence

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3.

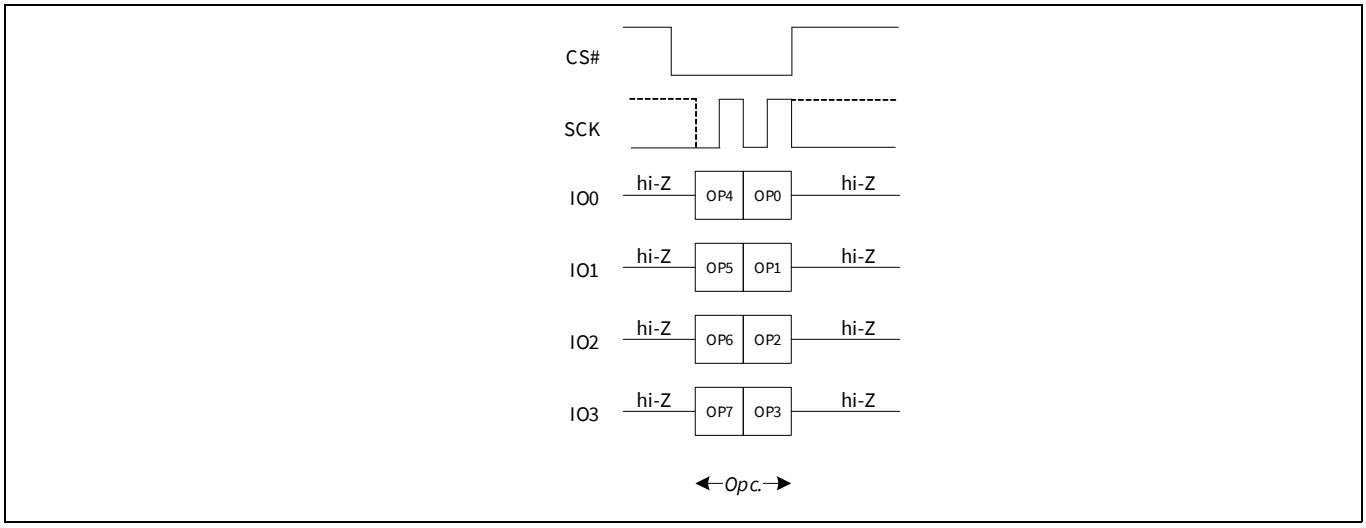


Figure 75 Erase Resume command sequence QPI mode

8.8 Reset commands

The software-controlled Reset commands restore the device to its initial power-up state by reloading volatile registers from non-volatile default values.

If a reset is initiated during a non-volatile register program operation it is possible that the configuration data may be irretrievably corrupted.

If a reset is initiated during an array program operation and the program operation is not a full 2 KB page it is possible that the data stored in locations left unwritten within that 2 KB page may be irretrievably corrupted.

If a reset is initiated during a scrub operation it is possible that the data stored within the 2 KB page which was actively being scrubbed at the time the reset command is issued may be irretrievably corrupted.

If a reset is initiated during an erase operation or during a page program of a full 2 KB page, the operation that was interrupted must be initiated again.

A software reset command (RSTEN 66h followed by RST 99h) is executed when CS# is brought HIGH at the end of the instruction and requires t_{Reset} time to execute.

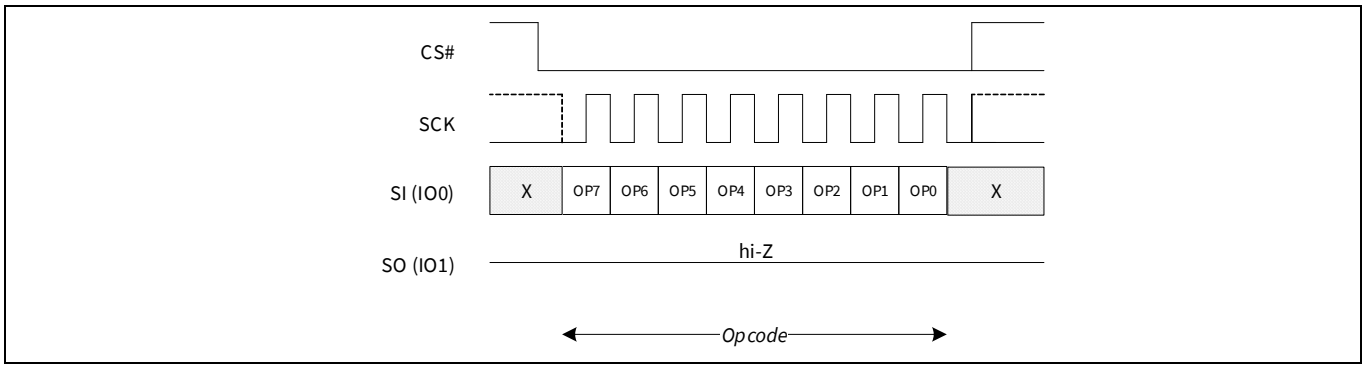


Figure 76 Software / Mode Bit Reset command sequence

This command is also supported in QPI mode. In QPI mode the instruction is shifted in on IO0–IO3.

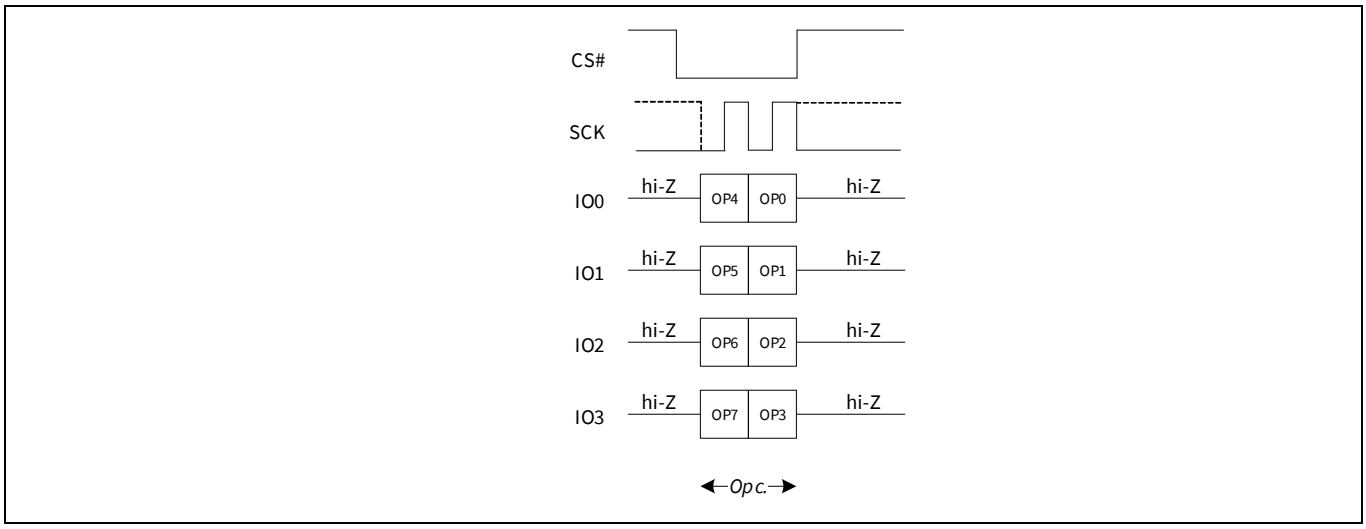


Figure 77 Software Reset / Mode Bit command sequence – QPI mode

8.8.1 Software Reset Enable (RSTEN 66h)

The Reset Enable (RSTEN) command is required immediately before a software reset command (RST 99h) such that a software reset is a sequence of the two commands. Any command, other than RST following the RSTEN command, will clear the Reset Enable condition and prevent a later RST command from being recognized.

8.8.2 Software Reset (RST 99h)

The Reset (RST) command immediately following a RSTEN command, initiates the software reset process. Any command, other than RST following the RSTEN command, will clear the Reset Enable condition and prevent a later RST command from being recognized.

8.8.3 Mode Bit Reset (MBR FFh)

The Mode Bit Reset (MBR) command is used to return the device from continuous high-performance read mode back to normal standby awaiting any new command.

The MBR command sends Ones on SI/IO0 for eight SCK cycles. IO1–IO3 are “don’t care” during these cycles. The MBR command is also available in QPI mode. In QPI mode, Ones are sent on IO0–IQ3 for two cycles.

9 Data integrity

9.1 Endurance / data retention

Table 37 Endurance / data retention

Program / Erase cycles	Temperature	Data retention
10K	≤ 85°C	10 years
1K (50% duty cycle)	≤ 125°C	

9.2 Read endurance

Table 38 Read endurance

Parameter	Test conditions	Min	Unit
Read accesses to the same main Flash array	10 PE cycles, operating range voltage and temperature	1×10^{12}	Read accesses
	10K PE cycles, operating range voltage and temperature	1×10^{9}	

Contact the local sales representatives or visit Infineon community for additional information regarding data integrity.

10 Software interface reference

10.1 JEDEC JESD216D serial flash discoverable parameters

This document defines the serial flash discoverable parameters (SFDP) revision D data structure used in the Infineon serial flash devices. These data structure values are an update to the earlier revision SFDP data structure currently existing in previous devices.

The Read SFDP (RSFDP) command (5Ah) reads information from a separate Flash memory address space for device identification, feature and configuration information in accordance with the JEDEC JESD216D standard for Serial Flash Discoverable Parameters.

The SFDP data structure consists of a header table that identifies the revision of the JESD216 header format that is supported and provides a revision number and pointer for each of the SFDP parameter tables that are provided. The parameter tables follow the SFDP header. However, the parameter tables may be placed in any physical location and order within the SFDP address space. The tables are not necessarily adjacent nor in the same order as their header table entries.

The SFDP header points to the following parameter tables:

- Basic flash
  - This is the original SFDP table. It has a few modified fields and new additional fields added at the end of the table.
- 4-byte address instruction
  - This is the original SFDP table. It has a few modified fields and new additional fields added at the end of the table.
- Status, Control and Configuration Register map.

The physical order of the tables in the SFDP address space is: SFDP header, 4-byte Instruction, Status, Control and Configuration Register map.

The SFDP address space is programmed by Infineon and read-only for the host system.

10.1.1 Serial flash discoverable parameters (SFDP) address map

The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. One basic flash parameter is mandated by the JEDEC JESD216D standard. Optional parameter tables for 4-byte address instructions follow the basic flash table. The SFDP space is 1.5 KB in length starting at address 000h and ending at address 5FFh.

Table 39 SFDP overview map

Byte address	Description
000h	Location zero within JEDEC JESD216B SFDP space - start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
300h	Start of SFDP parameter
...	Remainder of SFDP JEDEC parameter followed by undefined space

10.1.2 SFDP header field definitions

Table 40 SFDP header

SFDP byte address	SFDP DWORD name	Data	Description
00h	SFDP header	53h	This is the entry point for Read SFDP (5Ah) command i.e., location zero within SFDP space ASCII “S”.
01h		46h	ASCII “F”
02h		44h	ASCII “D”
03h		50h	ASCII “P”
04h		08h	SFDP Minor Revision (08h = JEDEC JESD216 Revision D)
05h		01h	SFDP Major Revision (01h = JEDEC JESD216 Revision D) This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		02h	Number of Parameter Headers (zero based, 02h = 3 parameters)
07h		FFh	SFDP Access Protocol (Backward Compatible)
08h	1st parameter header	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		07h	Parameter Minor Revision (07h = JEDEC JESD216 Revision D)
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
0Bh		14h	Parameter Table Length (14h = 20 DWORDs are in the Parameter table)
0Ch		00h	Parameter Table Pointer Byte 0 (DWORD = 4 Byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0300h
0Dh		03h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)

Table 40 SFDP header *(continued)*

SFDP byte address	SFDP DWORD name	Data	Description
10h	2nd parameter header	84h	Parameter ID LSB (84h = 4 Byte Address Instruction Table)
11h		01h	Parameter Table Minor Revision (01h = JEDEC JESD216 Revision D)
12h		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
13h		02h	Parameter Table Length (2h = 2 DWORDs are in the Parameter table)
14h		50h	Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned) 4 Byte Address Instruction Table byte offset = 0350h address
15h		03h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
18h	3rd parameter header	87h	Parameter ID LSB (87h = JEDEC Status, Control and Configuration Register Map)
19h		01h	Parameter Table Minor Revision (01h = JEDEC JESD216 Revision D)
1Ah		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
1Bh		1Ch	Parameter Table Length (1Ch = 28 DWORDs are in the Parameter table)
1Ch		58h	Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned) JEDEC Status, Control and Configuration Register Map = 0358h address
1Dh		03h	Parameter Table Pointer Byte 1
1Eh		00h	Parameter Table Pointer Byte 2
1Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)

10.1.3 JEDEC SFDP basic SPI flash parameter

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D

SFDP parameter relative byte address	SFDP Dword name	Data	Description
300h	JEDEC basic Flash parameter DWORD-1	F7h	Bits 7:5 = Unused = 111b Bit 4 = 06h is volatile status register write instruction and status register is default = 1b Bit 3 = Block Protect Bits are non-volatile / volatile = 0b Bit 2 = Program Buffer > 64 Bytes = 1b Bits 1:0 = Uniform 4 kilobyte erase is unavailable = 11b
301h		FFh	Bits 15:8 = 4 KB erase is not supported = FFh
302h		E2h	Bit 23 = Unused = 1b Bit 22 = Supports Quad Out (1-1-4) Read = Yes = 1b Bit 21 = Supports Quad I/O (1-4-4) Read = Yes = 1b Bit 20 = Supports Dual I/O (1-2-2) Read = No = 0b Bit 19 = Supports DDR = No = 0b Bit 18:17 = Number of Address Bytes = 3- or 4 Bytes = 01b Bit 16 = Supports Dual Out (1-1-2) Read = No = 0b
303h		FFh	Bits 31:24 = Unused = FFh
304h	JEDEC basic Flash parameter DWORD-2	FFh	Density in bits, zero based, 512Mb = 1FFFFFFFh
305h		FFh	
306h		FFh	
307h		1Fh	
308h	JEDEC basic Flash parameter DWORD-3	48h	Bits 7:5 = Number of Quad I/O (1-4-4) Mode cycles = 010b Bits 4:0 = Number of Quad I/O Dummy cycles = 01000b (Initial Delivery State)
309h		EBh	Quad I/O instruction code
30Ah		08h	Bits 23:21 = Number of Quad Out (1-1-4) Mode cycles = 000b Bits 20:16 = Number of Quad Out Dummy cycles = 01000b
30Bh		6Bh	1-1-4 Quad Out instruction code = 6Bh
30Ch	JEDEC basic Flash parameter DWORD-4	00h	Bits 7:5 = Number of Dual Out (1-1-2) Mode cycles = 000b (Not supported) Bits 4:0 = Number of Dual Out Dummy cycles = 00000b (Not supported)
30Dh		FFh	Dual Out instruction code (Not supported)
30Eh		00h	Bits 23:21 = Number of Dual I/O (1-2-2) Mode cycles = 000b (Not supported) Bits 20:16 = Number of Dual I/O Dummy cycles = 00000b (Not supported)
30Fh		FFh	Dual I/O instruction code not supported

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
310h	JEDEC basic Flash parameter DWORD-5	FEh	Bits 7:5 RFU = 111b Bit 4 = QPI supported = Yes = 1b Bits 3:1 RFU = 111b Bit 0 = 2-2-2 not supported = 0b
311h		FFh	Bits 15:8 = RFU = FFh
312h		FFh	Bits 23:16 = RFU = FFh
313h		FFh	Bits 31:24 = RFU = FFh
314h	JEDEC basic Flash parameter DWORD-6	FFh	Bits 7:0 = RFU = FFh
315h		FFh	Bits 15:8 = RFU = FFh
316h		00h	Bits 23:21 = Number of 2-2-2 Mode cycles = 000b (Not supported) Bits 20:16 = Number of 2-2-2 Dummy cycles = 00000b (Not supported)
317h		FFh	2-2-2 instruction code (Not supported)
318h	JEDEC basic Flash parameter DWORD-7	FFh	Bits 7:0 = RFU = FFh
319h		FFh	Bits 15:8 = RFU = FFh
31Ah		48h	Bits 23:21 = Number of QPI Mode cycles = 010b Bits 20:16 = Number of QPI Dummy cycles = 01000b
31Bh		EBh	QPI mode Quad I/O (4-4-4) instruction code
31Ch	JEDEC basic Flash parameter DWORD-8	14h	Erase type 1 size 2^N Bytes = 2^20 Bytes = 1MB
31Dh		20h	Erase type 1 instruction (sector erase)
31Eh		17h	Erase type 2 size 2^N Bytes = 2^23 Bytes = 8MB
31Fh		D8h	Erase type 2 instruction (block erase)
320h	JEDEC basic Flash parameter DWORD-9	00h	Erase type 3 size 2^N Bytes = not supported
321h		FFh	Erase type 3 instruction = not supported = FFh
322h		00h	Erase type 4 size 2^N Bytes = not supported
323h		FFh	Erase type 4 instruction = not supported = FFh

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
324h	JEDEC basic Flash parameter DWORD-10	A0h	Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1 s = 11b (not supported) Bits 29:25 = Erase type 4 Erase, Typical time count = 11111b (not supported) Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1 s = 11b (not supported) Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (not supported) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16 ms = 01b Bits 15:11 = Erase type 2 Erase, Typical time count = 00101b (typ erase time = count + 1 * units = 6 * 16 ms = 96 ms) Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1ms = 00b Bits 8:4 = Erase type 1 Erase, Typical time count = 01010b (typ erase time = count + 1 * units = 11 * 1 ms = 11 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) – 1 = 0000b
325h		28h	
326h		FDh	
327h		FFh	
328h	JEDEC basic Flash parameter DWORD-11	B7h	Bits 31 = Reserved = 1b Bits 30:29 = Device Erase Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 01b Bits 28:24 = Device Erase Typical time count = 00010b Bits 23:19 = Byte Program Typical Time, additional byte = 10000b Bits 18:14 = Byte Program Typical Time, first byte = 10000b Bits 13 = Page Program Typical Time unit (0: 8 µs, 1: 64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical Time Count = 11111 (typ Program time = count + 1 * units) Bits 7:4 = Page Size (2048B) = 2^N bytes = 1011h Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] – 1 = 0111b
329h		3Fh	
32Ah		84h	
32Bh		A2h	

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
32Ch	JEDEC basic Flash parameter DWORD-12	E0h	Bit 31 = Erase and Program Suspend/Resume not supported = 1b (not supported) Bits 30:29 = Suspend in-progress erase max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8 µs = 10b Bits 28:24 = Suspend in-progress erase max latency count = 00100b, max erase suspend latency = count + 1 * units = 5 * 8 µs = 40 µs Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count + 1 * 64 µs = 2 * 64 µs = 128 µs Bits 19:18 = Suspend in-progress program max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 11b (not supported) Bits 17:13 = Suspend in-progress program max latency count = 11111, max program suspend latency = count + 1 * units (not supported) Bits 12:9 = Program resume to suspend interval count = 1111b, interval = count + 1 * 64 µs = (not supported) Bit 8 = Reserved = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 0000b (not supported)
32Dh		FFh	
32Eh		1Fh	
32Fh		C4h	
330h	JEDEC basic Flash parameter DWORD-13	FFh	Bits 31:24 = Erase Suspend Instruction = 75h Bits 23:16 = Erase Resume Instruction = 7Ah Bits 15:8 = Program Suspend Instruction = FFh (not supported) Bits 7:0 = Program Resume Instruction = FFh (not supported)
331h		FFh	
332h		7Ah	
333h		75h	

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
334h	JEDEC basic Flash parameter DWORD-14	F7h	Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy). Bits 1:0 = RFU = 11b
335h		FFh	Bit 31 = DPD Supported = not supported = 1 Bits 30:23 = Enter DPD Instruction = FFh (not supported) Bits 22:15 = Exit DPD Instruction not supported = FFh (not supported) Bits 14:13 = Exit DPD to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 11b (not supported) Bits 12:8 = Exit DPD to next operation delay count = 11111b, Exit DPD to next operation delay = (count + 1) * units = not supported
336h		FFh	
337h		FFh	
338h	JEDEC basic Flash parameter DWORD-15	22h	Bits 31:24 = RFU = FFh Bit 23 = Hold or RESET Disable = not supported = 0b Bits 22:20 = Quad Enable Requirements = 101b Bits 19:16 = 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bit[7:0] = Axh + 1xxxb: RFU = 1101b Bits 15:10 = 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_x1xxb: RFU + xx_1xxxb: Input Fh (mode bit reset) on DQ0–DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + x1_xxxxb: Mode Bit[7:0] = Axh + 1x_x1xxb: RFU = 11_1101b Bit 9 = 0-4-4 mode supported = 1b Bits 8:4 = 4-4-4 mode enable sequences + x_1xxxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. = 00010b Bits 3:0 = 4-4-4 mode disable sequences + x1xxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. + 1xxxb: issue the Soft Reset 66/99 sequence = 0010b
339h		F6h	
33Ah		5Dh	
33Bh		FFh	

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
33Ch	JEDEC basic Flash parameter DWORD-16	F0h	Bits 31:24 = Enter 4 Byte Addressing = xxxx_xxx1b: issue instruction B7h (preceding write enable not required) + xx1x_xxxxb: Supports dedicated 4 Byte address instruction set. Refer to the vendor datasheet for the instruction set definition. + 1xxx_xxxxb: Reserved = 10100001b Bits 23:14 = Exit 4 Byte Addressing = xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_1110_0001b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2 or 4 wires depending on the device operating mode. + 1x_xxxxb: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 010000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Non-Volatile Register and Write Enable Instruction for Status Register-1 = +xxx_xxx1b Non-Volatile Status Register 1, powers up to last written value, use instruction 06h to enable Write = +xxx_1xxxb Non-Volatile/Volatile Status Register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile Status Register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. = + xx1_xxxxb: Status Register-1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1110000b
33Dh		50h	
33Eh		F8h	
33Fh		A1h	
340h	JEDEC basic Flash parameter DWORD-17	00h	Not supported
341h			
342h			
343h			
344h	JEDEC basic Flash parameter DWORD-18	00h	Bits 31: 24 = 00h Bit 23 = 0b = JEDEC SPI Protocol Reset not implemented as described in JESD252 Bit 22:18 = 01011b Driver Types 0, 1 and 3 supported Bits 17:16 = Reserved = 00b Bits 15:0 = Reserved = 0000h
345h		00h	
346h		2Ch	
347h		00h	

Table 41 Basic SPI flash parameter, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
348h	JEDEC basic Flash parameter DWORD-19	00h	Not supported
349h			
34Ah			
34Bh			
34Ch	JEDEC basic Flash parameter DWORD-20	F6h	Bits 31:16 = Not supported = 1111_1111_1111_1111b Bit 15:12 = 1111b = 4S-4D-4D Data Strobe is not supported Bit 11:8 = 1111b = 4S-4D-4D not supported Bit 7:4 = 1111b = 4S-4S-4S Data Strobe is not supported Bit 0:3 = 0110b = 133MHz 4S-4S-4S
34Dh		FFh	
34Eh		FFh	
34Fh		FFh	

10.1.4 JEDEC SFDP 4-byte address instruction table

Table 42 4-byte address instruction, JEDEC SFDP Rev D

SFDP parameter relative byte address	SFDP Dword name	Data	Description
350h	JEDEC 4 byte address instructions parameter DWORD-1	F3h	Supported = 1, Not supported = 0 Bits 31:25 = Reserved = 1111_111b Bit 24 = Support for (1-8-8) Page Program Cmd, Instruction = 8Eh = 0b Bit 23 = Support for (1-1-8) Page Program Cmd, Instruction = 84h = 0b Bit 22 = Support for (1-8-8) DTR READ Cmd, Instruction = FDh = 0b Bit 21 = Support for (1-8-8) FAST_READ Cmd, Instruction = CCh = 0b Bit 20 = Support for (1-1-8) FAST_READ Cmd, Instruction = 7Ch = 0b Bit 19 = Support for non-volatile individual sector lock write command, Instruction = E3h = 0b Bit 18 = Support for non-volatile individual sector lock read command, Instruction = E2h = 0b Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 0b Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 0b Bit 15 = Support for (1-4-4) DTR_Read Cmd, Instruction = EEh = 0b Bit 14 = Support for (1-2-2) DTR_Read Cmd, Instruction = BEh = 0b Bit 13 = Support for (1-1-1) DTR_Read Cmd, Instruction = 0Eh = 0b Bit 12 = Support for Erase Command – Type 4 = 0b Bit 11 = Support for Erase Command – Type 3 = 0b Bit 10 = Support for Erase Command – Type 2 = 1b Bit 9 = Support for Erase Command – Type 1 = 1b Bit 8 = Support for (1-4-4) Page Program Cmd, Instruction = 3Eh = 0b Bit 7 = Support for (1-1-4) Page Program Cmd, Instruction = 34h = 1b Bit 6 = Support for (1-1-1) Page Program Cmd, Instruction = 12h = 1b Bit 5 = Support for (1-4-4) FAST_READ Cmd, Instruction = ECh = 1b Bit 4 = Support for (1-1-4) FAST_READ Cmd, Instruction = 6Ch = 1b Bit 3 = Support for (1-2-2) FAST_READ Cmd, Instruction = BCh = 0b Bit 2 = Support for (1-1-2) FAST_READ Cmd, Instruction = 3Ch = 0b Bit 1 = Support for (1-1-1) FAST_READ Cmd, Instruction = 0Ch = 1b Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1b
351h		06h	
352h		00h	
353h		FEh	

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
354h	JEDEC 4 byte address instructions parameter DWORD-2	21h	Bits 31:24 = Instruction for Erase Type 4: Not supported Bits 23:16 = Instruction for Erase Type 3: Not supported Bits 15:8 = DCh = Instruction for Erase Type 2 Bits 7:0 = 21h = Instruction for Erase Type 1
355h		DCh	
356h		FFh	
357h		FFh	
358h	Status, Control and Configuration Register map DWORD-1	00h	Bits 31:0 = Address offset for volatile registers = 00800000h
359h		00h	
35Ah		80h	
35Bh		00h	
35Ch	Status, Control and Configuration Register map DWORD-2	00h	Bits 31:0 = Address offset for non-volatile registers = 00000000h
35Dh		00h	
35Eh		00h	
35Fh		00h	
360h	Status, Control and Configuration Register map DWORD-3	C0h	Bit 31 = Generic Addressable Read Status/Control register command supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands = 3 bytes = 10b Bit 27:26 = Use the number of bits as defined in bits 3:0 in this DWORD = 10b Bit 25:22 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode not supported = 1111b Bit 21:18 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (4S-4S-4S) mode = 1 = 0000b Bit 17:14 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (4S-4D-4D) mode not supported = 1111b Bit 13:10 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (8S-8S-8S) mode not supported = 1111b Bit 9:6 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (8D-8D-8D) mode not supported = 1111b Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b
361h		FFh	
362h		C3h	
363h		EBh	

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
364h	Status, Control and Configuration Register map DWORD-4	C0h	Bit 31 = Generic Addressable Read Status/Control register command for non-volatile registers supported for some (or all) registers = 1b Bit 30 = Generic Addressable Write Status/Control register command for non-volatile registers supported for some (or all) registers = 1b Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for non-volatile registers = 3 bytes = 10b Bit 27:26 = Use the number of bits as defined in bits 3:0 in this DWORD = 10b Bit 25:22 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (2S-2S-2S) mode not supported = 1111b (not supported) Bit 21:18 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (4S-4S-4S) mode = 1 = 0000b Bit 17:14 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (4S-4D-4D) mode not supported = 1111b (not supported) Bit 13:10 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (8S-8S-8S) mode not supported = 1111b (not supported) Bit 9:6 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command in (8D-8D-8D) mode not supported = 1111b (not supported) Bit 5:4 = Reserved = 00b Bit 3:0 = Number of dummy-cycles used for Generic Addressable Read Status/Control register command for non- volatile registers in (1S-1S-1S) mode = 0000b
365h		FFh	
366h		C3h	
367h		EBh	
368h	Status, Control and Configuration Register map DWORD-5	00h	Bits 7:0 = Command used for write access = read only = 00h
369h		65h	Bits 15:8 = Command used for read access = 65h
36Ah		00h	Bits 23:16 = Address of register where WIP is located = 00h (status reg 1 volatile)
36Bh		90h	Bit 31 = Write In Progress (WIP) bit is supported = 1b Bit 30 = Write In Progress polarity, WIP = 1 means write is in progress = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set /cleared by commands using address = 1b Bit 27 = 0: local address for WIP bit is found in last byte of address, 1: Local address for WIP bit is found in Byte 1 of 32 bit address = 0b Bits 26:24 = Bit location of WIP bit in register = bit [0] = 000b

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
36Ch	Status, Control and Configuration Register map DWORD-6	06h	Bits 7:0 = Command used for write access = 06h
36Dh		65h	Bits 15:8 = Command used for read access = 65h
36Eh		00h	Bits 23:16 = Address of register where WEL is located = 00h (status reg 1 volatile)
36Fh		B1h	Bit 31 = Write Enable (WEL) bit is supported = 1b Bit 30 = Write Enable polarity, WEL = 1 means write is in progress = 0b Bit 29 = Write command is a direct operation to set WEL bit = 1b Bit 28 = Bit is accessed by commands using address = 1b Bit 27 = Local address for WEL bit is found in last byte of the address = 0b Bits 26:24 = Bit location of WEL bit in register = bit [1] = 001b
370h	Status, Control and Configuration Register map DWORD-7	00h	Bits 7:0 = Command used for write access = read only = 00h = Read Only
371h		65h	Bits 15:8 = Command used for read access = 65h
372h		01h	Bits 23:16 = Address of register where Program Error is located = 01h (status reg 2 volatile)
373h		95h	Bit 31 = Program Error bit supported = 1b Bit 30 = Positive polarity (Program Error = 0 means no error, Program Error = 1 means last Program operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local address for Program error bit is found in last byte of address = 0b Bits 26:24 = Bit location of Program Error bit in register = bit [5] = 101b
374h	Status, Control and Configuration Register map DWORD-8	00h	Bits 7:0 = Command used for write access = read only = 00h = Read Only
375h		65h	Bits 15:8 = Command used for read access = 65h
376h		01h	Bits 23:16 = Address of register where Erase Error is located = 01h (status reg 2 volatile)
377h		96h	Bit 31 = Erase Error bit supported = 1b Bit 30 = Positive polarity Erase Error = 0 means no error, Erase Error = 1 means last erase operation created an error) = 0b Bit 29 = The device has separate bits for Program Error and Erase Error = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = 0b Bits 26:24 = Bit location of erase Error bit in register = bit [6] = 110b

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
378h	Status, Control and Configuration Register map DWORD-9	71h	Bits 7:0 = Command used for write access = 71h
379h		65h	Bits 15:8 = Command used for read access = 65h
37Ah		04h	Bits 23:16 = Address of register where wait states bits are located = 04h (Configuration Reg 3) volatile
37Bh		94h	Bit 31 = Variable number of dummy-cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states = 2 bit = 00b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [4] = 100b
37Ch	Status, Control and Configuration Register map DWORD-10	71h	Bits 7:0 = Command used for write access = 71h
37Dh		65h	Bits 15:8 = Command used for read access = 65h
37Eh		04h	Address of register where wait states bits are located = 04h (Configuration Reg-3 non-volatile)
37Fh		D0h	Bit 31 = Variable number of dummy-cycles supported = 1b Bits 30:29 = Number of physical bits used to set wait states = 4 bit = 10b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b
380h	Status, Control and Configuration Register map DWORD-11	00h	Bit 31 = 30 dummy-cycles not supported = 0b Bits 30:26 = Bit pattern used to set 30 dummy-cycles = 00000b Bit 25 = 28 dummy-cycles not supported = 0b Bits 24:20 = Bit pattern used to set 28 dummy-cycles = 00000b Bit 19 = 26 dummy-cycles not supported = 0b Bits 18:14 = Bit pattern used to set 26 dummy-cycles = 00000b Bit 13 = 24 dummy-cycles not supported = 0b Bits 12:8 = Bit pattern used to set 24 dummy-cycles = 00000b Bit 7 = 22 dummy-cycles not supported = 0b Bits 6:2 = Bit pattern used to set 22 dummy-cycles = 00000b Bits 1:0 = Reserved = 00b
381h		00h	
382h		00h	
383h		00h	

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
384h	Status, Control and Configuration Register map DWORD-12	B0h	Bit 31 = 20 dummy-cycles not supported = 0b Bits 30:26 = Bit pattern used to set 20 dummy-cycles = 00000b Bit 25 = 18 dummy-cycles not supported = 0b Bits 24:20 = Bit pattern used to set 18 dummy-cycles = 00000b Bit 19 = 16 dummy-cycles not supported = 0b Bits 18:14 = Bit pattern used to set 16 dummy-cycles = 00000b Bit 13 = 14 dummy-cycles supported = 1b Bits 12:8 = Bit pattern used to set 14 dummy-cycles = 01110b Bit 7 = 12 dummy-cycles supported = 1b Bits 6:2 = Bit pattern used to set 12 dummy-cycles = 01100b Bits 1:0 = Reserved = 00b
385h		2Eh	
386h		00h	
387h		00h	
388h	Status, Control and Configuration Register map DWORD-13	88h	Bit 31 = 10 dummy-cycles supported = 1b Bits 30:26 = Bit pattern used to set 10 dummy-cycles = 01010b Bit 25 = 8 dummy-cycles supported = 1b Bits 24:20 = Bit pattern used to set 8 dummy-cycles = 01000b Bit 19 = 6 dummy-cycles supported = 1b Bits 18:14 = Bit pattern used to set 6 dummy-cycles = 00110b Bit 13 = 4 dummy-cycles supported = 1b Bits 12:8 = Bit pattern used to set 4 dummy-cycles = 00100b Bit 7 = 2 dummy-cycles supported = 1b Bits 6:2 = Bit pattern used to set 2 dummy-cycles = 00010b Bits 1:0 = Reserved = 00b
389h		A4h	
38Ah		89h	
38Bh		AAh	
38Ch	Status, Control and Configuration Register map DWORD-14	71h	Bits 7:0 = Command used for write access = 71h
38Dh		65h	Bits 15:8 = Command used for read access = 65h
38Eh		03h	Address of register where wait states bits are located = 03h (Configuration Reg - 2 Volatile)
38Fh		93h	Bit 31 = QPI Mode Enable Volatile supported = 1b Bit 30 = QPI Mode Enable bit polarity (Positive QPI mode bit = 1 enabled) = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of QPI mode enable in register = bit [3] = 011b

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
390h	Status, Control and Configuration Register map DWORD-15	71h	Bits 7:0 = Command used for write access = 71h
391h		65h	Bits 15:8 = Command used for read access = 65h
392h		03h	Address of register where wait states bits are located = 03h (Configuration Reg 2 Non-Volatile)
393h		93h	Bit 31 = QPI Mode Enable Non-Volatile supported = 1b Bit 30 = QPI Mode Enable bit polarity (Positive QPI mode bit = 1 enabled) = 0b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = Local Address for Variable Dummy-Cycle Setting bits in last address = 0b Bits 26:24 = Bit location of QPI mode enable in register = bit [3] = 011b
394h	Status, Control and Configuration Register map DWORD-16	00h	Not supported
395h		00h	
396h		00h	
397h		00h	
398h	Status, Control and Configuration Register map DWORD-17	00h	Not supported
399h		00h	
39Ah		00h	
39Bh		00h	
39Ch	Status, Control and Configuration Register map DWORD-18	00h	Not supported
39Dh		00h	
39Eh		00h	
39Fh		00h	
3A0h	Status, Control and Configuration Register map DWORD-19	00h	Not supported
3A1h		00h	
3A2h		00h	
3A3h		00h	
3A4h	Status, Control and Configuration Register map DWORD-20	00h	Not supported
3A5h		00h	
3A6h		00h	
3A7h		00h	
3A8h	Status, Control and Configuration Register map DWORD-21	00h	Not supported
3A9h		00h	
3AAh		00h	
3ABh		00h	
3ACh	Status, Control and Configuration Register map DWORD-22	00h	Not supported
3ADh		00h	
3AEh		00h	
3AFh		00h	

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
3B0h	Status, Control and Configuration Register map DWORD-23	00h	Not supported
3B1h		00h	
3B2h		00h	
3B3h		00h	
3B4h	Status, Control and Configuration Register map DWORD-24	00h	Not supported
3B5h		00h	
3B6h		00h	
3B7h		00h	
3B8h	Status, Control and Configuration Register map DWORD-25	00h	Not supported
3B9h		00h	
3BAh		00h	
3BBh		00h	
3BCh	Status, Control and Configuration Register map DWORD-26	71h	Bits 7:0 = Command used for write access = 71h
3BDh		65h	Bits 15:8 = Command used for read access = 65h
3BEh		03h	Address of register where Output Driver Strength volatile bits are located = 03h (Configuration Reg-2 volatile)
3BFh		D4h	Bits 31:30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = local address for each bit is found in last byte of address = 0b Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [4] = 100b
3C0h	Status, Control and Configuration Register map DWORD-27	71h	Bits 7:0 = Command used for write access = 71h
3C1h		65h	Bits 15:8 = Command used for read access = 65h
3C2h		03h	Address of register where Output Driver Strength volatile bits are located = 03h (Configuration Reg 2 non-volatile)
3C3h		D4h	Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b Bit 29 = Reserved = 0b Bit 28 = Bit is set/cleared by commands using address = 1b Bit 27 = local address for each bit is found in last byte of address = 0b Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [4] = 100b

Table 42 4-byte address instruction, JEDEC SFDP Rev D *(continued)*

SFDP parameter relative byte address	SFDP Dword name	Data	Description
3C4h	Status, Control and Configuration Register map DWORD-28	00h	Bits 7:0 = Reserved = 00h
3C5h		00h	Bits 15:8 = Reserved = 00h
3C6h		20h	Bits 31:29 = Bit pattern to support Driver type 0 = 45 Ohms = 001b Bits 28:26 = Bit pattern to support Driver type 1 = 30 Ohms = 000b Bits 25:23 = Bit pattern to support Driver type 2 = 60 Ohms = N/A = 000b Bits 22:20 = Bit pattern to support Driver type 3 = 90 Ohms = 010b Bits 19:17 = Bit pattern to support Driver type 4 = N/A = 000b Bit 16 = Reserved = 0b
3C7h		20h	

10.2 Device ID address map

10.2.1 Field definitions

Table 43 Manufacturer device type

Byte address	Data	Description
00h	C1h	Manufacturer ID for Infineon
01h	60h	Device ID most significant byte - Memory Interface Type
02h	1Ah	Device ID least significant byte - 512Mb
03h	Undefined	Reserved for Future Use
04h	Undefined	Reserved for Future Use
05h	Undefined	Reserved for Future Use
06h	Undefined	Reserved for Future Use
07h	Undefined	Reserved for Future Use

Table 44 Unique Device ID

Byte address	Data	Description
00h to 07h	8-byte Unique Device ID	64-bit unique ID number, see **“Device unique ID”** on page 19.

10.2.2 Initial delivery state

The device is shipped from Infineon with non-volatile bits set as follows:

- The entire memory array is erased: i.e., all bits are set to ‘0’ (each byte contains 00h)
- The SFDP address space contains the values as defined in the description of the SFDP address space
- The ID address space contains the values as defined in the description of the ID address space
- The Status Register 1 Non-volatile contains 00h (all SR1NV bits are cleared to 0’s)
- The Configuration Register 1 Non-volatile contains 00h
- The Configuration Register 2 Non-volatile contains 00h
- The Configuration Register 3 Non-volatile contains 00h

11 Electrical specifications

11.1 Absolute maximum ratings

Table 45 Absolute maximum ratings[18]

Parameter	Maximum ratings
Storage temperature plastic packages	–65°C to +150°C
Ambient temperature with power applied	–65°C to +125°C
$V_{DD\ MAX}$, $V_{DDIO\ MAX}$	–0.5 V to +4.1 V
Input voltage with respect to ground (V_{SS}) [19]	–0.5 V to V_{DD} + 0.5 V
Electrostatic discharge - HBM	> 2000 V
Electrostatic discharge - CDM	> 500 V
Output short circuit current [20]	100 mA

11.2 Latchup characteristics

Table 46 Latchup specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input-only connections	–1.0	4.1	V
Input voltage with respect to V_{SS} on all I/O connections	–1.0	4.1	V
V_{DD} Current	–100	+100	mA

11.3 Thermal resistance

Table 47 Thermal resistance

Parameter	Description	100-pin TQFP	Unit
Theta JC	Thermal resistance (junction to case)	12.664	°C/W

Notes

18. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
19. See **“Input signal overshoot”** on page 118 for allowed maximums during signal transition.
20. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

11.4 Operating ranges

The operating ranges define those limits between which the functionality of the device is guaranteed.

11.4.1 Power supply voltages

Table 48 Power supply voltages

Parameter	Range	Voltage
V_{DD}		2.97 V to 3.63 V
V_{DDIO}	3.3 V range	2.97 V to 3.63 V
	1.8 V range	1.71 V to 1.89 V

11.4.2 Temperature ranges

Table 49 Temperature ranges

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Case temperature	T_C	Military (M)	–55	+125	°C

11.4.3 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{DD}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –1.0 V or overshoot to V_{DD} + 1.0 V, for periods up to 20 ns.

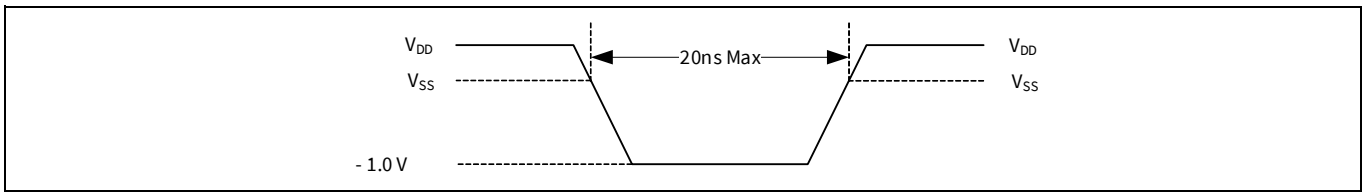


Figure 78 Maximum negative overshoot waveform

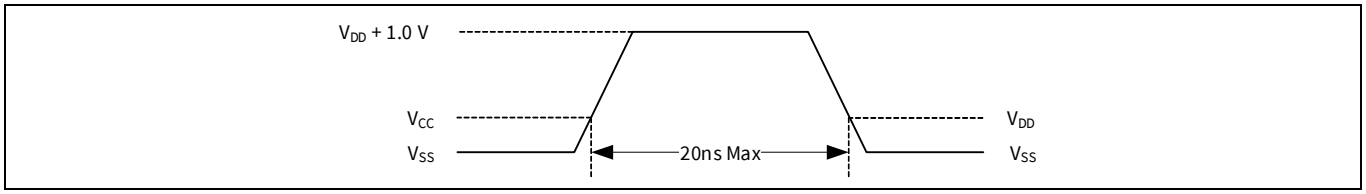


Figure 79 Maximum positive overshoot waveform

11.5 Power-up and power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{DD}) until V_{DD} reaches the correct value as follows:

- V_{DD} (min) at power-up, and then for a further delay of t_{PU}
- V_{SS} at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to ensure safe and proper power-up and power-down.

User is not allowed to enter any command until a valid delay of t_{PU} has elapsed after the moment that V_{DD} rises above the minimum V_{DD} threshold. See **Figure 80**. However, correct operation of the device is not guaranteed if V_{DD} returns below V_{DD} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

The device draws I_{POR} during t_{PU}. After power-up (t_{PU}), the device is in Standby mode, draws CMOS standby current (I_{SB}) and the WEL bit is reset.

During power-down or voltage drops below V_{DD}(cut-off), the voltage must drop below V_{DD} (low) for a period of t_{PD} for the part to initialize correctly on power-up. See **Figure 81**. If during a voltage drop the V_{DD} stays above V_{DD} (cut-off) the part will stay initialized and will work correctly when V_{DD} is again above V_{DD} (min). In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RSTEN 66h followed by RST 99h) will restart the POR process.

If V_{DD} drops below the V_{DD} (cut-off) during an embedded program or erase operation the embedded operation may be aborted and the data in that memory area may be incorrect.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{DD} supply at the device. Each device in a system should have the V_{DD} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1 µF).

Table 50 Power-up / power-down voltage and timing

Symbol	Parameter	Min	Max	Unit
V_{DD} (min)	V_{DD} (minimum operation voltage)	2.97	–	V
V_{DD} (cut-off)	V_{DD} (Cut off where re-initialization is needed)	2.85	–	V
V_{DD} (low)[21]	V_{DD} (low voltage for initialization to occur)	0.80	–	V
t_{PU}	V_{DD}(min) to Read operation	–	1.75	ms
t_{PD}	V_{DD}(low) time	170.0	–	µs

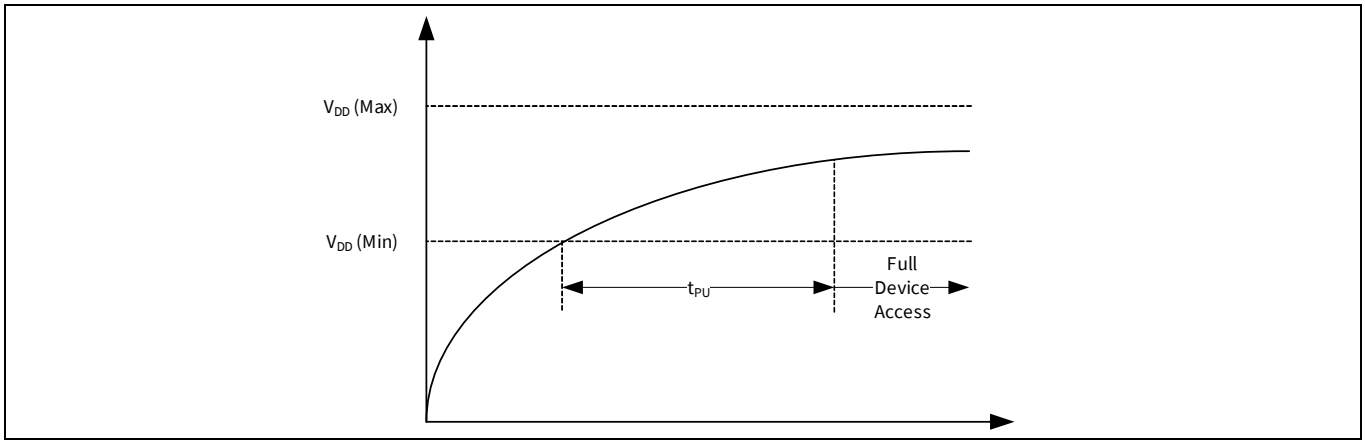


Figure 80 Power-up

Note
21.Guaranteed by design.

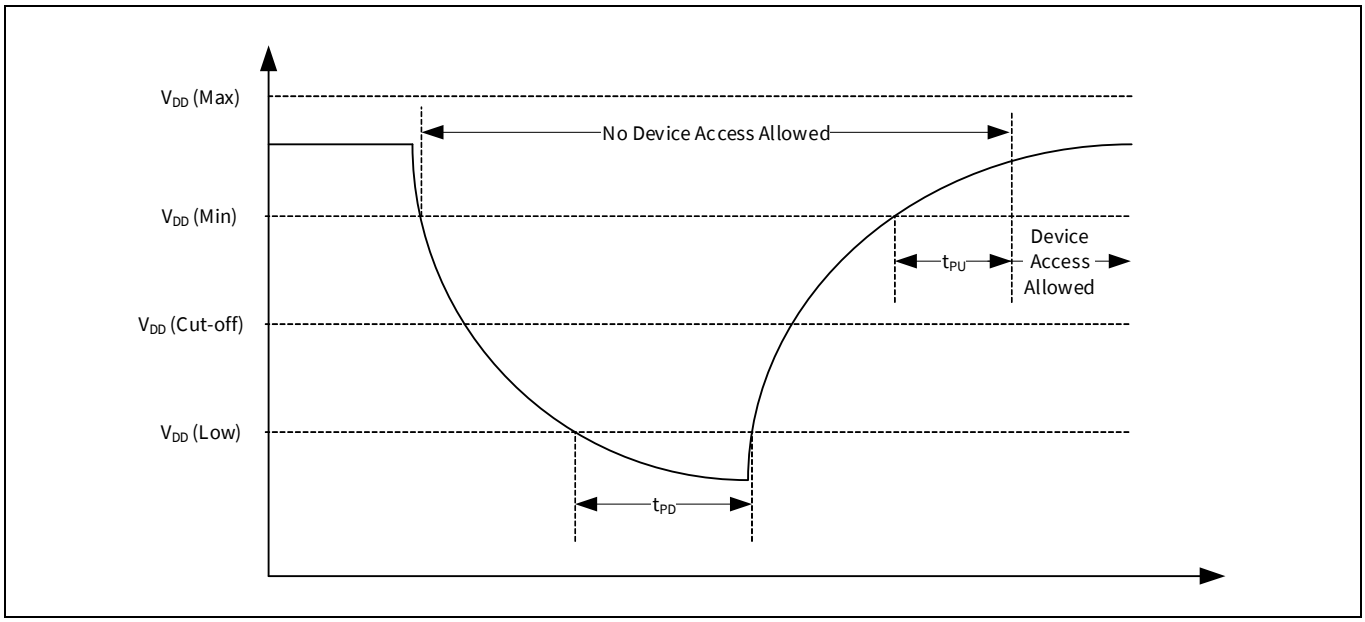


Figure 81 Power-down and voltage drop

11.6 DC characteristics

Table 51 DC characteristics - Operating temperature range –55°C to +125°C

Symbol	Parameter	Test conditions	Min	Typ[22]	Max	Unit
V_{IL}	Input low voltage	–	–0.3	–	$0.3 \times V_{DDIO}$	V
V_{IH}	Input high voltage	–	$0.7 \times V_{DDIO}$	–	$V_{DDIO} + 0.3$	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA, V_{DD} = V_{DD} min	–	–	0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	V_{DDIO} – 0.5	–	–	V
I_{LI}	Input leakage current (except RESET#)	V_{DD} = V_{DD} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	–10	–	+10	µA
I_{LI}	Input leakage current (RESET# only)	V_{DD} = V_{DD} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	–900	–	+200	µA
I_{LO}	Output leakage current	V_{DD} = V_{DD} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	–10	–	+10	µA
I_{CC1}	Active QIO/QPI Read Current (READ)[23]	QIO/QPI @ 133 MHz No output load	–	50	120	mA
I_{CC2}	Active Page Program Current	CS# = V_{DD}	–	50	120	mA
I_{CC3}	Active Non-Volatile Register Write Current (WRAR, WRR)	CS# = V_{DD}	–	50	120	mA
I_{CC4}	Active Sector / Block / Chip Erase Current	CS# = V_{DD}	–	50	120	mA
I_{CC5}	Active Page / Chip Scrub Current	CR1[7] = 0 (Flash); CS# = V_{DD}	–	50	120	mA
		CR1[7] = 1 (SRAM); CS# = V_{DD}	–	25	50	mA
I_{SB}	Standby Current QPI Mode	RESET#, CS# = V_{DD}; SI, SCK = V_{DD} or V_{SS}	–	5	12	mA
I_{POR}	Power On Reset Current (In-rush)[24]	RESET#, CS# = V_{DD}; SI, SCK = V_{DD} or V_{SS}	–	15	100	mA

11.6.1 Active power and standby power modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase and write operations have completed. The device then goes into the Standby Power mode and power consumption drops to I_{SB}.

Notes
22. Typical values are at T_A = 25°C. This parameter is guaranteed by characterization, not tested in production.
23. Outputs unconnected during read data return. Output switching current is not included.
24. Guaranteed by design.

12 Timing specifications

12.1 Key to switching waveforms

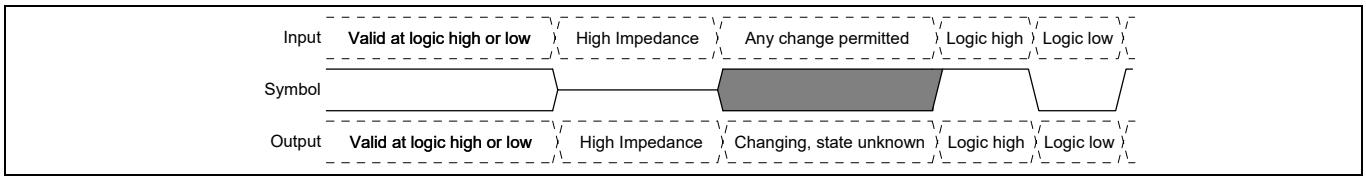


Figure 82 Waveform element meanings

12.2 AC test conditions

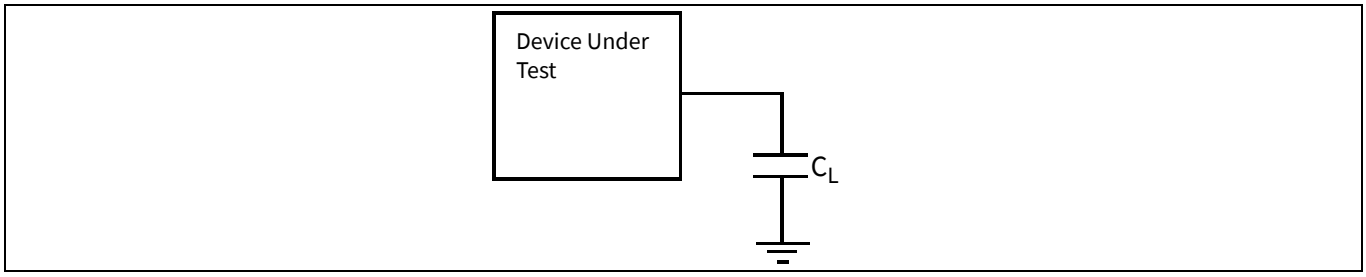


Figure 83 Test setup

Table 52 AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	–	(15 / 30)[25]	pF
–	Input Pulse Voltage	$0.2 \times V_{DD}$	$0.8 \times V_{DD}$	V
–	Input Timing Ref Voltage	$0.5 \times V_{DD}$		V
–	Output Timing Ref Voltage	$0.5 \times V_{DD}$		V

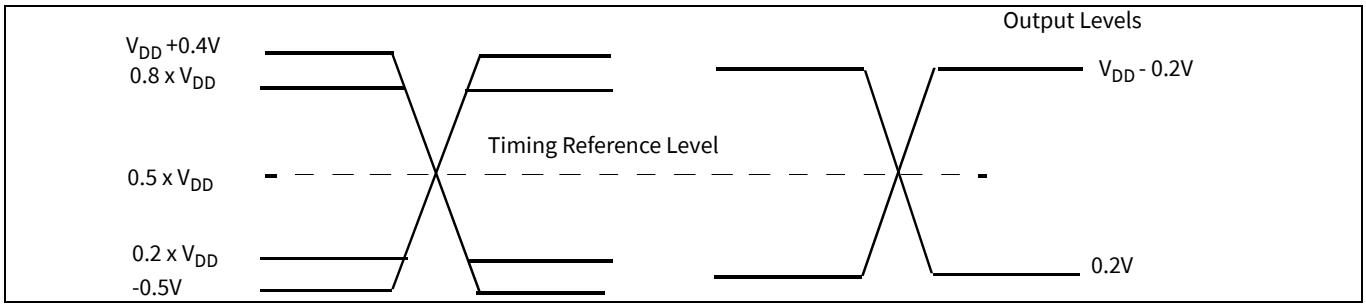


Figure 84 Input, output and timing reference levels[26]

Notes
25. Load Capacitance depends on the operation frequency or Mode of operation.
26. AC characteristics tables assume clock and data signals have the same slew rate (slope). See **Table 55**, Note 29 for Slew Rates at operating frequencies.

12.2.1 Capacitance characteristics

Table 53 Capacitance [27]

Symbol	Parameter	Test conditions	Min	Max	Unit
C_{IN}	Input capacitance (applies to SCK, CS#, RESET#)	1 MHz	–	8	pF
C_{OUT}	Output capacitance (applies to All I/O)	1 MHz	–	8	pF

12.3 Reset

If a Hardware Reset is initiated during a Erase, Program, Scrub or writing of a Register operation the data in that Sector, Page or Register is not stable, the operation that was interrupted needs to be initiated again. If a Hardware Reset is initiated during a Software Reset operation, the Hardware Reset might be ignored.

In addition, if a Hardware Reset is initiated during a Program, Scrub or writing of a Nonvolatile Register operation, all of the data in that Page may be corrupted and non-recoverable.

12.3.1 Power-on (cold) reset

The device executes a Power-On Reset (POR) process until a time delay of t_{PU} has elapsed after the moment that V_{DD} rises above the minimum V_{DD} threshold. See **Figure 80**, **Table 50**. The device must not be selected (CS# to go HIGH with V_{DD}) during power-up (t_{PU}), i.e. no commands may be sent to the device until the end of t_{PU}.

RESET# reset function is ignored during POR. If RESET# is LOW during POR and remains LOW through and beyond the end of t_{PU}, CS# must remain HIGH until t_{RH} after RESET# returns HIGH. RESET# must return HIGH for greater than t_{RS} before returning LOW to initiate a hardware reset.

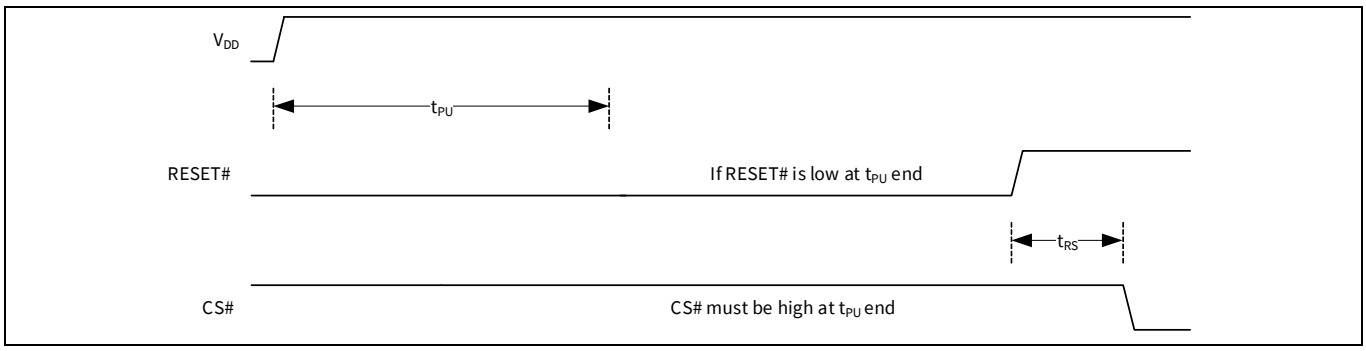


Figure 85 RESET# LOW at the end of POR

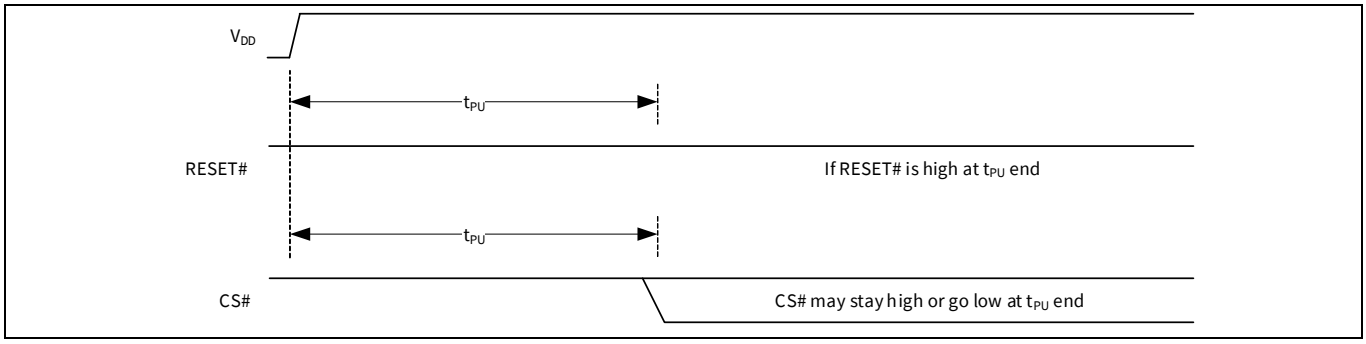


Figure 86 RESET# HIGH at the end of POR

Note
27.Guaranteed by design.

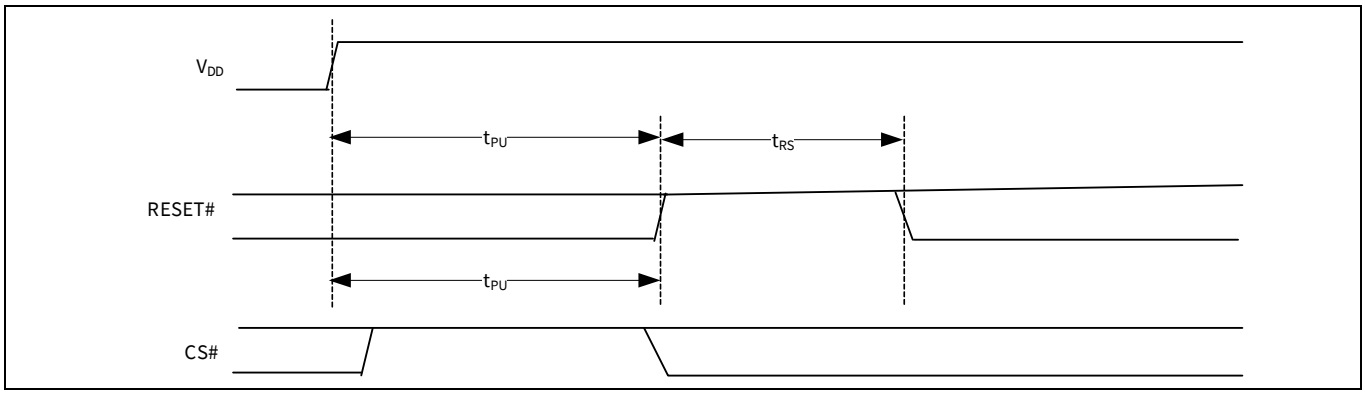


Figure 87 POR followed by hardware reset

12.3.2 RESET# input initiated hardware (warm) reset

The RESET# input initiates the reset operation when transitions from V_{IH} to V_{IL} for > t_{RP}. The device will reset register states in the same manner as power-on reset but does not go through the full reset process that is performed during POR.

The hardware reset process requires a period of t_{RPH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going LOW will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process.

The software reset command (RSTEN 66h followed by RST 99h) is independent of the state of RESET#. If RESET# is HIGH or unconnected and the software reset instructions are issued the device will perform software reset.

Table 54 RESET# parameters

Parameter	Description	Limit	Time	Unit
t_{RS}	RESET# setup	Min	50	ns
t_{RH} (t_{RPH})	RESET# hold (w.r.t CS#)	Min	1.5	ms
t_{RP}	RESET# pulse width	Min	200	ns
t_{RESET}	Internal device reset	Min	300	µs

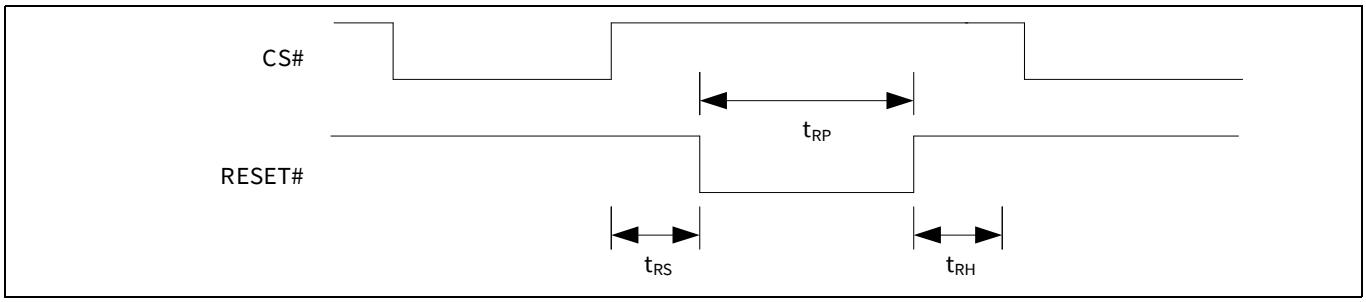


Figure 88 Hardware RESET# waveform[28]

Note
28. RESET# LOW is ignored during Power-up (t_{PU}). If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and t_{RH} will determine when CS# may go LOW.

12.4 AC characteristics

Table 55 AC characteristics

Symbol	Parameter	Min	Max	Unit
$F_{SCK, R}$	SCK clock frequency for READ and 4READ instructions	DC	33	MHz
$F_{SCK, C}$	SCK clock frequency for the following quad commands: FAST_READ, 4FAST_READ, QOR, 4QOR, QIOR, 4QIOR	DC	133	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}	–	–
t_{WH}, t_{CH}	Clock High Time	50% P_{SCK} ± 5%	–	ns
t_{WL}, t_{CL}	Clock Low Time	50% P_{SCK} ± 5%	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)[29]	1.5	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)[29]	1.5	–	V/ns
t_{CS}	CS# HIGH Time (Any Read Instructions)	40	–	ns
	CS# HIGH Time (All other Non-Read instructions)	50	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	4.5	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	5.5	–	ns
t_{SU}	Data in Setup Time	2.0	–	ns
t_{HD}	Data in Hold Time	4.0	–	ns
t_V1	Clock Low to Output Valid (30 pF Loading, VDDIO = 3.3 V)	–	8.5	ns
	Clock Low to Output Valid (15 pF Loading, VDDIO = 3.3 V)	–	6.5	ns
t_V2	Clock Low to Output Valid (30 pF Loading, VDDIO = 1.8 V)	–	10	ns
	Clock Low to Output Valid (15 pF Loading, VDDIO = 1.8 V)	–	8	ns
t_{HO}	Output Hold Time	1	–	ns
t_{DIS}[31]	Output Disable Time	–	12	ns
t_{DIS2}[31]	Output Disable Time (Reset & Quad enabled)	–	20	ns
t_{WPS}	WP# Setup Time[30]	20	–	ns
t_{WPH}	WP# Hold Time[30]	50	–	ns

Notes
29. t_{CRT}, t_{CLCH} Clock Rise and fall slew rate for Fast clock (133 MHz) min is 1.5 V/ns and for Slow Clock (40 MHz) min is 1.0 V/ns.
30. Only applicable as a constraint for WRR or WRAR instruction when SRP0 is set to '1'.
31. Guaranteed by design.

12.4.1 Clock timing

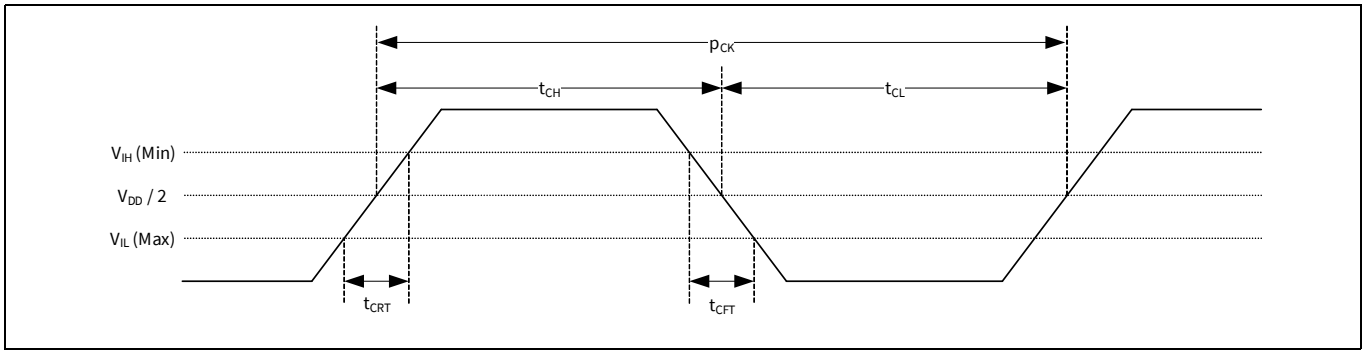


Figure 89 Clock timing

12.4.2 Input / output timing

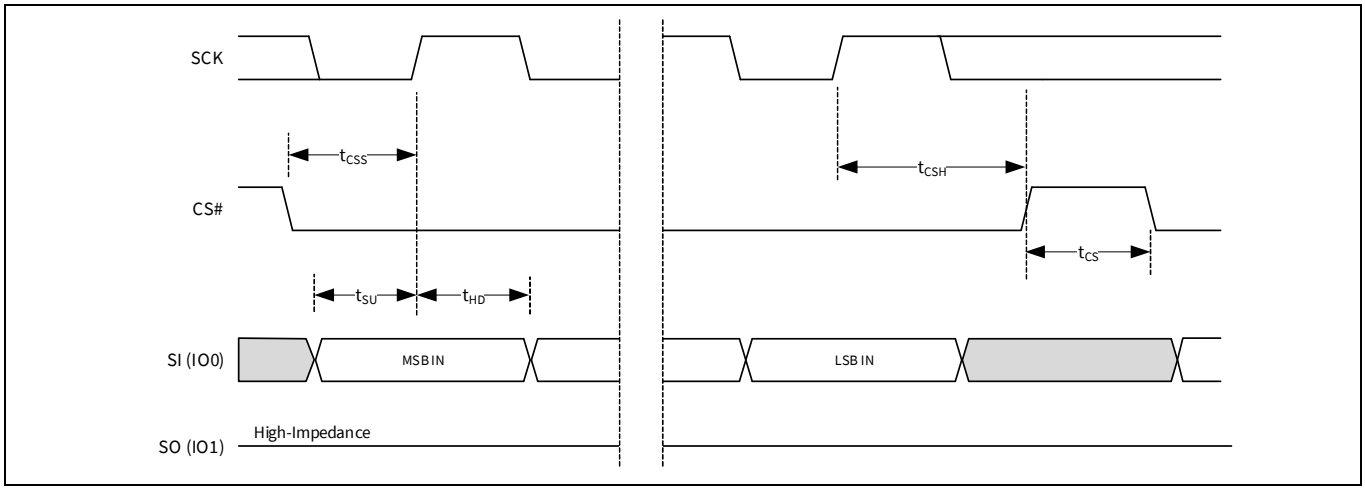


Figure 90 SPI single bit input timing

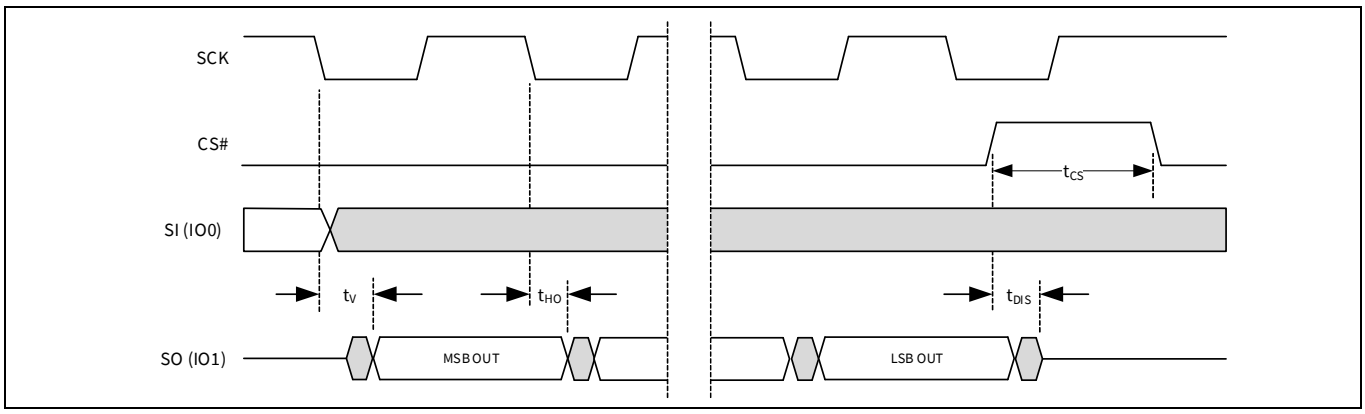


Figure 91 SPI single bit output timing

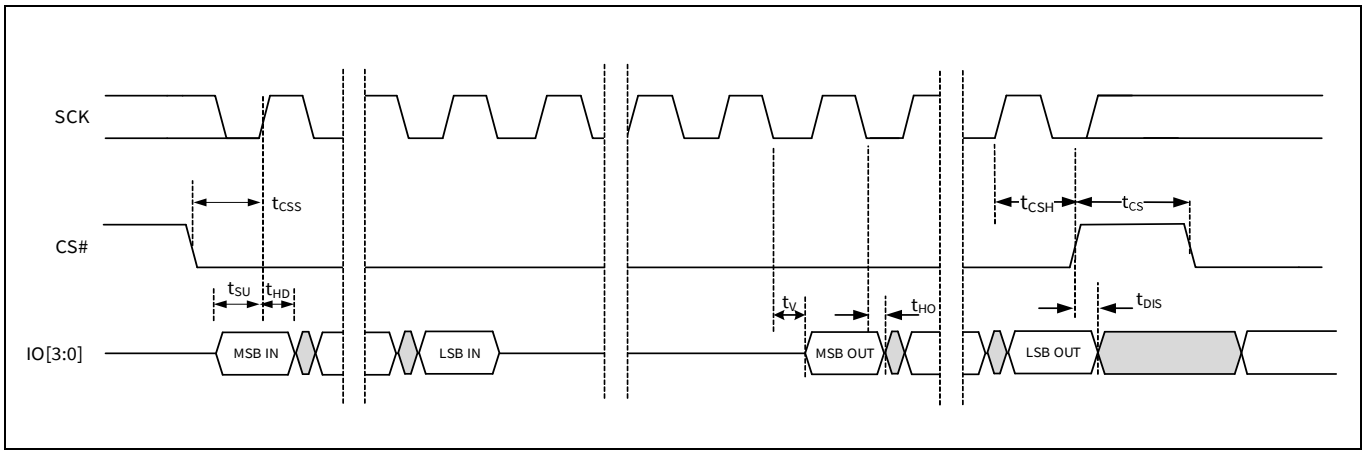


Figure 92 Quad / QPI timing

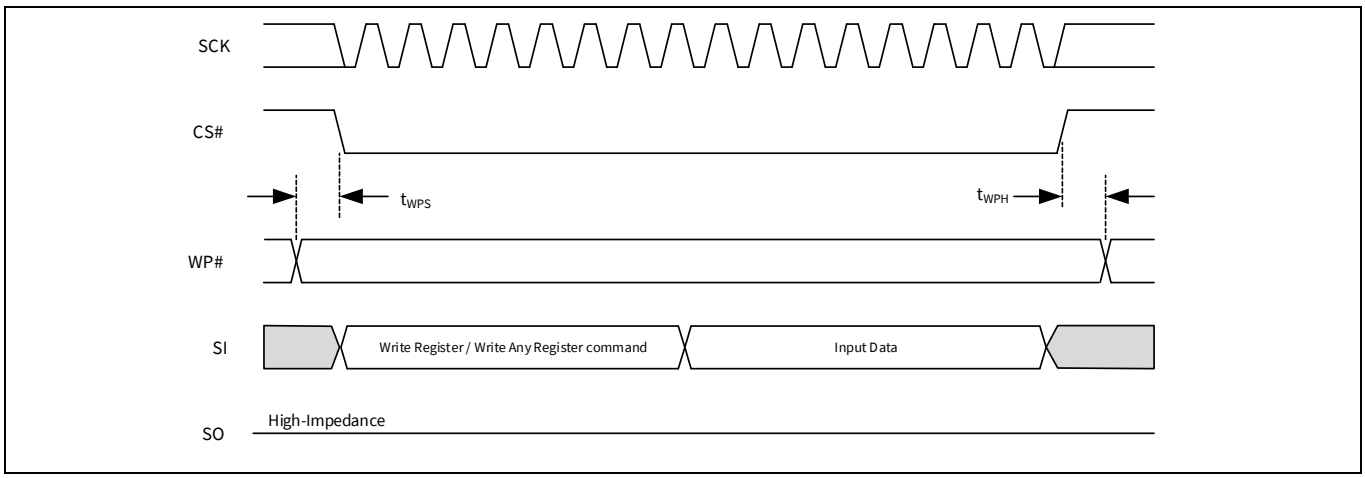


Figure 93 WP# input timing

12.5 Embedded algorithm performance tables

Table 56 Program and erase performance

Symbol	Parameter	Min	Typ[32]	Max	Unit
t_W	Non-volatile Register Write Time	–	–	32	ms
t_{PP}	Page Programming (2048 Bytes)	–	–	32	ms
t_{SE}	Sector Erase Time (1 MByte)	–	–	22	ms
t_{BE}	Block Erase Time (8 MBytes)	–	–	176	ms
t_{CE}	Chip Erase Time (64 MBytes)	–	–	1.41	s
t_{PSR}	Page Scrub Time (2048 Bytes)	–	–	32	ms
t_{CSR1}	Chip Scrub Time (64 MBytes) (CR1[7] = 0) Flash	–	–	1048	s
t_{CSR2}	Chip Scrub Time (CR1[7] = 1) SRAM	–	–	1	ms

Table 57 Program or Erase Suspend AC parameters

Parameter	Min	Max	Unit	Comments
Suspend latency (t_{SL})	–	40	µs	Time from Suspend command until the WIP bit is ‘0’
Resume to next suspend (t_{RNS})	100	–	µs	Is the time needed to issue the next Suspend command.

Note
32. Typical program and erase times assume the following conditions: 25°C, V_{DD} = 3.0 V; 10,000 cycles; checker-board data pattern.

13 Ordering information

Table 58 lists configurations planned to be supported in volume for this device.

Note: Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

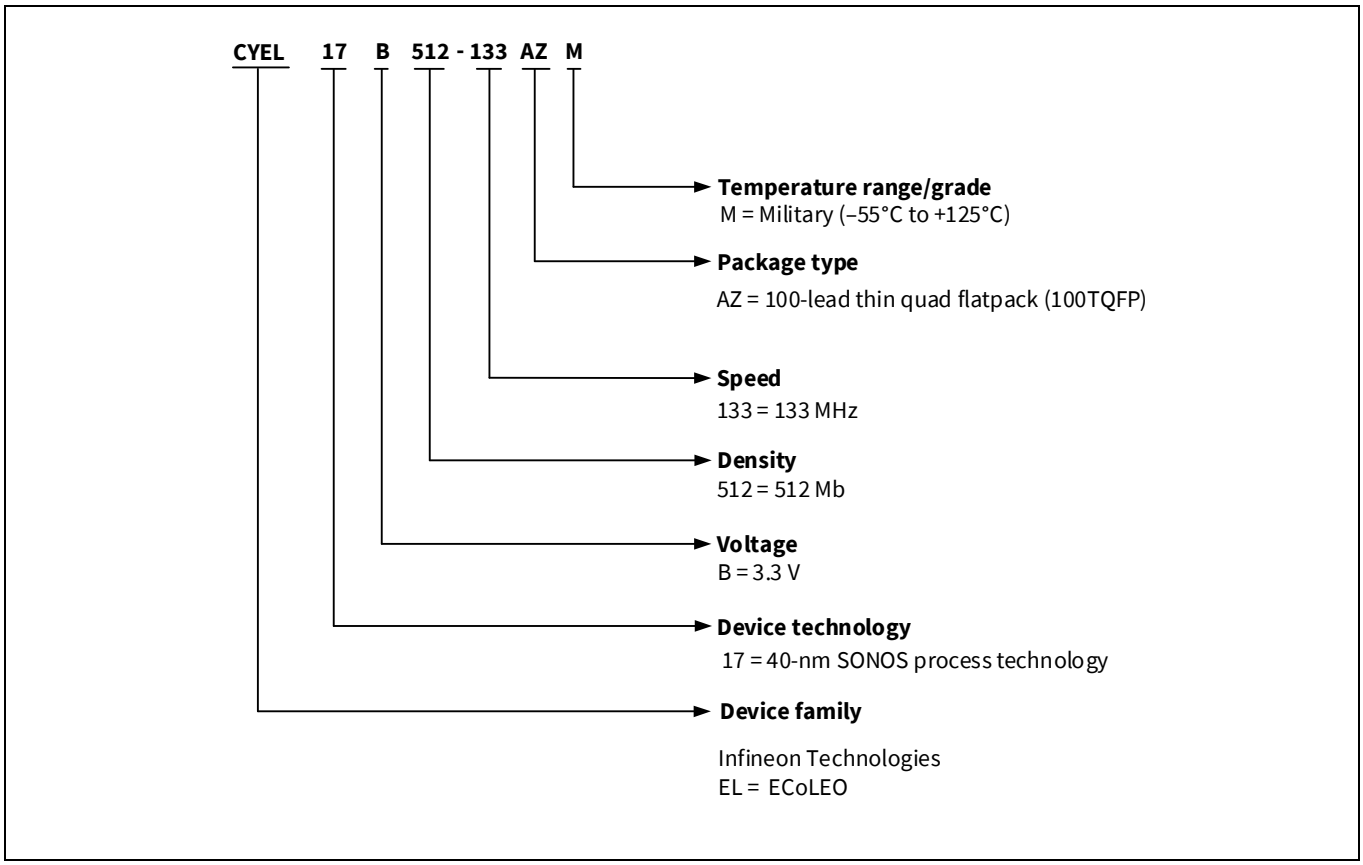
Table 58 Ordering information

Product	Package diagram	Package type	Operating range
CYEL17B512-133AZM	51-85050	100-pin plastic TQFP package	Military (-55°C to 125°C)

Note: These parts are Pb-free. Contact your local Infineon sales representative for availability of these parts.

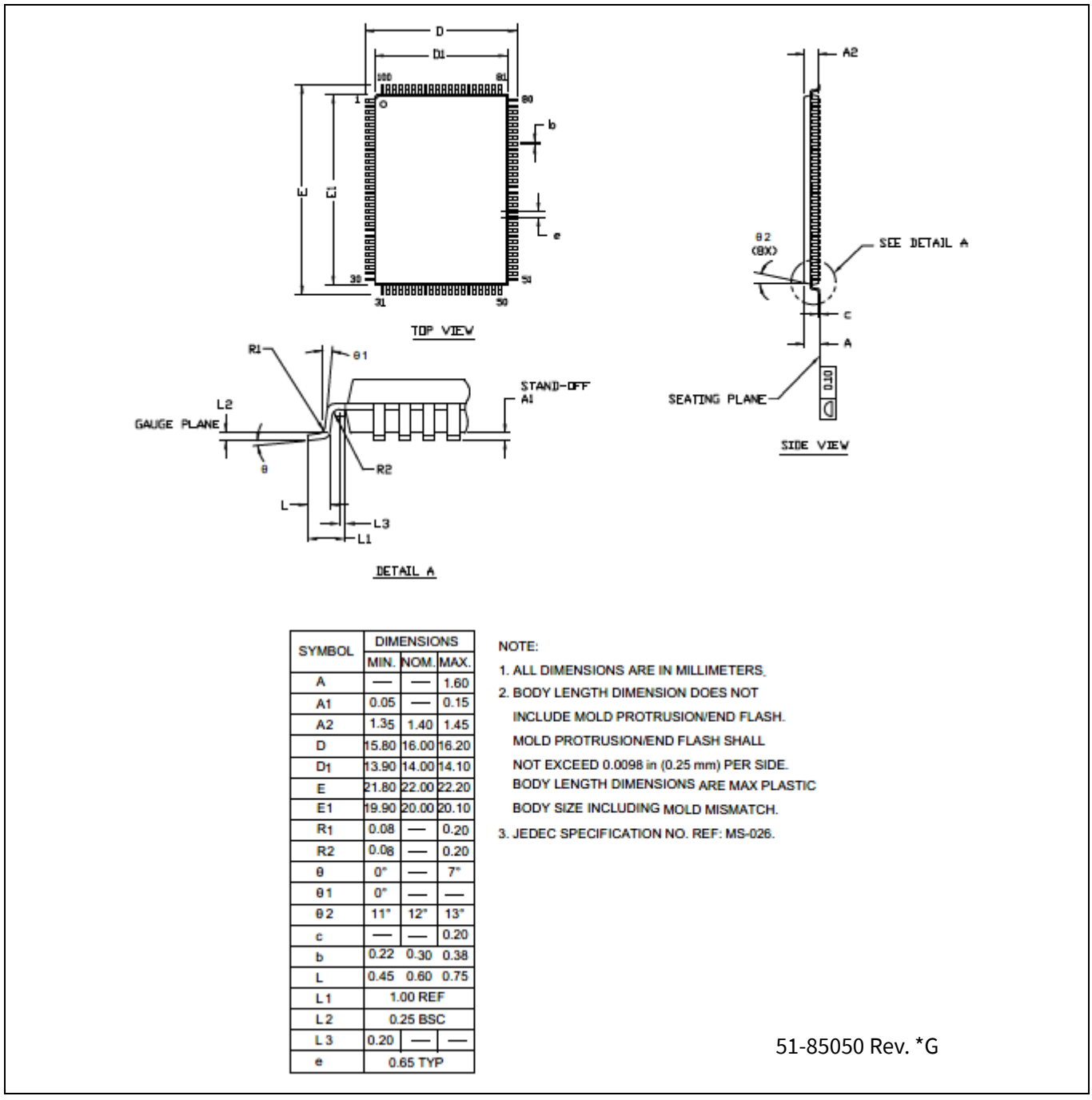
13.1 Ordering code definition

The ordering part number is formed by a valid combination of the following:



14 Package diagrams

14.1 100-lead thin quad flatpack (100AZ)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 Rev. *G

Figure 94 100-lead TQFP (14.0 × 20.0 × 1.4 mm) A100RA, (PG-TQFP-100)

Revision history

Document revision	Date	Description of changes
**	2024-04-24	New spec.
*A	2024-06-07	Updated the Default state for Bits 3 in**Table 16**. Added 'default' to 8 in **Table 18**. Updated the columns Data and Description for 308h, 30Ah, 31Ah and 31Bh in **Table 41**. Added Note 21 in **Table 50**. Added Note 24 in **Table 51**. Added Note 27 in **Table 53**. Added Note 31 in **Table 55**. Updated **Ordering information** section.
*B	2025-05-07	Updated **Table 2** table title. Updated columns Data and Description for 06h, 09h, 11h, 19h in **Table 40**. Updated columns Data and Description for 30Ch, 30Eh, 316h, 31Ch, 31Eh in **Table 41**. Updated columns Data and Description for 353h, 36Fh, 3C7h in **Table 42**. Updated the typical current value of 'Page/Chip Scrub SRAM' to '25' in **Table 3**. Updated the description of 'QUAD' field in **Table 11**. Updated the below figures: **Figure 7**, **Figure 8**, **Figure 30**, **Figure 59**, and **Figure 92**.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-05-07
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-39759 Rev. *B

Important notice
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.