PRELIMINARY

CYFP1002XXXX

CYFP1-8080 Datasheet

Features

- **Fingerprint Sensor**
  - BGA package consisting of a die mounted on a polymer substrate sensor
  - 8.0 mm × 8.0 mm active imaging area fingerprint sensor
  - 340 DPI 107 × 107 pixel array at 8-bits per pixel resolution
  - Great image quality with polymer, plastic, and ceramic coatings < 100µ in overall thickness
  - Superior image quality with polymer coatings, and ceramic and glass cover over sensor
  - 32-bit Arm® Cortex®-M0 CPU
  - Noise-suppression technologies for battery chargers, displays, and radios in the device
  - Self-calibration and self-testing
  - Factory tuned with on-chip baseline storage, no field tuning required
  - Secure firmware upgrades via bootloader
- **System Performance**
  - Live Finger Complete Acquisition Time (Get_Image): ~160ms)
  - 14 Finger Identify Match Time: ~500ms (average)
  - <1.5% FRR at FAR >1:100K using CY-supplied matching SW
  - 360 degree finger placement
- **Embedded Environment**
  - Embedded framework (CYFPEF) provided for porting into host processor
  - Recommended MCU Features: Cortex M4, 256KB of flash, and 96KB of RAM
  - Ability to import and export templates securely
  - Configurable security levels (1:10K to 1:1000K)
  - Simple secure external communication protocol over MCU UART Interface
- **Sensor Communication Interface**
  - SPI slave bit rates up to 7.8 Mbps
  - Strong 256-bit AES encryption secures the system interface from the sensor to the host processor
- **Power (configuration-dependent)**
  - Operation of single 3.3-V supply
  - 1.71 V to 1.95 V direct digital supply or 2.0 V to 5.5 V via LDO
  - 2.65 V to 5.5 V analog supply
  - <80-mW active power (average power while sensing)
  - 8-µW typical deep-sleep power
  - 400-µW Finger detection power @ 10 detects per second
- **Operating Temperature Range**
  - –40 °C to +85 °C
- **Package Options**
  - 73 BGA package, 8.87 × 9.26 mm rectangular sensor

Optional Features

- False finger rejection limiting host processor interruptions
- Fake finger rejection (anti-spoofing)
- Programmable finger detection timing (Wake-on-Finger)
- Navigation

Sensor Shown With Coating

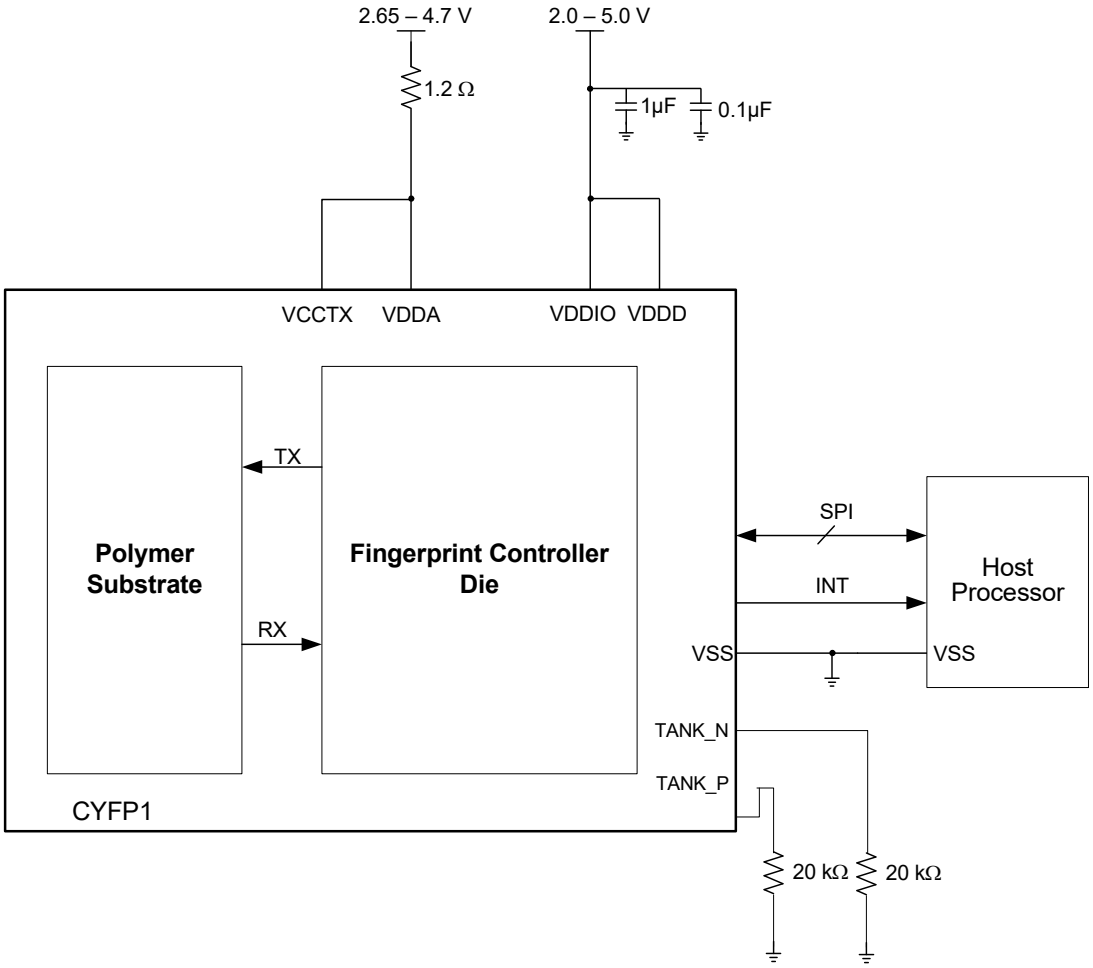
Back of the Sensor

Front of the Sensor

Contents

System Overview

Figure 1. CYFP1 Typical System Diagram



CYFP1 is a fingerprint reader that can read a fingerprint image from the attached polymer substrate, which contains a grid of row and column electrodes. CYFP1 securely transfers the fingerprint image to a host processor for feature extraction and pattern matching against a fingerprint template.

A typical fingerprint system consists of a fingerprint reader mounted on a flexible printed circuit board (FPC). The FPC connects the fingerprint reader to the host processor. Users interact with the system by placing a finger they intend to enroll or verify on the sensor.

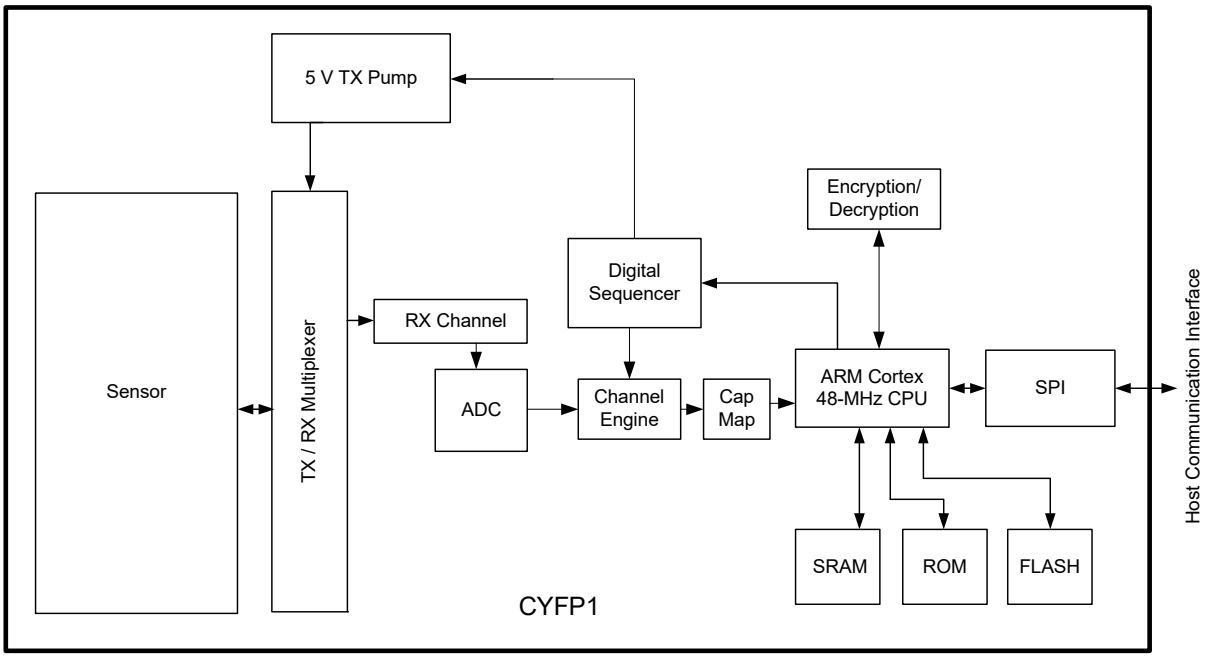
CYFP1 detects the change in capacitance and scans the sensor electrodes creating a capacitive map representing the ridge and valley flow of the specific user. The capacitive map is converted to digital values, encrypted and transferred to the host for creating a template or matching against an existing template.

Functional Overview

Figure 2 shows the CYFP1 block diagram. This device contains a high-performance Arm 32-bit CPU with an integrated hardware multiply unit. This CPU controls all sensing and processing of measured capacitance results to allow creating a fingerprint map from touches detected on the sensor. The controller is optimized for low power and fast response time, with built-in support for manufacturing test. CYFP1 communicates with a host through a slave SPI interface at up to 7.8 Mbps.

CYFP1 scans the sensor information using the fingerprint subsystem. This fingerprint subsystem consists of a 5-V TX pump, TX driver, RX channel, and a transmit/receive (TX/RX) multiplexer. The multiplexer electrically connects the RX channel and TX driver to the appropriate row and column electrodes of the fingerprint sensor.

Figure 2. Functional Block Diagram



Features Overview

- Provides great image quality with polymer coatings, ceramic and, glass cover over sensor:
  - CYFP1 requires a cosmetic cover that conceals and protects the fingerprint sensor. This cover needs to be thick enough to endure impacts, hard enough to survive scratches, yet thin enough to not interfere with imaging performance. CYFP1 employs proprietary technologies to optimize fingerprint image capture and boost SNR.
- Encryption
  - To ensure secure communication between the host and CYFP1, AES-256 encryption and SHA message authentication is included in CYFP1. Encryption is used to securely transfer a fingerprint image to the host processor. Each image is uniquely signed preventing replay attacks. Additionally, for firmware upgrades, signed firmware can be delivered to CYFP1 over an encrypted session.
- Responsive to user inputs
  - CYFP1 response reliably identifies the user quickly after a physical finger touch. This feature is enabled by the wakeup performance, acquisition speed, and biometric performance of the solution. The reader quickly wakes up to touch, acquires and transfers the fingerprint image to the host within 375 milliseconds, and optimizes and tunes the fingerprint software framework to allow the host to identify a user reliably within 225 milliseconds.
- Works with all finger types
  - CYFP1 is capable of dealing with a variety of fingers and variations to fingers due to external conditions. The diversity of finger types, dry and moist fingers, temporary damage to fingers, and other environmental and behavioral conditions are challenges to reliably enroll and match a finger over time. Enrollment and matching algorithms provided with CYFP1 can reliably detect these situations and dynamically update to fingerprint template to track these changes.
- Configurable and secure enrollment schemes
  - Using CYFP1, the end user can enroll reliably and in reasonable time, and with a reasonable number of touches. Enrollment schemes are configurable based on user experience including the level of security desired. The enrolment template is augmented dynamically as new pattern information becomes available during the authentication process.
- Reliable identification
  - CYFP1 strikes a balance between security and convenience for a great end-user experience. Fingerprint matching is performed by a proprietary software algorithm using the feature set extracted from the fingerprint image created during the enrollment process. The matching algorithm browses all the templates created during enrollment until it finds one that matches the required security setting. The fingerprint matching software is provided along with the CYFP1 sensor.
- Common-mode noise rejection
  - CYFP1 employs techniques that strongly suppress common-mode noise. This is especially important in dealing with the charger, LCD, and radio noise that is typical in most mobile devices.

Power Supply Information

CYFP1 power supplies are shown in the following table.

Table 1. CYFP1 Power Supplies

Supply	Function	Range (V)	Operating Mode
VCCD	Core low-voltage logic and analog	1.71–1.95	All
VDDD	Core LDO	1.71–1.95	LDO bypassed
		2.0–5.5	LDO enabled
VDDA	TSS RX, TX pump, and TX driver supply	2.65–5.50	TX pump disabled
		2.65-4.70	TX pump enabled
VCCTX	External VCCTX	2.65–5.50	TX pump disabled
	TX pump reservoir	4.7–5.3	TX pump enabled
VDDIO[1]	XRES and GPIO supply	1.71–5.50	All

Power Configurations

For those power configurations where the TX pump is used, the VCCTX supply in CYFP1 always requires an external reservoir cap. In addition to the primary power options described in the following section, which make use of the TX pump, multiple secondary power options that use a direct VCCTX supply are also available.

All bypass, filter, and reservoir capacitors require an X5R dielectric characteristic or better. While selecting components, ensure that the required resistance and capacitance is present when combined with the associated voltage and temperature coefficients of each component.

All external passives, when mounted to the circuit board, must not exceed the mounted device package thickness.

Primary Power Configurations

All primary power configurations make use of the internal TX pump. In these primary configurations, the digital and FPSS analog elements of CYFP1 may be powered in three base configurations:

- Separate digital and analog supplies, with the digital supply ≥ 2.0 V (core LDO enabled)
- Separate digital and analog supplies, with the digital supply 1.71 V–1.95 V (core LDO bypassed)
- Common (shared) digital and analog supply

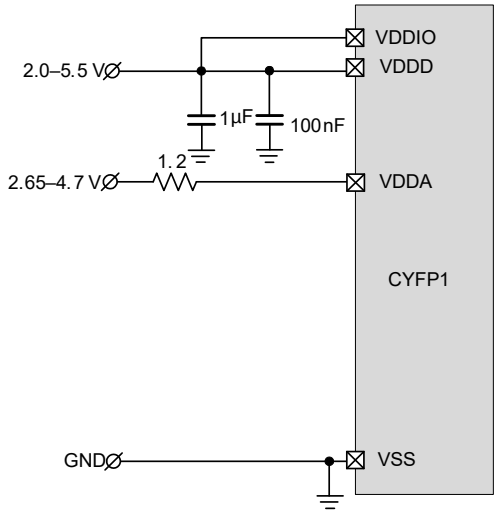
A 1.2-Ω ±5 percent resistor in series with the VDDA supply is used to filter high-frequency noise and limit the slew rate into VDDA. For VDDA supplies with significant noise in the integration passband, the 1-µF low-frequency capacitor can be replaced with a 2.2-µF capacitor. This larger capacitor moves the pole in the LPF around one octave lower, and reduces the VDDA noise in the integration passband by 6 dB.

Note
1. VDDD should be ≥ VDDIO.

Primary - Separate VDDD/VDDA, VDDD ≥ 2.0 V

This configuration should be used for systems requiring communications at voltages other than a nominal 1.8 V. In this configuration, VDDA is powered separately from VDDD, and VDDD provides power to the logic core through an internal LDO. The output of this LDO connects to a filter capacitor attached to the VCCD output. This configuration is shown in Figure 3.

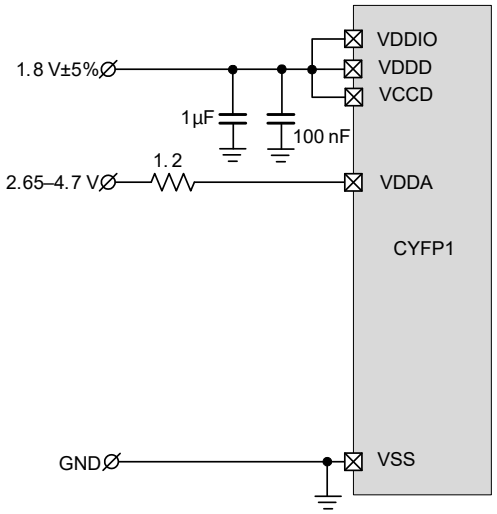
Figure 3. Separate VDDD/VDDA, VDDD ≥ 2.0 V



Primary - Separate VDDD/VDDA, VDDD = 1.8 V±5%

In this configuration, the I/O and logic core operate from the 1.8-V ±5% supply; the core LDO is bypassed. The VCCD pin is an input to the device and provides power to the logic core, while the VDDD supply provides power to the GPIO pins. This configuration is shown in Figure 4.

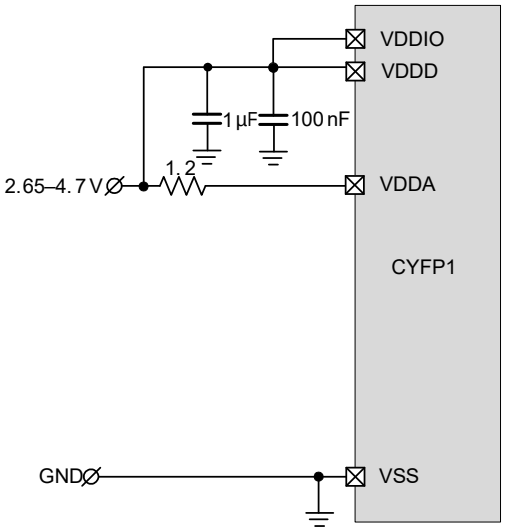
Figure 4. Separate VDDD/VDDA, VDDD = 1.8 V ±5%



Primary - Shared VDDD/VDDA Supply

This configuration allows operation from a single supply. Because the minimum supply for the analog domain is 2.65 V, the digital domain will also be powered from this same supply. In this configuration, the internal logic LDO is enabled, and VCCD is an output. This configuration is shown in Figure 5.

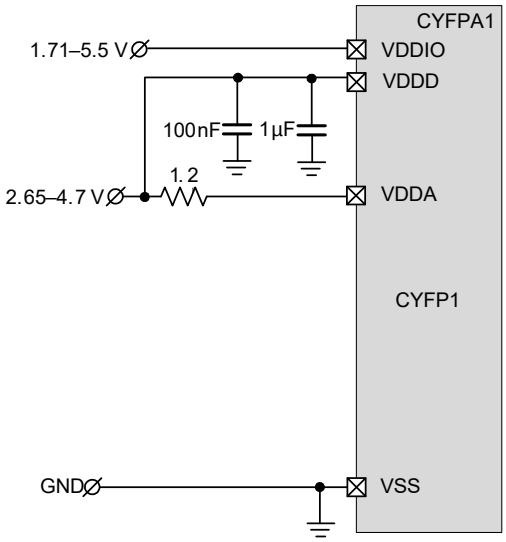
Figure 5. Shared VDDD/VDDA Supply



Primary - Shared VDDD/VDDA Supply, Separate VDDIO Supply

This configuration is an example of a separate VDDIO supply and a shared primary supply for VDDD and VDDA. All the examples described above can use a separate VDDIO supply. This configuration is shown in Figure 6.

Figure 6. Shared VDDD/VDDA Supply, Separate VDDIO Supply



Secondary Power Configurations

All secondary power configurations disable the internal TX pump, and power for the TX drivers is provided through the VCCTX pin. In the secondary configurations, the digital and FPSS analog elements of CYFP1 may be powered in three base configurations:

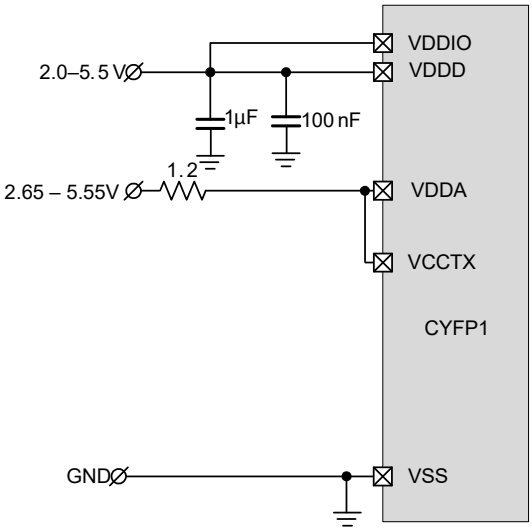
- Separate digital and analog supplies, with the digital supply >2.0 V (core LDO enabled)
- Separate digital and analog supplies, with the digital supply 1.71–1.95 V (core LDO bypassed)
- Common (shared) digital and analog supply

Each of these base configurations support only a shared VDDD/VCCTX supply. Note that the allowed supply voltage ranges for all secondary configurations require VDDA to always be equal to VCCTX.

Secondary - Separate VDDD/VDDA, VDDD ≥ 2.0 V

This configuration is similar to the primary configuration illustrated in Figure 3, but with the TX pump disabled and VCCTX connected externally to VDDA. This configuration is shown in Figure 7.

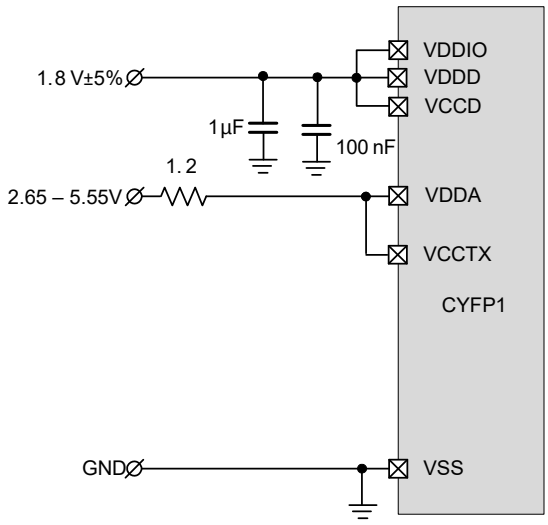
Figure 7. Separate VDDD/VDDA, VDDD ≥ 2.0 V



Secondary - Separate VDDD/VDDA, VDDD = 1.8 V ±5%

This configuration is similar to the primary documented in Figure 4, but with the TX pump disabled and VCCTX connected externally to VDDA. This configuration is shown in Figure 8.

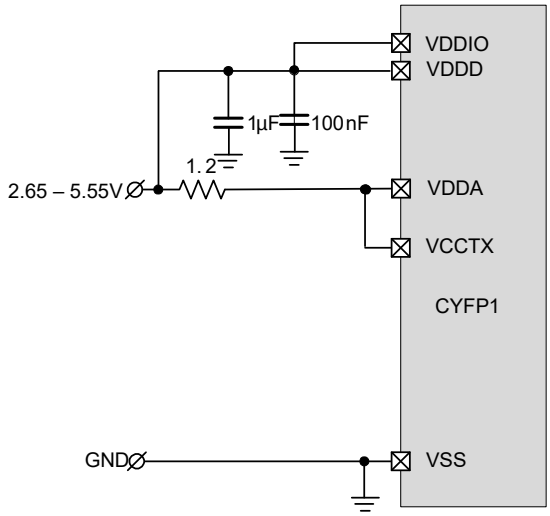
Figure 8. Separate VDDD/VDDA, VDDD = 1.8 V ±5%



Secondary - Shared VDDD/VDDA Supply

This configuration is similar to the primary configuration illustrated in Figure 5, but with the TX pump disabled and VCCTX connected externally to VDDA. This configuration is shown in Figure 9.

Figure 9. Shared VDDD/VDDA/VCCTX Supply



Voltage Coefficient

The actual capacitance of external capacitors may be reduced with higher bias voltage. Check the capacitor datasheet for the voltage coefficient. External capacitors require an X5R dielectric characteristic or better. It is recommended to use an X7R dielectric characteristic or better for high-frequency 0.1-µF capacitors. Capacitors used for power supply decoupling or filtering are operated under a continuous DC bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device, verify that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design.

While the temperature ratings of a capacitor are normally found as part of its catalog part number (for example, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to perform at less than the datasheet specifications.

Table 2. External Components

Component	Number of Components	Suggested Part Number	Usage	Package Ball Number
100 nF X5R 20%	1	C0603X5R1A104K030BC	VDDD decoupling capacitor	U12, V12
1 µF X5R 20%	1	C0603X5R0J105M030BC	VDDD decoupling capacitor	U12, V12
20 kΩ 5% 1/20 W	2	ERJ-1GEJ203C	TANK filtering resistors	V3, V4
1.2 Ω –200/+300 ppm/°C 5%	1	RC0603J1R2CS	VDDA series noise filtering resistor	U13, V13

Power States Summary

Active

In the Active mode, the CPU and other peripherals are functional. In this mode, power varies dynamically as the different sections of the device are enabled for operation.

When active, the CPU controls the power circuits for the RX and TX domains. These may be cycled up or down as needed for sensing. Internal blocks must automatically enter a power-down mode when they are not being used.

Sleep

In the Sleep mode, all device operations remain functional; however, the clock to the M0 CPU is stopped and the CPU waits for an interrupt. Device scanning and communications on the COMM interface may operate with the M0 CPU stopped in this mode. All regulators remain in their last programmed state. Sleep and watchdog timers may be enabled and functional. The communications interface may be configured to transfer data and to wake the device on receipt of a command or data. The CPU may be configured to wake on an external interrupt.

Deep Sleep

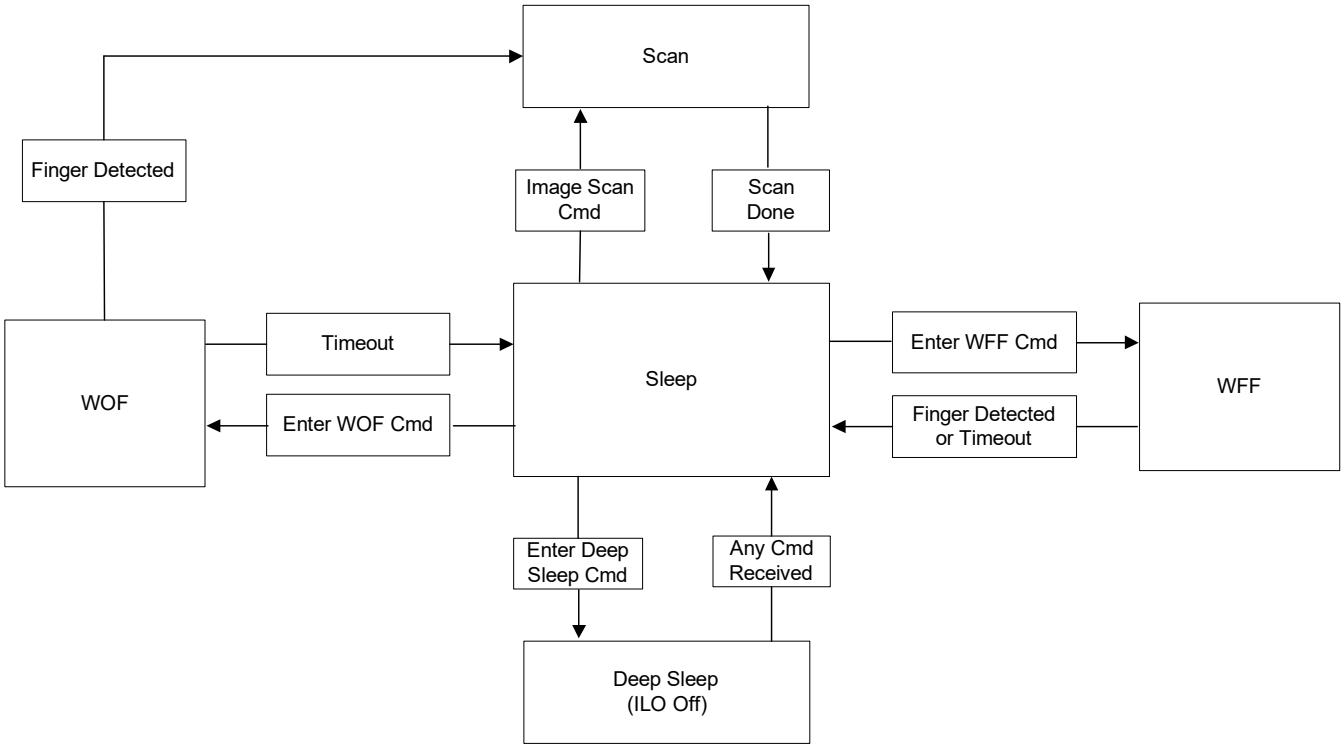
In the Deep Sleep mode, the CPU and IMO are both stopped. The low-speed oscillator (LSO) is active and is used to time the duration of deep-sleep events. The COMM port may remain active, and can wake the device on a host-SPI transaction. The COMM port may both send and receive data in this mode. The sleep/watchdog timers or GPIO may also be used to wake the device from deep sleep.

Wake-On-Finger and Wait-For-Finger

These are low-power modes under which the CYFP1 automatically detects the presence of a finger and triggers a scan. These modes provide the ability to shut down most of the CYFP1 blocks and periodically turn on some of them to check for fingers.

Wait-For-Finger is the lowest power consumption mode available.

Figure 10. Power Mode Transitions



Pin Information

CYFP1 is available in square BGA packages. All pins described in the following table are available on both packages. This section lists pin names, descriptions, and mapping to the physical packages.

■ P0[0:7]: 8-pin port, four SPIs, one INT, and three GPIOs

■ XRES: Reset pin, to be connected to VDDD if not used

Table 3. 8.87 × 9.26 mm Rectangular Sensor and 12.20 × 12.20 mm Square Sensor Pin List

Ball#	Name	Digital	Analog	Description
A2	VSSD	Power		Digital ground
A3	VSSD	Power		Digital ground
A4	VSSD	Power		Digital ground
A5	VSSD	Power		Digital ground
A6	VSSD	Power		Digital ground
A7	VSSD	Power		Digital ground
A8	VSSD	Power		Digital ground
A9	VSSD	Power		Digital ground
A10	VSSD	Power		Digital ground
A11	VSSD	Power		Digital ground
A12	VSSD	Power		Digital ground
A13	VSSD	Power		Digital ground
A14	VSSD	Power		Digital ground
A15	VSSD	Power		Digital ground
C1	VSSD	Power		Digital ground
C17	VSSD	Power		Digital ground
D1	VSSD	Power		Digital ground
D17	VSSD	Power		Digital ground
E1	VSSD	Power		Digital ground
E17	VSSD	Power		Digital ground
F1	VSSD	Power		Digital ground
F17	VSSD	Power		Digital ground
G1	VSSD	Power		Digital ground
G17	VSSD	Power		Digital ground
H1	VSSD	Power		Digital ground
H17	VSSD	Power		Digital ground
J1	VSSD	Power		Digital ground
J17	VSSD	Power		Digital ground
K1	VSSD	Power		Digital ground
K17	VSSD	Power		Digital ground
L1	VSSD	Power		Digital ground
L17	VSSD	Power		Digital ground
M1	VSSD	Power		Digital ground
M17	VSSD	Power		Digital ground

Table 3. 8.87 × 9.26 mm Rectangular Sensor and 12.20 × 12.20 mm Square Sensor Pin List (continued)

Ball#	Name	Digital	Analog	Description
N1	VSSD	Power		Digital ground
N17	VSSD	Power		Digital ground
P1	VSSD	Power		Digital ground
P17	VSSD	Power		Digital ground
R1	VSSD	Power		Digital ground
R17	VSSD	Power		Digital ground
T1	VSSD	Power		Digital ground
T17	VSSD	Power		Digital ground
U1	VSSD	Power		Digital ground
U3	VSSA	Power		Analog ground
U4	VSSA	Power		Analog ground
U5	VSSA	Power		Analog ground
U6	XRES	–		Reset
U7	P01	–		GPIO
U8	P03	–		Interrupt
U9	P05	–		SPI SELECT
U10	P07	–		SPI MOSI
U11	VCCD	Power		Core low-voltage and analog supply
U12	VDDD	Power		Core LDO supply
U13	VDDA	Power		Analog supply
U14	VCCTX	Power		TX pump supply
U15	VSSD	Power		Digital ground
U17	VSSD	Power		Digital ground
V2	VSSA	Power		Analog ground
V3	TANK_P	–		Connect to 20-kΩ resistor
V4	TANK_N	–		Connect to 20-kΩ resistor
V5	VSSA	Power		Analog ground
V6	P00	–		GPIO
V7	P02	–		GPIO
V8	P04	–		SPI MISO
V9	P06	–		SPI clock
V10	N/C	–		No connect
V11	N/C	–		No connect
V12	VDDIO	Power		XRES and GPIO supply
V13	VDDA	Power		Analog supply
V14	VCCTX	Power		TX Pump supply
V15	VSSD	Power		Digital ground
V16	VSSD	Power		Digital ground

■ Connect TANK_P and TANK_N to analog ground through 20-kΩ resistors as specified in the external component list.

Example Schematic and Layout Guidelines

- Sensor VSSD pins (V16, V15, U15) must be connected to the System GND by wide wire trace with minimal resistance.
- Sensor VDDD pins must be connected to the System digital power supply by wide wire trace with minimal resistance.
- Sensor VSSA pins (V2, U3, U4, U5, V5) must be connected to VSSD close to the VSSD pins (V16, V15, U15).
- Sensor pins (C1-K1, M1-U1,L1, L17, C17-K17, M17-U17) must be connected to VSSD pins (V16, V15, U15) close to the VSSD pins. These pins are in place for mechanical stability of the BGA package.
- Sensor pins (A2-A16) must be connected to a copper ring placed around the sensor. An ESD decorative ring of a conductive material must be soldered or glued to the copper ring using conductive adhesive. This net must be connected to the System GND close to VSSD pins (V16, V15, U15) or anywhere else in the system.
- Connect VDDA pin to VCCTX pin for TX pump disabled.
- Connect VDDD pin to VCCD pin in case of 1.8V ±5% digital power supply.
- Keep TANK_P and TANK_N traces to the 20-KΩ resistor as short as possible. A loop from and to VSSA pins (V2, U3, U4, U5, V5) must be placed around the TANK resistors.
- It is not recommended to have noisy lines under the sensor, if not possible use solid plate shield.
- Minimize cross talk from SPI interface into the VDDA net. Do not route VDDA net next to SPI nets.
- A cutout on the PCB under the BGA must be provided to allow the passives on the bottom of the BGA package to protrude through the PCB and for the BGA to be soldered down.

Figure 11. Examples of Flex Schematic

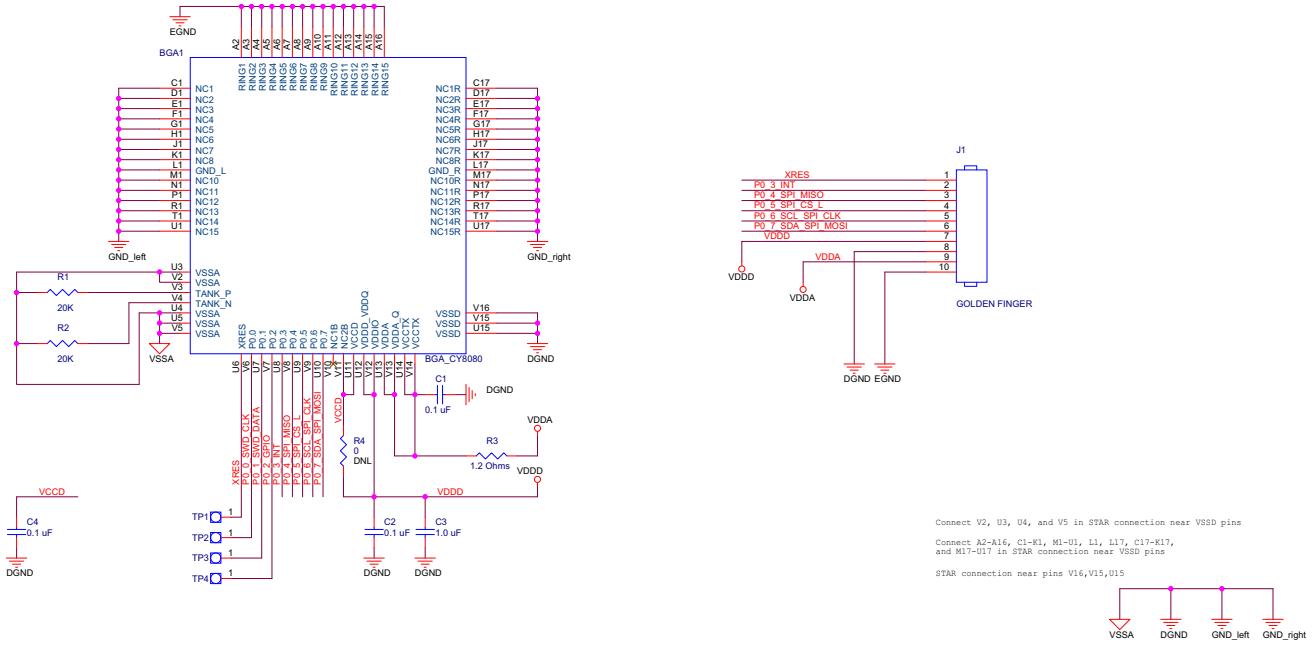


Figure 12. Example Flex Layout

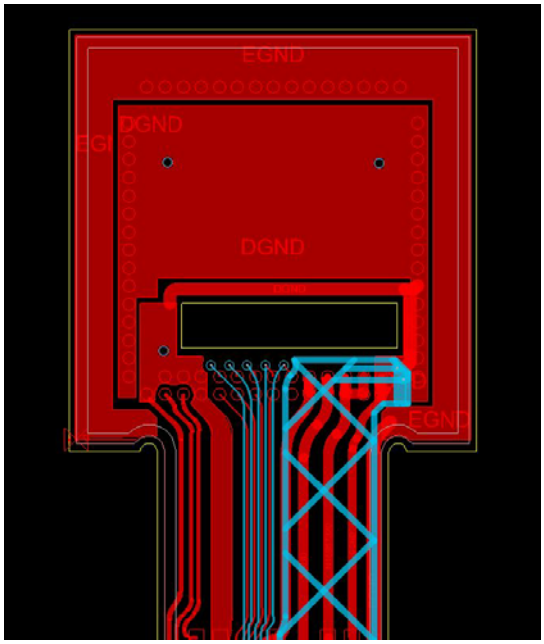


Figure 13. GND Connectivity

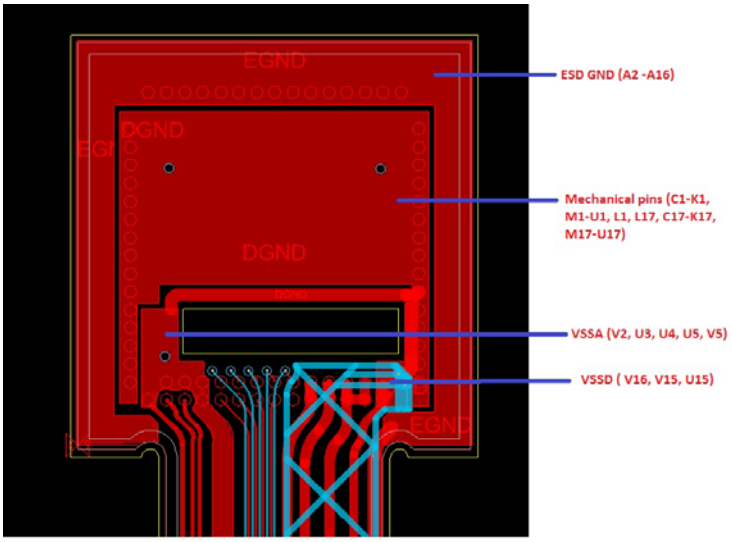


Figure 14. VSSA and TANK Connectivity

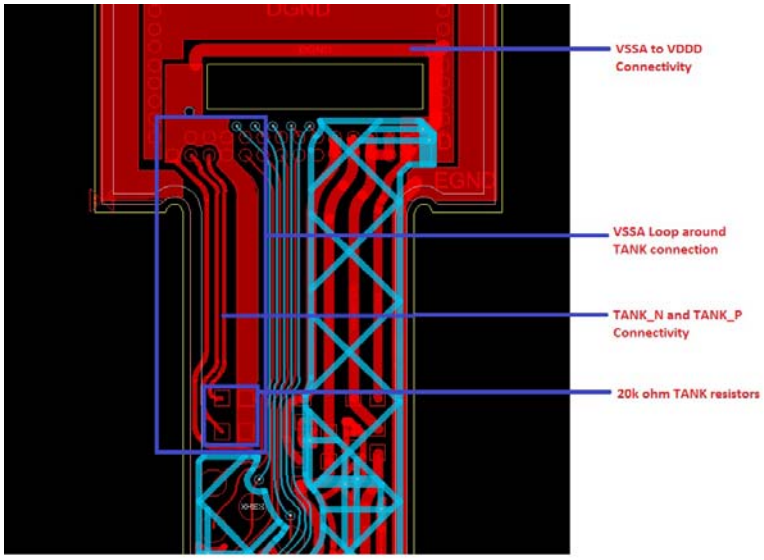
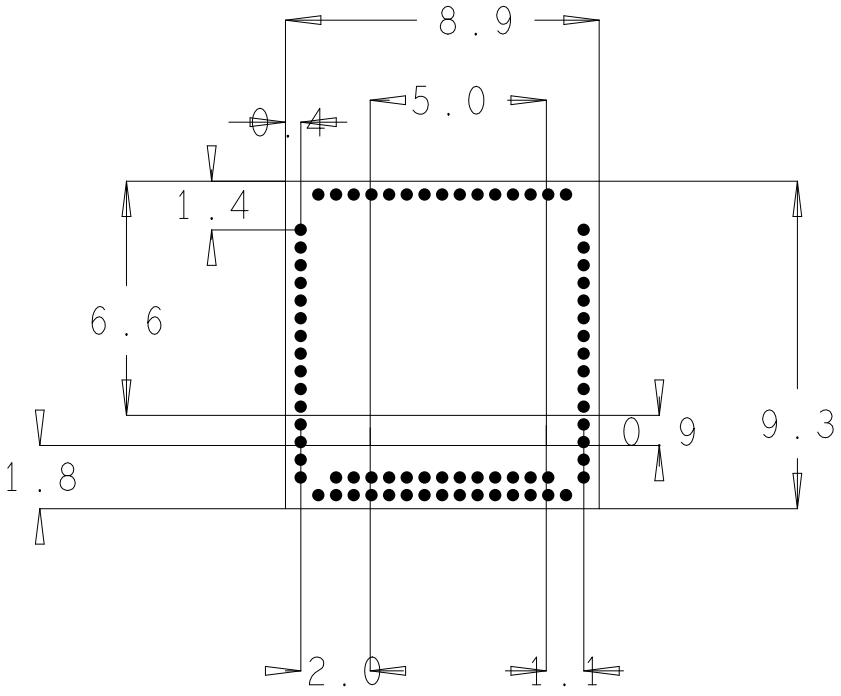


Figure 15. Passive PCB Cutout



Electrical Specifications

Table 4. CYFP1 Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
VDDD_D	Core supply, direct-LDO bypass	–40°C to 85°C T_A, min/max limits are simultaneous conditions with DC and supply noise	1.71	1.80	1.95	V
VDDD_L	Core supply, LDO enabled	–40°C to 85°C T_A	–	–	5.50	V
VDDIO	Digital I/O supply	–40°C to 85°C T_A	1.71	–	5.50	V
VDDA	Analog supply, TX pump disabled	–40°C to 85°C TA, input to the external low-pass filter, output of the filter connected to VDDA/VCCTX pins	2.65	–	5.50	V
VDDA	Analog supply, TX pump enabled	–40°C to 85°C T_A, input to the external low-pass filter	2.65	–	4.70	V
VDDD_AMAX	Core supply	–40°C to 85°C T_A, absolute maximum	–0.50	–	6	V
VDDIO_AMAX	Digital I/O supply	–40°C to 85°C T_A, absolute maximum	–0.50	–	6	V
VCCD_AMAX	Direct digital core voltage input	–40°C to 85°C T_A, absolute maximum	–0.50	–	2.30	V
VDDA_AMAX	Analog supply	–40°C to 85°C T_A, absolute maximum	–0.50	–	6	V
VDDA_XRIP	VDDA external regulator ripple, TX Pump enabled	–40°C to 85°C T_A, DC to 20 MHz, measured at the input to the external LPF	–	–	100	mV pp
VDDD_XRIP_LE	VDDD external regulator ripple, LDO enabled	–40°C to 85°C T_A; VDDD ≥ 2 V, DC to 20 MHz	–	–	100	mV pp
VDDD_XRIP_LB	VDDD external regulator ripple, LDO bypassed	–40°C to 85°C T_A; 1.71 V ≤ VDDD ≤ 1.95 V, DC to 20 MHz	–	–	50	mV pp
VCCTX_XRIP	VCCTX external regulator ripple, TX pump disabled	–40°C to 85°C T_A, DC to 150 kHz, +20 dB/decade for >150 kHz, max of 100 mV up to 20 MHz, measured at the input to the external LPF	–	–	15	mV pp
VCCTX	VCCTX supply operating voltage range	–40°C to 85°C T_A, input to the external low-pass filter, external VCCTX configuration	2.65	–	5.50	V
ESD_{CDM}	Electrostatic discharge voltage	Charge device model	1000	–	–	V
ESD_{HBM}	Electrostatic discharge voltage	Human body model	3000	–	–	V

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature	–	–40	–	85	°C

Flash Specifications

The specifications in Table 6 are valid under these conditions: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{DDD} ≤ 1.95 V or 2.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 2.65 V ≤ V_{DDA} ≤ 4.7 V. Typical values are specified at T_A = 25 °C, V_{DDD} = V_{CCD} = V_{DDIO} = 1.8 V, core LDO bypassed, and V_{DDA} = 2.7 V.

Table 6. Flash Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	10,000	–	–	cycles
$Flash_{DR}$	Flash data retention	Following maximum flash write cycles ($Flash_{ENPB}$), T_A ≤ 55 °C	20[2]	–	–	years
		Following maximum flash write cycles ($Flash_{ENPB}$), T_J ≤ 85 °C	10[2]	–	–	years

Chip-Level DC Specifications

The specifications in Table 7 are valid under these conditions: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{DDD} ≤ 1.95 V or 2.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 2.65 V ≤ V_{DDA} ≤ 4.7 V. Typical values are specified at T_A = 25 °C, V_{DDD} = V_{CCD} = V_{DDIO} = 1.8 V, core LDO bypassed, and V_{DDA} = 2.7 V.

Table 7. Chip-Level DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Digital supply voltage	Core LDO enabled (V_{CCD} output)	2.00	–	5.50	V
		Core LDO bypassed (V_{CCD} input)[4]	1.71	1.80	1.95	V
V_{DDIO}[3]	XRES and GPIO supply		1.71	–	5.50	V
V_{CCD}	Digital core supply voltage	Core LDO enabled (V_{CCD} output)	–	1.80	–	V
		Core LDO bypassed (V_{CCD} input)[4]	1.71	1.80	1.95	V
V_{DDA}[4]	Analog supply voltage	TX pump enabled	2.65	–	4.70	V
PSA_{RAMP}	V_{DDA} ramp up	–	–	–	100	mV/µs
I_{DDD_ACT}	V_{DDD} active current	–	–	15	30	mA
I_{DDA_ACT}	V_{DDA} active current	–	–	11	13	mA
I_{DDD_DS}	V_{DDD} deep sleep current	–	–	3	–	µA
I_{DDA_DS}	V_{DDA} deep sleep current	–	–	1	–	µA
I_{DDD_XR}	V_{DDD} current, $\overline{XRES}$ = LOW	–	–	2	–	µA
I_{DDA_XR}	V_{DDA} current, $\overline{XRES}$ = LOW	–	–	25	–	µA
I_{DDD_P}	V_{DDD} flash programming and flash verify current	–	–	5	25	mA

Notes
2. Storing programmed devices at or above the ambient temperature specified by $Flash_{DR}$ may reduce flash data retention time.
3. V_{DDD} should be ≥ V_{DDIO}.
4. These Min and Max limits are absolute limits, inclusive of noise. For proper operation, V_{DDA} or V_{DDD} with combined noise cannot go below or above the specified Min or Max limits.

I/O Port 0 (P0[0:7]) DC Specifications

The Port 0 specifications in Table 8 are valid under these conditions: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{DDD} ≤ 1.95 V or 2.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 2.65 V ≤ V_{DDA} ≤ 4.7 V. Typical values are specified at T_A = 25 °C, V_{DDD} = V_{CCD} = V_{DDIO} = 1.8 V, core LDO bypassed, and V_{DDA} = 2.7 V.

Table 8. I/O Port 0 (P0[0:7]) DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage	CMOS mode	0.7 × V_{DDIO}	–	–	V
		1.8-V mode, 1.71 V ≤ V_{DDIO} ≤ 5.5 V	1.26	–	–	V
V_{IL}	Input low voltage	CMOS mode	–	–	0.3 × V_{DDIO}	V
		1.8-V mode, 1.71 V ≤ V_{DDIO} ≤ 5.5 V	–	–	0.54	V
V_{OH}	High output voltage	I_{OH} = 1 mA at 1.8-V V_{DDIO}	V_{DDIO} – 0.5	–	–	V
		I_{OH} = 4 mA at 3.0-V V_{DDIO}	V_{DDIO} – 0.6	–	–	V
V_{OL}	Low output voltage	I_{OL} = 8 mA at 3.3-V V_{DDIO}	–	–	0.6	V
		I_{OL} = 4 mA at 1.8-V V_{DDIO}	–	–	0.6	
V_H	Input hysteresis	T_A = –40 °C to 85 °C	0.1 × V_{DDIO}	–	–	V
I_{IL}[5]	Input leakage current (absolute value)	T_A = 25 °C, V_{DDIO} = 3.0 V	–	–	14	nA
		T_A = 25 °C, V_{DDIO} = 0.0 V	–	–	10	µA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25 °C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25 °C	–	–	7	pF
R_{INT}[6]	Internal pull-up/pull-down resistance	Pin configured for internal pull-up or pull-down	3.5	5.6	8.5	kΩ

Chip-Level AC Specifications

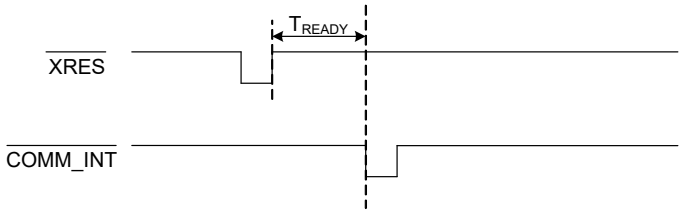
The specifications in Table 9 are valid under these conditions: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 2.65 V ≤ V_{DDA} ≤ 4.7 V. Typical values are specified at T_A = 25 °C, V_{DDD} = V_{DDIO} = V_{CCD} = 1.8 V, core LDO bypassed, and V_{DDA} = 2.7 V.

Table 9. Chip-Level AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{XRST}	External reset ($\overline{XRES}$) pulse width	After V_{DDD} is valid	10	–	–	µs
T_{READY}	Time from deassertion of $\overline{XRES}$ to COMM_INT	–	–	–	10	ms
T_{RISE_OV}	Output rise time Fast-Strong	25-pF load, 10%–90% V_{DDIO} = 3.3 V	2	–	12	ns
	Output rise time Slow-Strong	25-pF load, 10%–90% V_{DDIO} = 3.3 V	10	–	60	ns
T_{FALL_OV}	Output fall time Fast-Strong	25-pF load, 10%–90% V_{DDIO} = 3.3 V	2	–	12	ns
	Output fall time Slow-Strong	25-pF load, 10%–90% V_{DDIO} = 3.3 V	10	–	60	ns

Notes
5. Gang tested with all I/Os to 1 µA.
6. $\overline{XRES}$ is input only with no internal pull-up or pull-down resistor.

Figure 16. COMM_INT Timing Diagram



SPI Specifications

The specifications listed in Table 10 are valid under these conditions: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, 2.65 V ≤ V_{DDA} ≤ 4.7 V, and C_{LOAD} = 25 pF. Typical values are specified at T_A = 25 °C, V_{DDD} = V_{CCD} = 1.8 V, core LDO bypassed, and V_{DDA} = 2.7 V.

Figure 17. SPI Timing Diagram

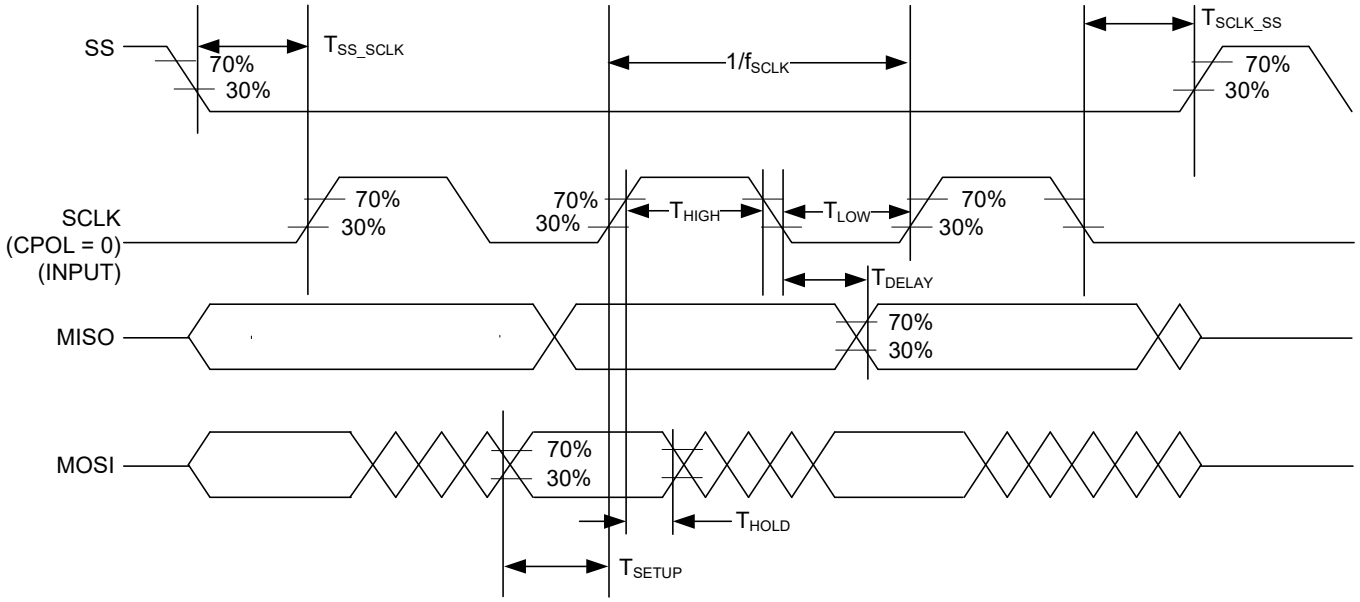


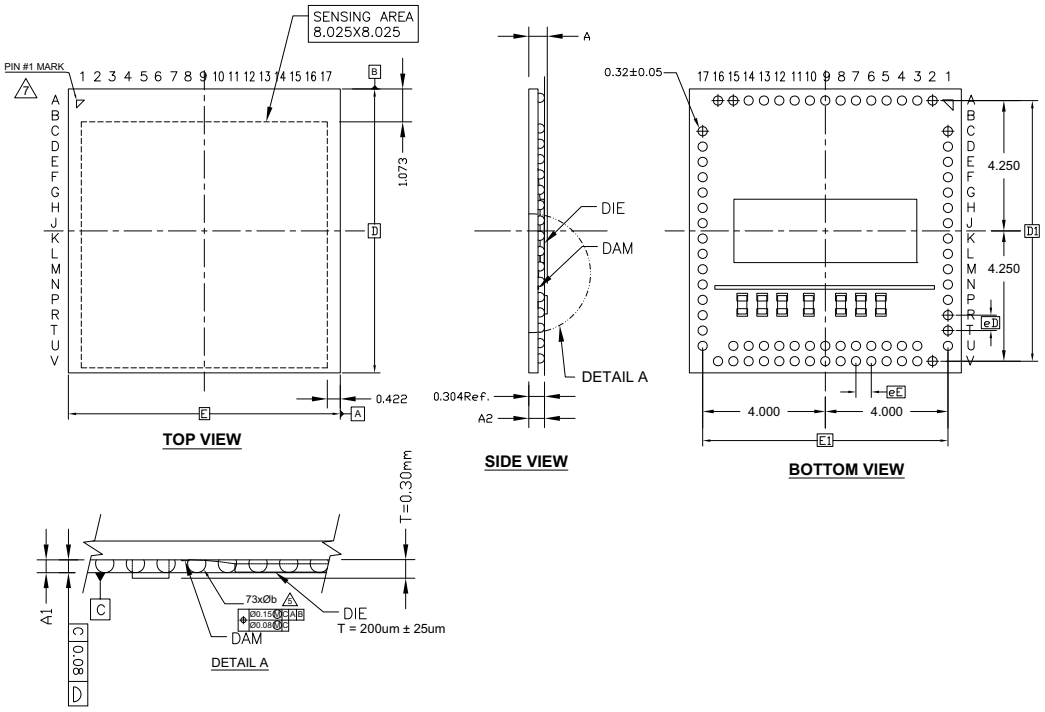
Table 10. AC Characteristics of the SPI Pins

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{SCLK}	SCLK clock frequency	–	–	–	8	MHz
$1/f_{SCLK}$	SPI SCLK cycle time (period)	–	125	–	–	ns
SDR_{SPI}	Sustained data rate for SPI transaction	–	–	–	8	Mbps
$T_{IDLESPI}$	Time between consecutive SPI transactions (duration between SS deactivation and the following SS activation)	–	125	–	–	ns
T_{LOW}	SCLK LOW time	–	50	–	–	ns
T_{HIGH}	SCLK HIGH time	–	50	–	–	ns
T_{SETUP}	MOSI setup to SCLK	–	30	–	–	ns
T_{HOLD}	MOSI hold from SCLK	–	30	–	–	ns
T_{DELAY}	MISO delay (hold) high voltage	$V_{DDIO} \geq 3$ V	0	–	45	ns
	MISO delay (hold) low voltage	$V_{DDIO} < 3$ V	0	–	65	ns
T_{SS_SCLK}	Time from SS LOW to first SCLK	–	125	–	–	ns
T_{SCLK_SS}	Time from last SCLK to SS HIGH	–	125	–	–	ns

Packaging Information

This section provides the CYFP1 device packaging specifications.

Figure 18. 73-Ball BGA 8.87 × 9.26 × 0.70 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.70
A1	0.16	-	0.26
A2	0.414	0.514	0.614
D	9.26 BSC		
E	8.87 BSC		
D1	8.50 BSC		
E1	8.00 BSC		
MD	17		
ME	17		
N	73		
∅ b	0.27	-	0.37
eD	0.50 BSC		
eE	0.50 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

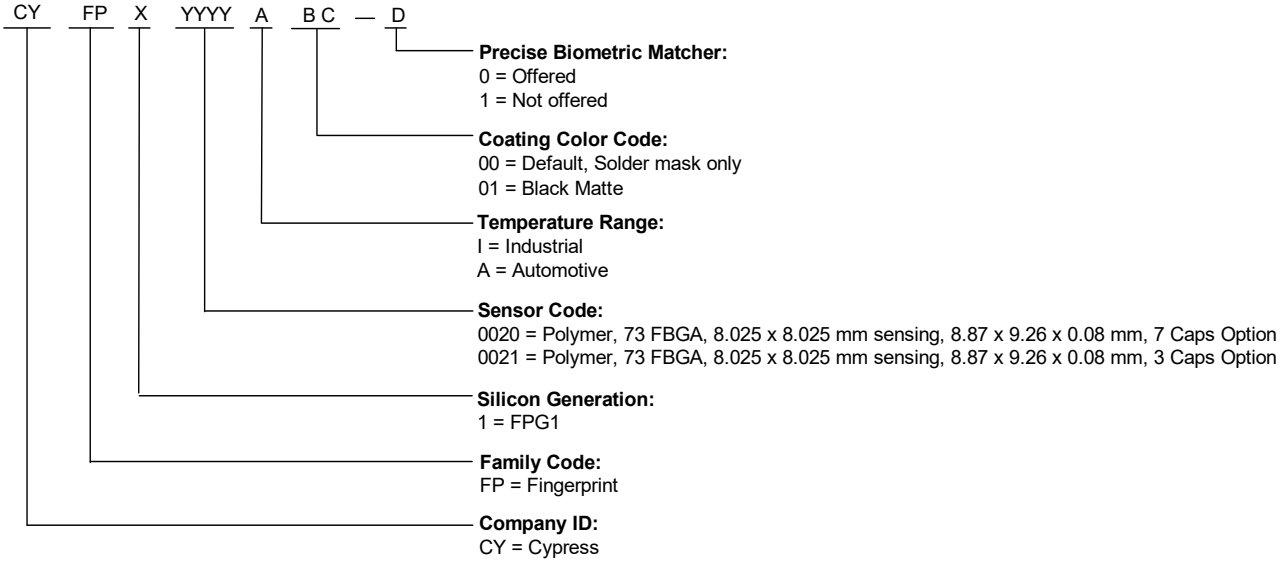
002-10940 *G

Ordering Information

Table 11. CYFP1 Device Key Features and Ordering Information

Silicon Type	Package Type	Package Size	Operating Temperature
CYFP10020I00	73-Ball BGA	8.87 × 9.26 × 0.80 mm	Industrial
CYFP10020I01			
CYFP10020I01-1			
CYFP10021I00		12.20 × 12.20 × 0.80 mm	
CYFP10021I01		8.87 × 9.26 × 0.80 mm	
CYFP10021I01-1			

Part Ordering Code Definitions



All devices in the CYFP1 family comply with the RoHS-6 specifications, demonstrating Cypress's commitment to Pb-free products. Lead (Pb) is an alloying element in solders, which has resulted in environmental concerns due to potential toxicity. Cypress uses the nickel-palladium-gold (NiPdAu) technology for a majority of the lead frame-based packages.

A high-level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other "end-of-life" requirements.

Acronyms and Abbreviations

Table 12. Acronyms Used in this Document

Acronym	Description
AES	Advanced Encryption Standard
CPU	central processing unit
Cu	copper
DNU	do not use
I/O	input/output
LDO	low dropout regulator
MTK	manufacturing test kit
SHA	Secure Hash Algorithm
SNR	signal-to-noise ratio
SPI	serial peripheral interface

Document Conventions

Units of Measure

Table 13. Units of Measure

Symbol	Unit of Measure
°C	degrees celsius
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µW	microwatt
Ω	ohm
Hz	hertz
kΩ	kilo-ohm
kbps	kilobits per second
kHz	kilohertz
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
Mbps	megabits per second
MHz	megahertz
nA	nanoampere
ns	nanosecond
pF	picofarad
s	second

Port Nomenclature

Px[y] describes a particular bit “y” available within an I/O port “x.” For example, P4[2] reads “port 4, bit 2."

Px[y:z] describes a particular range of bits “y to z” within an I/O port named “Px.” For example, P4[0:5] refers to bits 0 through 5 within an I/O port named P4.

Glossary

core LDO	Low drop out regulator that sources power to the digital core when enabled. Input to the LDO is VDDD. Output of the LDO is connected to the digital supply pin VCCD. When the core LDO is bypassed, power must be externally applied to the digital core supply pin, VCCD.
RX	Receive. A touchscreen electrode or touchscreen controller sense pin, mapped or switched to a charge-sensing circuit within the controller (known as a receive channel).
scan	The conversion of all sensor capacitances to digital values.
signal-to-noise ratio (SNR)	The ratio between a capacitive finger signal and system noise.
TEE	Trusted execution environment
TX	Transmit. A touchscreen electrode or touchscreen controller sense pin, mapped or switched to a charge-forcing circuit within the controller. This charge-forcing circuit drives a periodic waveform onto one or more touchscreen electrodes, which are coupled through mutual capacitance to adjacent receive electrodes.

Document History Page

Document Title: CYFP1002XXXX, CYFP1-8080 Datasheet Document Number: 002-11233				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5142522	HFO	02/18/2016	New datasheet.
*A	5359069	HFO	08/19/2016	Added CYFP1002XXXX to the title. Updated Features. Added board image on page 1. Updated Figure 1. Added Features Overview. Updated Table 1 and Table 2. Updated Figure 10. Updated Pin Information. Updated Example Schematic and Layout Guidelines. Added V_{DDIO} spec in Table 6. Updated Part Ordering Code Definitions.
*B	5523251	HFO	11/16/2016	Updated Copyright and Disclaimer. Updated Features and Ordering Information. Updated Example Schematic and Layout Guidelines. Added Figure 12 through Figure 15.
*C	5975003	RLIT	11/23/2017	Updated template Updated package drawing (002-10940)
*D	6288118	PMAD	08/22/2018	Updated template. Updated Features, Packaging Information, and Ordering Information.

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