1.3 Megapixel CMOS Sensor

Features

- 1.3-megapixel resolution (1297H x 1041V)
- 2.8µ x 2.8µ pixel size
- 1/4” optical format image sensor
- Progressive scan
- On-board readout sequencer
- Up to 17 frames per second at full resolution
- Fast preview/snapshot switching with dynamic power management
- Bidirectional serial command interface
- 10-bit parallel data port
- Low-power high frame rate preview mode
- Programmable frame size/rate, gain, exposure, blanking, left-right and up-down image reversal, windowing, auto black level offset correction, and panning

Applications

- Cellular phone camera modules
- Pocket PCs
- PDAs
- Toys
- Battery operated device

Table 0-1. Key Performance Parameters

Parameter	Typical Value
Pixel size	2.8µ x 2.8µ
Array format	1297H x 1041V
Imaging area	3.6 mm x 2.9 mm
Color filter array	RGB Bayer
Optical format	1/4 inch
Frame rate	15 fps @ 1280H x 1024V 60 fps @ 640H x 480V
Scan mode	Progressive
Sensitivity	TBA
Dynamic range	TBA
Shutter type	Electronic rolling shutter
ADC	10-bit
Programmable controls	Frame size, frame rate, gain, exposure, black, offset correction, all directions image flipping
Flash support	LED and Xenon
Pixel rate	24 Mps @ 24-MHz clock
Input clock range	4–27 MHz
Exposure time range	64 µs–66 ms
On-chip voltage regulator	2.65–3.1V / 1.8V
Supply voltage	Analog: 2.6–3.1V Digital: 1.7–1.9V or 2.65–3.1V IO: 1.7–3.1V
Power consumption	TBA
Operating temperature	–20 to +70°C
Package	TBA

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1.0 General Description

Cypress Semiconductor Corporation's (Cypress's) CYIWOSC1300AA is a 1.3-megapixel (SXGA) CMOS digital image sensor. It has a 1/4-inch active-pixel format, with an active imaging pixel array of 1297x1041 pixels and on-board readout sequencer. The device captures Bayer-pattern color still pictures, and offers a low-power video preview mode. Defective pixels are interpolated instantaneously to make them invisible in the output image.

Most of the chip's image readout parameters are doubled-up into two separate records, allowing the user to change from preview mode to snapshot and back in a minimum of time.

The imager also integrates features like programmable gain/exposure control and black level calibration. The sensor equips cameras with a frame rate of up to 15 fps at full resolution and image windowing to any size, while sustaining smooth, continuous video preview at reduced power consumption. The CMOS technology has the advantage of having a smaller form factor, lower power consumption, lower cost and ease of design compared to CCD.

The 1.3-Mp sensor operates in a system accepting commands from a bidirectional serial interface and deliver raw single images or video-like streams of raw Bayer-patterned images through a 10-bit parallel data interface. The low-power viewfinder mode enhances the support for battery-operated platforms. Automatic flash sequencing and single-supply operation provides reduced complexity of the camera system. The device runs off an external clock, ideally in the range of 20 to 27 MHz.

This sensor has no micro-lenses and yet can achieve a 70% fillfactor ratio, using Cypress proprietary process technology. It helps increase process yield and lower system cost.

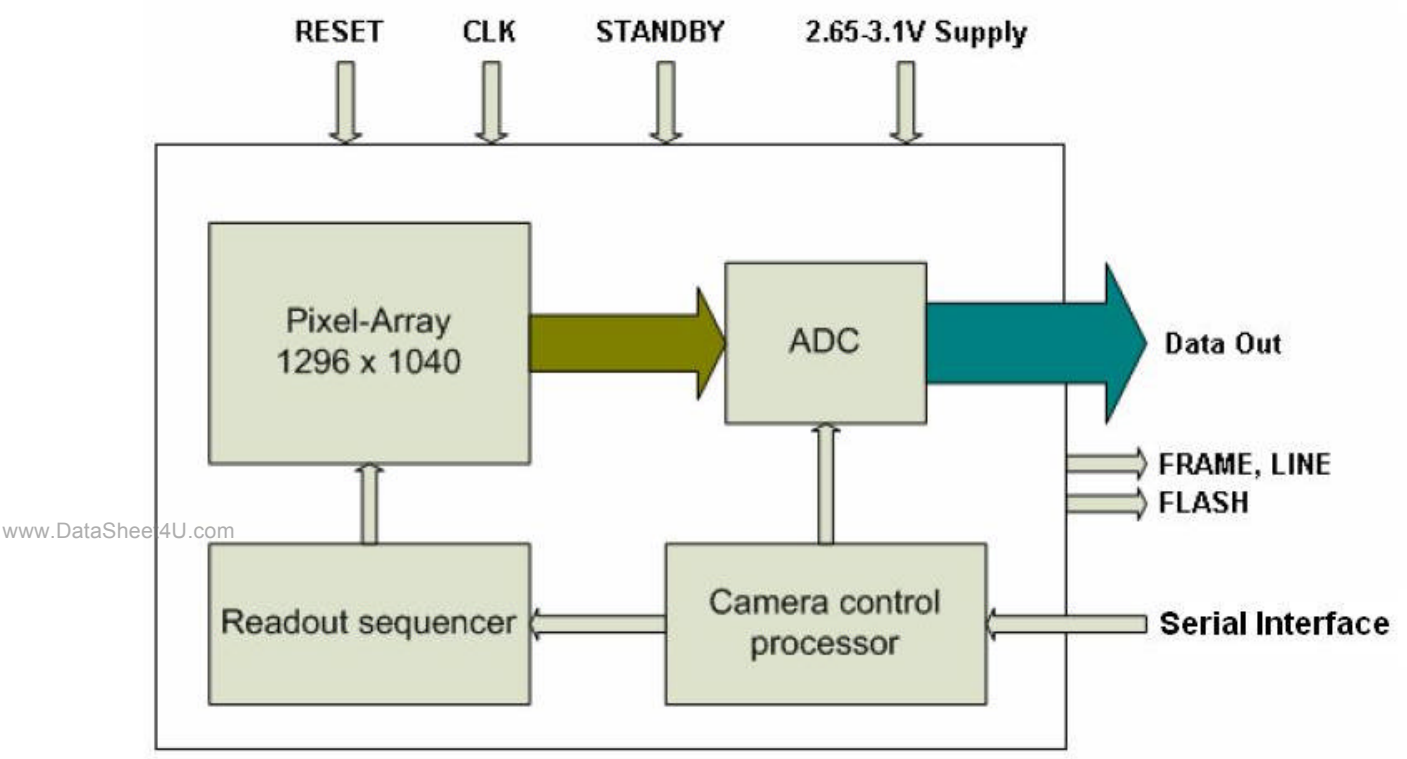

Figure 1-1. Block Diagram

2.0 Functional Overview

The analog core of the chip is comprised of the actual image sensor with its column amplifiers and addressing logic, and an analog processing block with a Programmable Gain Amplifier (PGA), and a 10-bit ADC. The column amplifiers perform double sampling on the pixel signals, thus reducing fixed pattern noise due to pixel non-uniformity.

The output of the column amplifiers is a single analog signal stream of Bayer-colored pixels, which is sent to the PGA for additional gain and offset conditioning. The single ADC accepts this stream and turns it into a 10-bit digitized stream of Bayer-colored pixel values.

The readout sequencer performs automated readout of images with given exposure time and gain settings. Mirrored readout and frame time adjustments are programmable.

Most of the chip's image readout parameters are doubled-up into two separate records, allowing the user to change from preview mode to snapshot and back in a minimum of time.

The output from the sensor is a Bayer pattern: alternate rows are a sequence of either green/red pixels or blue/green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

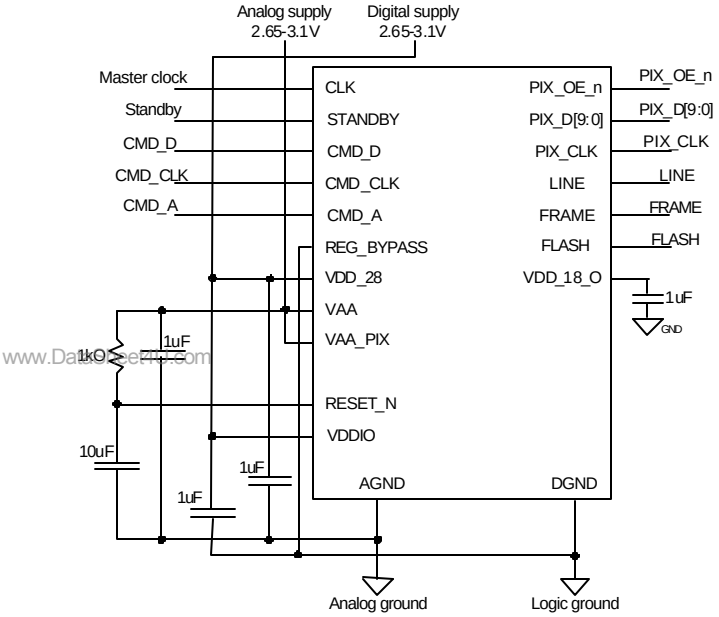

Figure 2-1. Typical Configuration using On-chip Regulator

Figure2-1 shows a typical module wiring diagram. When using the on-chip regulator REG_BYPASS has to be connected to ground. VDD_28 can be connected to a 2.65–3.1V supply like all other power supplies. There must be sufficient decoupling on the supplies to insure clean supply voltages. Note that RESET_N is typically connected with an RC circuit to hold RESET_N low until all power supplies have reached their proper level.

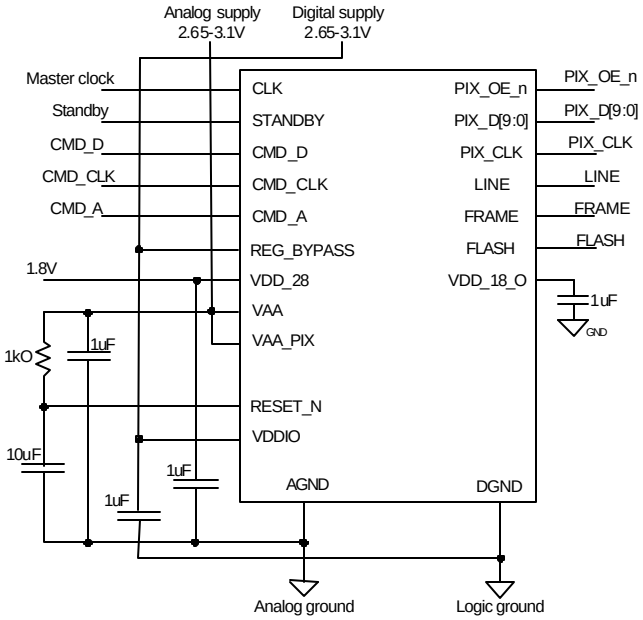

Figure 2-2. Typical Configuration without On-chip Regulator

Figure2-2 shows a typical module wiring diagram. When not using the on-chip regulator REG_BYPASS and the VDD_28 have to be connected to their appropriate levels. VDD_28 has to be connected to a 1.8V supply. There must be sufficient decoupling on the supplies to insure clean supply voltages. Note that RESET_N is typically connected with an RC circuit to hold RESET_N low until all power supplies have reached their proper level.

3.0 Signal Description

Signal Name	I/O	#Pins	Function
CLK	I	1	System clock, 4 .. 27 MHz
RESET_n	I	1	Asynchronous reset
STANDBY	I	1	Turns off device
CMD_D	I/O	1	Interface serial data in and out
CMD_CLK	I	1	Interface bit clock, up to 400 kHz
CMD_A	I	1	Interface device address selector
PIX_OE_n	I	1	Output enable for PIX_D, PIX_CLK, FRAME, LINE, EXT, FLASH
PIX_D[9:0]	O/Z	10	Output pixel data
PIX_CLK	O/Z	1	Output pixel data word clock
EXT[1:0]	O/Z	2	Extension port for debug
FRAME	O/Z	1	Frame valid strobe
LINE	O/Z	1	Line valid strobe
FLASH	O/Z	1	Flash strobe
VAA	PWR	2	Sensor core/ADC analog supply (2.65–3.1V)
VAA_PIX	PWR	1	Pixel array supply (2.65–3.1V)
AGND	GND	3	Sensor core/ADC analog ground
VAA_DIG	PWR	1	Sensor core digital supply (2.65–3.1V)
AGND_DIG	GND	1	Sensor core/ADC digital ground
VDD_28	PWR	1	Raw logic supply in; connect to 2.65–3.1V when regulator is used, otherwise to 1.7–1.9V
DGND	GND	2	Logic ground
REG_BYPASS	I	1	Puts regulator in bypass, use only when VDD_28 = 1.8V
VDD_18_O	PWR	2	Regulated 1.8V logic supply out; connect to bypass capacitor only (two pads, for bonding to one package pin)
VDDIO	PWR	3	IO supply (1.7–3.1V)
DGNDIO	GND	3	IO ground
RESET_OUT	O	1	Internal reset net out (POR test only)

4.0 Pixel Array Structure

The sensor device is a camera on a CMOS chip imager with 1.3-megapixel resolution (SXGA) in a 1/4" optical format.

Figure4-1 below shows the layout of the Pixel Array. The pixel plane consists of a total of 1041 lines, numbered 0 to 1040, each of 1297 pixels, numbered 0 to 1296. All lines are sensitive to light and pixels are optically active and addressable. All pixels can be addressed for readout. A border of width 8 at the periphery of the array, the overscan area, will be used only for image processing boundary conditioning, while the central 1281x1025 area can be output to the end-user. The number of lines and pixels is odd to assure invariance of color pattern when mirrored readout is used.

The sensor is designed with a mosaic of color filters arranged in a standard Bayer pattern shown in *Figure4-1*. The even numbered columns contain green and red pixels and the even rows contain red and green pixels. The imager will output either all Bayer patterned pixels or all physical pixels based upon register settings.

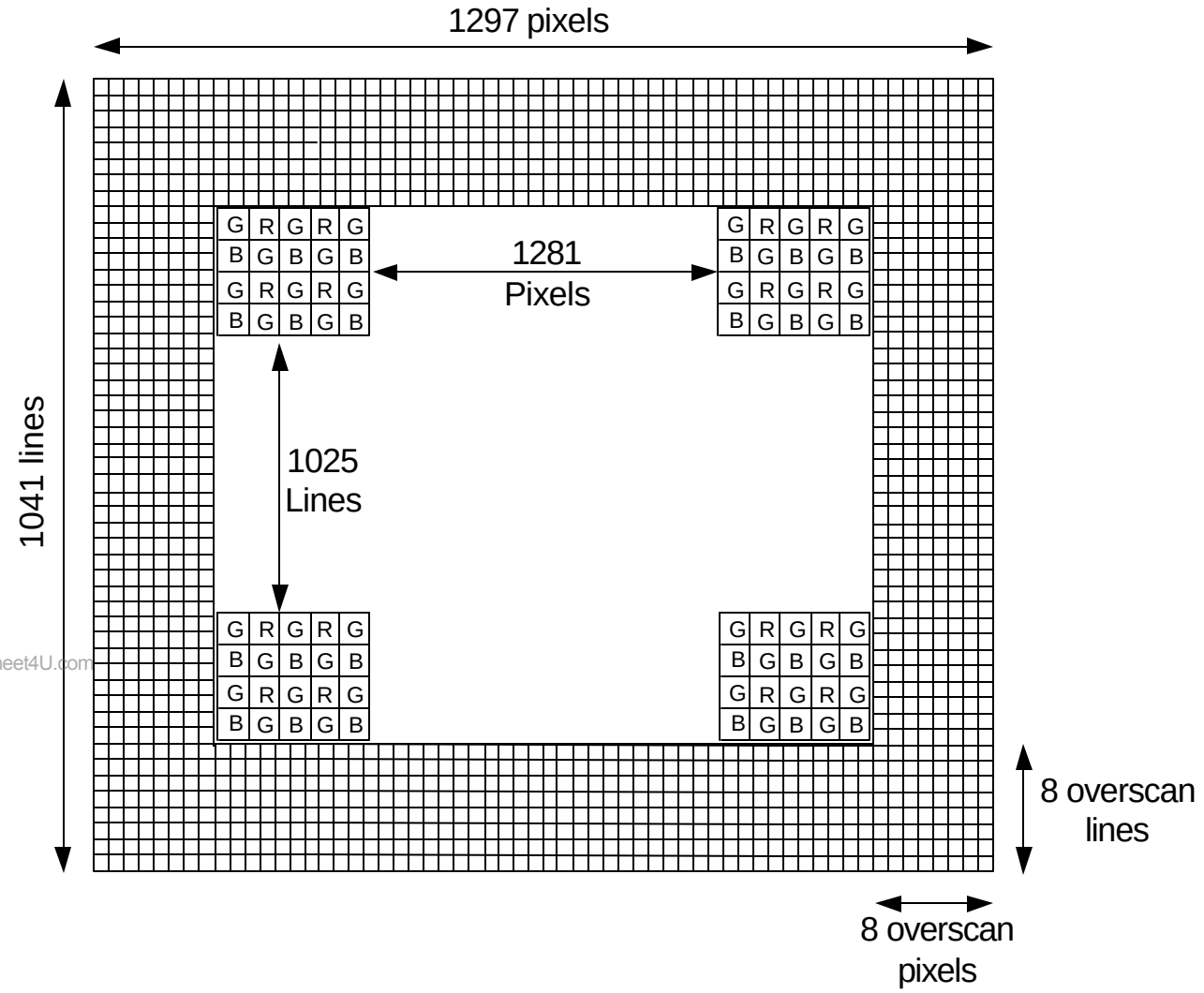

Figure 4-1. Pixel Array

5.0 Typical Use Scenario

The following describes a typical scenario of camera usage.

The camera starts in a viewfinder mode, displaying images at video rate (15 to 30 frames/s) on the mobile application LCD. As LCDs are typically of low resolution and low accuracy, the sensor can be run at a smaller image size and a lower image quality. This then allows power consumption to be reduced. This is relevant in a battery-powered application, as most users will run their cameras in viewfinder/preview mode for 99% of the camera-on time. When the end-user then wants to take a picture and store it in the camera's memory, he pushes the shutter release button. This action is communicated to the application processor, which then sends a stream of commands to the sensor chip.

These commands cause the sensor chip to:

1. Stop the present image acquisition
2. If the present image was an incomplete acquisition, eliminate any effect its data might have on the ISP (red frame in the figure).
3. Reconfigure itself for high-quality, high-power, full-frame image capture.
4. Capture a short sequence of images, one or more of them to be written by the application processor into cellphone memory
5. When finished, await a new command to re-enter the preview mode.

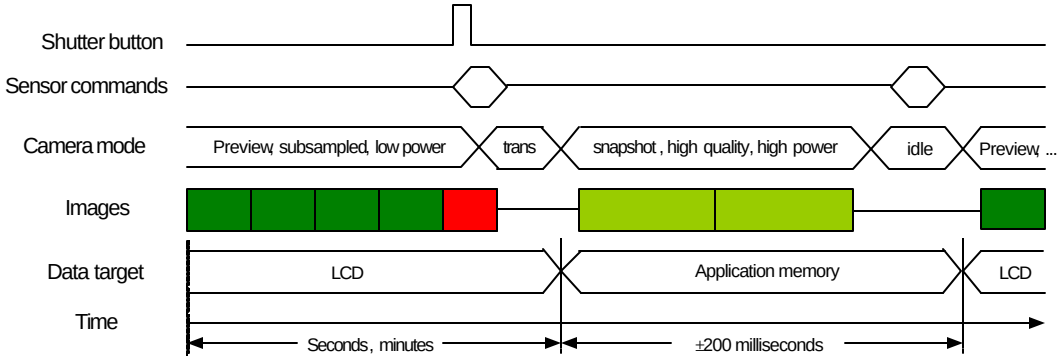

Figure 5-1. Typical Usage

6.0 Data Read Out

The imager is read out in a progressive scan fashion. This means that each successive row is read out in an increasing row number. The data are digitized via on-chip A/D converters and the output resolution is at a 10-bit resolution.

All of the lines are scanned at the same speed, all of them being scanned in the line time. The frame rate is the inverse of the total sum of line times, and the maximum exposure time is the total sum of line times.

The resolution is set by three factors. The resolution may be decreased by sub-windowing a smaller region of interest (ROI) as set in the internal registers. The imager can also be programmed to sub-sample the array to read out as much as at a 4-time rate. In 4x4 subsampling mode both lines and pixels are read in a 1:1:0:0:0:0:0:0 pattern (read-2-skip-6). This quarters the number of lines in a frame, as well as the number of pixels in a line. Also a 2x2 subsampling mode is user programmable. Finally, the imager can be programmed to bin (combine) adjacent pixels of similar color in one direction with strength of2.

6.1 Frame Timing

Figure6-1 shows a regular frame readout sequence with accompanying strobe signals. The FRAME and LINE strobe signals depend on the LN_FORM and FR_FORM register settings. We assume here that they are both set to 1. The FRAME pulse is asserted at the start of the first line that is physically read from the pixel array. This and the following lines are typically overscan lines used for preconditioning processing pipelines. These overscan areas are defined by the physical pixel area as shown in *Figure6-1*. FRAME is not asserted whenever the present image is blanked out (see *_BLANK_FIRST and *_BLANK_PERIOD). LINE is asserted to qualify those lines that belong to the ROI, and is asserted at the first pixel in the ROI of each such line. LINE is deasserted at the last pixel belonging to the ROI. FRAME is deasserted at the last line and last pixel of the overscan area, or the lower-right edge of the physically-scanned area.

As can be seen from *Figure6-1* it is possible to set a number of dummy lines/pixels. These pixels will follow the same readout rate as the pixels in the ROI but will fall outside the Line/FRAME pulses. Therefore they should be discarded by the camera system. The number of dummy lines/pixels is programmable to set integration times longer than the ROI readout time and to give the accompanying peripheral devices (e.g., ISP) time to process the image data. The minimum amount of dummy pixels/lines should be a multiple of 8. Using the appropriate registers the number of overscan pixels (physical pixels) is also programmable for image processing boundary conditioning.

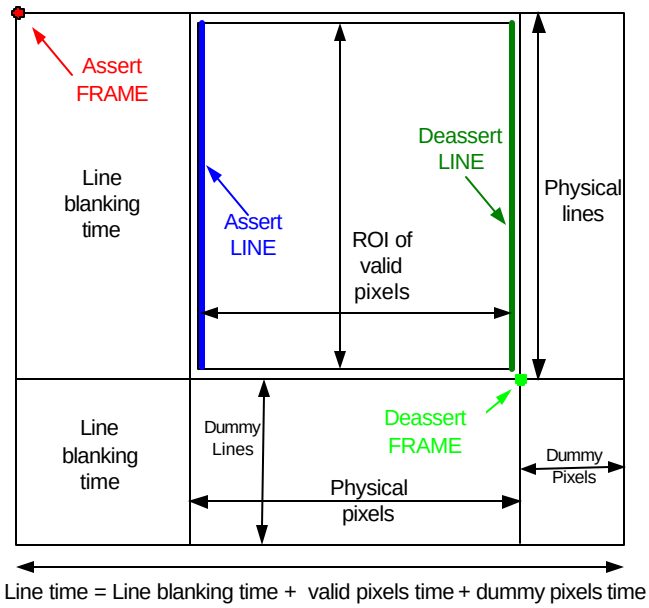

Figure 6-1. Regular Frame Readout Sequence with Accompanying Signals

Figure6-2 indicates the timing of the FRAME and LINE synchronization signals relative to the datastream on the PIX_D bus.

Figure6-3 depicts the horizontal/pixel timing on the parallel data interface.

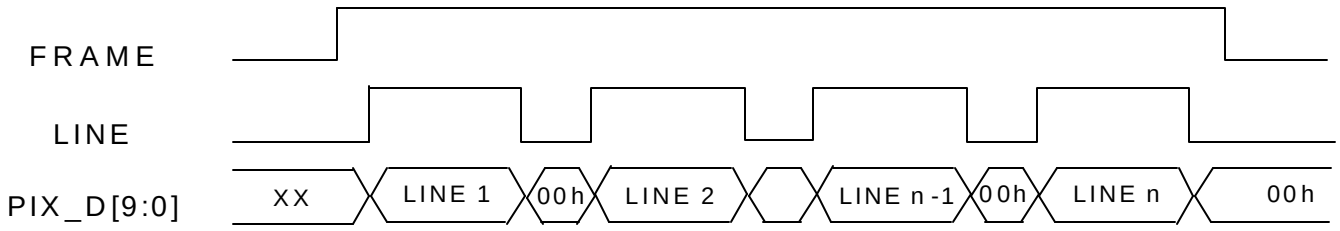

Figure 6-2. FRAME and LINE Timing

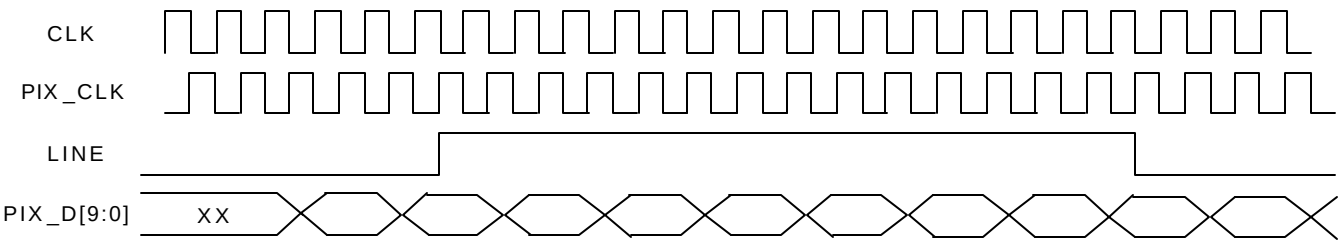

Figure 6-3. Horizontal Timing with PIX_CLK the Inverse of the Internal Chip Clock CLK

PIX_D bytes change state on a falling edge of PIX_CLK, and are to be sampled on the rising edge, or vice versa, as programmed by the user.

PIX_CLK is active for all physically scanned pixels (also for dummy pixels) and is inactive during line blanking intervals.

PIX_CLK is a gated and possibly inverted copy of the internal chip clock. In normal operation the internal clock is equal to the system clock CLK, but in low-power operation the internal clock, and thus PIX_CLK, can be divided by 2 or 4.

6.2 Frame Sequence Structure

6.2.1 Overview

The acquisition of a number of frames is an operation that is started by the CCP (camera control processor), following which the sequencer first initializes the sequence, then takes the frames in a regular, periodic fashion, and (when needed) terminates the sequence. The frame sequence itself can be adorned by optional attributes such as blanking out of a specific number of frames, blanking out of bad frames, Xenon flash ignition between two frames, etc.

Within the sequence of frames will be specific synchronization points for updating image-sensitive parameters such as exposure time and gain, without disrupting the frame sequence itself.

6.2.2 Frame Timelines Examples

The following timelines indicate a number of possible scenarios. The lower/orange band in each diagram houses the periods during which the lines of a frame are reset (top to bottom), the upper/green band the periods during which the lines are read out (top to bottom).

The frame size is kept constant (number of valid lines), but the number of dummy lines is varied to demonstrate several concepts of readout.

In *Figure6-4*, the shutter time is considerably shorter than the frame time. A moderate amount of dummy lines is included, extending the frame time somewhat.

As the diagram indicates, the acquisition of a sequence of frames is a periodic, regular process: at all times is one line of a particular frame being read, while a line belonging to that same frame, or to the next frame, is being reset.

The one exception to this rule is during sequence initialization: the first N lines (N corresponding to the desired exposure time) of the first frame are reset, while no lines of frame 1 are being read.

Figure6-5 illustrates a typical frame sequence with the exposure/shutter time (almost) equal to the total frame time.

This increases the maximally-allowed exposure time much more than in previous diagrams, while the frame rate is severely reduced. It illustrates increased exposure time at the cost of a lowered frame rate. This is only to be done when sufficient light is lacking and when the camera is held stable.

6.3 Controlling the Sequencer

An image or sequence acquisition is started when a positive edge is seen on the RUN bit in the CCP_CTRL register.

When CCP_CTRL is updated with a RUN transition from '0' to '1' (or remains at '1', see AUTO_START bit), any present image acquisition sequence is stopped (also see FAST_STOP bit) and a new acquisition is started in a potentially new record (see CTXT bit).

A frame sequence ends normally when the frame counter (N_FRAMES) is at zero after the last (dummy) line of a frame has been produced be the sequencer.

Deassertion of RUN at any time makes the sequencer finish its present line, after which it stops scanning and enters its idle state (also see FAST_STOP bit in the CCP _CTRL register).

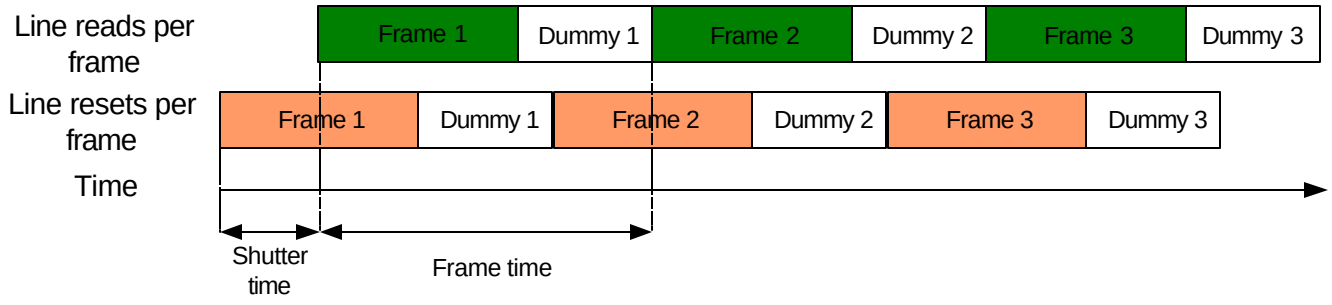

Figure 6-4. Typical Frame Sequence

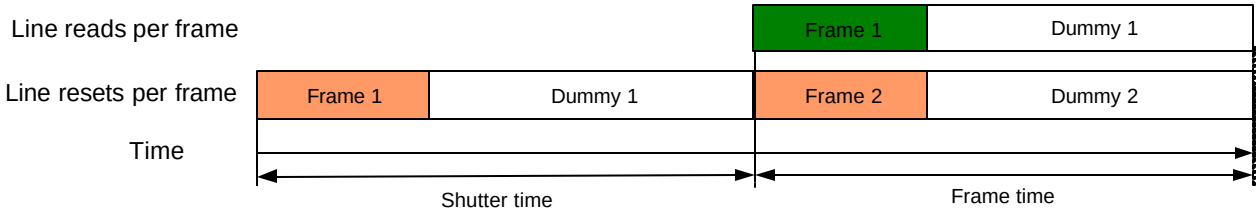

Figure 6-5. Frame Sequence with Addition of a Very Large Number of Dummy Lines

7.0 Serial Bus Description

The CYIWOSC1300AA interfaces with an external ISP through a bidirectional serial command interface and a unidirectional parallel data bus, in addition to a small number of direct-control pins for frame, line and flash synchronization, for device reset, for regulator configuration, and for the standby mode.

The device requires an external clock oscillator (up to 27 MHz) and a small number of strap connections to configure the device.

All I/O is CMOS IO with a programmable voltage range of 1.7–3.1V. All logic inputs have no leakage when they are driven high while the chip supply voltage is low/off.

The device control interface is compatible with the Philips I2C version 2.1 bus specification.

The device acts as a slave only, requiring the system host to act as the master. The device address can be selected from two addresses that are hard-wired on the chip, enabling the use of up to two identical devices simultaneously on the same bus. The address selection happens with the CMD_A pin.

CMD_A	Internal I2C Device Address
0	0xD2
1	0xD4

The D2h address is the same slave address as used on Cypress's programmable clock chips. This address does not collide with the most obvious competing image sensor chips.

The D4h address is an arbitrary modification of the device address to allow two identical sensor chips on the same command bus.

The command interface supports writing to and reading from 16-bit internal registers, with 8-bit address locations, at speeds of up to 400 kbits/s.

The interface clock CMD_CLK and the address pin CMD_A are driven by the serial interface master. The data pin is pulled up to a positive supply voltage by an off-chip resistor and can be pulled down both by the master and the slave device. The serial interface protocol determines which device can drive the data pin at any given time.

Data transfers to/from each 16-bit register can be 16 bits at once, the upper 8 bits, or the lower 8 bits. After any complete 16-bit transfer the internal register address is incremented automatically, anticipating the next similar transfer. There is no auto address increment for 8 bit transfers.

The bus is idle when both the CMD_CLK and CMD_D pins are HIGH. Control of the bus is initiated by a start bit (beginning of an access) and the bus is released again with a stop bit (end of the access). Only the master can generate these signals.

The transmission protocol defines several transmission codes:

- A start bit: The start bit is defined as a HIGH-to-LOW transition of the data line when the clock line is HIGH.
- The slave 8-bit address: The 7 MSB bits contain the device address: 0xD4 when CMD_A is HIGH and 0xD2 when CMD_A is LOW. The LSB bit of this address determines whether the request is a write (value is “0”) or a read (value is “1”).
- An acknowledge or no-acknowledge bit: This is the way for the receiver (either the slave in write mode or the master in read mode) to acknowledge the data sent by the transmitter. The master generates the acknowledge clock pulse. When the receiver pulls down the data line during that clock pulse, the previous byte is acknowledged. When the data line is not pulled down, the previous byte is NOT acknowledged. A no-acknowledge is used to terminate a read or a write sequence.
- An 8-bit message (register address or data byte): One data bit is transferred during each clock pulse. Data is always transferred 8 bits at a time, starting with the MSB bit, during 8 consecutive clock cycles, followed by an acknowledge bit.
- A stop bit: The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Except for the start and the stop bit, the data pin must always be stable during the HIGH period of the serial interface clock. It can only change when the clock is LOW.

7.1 16-bit Write Access Procedure

A 16-bit write access is performed as follows

1. The master sends a Start bit.
2. The master sends the 8-bit slave device address. The last bit will be set to “0”.
3. The slave acknowledges the address by sending the acknowledge bit back to the master.
4. The master sends the 8-bit register address to which a write should take place.
5. The slave sends an acknowledge bit to indicate that the register address was correctly received.
6. The master then transfers the data, 8 bits at a time. Internally, all register addresses have 16 bits, thus requiring two 8-bit transfers to write to one register.
7. The slave acknowledges every 8-bit word.
8. After every two 8-bit words written, the register address is automatically incremented, so that the next 16 bits are written to the next register address.
9. Steps 6, 7, and 8 are repeated for writing batches of data on consecutive register addresses.
10. The master stops the access by sending a Start or a Stop bit.

Figure7-1 gives an example of a 16-Bit write access (value 0x310b) to register 0x2a.

7.2 16-bit Read Access Procedure

A typical 16-bit read access is performed as follows:

1. The master sends a Start bit.
2. The master sends the 8-bit slave device address. The last bit will be set to “0” because the register address will be written first.
3. The slave acknowledges the address by sending the acknowledge bit back to the master.
4. The master sends the 8-bit register address to which a read should take place.

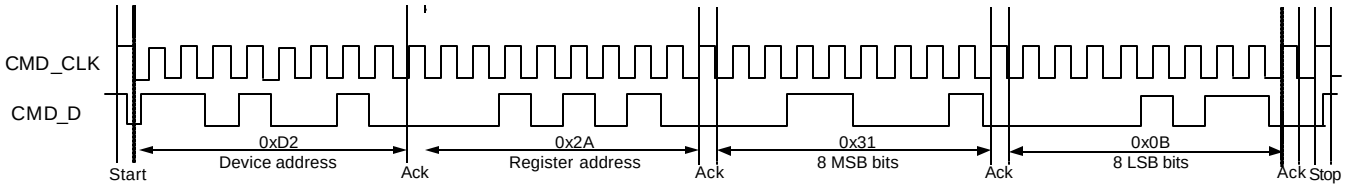

Figure 7-1. 16-bit Write

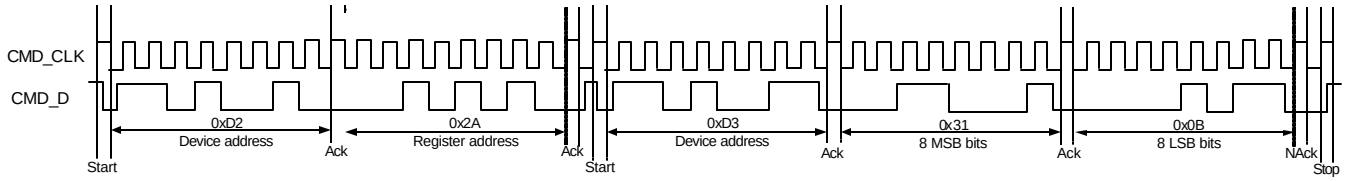

Figure 7-2. 16-bit Read

5. The slave sends an acknowledge bit to indicate that the register address was correctly received. The write access to set the register address is now finished.
6. The master sends a new Start bit.
7. The master sends the 8-bit slave device address. The last bit will be set to “1” for the actual read accesses.
8. The slaves transfers the data, 8 bits at a time. Internally, all register addresses have 16 bits, thus requiring two 8-bit transfers to read one register.
9. The master acknowledges every 8-bit word.
10. After every two data bytes written, the register address is automatically incremented, so that the next 16 bits are read from the next register address.
11. Steps 8, 9, and 10 are repeated for reading batches of data on consecutive addresses.
12. The data transfer is stopped when the master or slave sends a no-acknowledge bit.
13. The master generates a Start or Stop bit to finish the read access.

7.3 8-bit Write Access Procedure

To be able to write one byte at a time to the register, a special register address is added. The 8-bit write is started by writing the 8 MSB bits to the desired register, then writing the lower 8 bits to the special register (0xF1). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register.

An 8-bit write access is performed as follows

1. The master sends a Start bit.
2. The master sends the 8 bit slave device address. The last bit will be set to “0”.
3. The slave acknowledges the address by sending the acknowledge bit back to the master.
4. The master sends the 8-bit register address to which a write should take place.
5. The slave sends an acknowledge bit to indicate that the register address was correctly received.
6. The master then transfers the 8 MSB bits of the data.
7. The slave acknowledges the 8-bit word.
8. The master sends a Stop bit when the second part of the word is not written immediately.
9. Steps 1 to 8 are repeated for writing the 8 LSB bits. The only differences are the usage of the special address register (0xf1) instead of the real register address and replacing the MSB bits by the LSB bits.

The register address and the 8 MSB bits need to be stored temporarily.

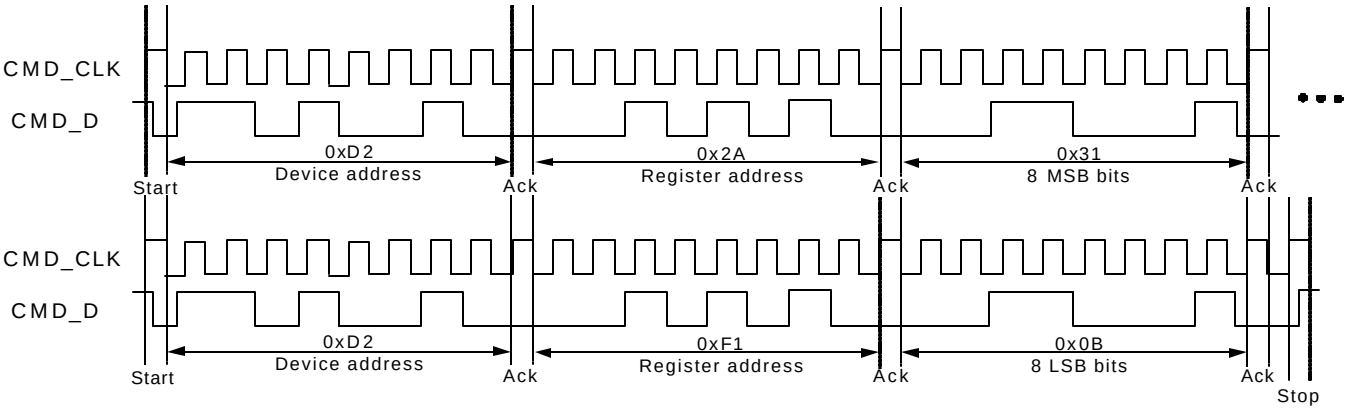

Figure 7-3. 8-bit Write

7.4 8-bit Read Access Procedure

To read one byte at a time, the same special register address is used for the lower byte. The 8 MSB bits are read from the desired register. By following this with a read from the special register, the 8 LSB bits are accessed. The master sets the no-acknowledge bits shown.

A typical 8-bit read access is performed as follows:

1. The master sends a Start bit.
2. The master sends the 8-bit slave device address. The last bit will be set to “0” because the register address will be written first.
3. The slave acknowledges the address by sending the acknowledge bit back to the master.
4. The master sends the 8-bit register address to which a read should take place.
5. The slave sends an acknowledge bit to indicate that the register address was correctly received. The write access to set the register address is now finished.
6. The master sends a new Start bit.
7. The master sends the 8-bit slave device address. The last bit will be set to “1” for the actual read accesses.
8. The slaves transfers the 8 MSB bits.
9. The master sends a no-acknowledge.

Steps 1 to 9 are repeated for the read procedure of the 8 LSB bits. This time, the register address used is the special register address (0xf1) and the slave will return the 8 LSB bits.

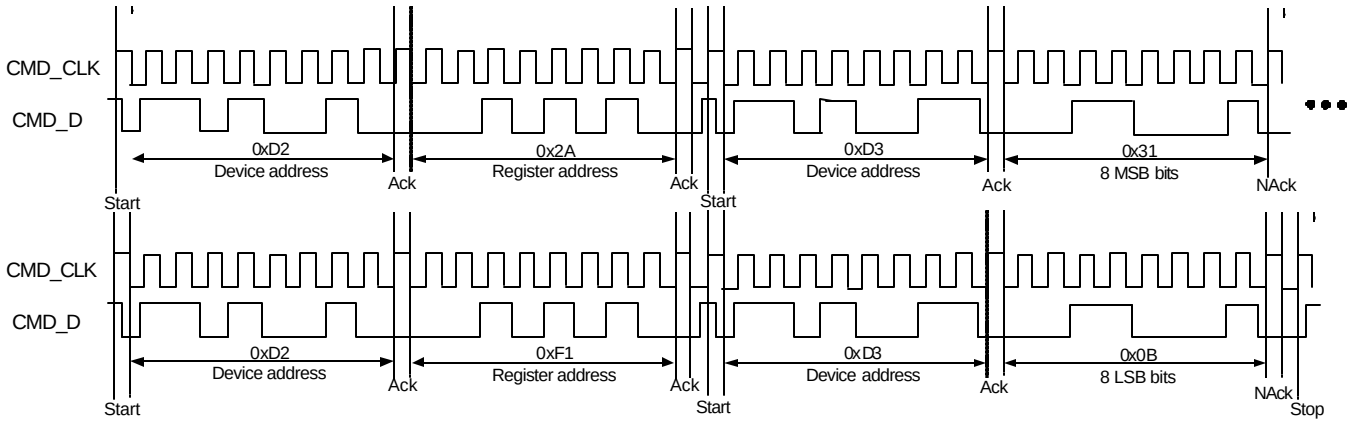

Figure 7-4. 8-bit Read

8.0 Registers

8.1 Register Map

The imager has 8-bit-wide register addresses that contain 16-bit-wide register values. All registers are explained in the tables below.

Address	Register Name	Reset Value	R/W	Description
0	CONFIG1	0x0000	R/W	configuration register 1, only upload value as described in this table
1	CCP_ID	0x0350	R/-	device identification code
3	CCP_CTRL	0x0000	R/W	camera control register (start/stop, record switch, Xenon flash)
4	CCP_CONFIG	0x0000	R/W	camera control configuration register (record clock division, Xenon flash arming)
5	CCP_GLOBAL	0x0000	R/W	camera control global settings (gain change synchroni-zation, subsampling, binning, LED flash control)
6	CCP_STAT	0x0000	R/-	camera control status (record, clock, and run status)
16	CONFIG2	0x5F9C	R/W	Configuration register 2, see CONFIG2 table below for more details
17	CONFIG3	0x0077	R/W	Configuration register 3 see CONFIG3 table below for more details
18	CONFIG4	0x0077	R/W	Configuration register 4 see CONFIG4 table below for more details
19	CONFIG5	0x0077	R/W	Configuration register 5 see CONFIG5 table below for more details
22	CONFIG6	0x0777	R/W	Configuration register 6, see CONFIG6 table below for more details
23	SEQ_A_FRAMES	0x0000	R/W	record A number of frames to grab and blank frame(s) configuration
24	SEQ_B_FRAMES	0x0000	R/W	record B number of frames to grab and blank frame(s) configuration
25	SEQ_A_ORIG	0x0000	R/W	record A start of physical scan window
26	SEQ_B_ORIG	0x0000	R/W	record B start of physical scan window
27	SEQ_A_SIZE	0x82A2	R/W	record A size of physical scan window
28	SEQ_B_SIZE	0x82A2	R/W	record B size of physical scan window
29	SEQ_A_ORIG_ROI	0x0101	R/W	record A start of region of interest window
30	SEQ_B_ORIG_RO	0x0101	R/W	record B start of region of interest window
31	SEQ_A_SIZE_ROI	0x80A0	R/W	record A size of ROI window
32	SEQ_B_SIZE_ROI	0x80A0	R/W	record B size of ROI window
33	SEQ_A_DUMMY	0x0100	R/W	record A number of dummy lines and pixels
34	SEQ_B_DUMMY	0x0100	R/W	record B number of dummy lines and pixels
38	SEQ_FLASH1	0x0041	R/W	flash configuration 1: flash firing delay, Xenon strobe length
39	SEQ_FLASH2	0x0011	R/W	flash configuration 2: flash frame definition, number of frames to flash in
40	CONFIG7	0x2F85	R/W	Configuration register 7, see CONFIG7 table below for more details
41	CONFIG8	0x4C7E	R/W	Configuration register 8, see CONFIG8 table below for more details
42	CONFIG9	0x1097	R/W	Configuration register 9, see CONFIG9 table below for more details
43	CONFIG10	0x000A	R/W	configuration register 10, only upload value as described in this table

Address	Register Name	Reset Value	R/W	Description
44	SEQ_STATUS	0x0000	R/-	sequencer status and BIST result: present black residue, BIST result, flicker detection results
45	SEQ_EXP	0x0400	R/W	exposure time
46	SEQ_GAIN	0x3F80	R/W	gain and offset for preamp and PGA
64	OUT_CONFIG	0x0000	R/W	output interface configuration: timing and polarity of PIX_CLK, FRAME, LINE
128	ISP_DEFECT	0x0002	R/W	defect pixel interpolator configuration
241	ACCESS_MODE	0x0000	R/W	special access mode register for 8-bit serial register read and write

Address	Register Name	Reset Value	R/W	Clients / Description
1	CCP_ID	0x0350	R/-	Interface registers Device identification code
Bits				
3:0	REV[3:0]	0d		revision
5:4	TYPE[1:0]	1d		1 - imager
11:6	FORMAT[5:0]	13d		6 - VGA
15:12	PROCESS[3:0]	0d		

Address	Register Name	Reset Value	R/W	Clients / Description
3	CCP_CTRL	0x0000		Central chip control register
Bits				
0	RUN	0		When CCP_CTRL is updated and RUN transitions from '0' to '1' (or remains at '1', see AUTO_START bit), any present image acquisition sequence is stopped (also see FAST_STOP bit) and a new acquisition is started in a potentially new record (see CTXT bit). When CCP_CTRL is updated and RUN transitions to '0' the present acquisition is stopped and the sensor enters idle/sleep mode (see FAST_STOP). When CCP_CTRL is updated and no new RUN condition exists the present acquisition is stopped and the sensor enters idle/sleep mode (see FAST_STOP).
1	CTXT	0		0 - record A: execute commanded image acquisition using record A register settings 1 - record B: execute commanded image acquisition using record B register settings
2	AUTO_CTXT	0		0 - when an acquisition in record B ends (also see register SEQ_B_FRAMES), no auto record return to A is done. 1 - automatically return to record A, and start a new acquisition there, when record B has finished its image acquisition sequence (see SEQ_B_FRAMES). This allows to execute a fully automatic preview-snapshot-preview sequence.
3	AUTO_START	0		Chooses between starting an acquisition when RUN is explicitly set, or whenever CCP_CTRL is written. 0 - RUN bit needs a transition from 0 to 1 to trigger an image acquisition 1 - RUN bit is level sensitive: any writing to CCP_CTRL with RUN = '1' will stop the present acquisition and start a new one

Address	Register Name	Reset Value	R/W	Clients / Description
4	FAST_STOP	0		0 - finish present frame completely when asked to stop or restart 1 - accelerated stop procedure, aborting present frame quickly (also see SEQ_CONFIG2.ABORT_DUMMY)
5	XE_FLASH_EN	0		0 - no Xenon flash 1 - fire Xenon flash when a new image acquisition starts (and Xenon flash has been armed in the record of that new acquisition, see 0:4 CCP_CONFIG)
14:6	-			
15	RESET	0		0 - chip operational 1 - execute a soft reset, which resets this register too; the other chip parameter registers are not reset.

Address	Register Name	Reset Value	R/W	Clients / Description
4	CCP_CONFIG	0x0000	R/W	CCP configuration
Bits				
3-2	B_CLK_DIV[1:0]	“00”		record B internal clock division: “00” - /1 “01” - /2 “10” - /4 “11” - N/A set to /1 if record B is to be used for snapshot image capture (recommended)
5-4	A_CLK_DIV[1:0]	“00”		record A internal clock division: “00” - /1 “01” - /2 “10” - /4 “11” - N/A set to /2 or /4 if record A is to be used for video preview (recommended)
7-6	IDLE_CLK_DIV[1:0]	“00”		idle mode internal clock division: “00” - /1 “01” - /2 “10” - /4 “11” - N/A set to /4 for lowest power consumption when idling (recommended)
8	IDLE_SEQ_SLEEP	0		0 - do not assert SEQ_SLEEP when idling 1 - assert SEQ_SLEEP for minimal analog power when idling
9	B_ARM_XE	0		record B arm Xenon flash (see 0: 3 CCP_CTRL for firing the flash)
10	A_ARM_XE	0		record A arm Xenon flash

Address	Register Name	Reset Value	R/W	Clients / Description
5	CCP_GLOBAL	0x0000	R/W	settings for CCP, SEQ, ISP
Bits				
0	LED_FLASH_EN	0		SEQ 0 - LED flash off (also see 0:39 SEQ_FLASH2 for automated flash turn-off) 1 - LED flash on; the switching of the FLASH strobe is not synchronized to the frame capture.
1	-	0		
2	A_BINNING	0		SEQ record A horizontal pixel binning 0 - binning off (snapshot mode) 1 - binning on (to be combined with subsampling)
3	B_BINNING	0		SEQ record B horizontal pixel binning 0 - binning off 1 - binning on (to be combined with subsampling)
5:4	A_SUB[1:0]	“00”		SEQ, ISP, CCP record A subsampling in X and Y 0 - 1:1:1:1:... 1 - 1:1:0:0:1:1:0:0:... 2 - 1:1:0:0:0:0:0:0:1:1:0:0:... 3 - N/A use subsampling when record A is used for video preview (recommended)
7:6	B_SUB[1:0]	“00”		SEQ, ISP, CCP record B subsampling in X and Y 0 - 1:1:1:1:... 1 - 1:1:0:0:1:1:0:0:... 2 - 1:1:0:0:0:0:0:0:1:1:0:0:... 3 - N/A do not use subsampling when record B is used for snapshot (recommended)
8	FAST_RESET	0		SEQ 0 - the frame reset cycle at the start of a Xe flashed acquisition is at normal frame rate (slow) 1 - the frame reset cycle at the start of a Xe flashed acquisition is at accelerated frame rate (fast) to reduce shutter lag.
10	SEQ_GAIN_SYNC	0		SEQ 0 - analog gain updates immediately take effect (for test/debug only) 1 - gain updates are post-synced to frames to bring them in line with exposure time updates

Address	Register Name	Reset Value	R/W	Clients / Description
6	CCP_STAT	0x0000	R/-	CCP status and diagnostics
Bits				
0	STAT_RUN	0		present running status 0 - idle or halting 1 - running

Address	Register Name	Reset Value	R/W	Clients / Description
1	STAT_CTXT	0		present record 0 - record A 1 - record B
3:2	STAT_DIV[1:0]	“00”		present clock division 0 - /1 1 - /2 2 - /4 3 - not used
4	STAT_SLEEP	0		Sleep mode
15:5	-	0		

Address	Register Name	Reset Value	R/W	Clients / Description
16	CONFIG2	0x5F9C	R/W	sets bias (power) of the ADC recommended value for record A preview, record B snap-shot, and low-power idling is 0x5F9B
Bits				
0	A_ADC_FPB_n	'0’		record A ADC bias value for preview: '1' value for snapshot: '0'
4:1	A_ADC_SB_n[3:0]	“1110”		record A ADC bias value for preview: “1101” value for snapshot: “1110”
5	B_ADC_FPB_n	'0’		record B ADC bias value for preview: '1' value for snapshot: '0'
9:6	B_ADC_SB_n[3:0]	“1110”		record B ADC bias value for preview: “1101” value for snapshot: “1110”
10	CONFIG2A	'1’		Fixed value
14:11	CONFIG2B	“1011”		Fixed value
15	CONFIG2C	'0’		Fixed value

Address	Register Name	Reset Value	R/W	Clients / Description
17	CONFIG3	0x0077	R/W	sets bias (power) of the column amplifiers recommended value for record A preview, record B snap-shot, and low-power idling is 0x0073
Bits				
3:0	A_COL_BIAS[3:0]	“0111”		record A COL bias snapshot value: “0111” preview value: “0011”
7:4	B_COL_BIAS[3:0]	“0111”		record B COL bias snapshot value: “0111” preview value: “0011”
11:8	CONFIG3A	“0000”		Fixed value

Address	Register Name	Reset Value	R/W	Clients / Description
18	CONFIG4	0x0077	R/W	sets bias (power) of the PGA recommended value for record A preview, record B snapshot, and low-power idling is 0x0073
Bits				
3:0	A_PGA_BIAS[3:0]	“0111”		record A PGA bias snapshot value: “0111” preview value: “0011”
7:4	B_PGA_BIAS[3:0]	“0111”		record B PGA bias snapshot value: “0111” preview value: “0011”
11:8	CONFIG4A	“0000”		Fixed value

Address	Register Name	Reset Value	R/W	Clients / Description
19	CONFIG5	0x0077	R/W	sets bias (power) of the preamp / column amp gain stage recommended value for record A preview, record B snapshot, and low-power idling is 0x0073
Bits				
3:0	A_PRE_BIAS[3:0]	“0111”		record A PRE bias snapshot value: “0111” preview value: “0011”
7:4	B_PRE_BIAS[3:0]	“0111”		record B PRE bias snapshot value: “0111” preview value: “0011”
11:8	CONFIG5A	“0000”		Fixed value

Address	Register Name	Reset Value	R/W	Clients / Description
22	CONFIG6	0x0777	R/W	sets bias for the current reference recommended value for record A preview, record B snapshot, and low-power idling is 0x0777
Bits				
3:0	CONFIG6A	“0111”		Fixed value
7:4	CONFIG6B	“0111”		Fixed value
15:8	SPARE[7:0]	0x07		spare control port for analog core: SPARE[3:0]: bias for precharge SPARE[4]: use internal resistor for current reference (also see IREF_SELECT) SPARE[7:5]: -

Address	Register Name	Reset Value	R/W	Clients / Description
23	SEQ_A_FRAMES	0x0000	R/W	record A frame capture sequences
Bits				
7:0	A_NRFRAMES[7:0]	0x00		record A number of frames to acquire; 128 means never-ending, values 0 and above 128 are illegal
11:8	A_BLANK_FIRST[3:0]	0x0		record A number of frames to blank out after start of acquisition
15:12	A_BLANK_PERIOD[3:0]	0x0		record A number of frames to blank out between any valid frames

Address	Register Name	Reset Value	R/W	Clients / Description
0:24	SEQ_B_FRAMES	0x0000	R/W	record B frame capture sequences
Bits				
7:0	B_NRFRAMES[7:0]	0x00		record B number of frames to acquire; 128 means never-ending, values 0 and above 128 are illegal
11:8	B_BLANK_FIRST[3:0]	0x0		record B number of frames to blank out after start of acquisition
15:12	B_BLANK_PERIOD[3:0]	0x0		record B number of frames to blank out between any valid frames

Address	Register Name	Reset Value	R/W	Clients / Description
25	SEQ_A_ORIG	0x0000	R/W	record A physical frame origin
Bits				
7:0	A_X1[7:0]	0x00		record A address of first pixel to read; multiply by 8 to get the effective address; 0 in normal operation.
15:8	A_Y1[7:0]	0x00		record A address of first line to read; multiply by 8 to get the effective address; 0 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
26	SEQ_B_ORIG	0x0000	R/W	record B physical frame origin
Bits				
7:0	B_X1[7:0]	0x00		record B address of first pixel to read; multiply by 8 to get the effective address; 0 in normal operation.
15:8	B_Y1[7:0]	0x00		record B address of first line to read; multiply by 8 to get the effective address; 0 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
27	SEQ_A_SIZE	0x82A2	R/W	record A physical frame size
Bits				
7:0	A_XD[7:0]	162d		record A line length in physical pixels; multiply by 8 to get the effective length; 1296/8 in normal operation.
15:8	A_YD[7:0]	130d		record A frame height in physical lines; multiply by 8 to get the effective length; 1040/8 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
28	SEQ_B_SIZE	0x82A2	R/W	record B physical frame size
Bits				
7:0	B_XD[7:0]	162d		record B line length in physical pixels; multiply by 8 to get the effective length; 1296/8 in normal operation.
15:8	B_YD[7:0]	130d		record B frame height in physical lines; multiply by 8 to get the effective length; 1040/8 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
29	SEQ_A_ORIG_ROI	0x0101	R/W	record A Region Of Interest origin
Bits				
7:0	A_X1_ROI[7:0]	1d		record A address of first pixel in ROI (i.e., qualified by LINE on the output interface); multiply by 8 to get the effective address; 8/8 in normal operation.
15:8	A_Y1_ROI[7:0]	1d		record A address of first line in ROI (i.e., qualified by FRAME on the output interface); multiply by 8 to get the effective address; 8/8 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
30	SEQ_B_ORIG_ROI	0x0101	R/W	record B Region Of Interest origin
Bits				
7:0	B_X1_ROI[7:0]	1d		record B address of first pixel in ROI; multiply by 8 to get the effective address; 8/8 in normal operation.
15:8	B_Y1_ROI[7:0]	1d		record B address of first line in ROI; multiply by 8 to get the effective address; 8/8 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
31	SEQ_A_SIZE_ROI	0x80A0	R/W	record A physical ROI size
Bits				
7:0	A_XD_ROI[7:0]	160d		record A ROI line length in physical pixels; multiply by 8 to get the effective length; 1280/8 in normal operation.
15:8	A_YD_ROI[7:0]	128d		record A ROI frame height in physical lines; multiply by 8 to get the effective length; 1024/8 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
32	SEQ_B_SIZE_ROI	0x80A0	R/W	record B physical ROI size
Bits				
7:0	B_XD_ROI[7:0]	160d		record B ROI line length in physical pixels; multiply by 8 to get the effective length; 1280/8 in normal operation.
15:8	B_YD_ROI[7:0]	128d		record B ROI frame height in physical lines; multiply by 8 to get the effective length; 1024/8 in normal operation.

Address	Register Name	Reset Value	R/W	Clients / Description
33	SEQ_A_DUMMY	0x0100	R/W	record A number of dummy pixels and lines
Bits				
7:0	A_XD_DUMMY[7:0]	0d		record A dummy pixels (ref non-subsampled array); multiply by 8 to get the effective number. These pixels are appended at the end of each line, but do not appear at the output. Use this to set desired line time or to clear pipelines in the image signal processor.
15:8	A_YD_DUMMY[7:0]	1d		record A dummy lines (ref non-subsampled array); multiply by 8 to get the effective number. These lines are appended to the frame, but do not appear in the output. Use this to set desired frame time, to clear pipelines in the image signal processor, or to enforce an exposure time in excess of the number of physical lines. Minimum value is 1.

Address	Register Name	Reset Value	R/W	Clients / Description
34	SEQ_B_DUMMY	0x0100	R/W	record B number of dummy pixels and lines
Bits				
7:0	B_XD_DUMMY[7:0]	0d		record B dummy pixels (ref non-subsampled array); multiply by 8 to get the effective number. These pixels are appended at the end of each line, but do not appear at the output. Use this to set desired line time or to clear pipelines in the image signal processor.
15:8	B_YD_DUMMY[7:0]	1d		record A dummy lines (ref non-subsampled array); multiply by 8 to get the effective number. These lines are appended to the frame, but do not appear in the output. Use this to set desired frame time, to clear pipelines in the image signal processor, or to enforce an exposure time in excess of the number of physical lines. Minimum value is 1.

Address	Register Name	Reset Value	R/W	Clients / Description
38	SEQ_FLASH1	0x0041	R/W	Flash configuration 1
Bits				
5:0	FLASH_DELAY[5:0]	0x001		Xenon flash delay in line times (multiply by 8 for effective number) from the last physical line reset in the fast-reset preamble to the firing of the flash strobe. Note that for Xe flash to be operated the exposure time must be set to its maximum allowed value.
11:6	FLASH_LENGTH[5:0]	0x001		Xenon flash strobe burning time in line times, multiply by 8.

Address	Register Name	Reset Value	R/W	Clients / Description
39	SEQ_FLASH2	0x0011	R/W	Flash configuration 2
Bits				
3:0	FLASH_FIRST[3:0]	0x1		Xenon flash: first frame after start of imaging sequence for which FLASH is to fire.
7:4	FLASH_NR_FRAMES[3:0]	0x1		Xenon flash: number of consecutive frames, up to 13, in which the flash is fired. Values 14 and 15 are illegal. LED flash: number of consecutive frames, up to 13, during which FLASH remains enabled before being extinguished automatically (see AUTO_FLASH). 14 or more means FLASH strobe remains asserted until CCP_GLOBAL.LED_FLASH_EN is deasserted.

Address	Register Name	Reset Value	R/W	Clients / Description
40	CONFIG7	0x2F85	R/W	
Bits				
1:0	CONFIG7A	“01”		Fixed value
3:2	CONFIG7B	“01”		Fixed value
4	INV_X	'0’		pixel scan direction 0 - straight 1 - inverted
5	INV_Y	'0’		line scan direction 0 - straight 1 - inverted
7:6	CONFIG7C	“10”		Fixed value
8	CONFIG7D	'1’		Fixed value
9	CONFIG7E	'1’		Fixed value
12:10	CONFIG7F	“011”		Fixed value
13	CONFIG7G	'1’		Fixed value

Address	Register Name	Reset Value	R/W	Clients / Description
41	CONFIG8	0x4C7E	R/W	
Bits				
0	CONFIG8A	'0’		Fixed value
7:1	CONFIG8B	3Fh		Fixed value
9	CONFIG8C	'0’		Fixed value
11:10	CONFIG8D	“11”		Fixed value
15:14	ABORT_DUMMY[1:0]	“01”		number of dummy lines scanned when frame aborted. Multiply by 8 for the effective number, regardless of sub-sampling factor.

Address	Register Name	Reset Value	R/W	Clients / Description
44	SEQ_STATUS	0x0000	R/-	black level, status and BIST results readout
Bits				
5:0	BLACK_RESIDUE[5:0]	0		black signal measured at ADC at the end of the most recent black level calibration Read this register during a frame, or at the end of a frame, to learn its effective black level.
7:6	BIST_RESULT[1:0]	0		X BIST result
8	FL_100_DETECTED	0		100-Hz component detected in light
9	FL_120_DETECTED	0		120-Hz component detected in light

Address	Register Name	Reset Value	R/W	Clients / Description
45	SEQ_EXP	0x0400		exposure time setting
Bits				
11:0	EXPOSURE_TIME[11:0]	1024d	R/W	exposure time, in line times The exposure time should always be between 1 and the total number (physical + dummy) of lines read in the frame. There is no automatic scaling for subsampling: when no dummies are configured, the maximum exposure time for a full frame is 1024, and for a 2:1-subsampled frame 512. The sensor behavior is undefined when illegal values are entered. Changing exposure time will have effect from the second frame on after the present frame. Maximum exposure time = physical + dummy -1

Address	Register Name	Reset Value	R/W	Clients / Description
46	SEQ_GAIN	0x3F80		gain and offset settings see CCP_GLOBAL.SEQ_GAIN_SYNC for the automatic synchronization of gain changes with exposure time changes and with frame boundaries.
Bits				
4:0	PGA_GAIN[4:0]	“00000”		programmable gain amp gain 0 - 1x (nominal) 1 - 1.1x ... 31 - 19 x
6:5	COL_AMP_GAIN[1:0]	“00”		column amp gain 0 - 1x 1 - 2x 2 - 4x 3 - not used
7	PGA_OFFSET_AUTO	'1’		PGA offset generation 0 - use value PGA_OFFSET 1 - use self-calibration
14:8	PGA_OFFSET[6:0]	3Fh		PGA offset value for manual mode

Address	Register Name	Reset Value	R/W	Clients / Description
64	OUT_CONFIG	0x0000		Output interface configuration
Bits				
0	CLK_POL	'0'		PIX_CLK polarity 0 - straight 1 - inverted
1	FR_POL	'0'		FRAME polarity 0 - straight 1 - inverted
2	FR_FORM	'0'		FRAME timing 0 - with PREFRAME (early) 1 - with FRAME (late)
3	LN_POL	'0'		LINE polarity 0 - straight 1 - inverted
4	LN_FORM	'0'		LINE timing 0 - only ROI lines have LINE asserted 1 - all lines (physical, dummies, ...) have LINE asserted

Address	Register Name	Reset Value	R/W	Clients / Description
128	ISP_DEFECT	0x0002	R/W	ISP - Defect Pixel
Bits				
0	EN_DEFECT_PIXEL	'0'		0 - disable defect interpolation, passing on all data unchanged 1 - enable defect interpolation
2:1	DEF_PIX_SCALE[1:0]	"01"		scale factor for defect gradient 0 - 0.5: aggressive interpolation, detects more pixel defects, but may impair picture sharpness 1 - 1.0 2 - 1.5 3 - 2.0: soft interpolation

Address	Register Name	Reset Value	R/W	Clients / Description
241	ACCESS_MODE (SPECIAL)	0x0000	R/W	Special register for 8-bit transfer mode
7:0	byte	0		

9.0 Feature Descriptions

9.1 Efficient Well Pixel

Special Cypress technology allows large volume well capacity.

9.2 Windowing

Two windows can be programmed. The first window determines which physical pixels of the array are to be read. The second window lies entirely within the first window, and denotes the actual region of interest to be read out to the user. The difference between both windows is the overscan area, used in setting up the correct boundary conditions of the ROI pixels in all subsequent image processing.

9.3 Subsampling

Subsampling can be programmed in X and Y independently, for two schemes that preserve the Bayer-ordering of colors:

- 1:1:0:0: two pixels/lines are read, two skipped, for a 2x2 reduction in image size.
- 1:1:0:0:0:0:0:0: two pixels/lines are read, six skipped, for a 4x4 reduction in image size.

When subsampling is enabled in Y all lines that are skipped are reset to avoid blooming.

9.4 Flash Synchronization

A flash strobe signal is generated for LED and Xenon flash types. Start and stop instants and duration are programmable, as well as the frame(s) in which the flash should be triggered.

9.5 Xenon Flash

Fixed amplifier gains and exposure time can be programmed for Xenon flash operation, with automatic changeover between flash and non-flash modes.

Note: All of the following sequences are preceded by one of the two image capture start sequences with hard reset burst described in a previous section.

The Xenon flash can only be used in snapshot mode.

The conditions to start the Xenon flash sequence are:

- XE_FLASH_EN='1', and
- RUN = '1

These bits are all programmable in the CCP_CTRL register.

This then will initiate one of the following two possible image capture sequences.

The first possible sequence is for the flash to be ignited after the last physical line of the frame has been reset, and before the first physical line is read. This scheme only works when the exposure time is close to the total frame time. Note the long duration between the start of the sequence and the time the first flash is fired.

Figure9-1 illustrates a typical Xenon flash frame sequence, including its start-up:

First the lines in the frame are all reset. Then, during the run time of the dummy line 'resets', the FLASH strobe is asserted. The readout of the first frame starts. The sequence is repeated if so required.

The exposure time shall be set to be (almost) equal to the total allowed exposure time (i.e., *_YD + *_YD_DUMMY).

The second possible sequence can be seen in *Figure9-2*.

The reset phase for frame 1 is shortened by applying resets to all physical lines as fast as possible. This skews the effective exposure time for frame 1, but also reduces the time elapsed between the start of the sequence and the first firing of the flash. The skewed exposure time is of little consequence as most of the light is captured during the flash burn time.

When FAST_RESET is asserted with Xenon flash operation the initial reset sequence for the first frame is shortened: instead of resetting one physical line per nominal line time, all physical lines of the first frame are reset as fast as possible, one after the other. This considerably reduces the time between starting the sequence ('pushing the button') and the readout of the first valid frame.

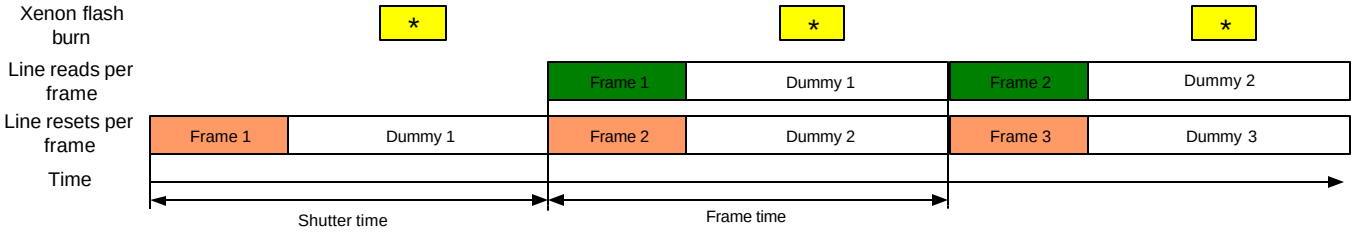

Figure 9-1. Xenon Flash Frame Sequence

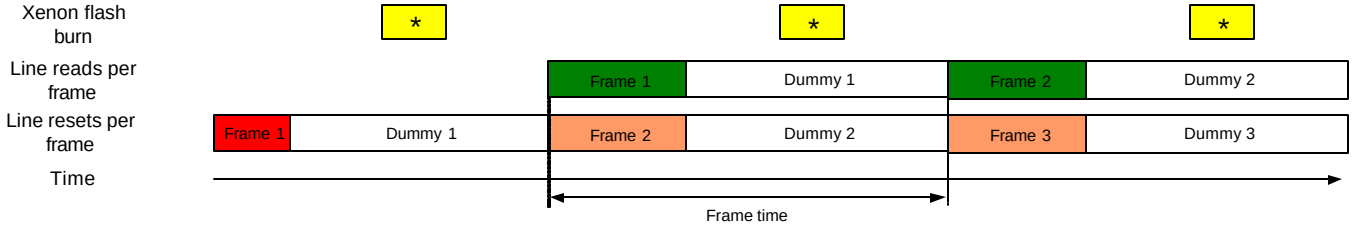

Figure 9-2. Xenon Flash Sequence with Accelerated Initial Reset

Note that the line time used in generating the dummy idle time is not accelerated, as this is the time gap in which the flash must fire!

FLASH_FIRST[3:0] programs the first frame after the start of the sequence prior to whose readout FLASH is to be asserted. FLASH_FIRST = 0 sets this action to the first frame, as in the above pictures.

FLASH_N[3:0] programs the number of frames prior to which FLASH must be strobed. FLASH_N = 0 is a reserved value and should not be used. If FLASH_N = 15 FLASH shall be fired before every frame, until either XE_FLASH_EN or RUN is deasserted, or until N_FRAMES have been taken.

The instant of firing and the duration of the FLASH strobe can be programmed (See *Figure9-3*):

FLASH_DELAY[7:0] is the time elapsed, in line times, between the reset of the last physical line in the scan window and the assertion of FLASH.

FLASH_LENGTH[7:0] is the duration, in line times, during which FLASH remains asserted.

It is required that sufficient dummy black lines be configured to allow the flash timing (however, the sequencer is not checking this requirement):

FLASH_DELAY + FLASH_LENGTH < *_YD_DUMMY

It is recommended that fixed exposure time and gain settings (also white balance settings where applicable) for Xenon flash use are programmed in the record B exposure settings. At the trigger a record change to B is then done.

Note that Xenon flashing only works properly if the exposure time is almost equal to the total frame time, and if sufficient black dummy lines are available to house the flash burning time.

9.6 LED Flash

The LED flash is controlled by the user and typically remains lit over a number of consecutive frames.

On/off control can be direct, or off can be programmed to happen a number of frames after the LED was lit.

When RUN = '1' the strobe FLASH will be asserted whenever LED_FLASH_EN is seen to be asserted. The FLASH remains active for FLASH_N frames. This frame count is restarted at the instant LED_FLASH_EN is asserted, but also at a record change.

FLASH_N has an option to keep FLASH asserted indefinitely, in which case FLASH will be deasserted by the user deasserting FLASH_EN.

Due to the action of the rolling shutter, the switching on and off of the LED flash will each give rise to one frame with non-homogeneous illumination. This is unavoidable. However, as such corrupt images can be seen as a linear combination of an unLEDed image and a LEDed image, this phenomenon can be ignored.

White balance should be set to fixed values matched to the LED illuminant.

9.7 Normal Operation Mode

When STANDBY and RESET_n are deasserted and a clock CLK is running, the device is in its normal operating mode, capable of receiving commands on its serial bidirectional interface, and of outputting images on its parallel bus.

In normal operating mode two further power modes can be distinguished: high-power snapshot and low-power preview. These modes are not hardwired on the device, but are defined by the user in terms of image size, subsampling, output data format and power consumption. The snapshot mode will typically be used for taking delivery-quality pictures, engaged for short periods of time with high image quality at the cost of high power consumption. Preview mode is used most of the time, generating subsampled images at video rate, and at low power consumption.

9.8 Standby Mode

When STANDBY is asserted the device is in a power-off state: all outputs and the command interface pins are tri-stated, the core logic is powered off, and analog core and ADC are in low-power bias mode. Register contents are undefined, and a chip reset is a mandatory part of a changeover to normal operating mode.

Inputs to the chip, including CLK, may be driven. The time required to get back from standby mode to normal mode is less than 100 ms.

At start-up, STANDBY needs to be deasserted after RESET for the normal image sequence to start.

9.9 Idle Mode

The user can program the device to run at a lower clock speed and set the analog core to run at zero bias to reduce power consumption. This mode can be set like the A and B records and behaves like a third record. See the register map for more explanation.

In this idle mode grabbing images is not possible.

9.10 Readout Modes

The sensor supports two fundamentally different readout modes, one for continuous-time viewfinder operation, one for snapshot operation. Both modes can be custom-tailored through the Camera Control Processor

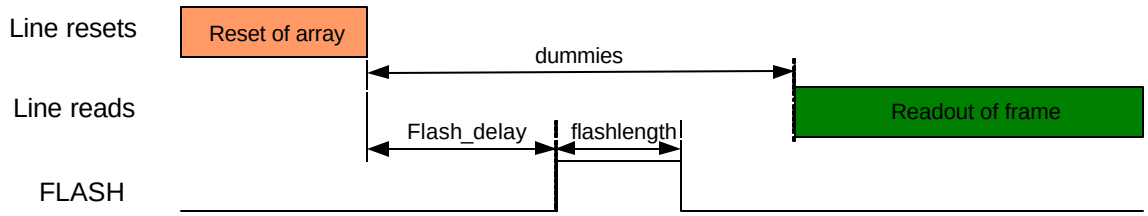

Figure 9-3. Xenon FLASH Strobe Timing Configuration

9.11 Viewfinder Mode

In viewfinder mode the pixel array is operated in subsampled low-power mode at up to 30 fps, continuously streaming, with rolling shutter operational. The chip's logic can be clocked by fCLK/2 or fCLK/4 compared to the normal fCLK and all timings can be scaled to keep the line and frame time invariant.

This mode is soft-configurable through user-writable registers. These registers contain settings for:

- analog module bias/power levels
- internal system clock divisions

A typical user-defined setting for viewfinder mode will be low bias, low power, slow operation, divided clock.

9.12 Snapshot Mode

In snapshot mode the pixel array is typically operated in full-frame full-power mode, during a programmable number of frames and with the rolling shutter operational, continuously streaming.

When snapshot mode is entered, an optional accelerated reset of all lines can be generated. The time from entering snapshot mode to the first line of the first available frame is limited to the desired exposure time plus a small overhead period. Windowing to increase frame rate is supported: the number of lines in a frame, and their position, can be programmed. Frame rate increases. This allows the readout of (for example) the 640x512 center area of the 1.3M-pixel array at 30 fps without subsampling.

9.13 Power-on Reset

A power-on-reset circuit allows the device to generate an internal chip reset when the power comes up while STANDBY is deasserted, or when power is up while the STANDBY pin gets deasserted and the RESET_n pin is accidentally left floating.

Thus, the internal logic reset net can be driven from three different sources/origins:

- the POR block
- the external pin RESET_n
- a user command issued on the serial interface

9.14 On-Chip Pixel Binning

Binning can be used in all modes however only makes sense in 2-subsampling mode (read 2, skip 2). When horizontal factor-2 subsampling is used, each two pixels of the same color can be summed and output as a single pixel. This reduces aliasing in preview mode.

10.0 1.3MP Imager Pad Numbering

Table 10-1. Pin Map Table (Left Side)

PAD #	Signal Name	I/O	Type	Function
1	VDD_28	PWR		Raw logic supply in; connect to 2.65–3.1V when regulator is used, otherwise to 1.7–1.9V
2	DGND	GND		Logic ground
3	VAA_PIX	PWR		Pixel array supply (2.65–3.1V)
4	AGND	GND		Analog/pixel array ground
5	VDD_18_O	PWR		Regulated 1.8V logic supply out (for test and bypass cap only)
6	VDD_18_O			Regulated 1.8V logic supply out (for test and bypass cap only)
7	Not used			Do not use
8	REG_BYPASS		CMOS	Regulator bypass
9	Not used			Do not use
10	STANDBY		CMOS	Turns off device
11	RESET_n		CMOS	Asynchronous reset
12	CMD_D		I2C compatible	Interface serial data in and out
13	CMD_CLK		I2C compatible	Interface bit clock, up to 400 kHz
14	CMD_A		CMOS	Interface device address selector
15	FLASH		CMOS	Flash strobe
16	Not used			Do not use
17	FRAME		CMOS	Frame valid strobe
18	VDDIO			IO supply (1.7–3.1V)
19	GNDIO			IO ground
20	Not used			Do not use
21	Not used			Do not use
22	Not used			Do not use
23	Not used			Do not use
24	Not used			Do not use
25	Not used			Do not use
26	Not used			Do not use
27	VAA			Sensor core/ADC analog supply (2.65–3.1V)
28	AGND			Sensor core/ADC analog ground

Table 10-2. Pin Map Table (Right Side)

PAD #	Signal Name	I/O	Type	Function
29	Not used			Do not use
30	Not used			Do not use
31	Not used			Do not use
32	PIX_OE	I	CMOS	Output enable for PIX_D/PIX Set to 1 enables outputs, set to 0 tri-states outputs
33	CLK	I	CMOS	System clock, 4 .. 27MHz
34	LINE	O/Z	CMOS	Line valid strobe
35	PIX_CLK	O/Z	CMOS	Output pixel data word clock
36	GNDIO	GND		IO ground
37	VDDIO	PWR		IO power
38	PIX_D[9]	O/Z	CMOS	Output pixel data
39	PIX_D[8]	O/Z	CMOS	Output pixel data
40	PIX_D[7]	O/Z	CMOS	Output pixel data
41	PIX_D[6]	O/Z	CMOS	Output pixel data
42	PIX_D[5]	O/Z	CMOS	Output pixel data
43	PIX_D[4]	O/Z	CMOS	Output pixel data
44	PIX_D[3]	O/Z	CMOS	Output pixel data
45	VDDIO	PWR		IO power
46	GNDIO	GND		IO ground
47	PIX_D[2]	O/Z	CMOS	Output pixel data
48	PIX_D[1]	O/Z	CMOS	Output pixel data
49	PIX_D[0]	O/Z	CMOS	Output pixel data
50	Not used			Do not use
51	Not used			Do not use
52	DGND	GND		Logic ground
53	AGND_DIG	GND		Sensor core/ADC digital ground
54	VAA_DIG	PWR		Sensor core digital supply (2.65–3.1V)
55	AGND	GND		Sensor core/ADC analog ground
56	VAA	PWR		Sensor core/ADC analog supply (2.65–3.1V)

11.0 Electrical Specifications

11.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Storage Temperature: .....–40°C to 85°C

Input Voltage: ..... –0.2V to V_{CC} +0.2V

ESD Susceptibility (HBM): 2000V

11.2 Operating Conditions

Supply Voltage: ..... 2.8 and 1.8VDC

Operating Temperature: ..... –20°C to +70°C

11.3 Electrical Characteristics

The following specifications apply for T_A = 25°C

Table 11-1.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Vdd	Digital Supply voltage		1.7	1.8	1.9	V
Vaa	Analog Supply voltage		2.65	2.8	3.1	V
$P_{15, SXGA}$	Active power consumption	Full frame 15 fps 10-bit resolution		100		mW
I_{SBE}	Stand-by current consumption			TBD		mA
Digital I/O						
V_{IO}	Output level [high]		Vdd-IO – 0.4			V
V_{IO}	Output level [low]				0.4	V
V_{OH18}	Output level [high]					V
V_{OL18}	Output level [low]					V
V_{IO}	Input level [high]		Vdd-IO – 0.7			V
V_{IO}	Input level [low]				Vdd-IO – 0.3	V
V_{IH18}	Input level [high]					V
V_{IL18}	Input level [low]					V
I_{LOAD}	Input leakage current					µA
C_{IN}	Input capacitance					pF
C_{OUT}	Output capacitance					pF
PCLK max	Pixel Output rate					MHz
t_r, t_f	Rise / Fall time					ns

12.0 Environmental Specifications

Table 12-1.

Specification	Value	Comment
Operating Temperature	–20°C to 70°C	See performance specifications for sensitivity de-rating over temperature
Storage Temperature	–40°C to 85°C	
Humidity	90% relative humidity @ 60°C	
Salt Mist Atmosphere		
Dust		100 mg/m^3
Chemical Resistance		

Document History Page

Document Title: CYIWOSC1300AA 1.3 Megapixel CMOS Sensor] Document Number: 38-19008				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	354077	See ECN	HBH	New data sheet
*A	392759	See ECN	HBH	Added detail to meet final product specifications