CYIWOSC3000AA

3.1 Megapixel CMOS Sensor

Features

- HiSENS™ High Sensitivity in low-light conditions
- 1/2.8” optical format image sensor
- Fast frame readout at full resolution
- Progressive scan
- I^2C serial control interface
- Selectable 8 and 12 bit parallel data port
- Low-power 30 frames/s preview mode
- Programmable controls: frame size, frame rate, gain exposure, blanking, flip and mirroring, windowing, auto black level offset correction and panning
- Horizontal and vertical binning for increased sensitivity
- Available in 48-pin PLCC package

Applications

- Cellular phone camera modules
- Pocket PCs
- PDAs
- Toys
- Battery operated devices

Table 0-1. Key Performance Parameters

Parameter	Typical Value
Optical Format	1/2.8-inch
Active Imager Size	5.2 mm x 3.9 mm
Active Pixels	2048H x 1536V
Pixel Size	2.54 µm x 2.54 µm
Color Filter Array	RGB Bayer Pattern
Shutter Type	Electronic Rolling Shutter
Maximum Data Rate/ Master Clock	48 MPS/48 MHz
Frame Rate	14 fps (2048 x 1536) 80 fps (640 x 480)
ADC Resolution	12-bit (72 dB), on-chip
Dynamic Range	55 dB
Responsivity	>1.0V/lux-sec (550 nm)
SNR_{MAX} in dB	QXGA: 35 VGA: 40
Supply Voltage @ 25°C	Analog: 2.5V–3.1V Digital: 1.65V–2.0V I/O: 1.8V–2.8V
Analog and Digital Power Consumption	60 mW @ 30 fps (640 x 480) 215 mW @ 15 fps (2048 x 1536)
Operating Temperature	–30°C to +70°C
Packaging	48-pin PLCC

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1.0 General Description

Cypress Semiconductor Corporation's (Cypress's) CMOS sensor is a 3.1-megapixel (QXGA) format, 1/2.8-inch active-pixel digital image sensor with an active imaging pixel array of 2048H x 1536V. The sensor incorporates camera functions such as frame size/rate, flip, mirroring and binning for increased sensitivity. The sensor functions are all programmable through a I^2C serial interface.

The megapixel CMOS sensor features Cypress's HiSENS circuitry, which dramatically improves low light sensitivity without increasing the number of transistors used in the pixel and maintains the fill factor while reducing the cost and complexity of the sensor.

An on-chip analog-to-digital converter (ADC) provides 12 bits per pixel. The sensor can be programmed by the user to meet the application specific requirements such as windowing, gain, panning and other parameters. The sensor can output a QXGA image up to 14 frames per second (fps).

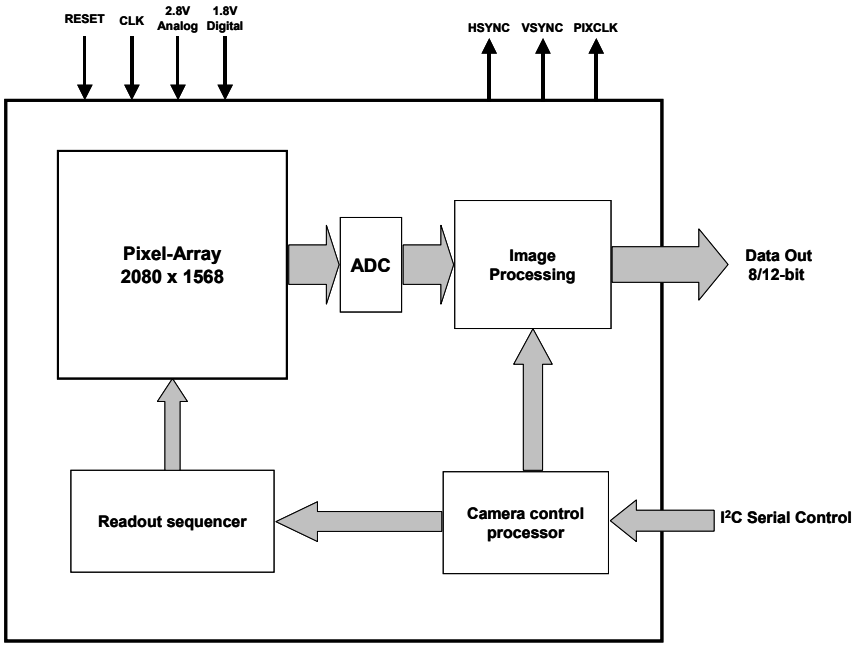
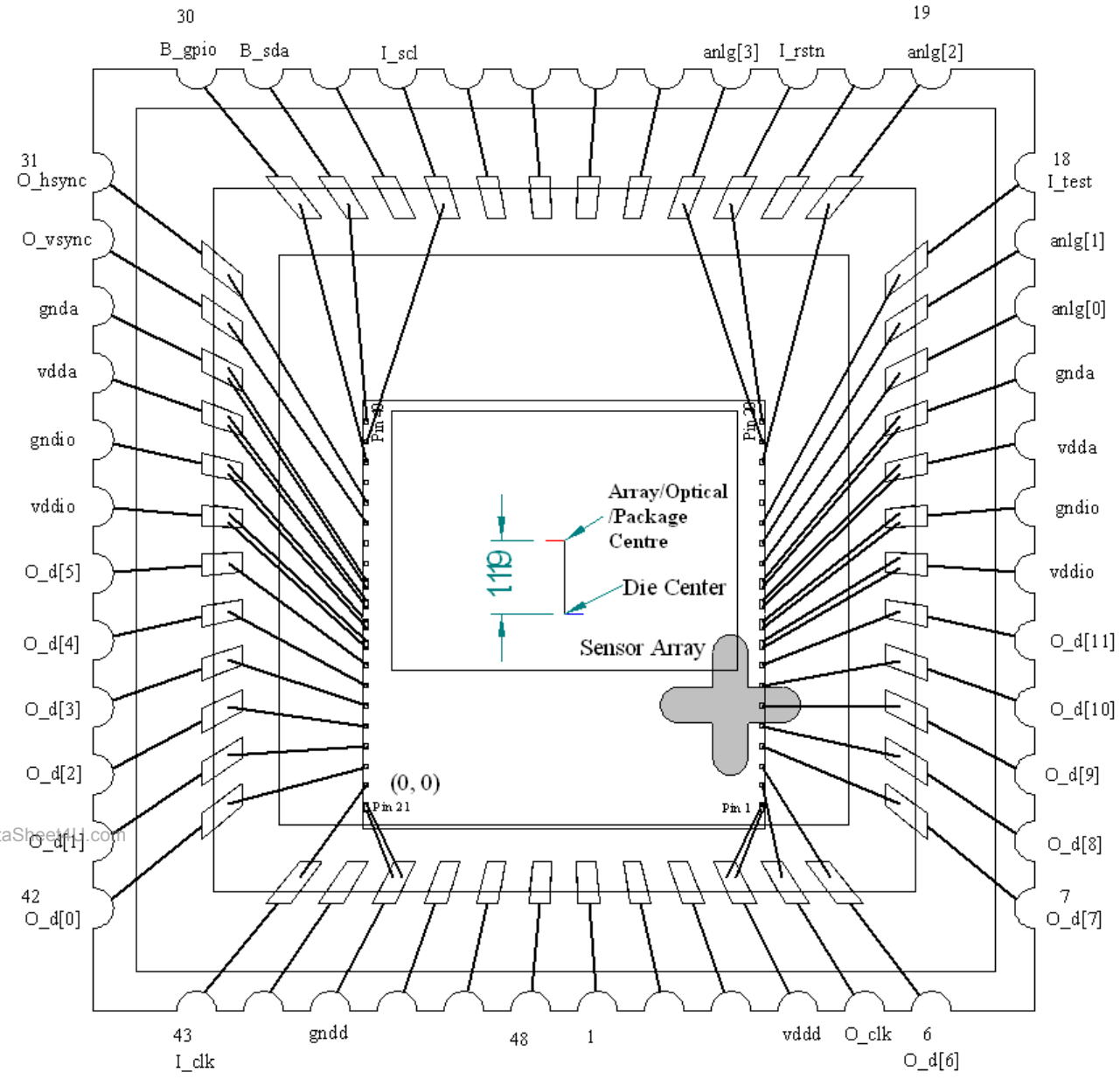


Figure 1-1. Block Diagram

2.0 Pin Description



All Dimensions: mm

Figure 2-1. Bond Diagram for 48-PLCC Package

Note: The sensor die is placed in the package so that the array center (optical center) of the die is centered in the package. The die is offset in the "Y" direction by 1.119 mm to achieve this.

3.0 Functional Overview

The sensor is a progressive-scan sensor that generates a stream of pixel data qualified by HSYNC and VSYNC signals. In default mode, the data rate (pixel clock) is the same as the master clock frequency, one pixel is generated every master clock cycle.

The core of the sensor is an active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row. In the time interval between resetting and reading a row, the pixels in that row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. After a row is read, the data from the columns is sequenced through an analog signal chain (providing offset correction), and then through an ADC. The output from the ADC is a 12-bit value for each pixel in the array. The pixel array contains optically active and light-shielded “black” pixels. The black pixels are used to provide data for on-chip offset correction algorithms (black level control).

The sensor contains a set of 8-bit control and status registers that can be used to control many aspects of the sensor operations. These registers can be accessed through a I^2C serial interface. In this document, registers are specified either by name (e.g., column start) or by register address (e.g., Reg0x04). Fields within a register are specified by bit or by bit range (e.g., Reg0x20[0] or Reg0x0B[13:0]. The control and status registers are described in Registers, Section 8.0.

The output from the sensor is a Bayer pattern: alternate rows are a sequence of either green/red pixels or blue/green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

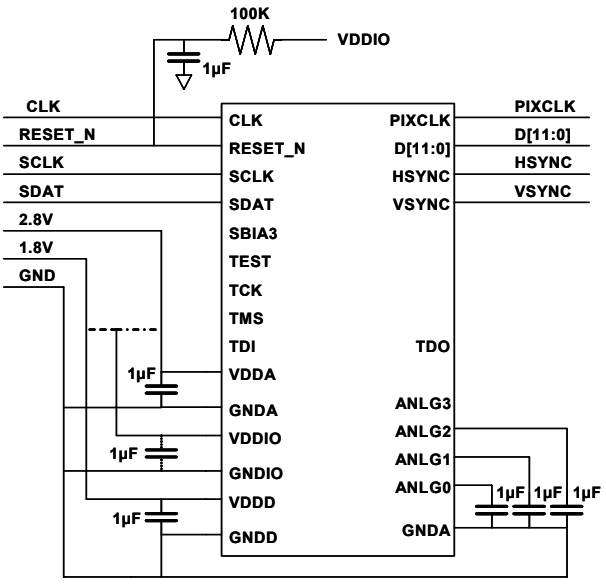


Figure 3-1. Typical Configuration

Figure 3-1 shows a typical module wiring diagram. VDDIO can be connected to either the 1.8V supply or the 2.8V supply (but not both) to match the voltage requirements of the back-end processing chip. It is recommended that the 1.8V supply be used to minimize power consumption. The capacitor for the VDDIO supply is optional but the capacitors for VDDD and VDDA are required and must provide sufficient decoupling on the module to insure clean supply voltages. Note that ANLG[2:0] must be connected to capacitors to minimize image noise. ANLG[3] is only for test purposes and should be unconnected. Note that RESET_N is typically connected with an RC circuit to hold RESET_N low until both power supplies have reached their proper level.

4.0 Signal Description

Table 4-1. Signal Description

Pin	Function	Type	Note
1	Vddd	Power	Digital Core Power (1.8V nominal)
2	PIXCLK	Output	Pixel Clock (data strobe)
3	D6	Output	Digital Video Out
4	D7	Output	Digital Video Out
5	D8	Output	Digital Video Out
6	D9	Output	Digital Video Out
7	D10	Output	Digital Video Out
8	D11	Output	Digital Video Out (MSB)
9	Vddio	Bidirectional	Digital IO Supply (1.8V nominal or 2.8V)
10	GNDIO	Power	IO Ground
11	Vdda	Power	Analog Supply to Pixel Array (2.8V nominal)
12	GNDA	Power	Analog Ground
13	ANLG[0]	Bidirectional	Analog Debug
14	ANLG[1]	Bidirectional	Analog Debug
15	TEST	Input	Test Mode
16	SBIA3	Input	Serial Bus Interface Address bit 3
17	TDI	Input	JTAG Data In
18	ANLG[2]	Bidirectional	Analog Debug
19	ANLG[3]	Bidirectional	Analog Debug
20	RESET_N	Input	Reset active low
21	GNDD	Power	Digital Ground
22	CLK	Input	Input Clock (up to 48 MHz)
23	D0	Output	Digital Video Out
24	D1	Output	Digital Video Out
25	D2	Output	Digital Video Out
26	D3	Output	Digital Video Out
27	D4	Output	Digital Video Out
28	D5	Output	Digital Video Out
29	VDDIO	Bidirectional	Digital IO Supply (1.8V nominal or 2.8V)
30	GNDIO	Bidirectional	IO Ground
31	VDDA	Bidirectional	Analog Supply to Pixel Array (2.8V nominal)
32	GNDA	Power	Analog Ground
33	TCK	Input	JTAG Clock
34	TMS	Input	JTAG
35	VSYNC	Output	Frame Sync
36	HSYNC	Output	Line Sync
37	TDO	Output	JTAG Data Out
38	GPIO	Bidirectional	General Purpose Digital IO
39	SCLK	Input	I^2C Serial Communications Clock
40	SDAT	Bidirectional	I^2C Serial Communications Data

5.0 Pixel Array Structure

The sensor device is a camera on a chip CMOS imager with 3-megapixel resolution (QXGA) in a 1/2.8" optical format. This requires a 2.54-μm square pixel pitch for adequate sensitivity. *Figure 5-1* below shows the layout of the Pixel Array. The 12 outermost rows and columns of the array are covered with metal and are thus optically black. The black rows can also be set via internal registers to be read out as valid frame data. There are 2048H x 1536V optically active pixels surrounded by an additional 2 Bayer patterns (4 pixels) around the image to avoid boundary effects during color interpolation and correction.

The sensor is designed with a mosaic of color filters arranged in a standard Bayer pattern shown in *Figure 5-1*. The odd numbered columns contain green and blue pixels as do the odd numbered rows. Correspondingly, the even rows and even columns contain green and red pixels. The imager will output either all Bayer patterned pixels or all physical pixels based upon register settings. The Bayer primitive pattern at the periphery should be used for border interpolation.

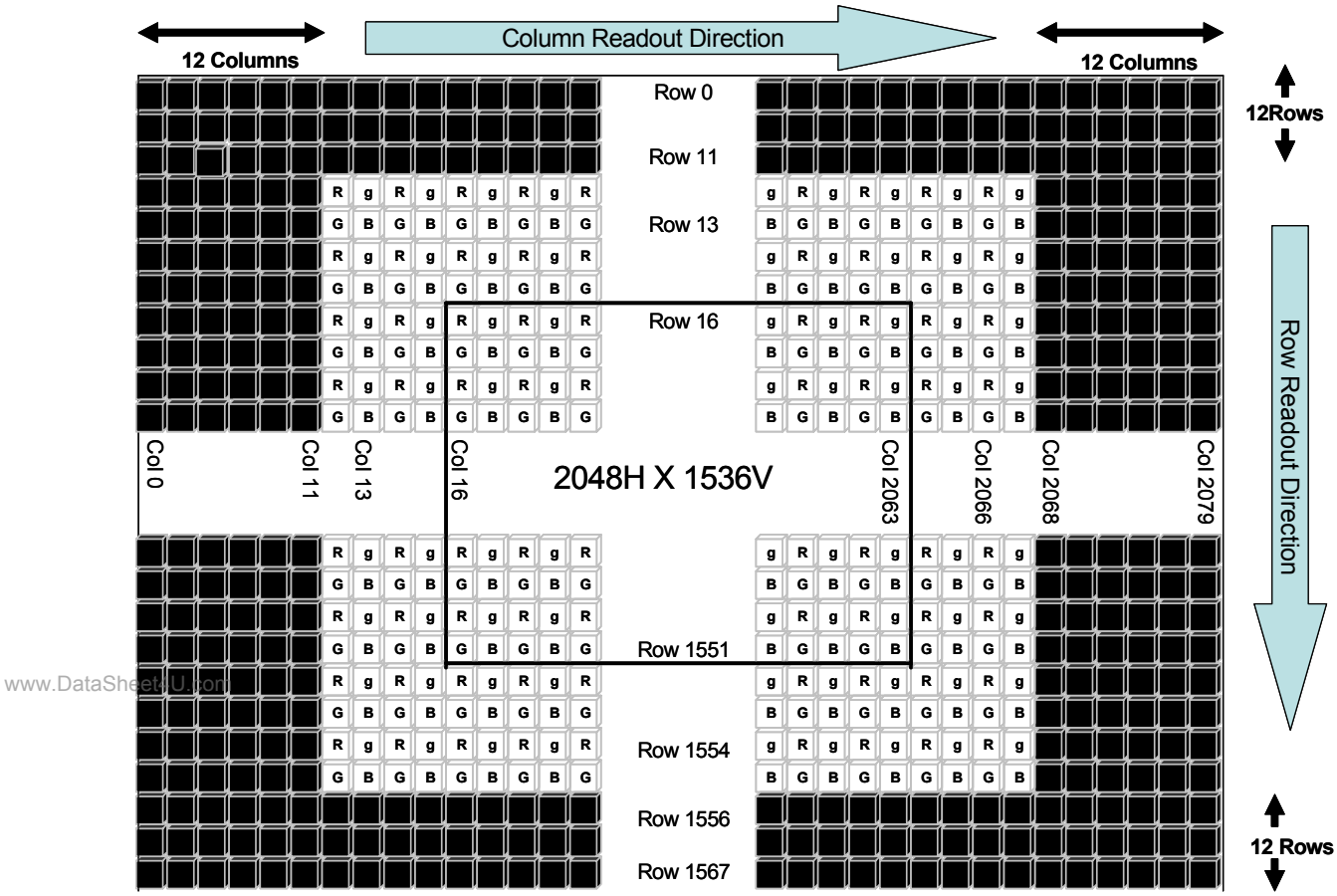


Figure 5-1. Pixel Array

6.0 Data Formats

The imager is read out in a progressive scan fashion. This means that each successive row is read out in an increasing row number. The data is digitized via on chip A/D converters and the output resolution is selectable at 8 and 12 bits resolution. The pixel data is output in parallel with synchronization signals for frame (VSYNC), line (HSYNC), and pixel (PIXCLK). The frame and line sync signals may be embedded in the data as set by internal registers. When sync signals are embedded in the data, the numbers of available colors is reduced by one value. The embedded SYNC values are indicated by a pattern of 0xFF, 0x00, 0x00, SYNC_VALUE where SYNC_VALUE is listed in *Table 6-1*.

Table 6-1. Embedded Sync

SYNC_VALUE	Description
00	Row Start
01	Row End
02	Frame Start
03	Frame End

To prevent SYNC from being inadvertently indicated in the active portion of the image, the 0xFF value is remapped to 0xFE when operating in 8-bits/pixel mode. The embedded sync format follows several industry standards including ITU-R BT.656.

With discrete sync signals, the polarity of the HSYNC, VSYNC, and PIXCLK may be independently inverted with respect to the active pixel readout. HSYNC and VSYNC toggle even when embedded syncs are enabled.

The resolution is set by three factors. The resolution may be decreased by sub-windowing a smaller region of interest (ROI), as set in the internal registers. The imager can also be programmed to sub-sample the array to read out every n^{th} Bayer rows and m^{th} Bayer columns. Finally, the imager can be programmed to bin (combine) adjacent pixels of similar color in both row and column directions independently with strengths of 2, 3, or 4.

The output data can be shifted down by 4 bits to accommodate back-end processors that want to switch from processing 12-bit data to 8-bit data where the LSBs must remain at bit zero on the Pixel Bus.

6.1 Frame Timing

A frame of data is comprised of valid image data which is output when the HSYNC and VSYNC signals are inactive (1). Frame rate is computed as a function of the CLK frequency, the row timing, the number of rows and the number of vertical blanking (VBLANK) rows programmed. The frame timing is programmable via a number of registers described later in this document.

Interfacing to a back-end processor involves the control signals, HSYNC and VSYNC, and the appropriate PIXCLK timing. The Imager has several programmable modes to allow interfacing to a wide variety of back-end processors. *Figure 6-2* shows typical interface signals.

There are two basic modes of operation, HSYNC and DATVAL. In HSYNC mode, the HSYNC signal indicates the start of a new row of the image. In this mode PIXCLK only clocks when there is valid data on the PIXDATA bus.

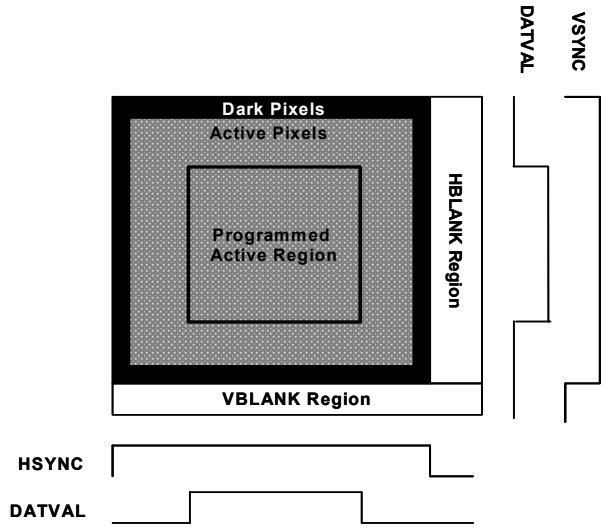


Figure 6-1. Frame Timing

In DATVAL mode, PIXCLK runs throughout the HBLANKING period (or optionally free-runs) and the HSYNC signals becomes a Data Valid signal which tells the back-end processor when there is valid data on the PIXDATA bus.

Note that if Dark Pixels are enabled to be output or if digital horizontal binning is used, DATVAL will toggle many times during a single row. Enabling Embedded Syncs does not change the row or frame timing. The 4-byte SYNC fields are inserted into the data stream during the HBLANK time (HBLANK must be at least 8).

The timing diagram in *Figure 6-2* shows the detailed row timing of all of the modes that the imager can produce. The HSYNC signal can be programmed to be either HSYNC or DATVAL. PIXCLK can be programmed in four different operating modes. Depending on the back-end processor, some modes will work better than others. Generally DATVAL mode with PIXCLDK mode = 10 is the most common mode. In this mode the HSYNC signal is acting as a DATA VALID pulse. PIXCLK runs continuously except when invalid data is on the PIXDATA bus. In the diagram above, CLK 4 is when the dark pixels are being processed. If the dark pixels were enabled to be output then CLK 4 would be high. Note that the number of clocks is significantly reduced in this diagram for ease of viewing. HSYNC is typically low for 16 or more clocks and there are 24 dark pixels, not just the one shown here.

The row timing gets more complicated when horizontal binning or subsampling is enabled (see *Figure 6-3*). The timing diagram shows the case where HBIN by 2 is enabled. Note that since the output format is Bayer patterns, it outputs 2 pixels, then skip (or bin) 2 pixels. Note that when using DATVAL mode, the DATVAL signal will toggle many times each row. However, using PIXCLK mode = 01, the backend processor will not clock in the pixels when DATVAL is low and thus it looks to the processor like DATVAL is always high when there is valid data.

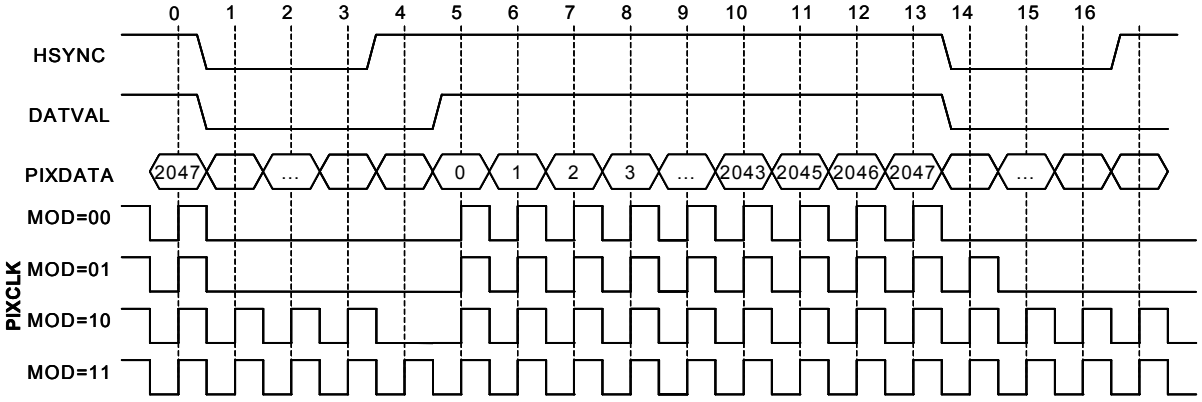


Figure 6-2. Row Timing

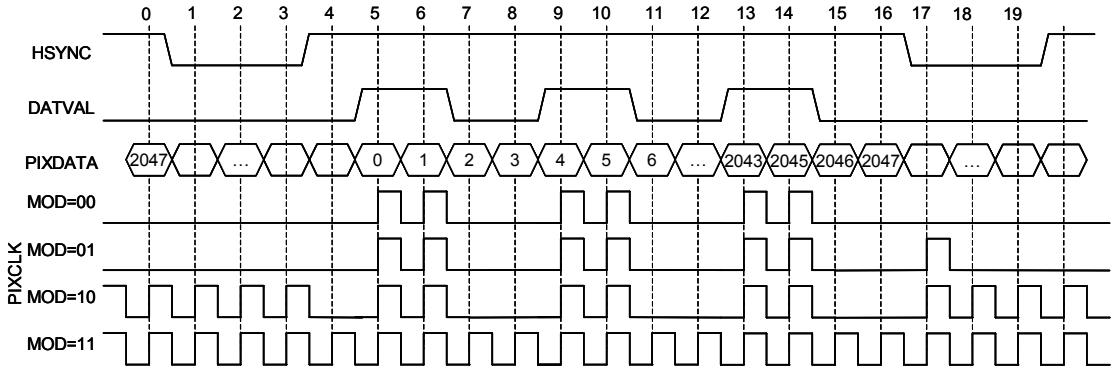


Figure 6-3. Row Timing With Binning

PIXCLK mode = 11 is typically only used in DATVAL mode. Otherwise, the processor has to clock in every pixel in a frame and then compute which ones are valid and which ones re not based on the bin/subsampling modes.

6.2 Frames per Second and Integration Time Calculation

The number of frames per second taken by the Osprey is programmable. It can vary from less then 1 fps to 14 fps in full resolution capture mode (and can be much higher in reduced resolution modes). The frame rate is dictated by input clk frequency, the total number of rows output per frame and the time required to read out a single row. The total number of rows output and the time required to output a row can be calculated using simple formula's based on I^2c register reads.

RowNum register (0x4) stores the number of active rows output.COLCNT register (0xa8) stores the # of clks required to read out a single row (hence time required to read out a single row is COLCNT / CLK FREQ. COLCNT is modified based on active number of columns output (COLNUM register (0x6) and the HBLANK register (0x8,0x9), which adds additional clk cycles onto the end of the row readout). Note that COLCNT is a 12bit register.

Frames/Second = Clock Frequency / (Total number of Rows per frame * COLCNT (register 0xa8 and 0xa9))

Where Total number of Rows per frame =RowNum(register 0x4 and 0x5 +1)+ VBLANK(0xC and 0xD) + Number of Dark rows.

The RowNum register will have a value 1 less than actual number of active rows and hence an addition of 1 in the formula.

The Dark rows are the optically black rows located towards the periphery to calculate the black level. At least 4 rows must be turned on to properly compute the dark current. By default, the middle 4 rows are turned on which typically are the best for computing Dark current. Please refer section 7.2.36.

Integration Time Calculation

TINT (in Seconds) = COLCNT (register 0xa8 and 0xa9) * INTTIME (register 0xE and 0xF) / Clock Frequency

It is recommended that INTTIME should not be set larger than the Total Number of Rows per Frame.

6.3 Output Data Timing

The Pixel Output bus has programmable polarities for the clock and the sync signals to simplify timing to the back-end processor. The timing of all of the signals is relative to PIXCLK. The delay time for HSYNC, VSYNC and the PIXDAT bus to be valid relative to the selected edge of PIXCLK is a minimum of 0 ns (Ddsmin) and a maximum of 4 ns (Tdsmax).

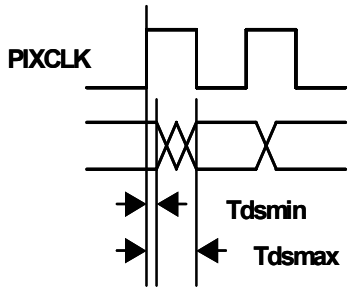


Figure 6-4. Pixel Data Timing

7.0 Serial Bus Description

The CYIWOSC3000AA includes a serial control interface that allows the application processor to control the imager using only two signals. The Serial Bus Interface (SBI) is a simple bidirectional communication interface based on the I^2C protocol that is in wide use throughout the industry. The serial bus operates at speeds of up to 400,000 bits per second. The Interface is a multi-drop protocol which allows multiple devices to be connected to a single pair of wires and can be used between numerous standard image processing chips.

The two interface signals are called SCLK and SDAT. SCLK provides a clock for asserting and sampling the SDAT signal. SCLK is unidirectional from the bus master, typically an image processing chip, to the CYIWOSC3000AA image sensor. SDAT is the data bus and is bidirectional. Both signals are open-drain and require a pull-up resistor of 1.5K Ohms.

Data is always transmitted with the Most-Significant-Bit (MSB) first. Eight bits of data are always transferred and are followed by a single ACKnowledge bit.

7.1 Serial Bus Protocol

Data transfer on the Serial Bus Interface is initiated with a START condition. The START condition is indicated when the SDAT signal goes low while SCLK remains high. The START condition may be initiated at anytime during a transfer and the imager will restart the transfer to begin accepting the SLAVE ADDRESS which must immediately follow the START.

The SDAT line must only transition when SCLK is low when data is being transferred. If SDAT transitions while SCLK is high, then it will be interpreted as either a START or a STOP condition. Sufficient timing margins must be provided around the rising and falling edges of SCLK to insure that a START or STOP condition are not mistakenly recognized.

The SLAVE ADDRESS is a sequence of 7 bits, a READ/WRITE bit and an ACKnowledge bit. Data is always transmitted MSB first and LSB last as shown in *Figure 7-1*. The SLAVE ADDRESS is 7 bits long and must be 1110_x10 (0xE4 or 0xEC) where x is the state of the SBIA3 pin. The SBIA3 pin allows two CYIWOSC3000AA Image Sensors to be connected to the same Serial Bus Interface. The LSB of the SLAVE ADDRESS is the READ/WRITE bit where a high (1) indicates that a READ cycle will follow and a low (0) indicates that a write cycle will follow. After the READ/WRITE bit, the CYIWOSC3000AA Image Sensor will assert SDAT low shortly after SCLK goes low to acknowledge that the SLAVE ADDRESS has been recognized and is ready to process the command that will follow.

If a read transaction has been requested (READ/WRITE is high), then the imager will begin driving SDAT with the register data at the current address. If a write transaction has been requested then the bus master should send the two REG ADDRESS bytes. The REG ADDRESS bytes specifies which register in the imager is to be accessed.

The next byte of data is the write data. Additional bytes of data can be written and the ADDRESS will be automatically incremented to the next register. Upon completion of all data being transferred, the master should issue a STOP command to place the SBI in an idle state. A STOP command is initiated by first driving SDAT low and SCLK high, then bringing SDAT high while SCLK remains high.

7.2 Detailed Timing

Figure 7-1 shows the detailed timing of each byte of data to be transferred on the SBI. A transfer begins with the START condition. This is always followed by 8-bits of data. The Acknowledge bit always follows the data which is from the receiver of the data to the transmitter. Additional bytes of data can then be transferred until either the STOP condition or another START condition is detected. Data is always transferred most-significant-bit first.

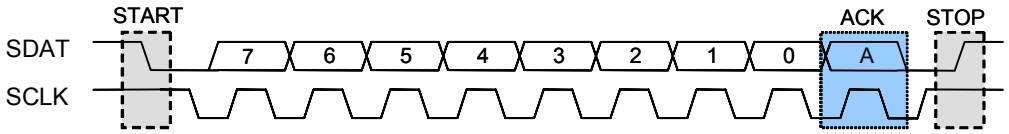


Figure 7-1. Serial Bus Timing

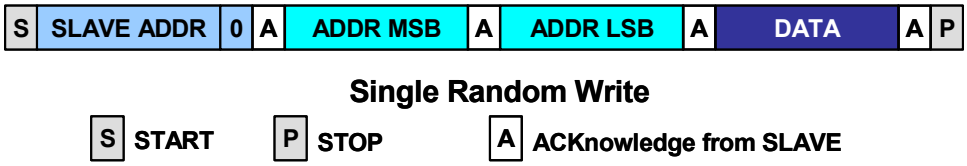


Figure 7-2. Single Random Write

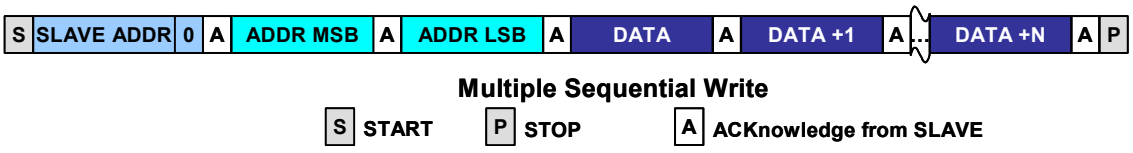


Figure 7-3. Multiple Write

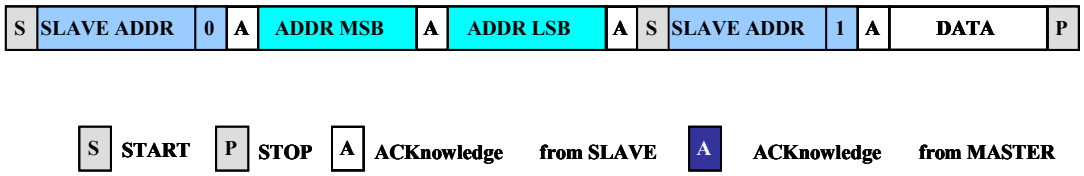


Figure 7-4. Single Random Read

7.3 Single Random WRITE

A WRITE cycle to any register is accomplished by sending a START followed by a 7 bit SLAVE ADDRESS, one bit of zero (the read/write indicator) and an ACK bit (see *Figure 7-2*). Then the 16-bit register address must be sent in two bytes, each with an ACK bit from the slave. Finally the 8-bits of data are sent and the slave will respond with a final ACK bit. The master can then either issue a STOP command or write to the next sequential address by sending additional data bytes.

7.4 Multiple WRITE

Multiple registers can be written in a single stream of data which reduces the time required to update registers. In *Figure 7-3*, DATA would be written to the address given in ADDR. DATA+1 would be written to ADDR+1 and so on with each byte of data being written to the next higher register address.

7.5 Single Random READ

A single random read cycle requires that a dummy write cycle be done first so that the register address can be set. The first SLAVE ADDR is followed with a 0 bit which indicates that this is a write cycle. The register address follows but instead of sending the data to write, a new START condition is sent which restarts the SBI state machine but the REG ADDR remains initialized. The SLAVE ADDR must be sent again but this time is followed with a 1 bit indicating that this is a read cycle. The slave responds with the ACK bit and then drives the 8 data bits of the register which has been read. After the eight data bits, the slave does NOT assert the ACK bit. Instead, it tri-states the SDAT signal so that the master can either ACK, or assert the STOP condition.

7.6 Multiple Sequential READ

Multiple sequential registers can be read without having to resend the SLAVE ADDR and register addresses. To read multiple registers, simply continue to issue more SCLKs and the imager will increment to the next higher register address. After each byte that is transferred, the master must issue an ACK by driving SDAT low if it wishes to continue to read more data. The last byte that is read should not ACK, which allows the master to drive SDAT low before releasing SCLK and then release SDAT to cause a STOP condition to be recognized. Alternatively, if the master does not drive SDAT low during the ACK bit, the imager will release the SDAT line and the state machine will return to its idle state waiting for the next START condition.

The register ADDR is always retained at the current address as long as power is applied to the chip. A register read at the current address can be initiated at any time without having to send the register ADDR first if the desired register is already being addressed. Note that the register address is incremented on the rising edge of SCLK at the start of the ACK bit.

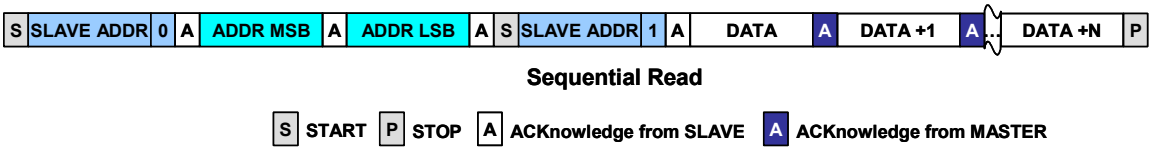


Figure 7-5. Multiple Sequential Read

8.0 Registers

8.1 Register Map

Table 8-1. Register Map

ADDR	Name	7	6	5	4	3	2	1	0	Description
00	ROWSH[1]	F				ROWSH				Row Start Address High
01	ROWSL[1]	ROWSL								Row Start Address Low
02	COLSH[1]	M				COLSH				Column Start Address High
03	COLSL[1]	COLSL								Column Start Address Low
04	ROWNUMH[1]					ROWNUMH				Number of Rows High
05	ROWNUML[1]	ROWNUML								Number of Rows Low
06	COLNUMH[1]					COLNUMH				Number of Columns High
07	COLNUML[1]	COLNUML								Number of Columns Low
08	HBLANKH					HBLANKH				Horizontal Blanking High
09	HBLANKL	HBLANKL								Horizontal Blanking Low
0A	DEVID	DEVID=0x4F('O')								Device Identification
0B	VERSION	VERSION								Silicon Version
0C	VBLANKH	VBLANKH								Vertical Blanking High
0D	VBLANKL	VBLANKL								Vertical Blanking Low
0E	INTTIMEH	INTTIMEH								Integration Time High
0F	INTTIMEL	INTTIMEL								Integration Time Low
10	RGAINH[1]					RGAINH				Red Gain Integer
11	RGAINL[1]	RGAINL								Red Gain Fraction
12	GrGAINH[1]					GrGAINH				Green-red Gain Integer
13	GrGAINL[1]	GrGAINL								Green-red Gain fraction
14	GbGAINH[1]					GbGAINH				Green-blue Gain Integer
15	GbGAINL[1]	GbGAINL								Green-blue Gain fraction
16	BGAINH[1]					BGAINH				Blue Gain Integer
17	BGAINL[1]	BGAINL								Blue Gain fraction
18	GAIN								E	Digital Gain Enable
1E	TINTINCH	E				TINTINC				TINT Increment High
1F	TINTINVL	TINTINC								TINT Increment Low
20	ROIXSH[1]					ROIXSH				Region Of Interest X Start High
21	ROIXSL[1]	ROIXSL								Region Of Interest X Start Low
22	ROIWXH[1]					ROIWXH				Region Of Interest X Width High
23	ROIWXL[1]	ROIWXL								Region Of Interest X Width Low
24	ROIYSH[1]					ROIYSH				Region Of Interest Y Start High
25	ROIYSL[1]	ROIYSL								Region Of Interest Y Start Low
26	ROIWYH[1]					ROIWYH				Region Of Interest Y Width High
27	ROIWYL[1]	ROIWYL								Region Of Interest Y Width Low
28	AEMAXH	AEMAXH								Auto Exposure Maximum High
29	AEMAXL	AEMAXL								Auto Exposure Maximum Low

Note:
1. Registers controlled by the SYNC bit.

Table 8-1. Register Map (continued)

ADDR	Name	7	6	5	4	3	2	1	0	Description
2A	AEMINH	AEMINH								Auto Exposure Minimum High
2B	AEMINL	AEMINL								Auto Exposure Minimum Low
2C	AEAVGH	AEAVGH								Auto Exposure desired average luminance High
2D	AEAVGL	AEAVGL								Auto Exposure desired average luminance Low
2F	EXPOSURE	E	I					D	F	Exposure Controls
30	BLKLVLH[1]	BLKH								Black Level High
31	BLKLVLL[1]	BLKL							O	Black Level Low
32	DARKMODE	E					MOD			Dark Current Subtraction Mode
33	FPNMODE			HM				VM		Fixed Pattern Noise Modes
35	ABIN		ABIN			VBIN				Analog Binning
36	HBIN	S	B	HB1		W	B	HB2		Horizontal Binning
37	VBIN	S	B	VBO		W	B	VBIN		Vertical Binning
38	PIXREPL							T	E	Pixel Replacement
39	DATAFMT	E			F	C	P	8	D	Pixel Data Format (8/12 bits)
3A	SYNCPOL	V	H		D	P		MOD		VSYNC, HSYNC, PIXCLK polarity
3B	TSTPTN						MOD			Test Pattern Enable
3C	FLIP							M	F	Flip/Mirror
3E	DARKTOPH									Top Dark Row Enable High
3F	DARKTOPL									Top Dark Row Enable Low
60	GPIO									
61	I^2CIO									
62	PCLKIO									
63	PIXIO									
70	PWRCTL						I	H	T	Power and IO Control
7E	RESET	RESET								Device Reset register
7F	SYNC	E	N	V						Register Synchronization
Status & Statistics Registers										
80	GrAVGH	GrAVGH								Green-red Average High
81	GrAVGL	GrAVGL								Green-red Average Low
82	GbAVGH	GbAVGH								Green-blue Average High
83	GbAVGL	GbAVGL								Green-blue Average Low
84	RAVGH	RAVGH								Red Average High
85	RAVGL	RAVGL								Red Average Low
86	BAVGH	BAVGH								Blue Average High
87	BAVGL	BAVGL								Blue Average Low
88	LUMAVGH	LUMAVGH								Luminance Average High
89	LUMAVGL	LUMAVGL								Luminance Average Low

Table 8-1. Register Map (continued)

ADDR	Name	7	6	5	4	3	2	1	0	Description
A0	REPLPIX	REPLPIX								Number of Pixels Replaced
A1	CURROW	CURROW								Current Row being output (8 MSBs only)
A2	NOISEVARH	NOISEVARH								Dark Noise Variance High
A3	NOISEVARL	NOISEVARL								Dark Noise Variance Low
A4	ACTROWSH					ACTROWSH				Number of Active Rows High
A5	ACTROWSL	ACTROWSL								Number of Active Rows Low
A6	ACTCOLSH					ACTCOLSH				Number of Active Columns High
A7	ACTCOLSL	ACTCOLSL								Number of Active Columns Low
A8	COLCNTH	COLCNT								Column Count High
A9	COLCNTL	COLCNT								Column Count Low
AA	TINTAEH					TINTAEH				AutoExposure Tint High
AB	TINTAEL	TINTAEL								AutoExposure Tint Low
										Reserved
FF	DEVID_N	DEVID_N								Ones Complement of DEVID (register 0x0A)
7FF - 100	Reserved									Reserved for Row Timing Generators.

8.2 Control Registers

8.2.1 ROWSH(00) & ROWSL(01)

Bit #	Name	DIR	Default	Function
15:12	Reserved		0	
11:0	ROWS	RW	12	Starting row address

ROWSH and ROWSL are a register pair that make up a twelve-bit register. The upper 3 bits of ROWSH are reserved. The lower 4 bits of ROWSH make up the 4 most significant bits of the starting row and ROWSL make up the low eight bits. The starting row address is normally twelve to begin the display with the first row of active pixels. When zooming in, the ROWS registers are used to start the image in the sub-window area of the image.

8.2.2 COLSH(02) & COLSL(03)

Bit #	Name	DIR	Default	Function
15:12	Reserved		0	
11:0	COLS	RW	12	Starting Column address

COLSH and COLSL are a register pair that make up a twelve-bit register. The upper 3 bits of COLSH are reserved. The lower 4 bits of COLSH make up the 4 most significant bits of the starting column and COLSL make up the low eight bits. The starting column address is normally twelve to begin the display with the first column of active pixels. When zooming in, the COLS registers are used to start the image in the sub-window area of the image.

8.2.3 ROWNUMH(04) & ROWNUML(05)

Bit #	Name	DIR	Default	Function
15:12	Reserved		0	
11:0	ROWNUM	RW	1555	Number of active pixels in each column

ROWNUMH and ROWNUML are a register pair that make up a twelve-bit register. The upper 4 bits of ROWNUMH are reserved. The lower 4 bits of ROWNUMH make up the 4 most significant bits of the number of active columns and ROWNUML make up the low eight bits. The ROWS and COLS register specify the upper left corner of the active window. This register specifies how high the active window should be. Bit zero should always be zero to insure whole Bayer Patterns are in the window. The number of rows also affects the frame rate. The fewer columns that are read out, the higher the frame rate.

8.2.4 COLNUMH(06) & COLNUML(07)

Bit #	Name	DIR	Default	Function
15:12	Reserved		0	
11:0	COLNUM	RW	2067	Number of active pixels in each row.

COLNUMH and COLNUML are a register pair that make up a twelve-bit register. The upper 4 bits of COLNUMH are reserved. The lower 4 bits of COLNUMH make up the 4 most significant bits of the number of active pixels in each column and COLNUML make up the low eight bits. This register specifies how wide the active window should be. Bit zero should always be zero to insure whole Bayer Patterns are in the window.

Changing the number of columns does not alter the frame rate. The column timing remains constant regardless of the number of columns programmed in the COLNUM register. However, the data rate will be reduced as only the columns requested will be clocked out on the pixel data bus.

8.2.5 HBLANKH(08) & HBANKL(09)

Bit #	Name	DIR	Default	Function
15:11	Reserved		0	
10:0	HBLANK	RW	TBD	Duration of HBLANK.

HBLANKH and HBLANKL are a register pair that make up an eleven-bit register. The upper 5 bits of HBLANKH are reserved. The lower 3 bits of HBLANKH make up the 3 most significant bits of the duration of Horizontal Blanking for each row and HBLANKL makes up the low eight bits. HBLANK can be made larger to lower the data rate however, it will decrease the resolution of the Integration Time (Tint) so it is recommended to keep HBLANK at its default value. HBLANK must be a minimum of TBD CLKs to allow for quiet time during certain sampling periods of each row.

8.2.6 DEVID(0A)

Bit #	Name	DIR	Default	Function
7:0	DEVID	R	0x4F	Device ID

The DEVID register provides a unique indicator for software to determine the capabilities of the imager. The CYIWOSC3000AA imager value is 0x4F (ASCII ‘O’). The ones-complement of DEVID is also available at address 0xFF. This can be used to verify a “signature” so the software knows what type of imager it is connected to.

8.2.7 VERSION(0B)

Bit #	Name	DIR	Default	Function
7:0	VERSION	R	1	Silicon Version

The VERSION register is an eight-bit register that specifies what version of silicon this chip is. Some features may not be present in various versions of the silicon.

8.2.8 VBLANKH(0C) & VBLANKL(0D)

Bit #	Name	DIR	Default	Function
11:0	VBLANK	RW	16	Duration of VBLANK.

VBLANKH and VBLANKL are a register pair that make up a twelve-bit register. VBLANK is the number of rows of vertical blanking time. The register is a twelve-bit register to allow for a wide range of frame rates. Each VBLANK value decreases the frame rate by one row. The minimum number of rows is 8, which are required to perform column FPN calculations.

8.2.9 INTTIMEH(0E) & INTTIMEL(0F)

Bit #	Name	DIR	Default	Function
11:0	INTTIME	RW	240	Duration of Integration Time (exposure time).

INTTIMEH and INTTIMEL are a register pair that make up a twelve-bit register. The Integration Time is the number of row times that the pixels are exposed before being read out.

Note that the INTTIME register may be updated at any time during the frame. It is only used by the timing logic when at a specific point in each frame (when the TINT reset pointer is at the first row of bottom dark pixels). The INTTIMEH register should utilize the SYNC register so that it only gets updated during VSYNC. Note that when AutoExposure is enabled, this register is ignored.

When the INTTIME value is increased, it must only be increased by the number of bottom dark rows plus the number of VBLANK rows or a split frame may be output. INTTIME can be decreased by any amount from one frame to the next. When INTTIME is increased by a large number (the image pans from a bright to a dark scene), the user has the option of accepting the split frame or increasing TINT by only the amount listed above. You can also increase the number of VBLANK rows to allow a rapid increase in the number of rows.

8.2.10 RGAINH(10) & RGAINL(11)

Bit #	Name	DIR	Default	Function
11:8	RGAINH	RW	0x01	Red Gain Integer
7:0	RGAINL	RW	0	Red Gain Fraction

The Red Gain is applied only to Red pixels. Each pixel is digitally multiplied by the RGAIN value. The GAIN value is a 4.8 fixed point integer thus the Red pixels can be digitally gained up by a factor of 16. By default the multiplication factor is 1 (0x100). If the result of the multiplication is greater than 4095, then the value is saturated to 4095.

8.2.11 GrGAINH(12) & GrGAINL(13)

Bit #	Name	DIR	Default	Function
11:0	GrGAIN	RW	0x100	Green-Red Gain

The Gr Gain is applied only to Green pixels on a red row. Each pixel is digitally multiplied by the GrGAIN value.

8.2.12 GbGAINH(14) & GbGAINL(15)

Bit #	Name	DIR	Default	Function
11:0	GbGAIN	RW	0x100	Green-Blue Gain

The GbGain is applied only to Green pixels on a blue row. Each pixel is digitally multiplied by the GbGAIN value.

8.2.13 BGAINH(16) & BGAINL(17)

Bit #	Name	DIR	Default	Function
11:0	BGAIN	RW	0x100	Blue Gain

The BGain is applied only to Blue pixels. Each pixel is digitally multiplied by the BGAIN value.

8.2.14 GAIN(18)

Bit #	Name	DIR	Default	Function
0	ENB	RW	0	0 = Bypass digital gain 1 = Enable digital gain

The ENB bit of he GAIN register must be a 1 for the following four gain registers to have an effect on the image data. When ENB is zero, the gain multipliers are bypassed and the data is passed through unaltered.

8.2.15 ROIXSH(20) & ROISXL(21)

Bit #	Name	DIR	Default	Function
11:0	ROISX	R/W	0	Region of Interest Start X

The ROIXSH and ROIXSL registers form a twelve-bit register. The ROIXS register is the starting column of the Region of Interest. The ROI is the area of the active array where statistics will be collected. The ROI can either be inside or outside of the rectangle defined by the ROI registers. The ROI does not include the Dark Pixels.

8.2.16 TINTINCH(1E) & TINTINCL(1F))

Bit #	Name	DIR	Default	Function
15	ENB	R/W	0	0 = Disable Tint Increment 1 = Enable Tint Increment
14:12		R	0	Reserved
11:0	TINTINC	R/W	0	Number of rows that TINT can change by

The ENB bit of the TINTINC register enables the 50/60 flicker mode for the Auto Exposure unit. When TINTINC mode is enabled, Tint is forced to be the nearest increment of the value programmed in TINTINC. If the Auto Exposure unit wants to set Tint to a value less than TINTINC, it will be set to exactly the desired value. If the Auto Exposure unit wants to set Tint to a value larger than TINTINC, then it will only set Tint to be an integer multiple of TINTINC.

TINTINC must be programmed with the number of row times that corresponds to either 1/100th of a second or 120th of a second. This will eliminate flicker that is observed when operating the camera under fluorescent lights.

8.2.17 ROIXSH(20) & ROISXL(21)

Bit #	Name	DIR	Default	Function
11:0	ROISX	R/W	0	Region of Interest Start X

The ROIXSH and ROIXSL registers form a twelve-bit register. The ROIXS register is the starting column of the Region of Interest. The ROI is the area of the active array where statistics will be collected. The ROI can either be inside or outside of the rectangle defined by the ROI registers. The ROI does not include the Dark Pixels.

8.2.18 ROIWXH(22) & ROIWXL(23)

Bit #	Name	DIR	Default	Function
11:0	ROIWX	R/W	2063	Width of the Region of Interest End X+1

The ROIWXH and ROIWXL registers form a twelve-bit register. The ROIWX register is the number of columns of the Region of Interest plus 1. A value of zero will result in an ROI of 1 column. The width should always be programmed to include whole Bayer patterns. Thus, ROIWX should be odd.

8.2.19 ROIYSH(24) & ROIYSL(25)

Bit #	Name	DIR	Default	Function
11:0	ROIYS	R/W	0	Region of Interest Start Y

The ROIYSH and ROIYSL registers form a twelve-bit register. The ROIYS register is the starting row of the Region of Interest.

8.2.20 ROIWYH(26) & ROIWYL(27)

Bit #	Name	DIR	Default	Function
11:0	ROIWY	R/W	1551	Width of the Region of Interest End Y +1

The ROIWYH and ROIWYL registers form a twelve-bit register. The ROIWY register is the number of rows of the Region of Interest plus 1.

8.2.21 AEMAXH(28) & AEMAXL(29)

Bit #	Name	DIR	Default	Function
11:0	AEMAX	RW	0	AEMAX is the maximum allowed value for Tint (integration time) expressed in number of row-times.

AEMAX sets the maximum value for Tint expressed in number of rowtimes. When Auto exposure mode is enabled, this value forces Tint to always be less than or equal to this value. Auto exposure mode always has the upper 4 bits of Tint to be zero.

8.2.22 AEMINH(2A) & AEMINL(2B)

Bit #	Name	DIR	Default	Function
11:0	AEMIN	RW	0	AEMIN is the minimum allowed value for Tint (integration time) expressed in number of row-times.

AEMIN sets the minimum value for Tint expressed in number of rowtimes. When Auto exposure mode is enabled, this value forces Tint to always be more than or equal to this value.

8.2.23 AEAVGH(2C) & AEAVGL(2D)

Bit #	Name	DIR	Default	Function
15:4	AEAVG	RW	0x800	AEAVG is the desired image average.

AEAVG is the desired image average. If the current image average is below this value, then Tint will be increased. If the current image average is below this value then Tint will be decreased.

8.2.24 EXPOSURE(2F)

Bit #	Name	DIR	Default	Function
7	AUTOENB	RW	0	0 = Manual exposure control 1 = Automatic adjustment of Tint
6	INSIDE	RW	0	0 = Statistics are computed inside the ROI 1 = Statistics are computed outside of the ROI
0	FAST	RW	0	0 = Normal rate of Exposure control 1 = Fast adjust of Tint

AUTOENB causes the value of Tint to be computed based on the current image average. This is a relatively crude automatic exposure control mode. The image average is computed in the ROI specified in the ROI registers.

INSIDE determines whether the image statistics are to be computed from the area inside the ROI or outside.

FAST determines the rate of adjustment of the auto exposure. When FAST=1, the exposure control is adjusted each frame to ½ of the difference between the current Tint and the calculated new Tint. When FAST=0, tint is adjusted by 1/8th of the difference.

8.2.25 BLKLVLH(30) & BLKLVLL(31)

Bit #	Name	DIR	Default	Function
0	OVERRIDE	RW	0	0 = Automatic Black Level computation 1 = Override Black Level
15:4	BLKLVL	RW	0	Black Level subtracted from each pixel when enabled. Pixnew = pix – BLKLVL

In normal operation, BLKLVL is automatically computed by accumulating the value of the first 8096 pixels in the top dark rows. This value is then subtracted from each pixel to remove the dark current if DARKMODE ENB = 1. The automatic computation of BLKLVL can be overridden by setting the OVERRIDE bit. In this case, BLKLVL must be written with the desired black level to be subtracted. The automatic Black Level is enabled by the ENB bit in the DARKMODE register.

8.2.26 DARKMODE(32)

Bit #	Name	DIR	Default	Function
7	ENB	RW	0	0 = Disable Black Level Subtraction 1 = Enable Black Level Subtraction
6	STATUS	R		0 = Dark Subtraction working 1 = Dark Subtraction Error
6:3		R	0	Reserved
2:0	MOD	RW	000	000 = Accumulate 8096 pixels for Dark Current 001 = 4096 Pixels 010 = 2048 Pixels 011 = 1024 Pixels 100 = 512 Pixels 101 = 256 Pixels 110 = 128 Pixels 111 = 64 Pixels (not recommended)

ENB enables an FPN mode where the dark rows across the top of the imager are averaged to compute a Black Level. The Black Level is then subtracted from each pixel in the rest of the current frame. The dark values are clipped to acceptable values before being accumulated. The digital gain should be adjusted slightly depending on the Black Level being subtracted to insure that saturated pixels remain saturated. The Black Level can be manually controlled with the BLKLVL register.

The STATUS bit is a flag indicating that there are not enough dark pixels to properly compute the dark current in the current operating mode. If STATUS = 1, then MOD should be increased until STATUS is 0. Otherwise the dark current subtraction will be incorrect. Typically MOD will need to be increased when binning or subwindowing in X.

The MOD bits allow for a few different numbers of pixels to be accumulated. When the ABIN register is set to combine pixels in the horizontal direction, the MOD bits must be changed to reduce the number of pixels used for the dark current subtraction. There must be at least the desired number of dark pixels or the calculation will be incorrect. When HBIN by 2 is enabled, there are only 1040 dark pixels per row and MOD must be set to 1. Additional dark rows can also be enabled with the DARKTOP register.

8.2.27 FPNMODE(33)

Bit #	Name	DIR	Default	Function
7		R	0	Reserved
6	FPNFLUSH	RW	0	0 = Normal operation 1 = Rapid stabilizing of Column FPN data
5	TESTSIGCOL	RW	1	0 = Use Dark row for ColFPN data 1 = Use TestSig for ColFPN data
4	DISPLAYCOL	RW	0	0 = Normal operating mode 1 = Output test column data as pixels
3	COLMAX	RW	1	0 = Average Mode Column FPN 1 = MAX mode Column FPN
2	COLLPF	RW	1	0 = Column FPN low-pass filter disabled 1 = Column FPN low-pass filter enabled
1	COLCLIP	RW	1	0 = Disable clipping in Average Mode Column FPN 1 = Enable clipping in Average Mode Column FPN
0	FPNCOLENB	RW	0	0 = Disable Column Fixed Pattern Noise reduction 1 = Enabled Column FPN reduction

Fixed Pattern Noise removal is enabled with the FPNMODE register.

FPNFLUSH mode is typically used to quickly stabilize the Column FPN data when changing modes, especially when switching to or from one of the binning modes. When FPHFLUSH is a 1, the imager does not output data but will instead output black so the back-end processor will have to discard all frames when FPNFLUSH is a 1. It it recommended to leave FPHNFLUSH a 1 for one frame time to insure the Column FPN data is stable.

TESTSIGCOL selects an internal voltage signal as the reference signal for Column FPN data collections. When TESTSIGCOL is a zero, the data is sourced from one of the bottom dark rows instead of the internal voltage. It is recommended to keep this signal as a 1.

FPNCOLENB enables a sophisticated column noise removal algorithm. Each column has a value that is sampled from a test voltage and averaged across all rows of vertical blanking. This accumulated value is stored for each column and is subtracted from each pixel in that column.

COLMAX enables maximum mode for Column FPN removal. In this mode, the maximum value of the columns is searched for and kept in a register. Each pixel is then computed with the following equation:

Pixel_out = Pixel_in + FPNmax – FPNcol

Note that this mode is susceptible to outlyers in column FPN data and will tend to oversaturate pixels as it adds a significant offset. This offset is normally removed by the dark current removal logic later in the image pipeline.

When COLMAX is 0, then Average Mode Column FPN is enabled. This is the recommended mode of operation. In Average mode, the average value of all of the columns is added to each pixel and the value in the FPN RAM is subtracted from each pixel. In this mode, pixels are saturated both in the max and min direction.

Pixel_out = Pixel_in = FPNavg – FPNcol

COLCLIP is only used in Average Mode and lowers the saturation clip value for each pixel by the following equation:

Saturate_max = 0xfff – FPNavg

COLLPF is normally left at its default value of 1. The Low-Pass filter insures that the Column FPN data is accumulated slowly across many frames to compensate for changes in temperature or voltage. COLLPF should be cleared to 0 to initialize the Column FPN data for at least 1 frame. Otherwise it may take several seconds for the Column FPN data to stabilize to its correct value.

DISPLAYCOL is for testing purposes only and this bit should always remain 0 in normal operation. When 1, the values from the COLFPN RAM are output on the first row of vertical blanking.

8.2.28 ABIN(35)

Bit #	Name	DIR	Default	Function
7		R	0	Reserved
6:4	HBIN	RW	000	000 = 1:1 (no binning) 001 = 2:1 010 = Reserved 011 = 4:1 1XX = Reserved
4		R	0	Reserved
2:0	VBIN	RW	000	000 = 1:1 (no binning 001 = 2:1 010 = 3:1 011 = 4:1 100 = 6:1 (bin by 3 and subsample by 2) All other values are reserved

The ABIN register sets the analog binning mode.

8.2.29 HBIN(36)

Bit #	Name	DIR	Default	Function
7	SUM	RW	0	0 = Average the binned pixel 1 = Sum the binned pixels
6	BIN2	RW	0	0 = Subsample stage 2 1 = Bin
5:4	HBIN2	RW	00	00 = No 2nd stage binning/skipping 01 = 2nd stage bin/skip by 2 10 = 2nd stage bin/skip by 3
3	WEIGHT	RW	0	0 = 1:2:1 weighting for binx3 1 = Spatial based weighting for bin X3 and X4
2	BIN1	RW	0	0 = Subsample stage 1 1 = Bin
1:0	HBIN1	RW	00	00 = No Horizontal binning/skip—disabled 01 = Bin/skip every 2 pixels 10 = Bin/skip every 3 pixels 11 = Bin/skip every 4 pixels

The HBIN register enables and sets the value for Horizontal Binning mode or skip mode. In effect, HBIN sets the horizontal zoom factor. There are two stages of bin/skip. The first stage can bin by 2, 3, or 4 pixels. The second stage can only bin by 2 or 3. Each stage can either BIN or Skip independently. The BIN1/2 bits determine if subsampling (skip) or binning it to be performed. Subsampling requires less power but may result in a sparkling of the image if details line up with the active pixel or not. Binning averages many pixels together which is a fairly compute intensive operation and thus requires more power. Horizontal Binning is done digitally.

The WEIGHT bit is only used if binning is enabled for X3 or X4. If X3 binning is enabled, then a weighting is applied so that the average can be obtained with a simple shift operation instead of a divide. When WEIGHT = 1, this weighting is changed for Red or Green-Blue pixels and for Green–red or Blue pixels. This shifts the weight from the center of the superpixel to a more correct spatial weighting. In bin X4 mode, if WEIGHT = 1 then a weighting is applied. WEIGHT has no effect on bin X2.

The SUM bit is also only used when binning is enabled. When SUM=1, then the result of the bin is not shifted down after adding the pixels together. This results in a 2, 3, or 4X gain which can improve images in low-light conditions.

8.2.30 VBIN(37)

Bit #	Name	DIR	Default	Function
7	SUM	RW	0	0 = Average the binned pixel 1 = Sum the binned pixels
6	BIND	RW	0	0 = Subsample Digital 1 = Bin Digital

Bit #	Name	DIR	Default	Function
5:4	VBIND	RW	00	00 = No Digital binning 01 = Digital Bin by 2 10 = Digital Bin by 3
3	WEIGHT	RW	0	0 = 1:2:1 weighting for binx3 1 = Spatial based weighting for digital bin X3
2	BINA	RW	0	0 = Subsample Analog 1 = Bin Analog
1:0	VBINA	RW	00	00 = No Vertical binning—disabled 01 = Bin every 2 pixels together 10 = Bin every 3 pixels together 11 = Bin every 4 pixels together

The VBIN register enables and sets the value for Vertical Binning mode. Vertical Binning causes the number of vertical pixels to be averaged together. Horizontal and Vertical Binning as normally set to the same value at the same time. Binning causes the pixels of the same color to be averaged together. This allows a full field-of-view image at a lower resolution to be output without the “sparkling” effects of a sub-sampled windowing mode. Subsampling will significantly increase the frame rate and reduce the overall power consumption. The choice of binning or subsampling is independent for both the analog and digital stages.

There are two stages of Vertical Binning, Analog and Digital. Analog Binning is done in the analog domain and Digital Binning is done digitally. Analog binning requires a number of changes to the timing control registers.

The WEIGHT and SUM bits have the same meaning here as they do for digital binning (see the HBIN register) but only apply to the digital binning stage. The analog stage is not affected by either the WEIGHT or SUM bits. Independent bits are provided here but typically they should be set to the same value as the HBIN register.

8.2.31 PIXREPL(38)

Bit #	Name	DIR	Default	Function
1	THRESHOLD	RW	0	0 = Disable Threshold Mode 1 = Enable Threshold Mode
0	PIXREPLENB	RW	0	0 = Disable Pixel Replacement 1 = Enable Pixel Replacement

PIXREPLENB enables the Pixel replacement algorithm that hides normal defects in the image array. Pixel Replacement must be turned off when Binning or Boosting. Pixel replacement is not needed when Binning since multiple pixels are averaged together. The maximum error a bad pixel can contribute is only ¼ of a pixel in bin by 3 where the bad pixel is in the center and thus weighted 2X. Do not turn off Pixel Replacement when subsampling.

THRESHOLD enables a 4-bit threshold mode for the pixel replacement algorithm. When THRESHOLD is a one, the difference between the current pixel and the minimum or maximum of its adjacent same-color pixels must have a magnitude that extends into the upper 4 bits of the 12-bit pixel. Thus, for a pixel to be replaced, the pixel difference must be more than 1/16th of a the full scale. This insures that only significantly bad pixels are replaced. When THRESHOLD mode is a zero, then any pixel that is greater than the maximum or less than the minimum is replaced. This occurs many thousands of time in a typical image.

8.2.32 DATAFMT(39)

Bit #	Name	DIR	Default	Function
7	EMBDSYNC	RW	0	0 = Disable Embedded Sync 1 = Enable Embedded Sync
4	CPDFMT	RW	0	0 = Companding format 1 1 = Companding format 2
3	CONFIGROW	RW	0	0 = Normal Operation 1 = Include the Configuration Row data
2	COMPAND	RW	0	0 = Normal operation 1 = Compand the 12-bit pixel to 8-bits
1	8BMODE	RW	0	0 = Normal operating mode 1 = Shift PIXDAT down by 4 bits
0	DARKENB	RW	0	0 = Only Active pixels are read out 1 = All pixels are read including all dark pixels

EMBDSYNC enables embedded SYNC information to be embedded in the pixel data stream. When EMBDSYNC is disabled, the HSYNC and VSYNC pulses must be used to identify when a frame or row begins and ends. When EMBDSYNC is enabled, then the SYNC signals are identified when a pattern of 0xFF, 0x00, 0x00 is seen in the pixel stream. Any color values that are 0xFF are clipped to 0xFE to insure that the data is not seen as a sync indicator. Following the SYNC pattern the following values indicate what SYNC is present – 0x00 = Row Start, 0x01 = Row End, 0x02 = Frame Start, 0x03 = Frame End.

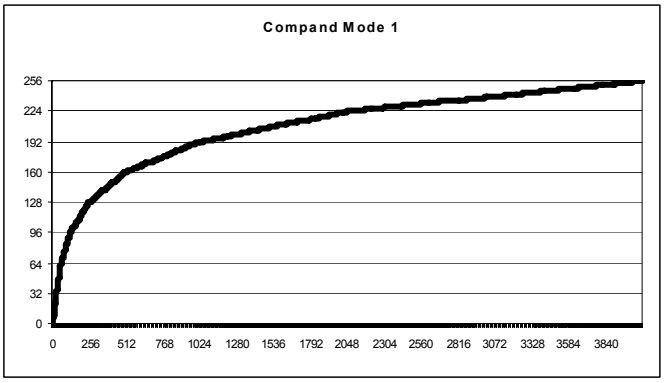
CONFIGROW enables a packet of data to be output on the PIXDATA bus during vertical blanking. The data is embedded in the last row of vertical blanking and is prefixed with the code 0xFF, 0x00, 0x00, 0x0C. The data is always output as bytes of data regardless of the setting of 8BMODE. Thus, when 8BMODE is 0, the data is broken up as 3 bytes of data every 2 pixels (12 bits). When 8BMODE is 1, then the config row matches the data width. The following table lists the bytes of data in the config row:

Bit #	Name	VALUE	Function
1–3	SYNC	0xFF 0x00 0x00	SYNC indicator. Note that this pattern can occur in the image data unless embedded sync is enabled.
4	TYPE	0x0C	Config Row indicator
5–6	Length	48	Number of bytes following these 2 bytes. The most significant 8-bits are sent first.
7	VERSION	0	Version of the Configuration Row
8	Key	0x03	Frame Count Key
9–10	FrameCount		16-bit incrementing frame count. MSBs are sent first.
11	Key	0x06	Integration Time Key
12–13	Tint		Integration Time used on this frame. See the INTTIME register for more details. 4 MSBs are always zero.
14	Key	0x2E	Image Average Red Key
15–16	AVGRED		Image Average of the Red Channel. See the RAVG register for more details.
17	Key	Ox2F	Image Average GreenRed Key
18–19	AVGGrR		Image Average of the GreenRed Channel
20	Key	0x30	Image Average GreenBlue Key
21–22	AVGGrB		Image Average of the GreenBlue Channel
23	Key	0x31	Image Average Blue Key
24–25	AVGBLUE		Image Average of the Blue Channel
26	Key	0x32	Image Average Luminance Key
27–28	AVGLUM		Image Average of the sum of all 4 color Channels
29	Key	0x33	Black Level Key
30–31	BLKLVL		Black Level that was subtracted from this frame. See the BLKLVL register for more details
32	Key	0x34	Noise Variance key
33–34	NoiseVar		Noise Variance computed for this frame. See the NOISEVAR register for more details.
35	Key	0x34	RGAIN Key
36–37	RGAIN		Red Gain. 4 MSBs are always 0
38	Key	0x34	GrGain Key
39–40	GrGAIN		GreenRed Gain. 4 MSBs are always 0.
41	Key	0x34	GreenBlue Key
42–43	GbGAIN		GreenBlue Gain. 4 MSBs are always 0
44	Key	0x34	BGAIN Key
45–46	BGAIN		Blue Gain. 4 MSBs are always 0.
47–48	EndPkt	0x00	2 bytes of zero

COMPAND enables a 12-bit to 8-bit non-linear companding of the data. This enhances the dynamic range but allows the processor to work with 8-bit pixels. Normally the 8-bits are output on the most significant 8-bits unless 8BMODE is 1. There are two companding functions provided. CMPFMT selects between these two formats.

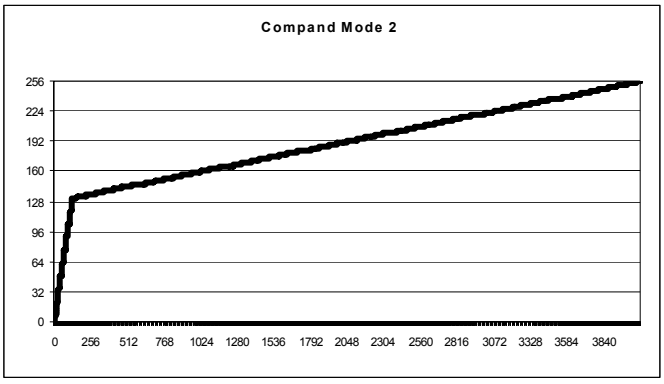
Companding format 1: Modified A-law

12-bit original	8-bit	12-bit recovered
000000wxyzab	00wxyzab	000000wxyzab
000001wxyzab	010wxyza	000001wxyza0
00001wxyzabc	011wxyza	00001wxyza00
0001wxyzabcd	100wxyza	0001wxyza000
001wxyzabcde	101wxyza	001wxyza0000
01wxyzabcdef	110wxyza	01wxyza00000
1wxyzabcdefg	111wxyza	1wxyza000000



Companding format 2: Simple 2-segment

12-bit original	8-bit	12-bit recovered
00000wxyzabc	0wxyzabc	00000wxyzabc
wxyzabcdefgh	1xyzaabc	1wxyzabc0000



8BMODE simply shifts the PIXDAT bus to the right by 4 bits. This allows a linear mapping of 12-bit to 8-bits by simply dividing the pixel value by 16.

DARKENB enables the dark pixels to be output on the PIXDAT bus as if they were part of the image. This mode is usually used for testing purposes but can be used to improve noise reduction if black-level correction is turned off and instead the function is performed by the back-end processor.

8.2.33 SYNCPOL(3A)

Bit #	Name	DIR	Default	Function
7	VSYNCPOL	RW	0	0 = VSYNC Active Low 1 = VSYNC Active High
6	HSYNCPOL	RW	0	0 = HSYNC Active Low 1 = HSYNC Active High
5	EXTRACLK	RW	0	0 = PIXLCK only when pixels are present 1 = One extra PIXCLK when a row starts and ends
4	DATVAL	RW	0	0 = PIXCLK only clocks when HSYNC is inactive; HSYNC is a SYNC pulse 1 = PIXCLK clocks continuously; HSYNC is a DATVAL pulse
3	PCLKPOL	RW	0	0 = PIXDATA transitions relative to the falling edge of PIXCLK 1 = PIXDATA transitions relative to the rising edge of PIXCLK
2	Reserved	R	0	
1:0	MOD	RW	00	00 = PIXCLK on valid data only 01 = PIXCLK on valid data and on ROWEND 02 = PIXCLK on valid data and when HSYNC inactive 03 = PIXCLK freeruns

The SYNCPOL register provides polarity control of the pixel data output pins. VSYNC will be high during Vertical Blanking time when VSYNCPOL = 1. HSYNC will be high during the Horizontal Blanking time when HSYNCPOL = 1. The edge that PIXDATA transitions on can be selected with the PCLKPOL bit. Normally PCLKPOL will want to be zero which sets the rising edge of PIXCLK in the middle of a clock period where PIXDATA is stable. This will insure sufficient setup and hold times across a flex cable to the back-end processor. If the back-end processor clocks data in on the falling edge of the clock or if there is a significant amount of delay of PIXCLK, PCLKPOL may be programmed with a 1.

DATVAL = 1 changes the functionality of the HSYNC pin to be a “Data Valid” signal instead of a synchronization pulse. This mode is normally used when MOD = 11 as PIXCLK is free-running and the back-end processor needs a signal to tell it when valid data is present on the PIXDATA bus.

The MOD bits provide four different clocking modes that provide different options for clocking data into the back-end processor. The simplest mode is MOD=00 where PIXCLK runs only when there is valid data on the PIXDATA bus. The problem with this mode is that there are no clocks during HSYNC and VSYNC and many back-end processors need a few clocks during this time.

If the back-end processor needs to clock in HSYNC and VSYNC, use MOD = 01. This mode provides one extra clock each row at the end of a row. This insures that HSYNC and VSYNC are sampled by the back-end processor. Note that this will increase the size of the image by 1 pixel and this pixel must be ignored when doing image processing.

If PIXCLK needs to free-run during the syncs, use MOD = 10. In this mode it is assumed that the back-end processor knows that it does not need to clock in the data when HSYNC is active. Note that PIXCLK will skip some pulses during the active portion of a row if binning is enabled.

If PIXCLK needs to always free-run, then use MOD = 11. In this mode PIXCLK is the same as CLK except that it is delayed by the internal clock buffers to match the output delay on the PIXDATA bus. In this mode DATVAL is normally set to 1 so that the back-end processor knows which pixels have valid data or not. Some back-end processors are able to compute where the valid pixels are in a row but care must be taken to properly align the data.

8.2.34 TSTPTN(3B)

Bit #	Name	DIR	Default	Function
2:0	TSTPTN	RW	00	000 = Test pattern disabled 001 = SMPTE colorbars 010 = Incrementing gradient in X 011 = Incrementing gradient in Y 1XX = Reserved

The TSTPTN register enables a test pattern to be output. There are three test patterns available. The standard SMPTE color bars pattern, a 12-bit incrementing gradient in X and a 12-bit incrementing gradient in Y.

8.2.35 FLIP(3C)

Bit #	Name	DIR	Default	Function
1	MIRROR	RW	0	0 = Normal operation 1 = Mirror image in X
0	FLIP	RW	0	0 = Normal operation 1 = Flip Image in the Y dimension

The MIRROR bit is used to reverse the order that pixels are read out which allows the image to be mirrored in the X dimension. In this case, the column counter is decremented instead of being incremented. Note that the Dark Rows on the left and right side of the image are still read out first so they can be used for Row FPN reduction. COLS should be programmed with the rightmost red column of active pixels to insure proper Bayer pattern alignment.

The FLIP bit is used to reverse the order that rows are read out of the imager. When FLIP = 1, then the ROW counter is decremented instead of being incremented. This allows the image to be flipped in the Y dimension under software control. Note that the top Dark Rows are still read out first. ROWS should be programmed with the bottom red row of active pixels to maintain proper Bayer pattern alignment.

8.2.36 DARKTOPH(3E) & DARKTOPL(3F)

Bit #	Name	DIR	Default	Function
11:0	DARKTOP	RW	0x0F0	Bit mask of valid rows to use for Dark Current Statistics

The DARKTOP registers make up a 12-bit register. Each bit of the register enables the respective dark row at the top of the imager. If the bit is a 1, then the row is used in the dark current calculation. If the bit is 0, then the row is ignored. DARKTOP[0] corresponds to row 0, DARKTOP[1] corresponds to row 1 and so on. At least 4 rows must be turned on to properly compute the dark current. By default, the middle 4 rows are turned on which typically are the best for computing the dark current.

8.2.37 GPIO(60)

Bit #	Name	DIR	Default	Function
7	LEVEL	RW	0	Write = Level driven onto GPIO if enabled Read = Level on the GPIO pin
6	TRISTATE	RW	1	0 = Drive LEVEL onto the GPIO pin 1 = GPIO is tristate
5	KEEP	RW	0	0 = Bus Keeper is disabled 1 = Bus Keeper enabled
4	INENB	RW	1	0 = Input is disabled 1 = Input is enabled
3	PULLDIR	RW	0	0 = Pull down 1 = Pull up
2	PULLENB	RW	1	0 = Pull-up/down resistor disabled 1 = Pull-up/down resistor enabled
1	DRV	RW	1	0 = 8 mA drive 1 = 2 mA drive
0	VSEL	RW	0	0 = Vddio 1.8V 1 = Vddio 2.8–3.3V

The GPIO register controls the state of the GPIO pin. The GPIO pin is a general purpose IO pin that is controlled via this register. The default state of the GPIO pins is for a weak pulldown resistor to pull the pin to ground and insure a proper logic level even if the pin is left unconnected.

The LEVEL bit is used to set the output level of the GPIO pin when TRISTATE is 0. Note that when this bit is read, it reflects the current level on the GPIO pin and not the value programmed in the LEVEL bit of this register. Thus, when TRISTATE is a 1, this bit is effectively a read-only bit that is the current logic level of the GPIO pin.

The TRISTATE bit is used to program the GPIO pin as either an input or an output. When TRISTATE = 0, the GPIO pin is an output and the value programmed in the LEVEL bit will be driven onto the GPIO pin. If TRISTATE = 1, the GPIO pin is an input.

The KEEP bit will enable a weak bus keeper on the GPIO pin. If TRISTATE = 1 and PULLENB = 0, this pin should be programmed as a 1 to insure a valid logic level is maintained on the GPIO pin. GPIO should not be allow to float.

The INENB bit enables the input. If TRISTATE=1 this bit should be a 1. This pin also gates the bus keeper function so it has to be 1 for the bus keeper to be enabled.

PULLDIR determines the direction of the optional pull-up resistor. 0 = pull-down, 1 = pull-up.

The PULLENB bit enables an on-chip pull-up or pull-down resistor. PULLDIR selects if a pull-up or pull-down is selected.

DRV selects the drive strength of the output driver. 0 = 8 mA nominal drive, 1 = 2 mA low-power drive. The 2-mA drive strength is recommended to keep power consumption low.

The VSEL bit must be programmed to match the power supply that Vddio is connected to. If Vddio is connected to a 1.8V supply, then VSEL must be programmed with a 0. If Vddio is connected to a 2.8 to 3.3V supply, then VSEL must be programmed with a 1.

8.2.38 I²CIO(61)

Bit #	Name	DIR	Default	Function
7		R	0	Reserved
6	PDIRA3	RW	0	0 = SBIA3 Pulled down 1 = SBIA3 Pulled up
5	PEA3	RW	1	0 = Disable Pull-up/down on SBIA3 1 = Enable Pull-up/down on SBIA3
4	KEEP	RW	0	0 = Disable Bus Keeper on SDAT 1 = Enable Bus Keeper on SDAT
3	PULLDIR	RW	1	0 = Pull down on SCLK, SDAT 1 = Pull up on SCLK, SDAT
2	PULLENB	RW	1	0 = Pull-up/down resistor disabled on SCLK, SDAT 1 = Pull-up/down resistor enabled on SCLK, SDAT
1	DRV	RW	1	0 = 8 mA drive on SDAT 1 = 2 mA drive on SDAT
0	VSEL	RW	0	0 = Vddio 1.8V on SDAT 1 = Vddio 2.8–3.3V on SDAT

The I²CIO register controls the IO pin settings of the SBIA3, SCLK and SDAT I²C pins. SCLK and SBIA3 are input only pins but each pin has its own control bits for a pull-up or pull-down resistor. SCLK and SDAT share the same pull-up/down controls. SDAT is a bidirectional pin and has an additional 2 control bit for selecting the IO voltage and drive strength as well as a weak Bus Keeper function.

8.2.39 PCLKIO(62)

Bit #	Name	DIR	Default	Function
7		R	0	Reserved
6	TRISTATE	RW	0	0 = PIXCLK enabled 1 = PIXCLK tri-stated
5	KEEP	RW	0	0 = Bus Keeper disabled 1 = Bus Keeper enabled
4		R	1	Reserved
3	PULLDIR	RW	0	0 = Pull Down 1 = Pull Up
2	PULLENB	RW	0	0 = Pull-up/down resistor disabled 1 = Pull-up/down resistor enabled
1	DRV	RW	0	0 = 8 mA drive on PIXCLK 1 = 2 mA drive on PIXCLK
0	VSEL	RW	0	0 = Vddio 1.8V on PIXCLK 1 = Vddio 2.8–3.3V on PIXCLK

The PCLKIO register controls the IO pin settings of the PIXCLK pin. PIXCLK can operate at up to 48 MHz so individual control of the IO pin is provided to meet the timing and drive strength needs of the application. The TRISTATE bit will tri-state the PIXCLK pin. When PIXCLK is tri-state, the KEEP or the PULLENB bit must be set or an external pull-up resistor must be used to insure that PIXCLK does not float or the pin will draw excess power. The DRV and VSEL bits select the drive strength and Vddio voltage respectively.

8.2.40 PIXIO(63)

Bit #	Name	DIR	Default	Function
7		R	0	Reserved
6	TRISTATE	RW	0	0 = Outputs enabled 1 = Tri-stated
5	KEEP	RW	0	0 = Bus Keeper disabled 1 = Bus Keeper enabled
4		R	1	Reserved
3	PULLDIR	RW	0	0 = Pull Down 1 = Pull Up
2	PULLENB	RW	0	0 = Pull-up/down resistor disabled 1 = Pull-up/down resistor enabled
1	DRV	RW	1	0 = 8 mA drive 1 = 2 mA drive
0	VSEL	RW	0	0 = Vddio 1.8V on PIXCLK 1 = Vddio 2.8–3.3V on PIXCLK

The PIXIO register controls the IO pin settings of the D[11:0], HSYNC and VSYNC pins. The TRISTATE bit will tri-state the pins. When the pins are tri-state, the KEEP or the PULLENB bit must be set or an external pull-up resistor must be used to insure that the pins do not float or there will be excess power consumed. The DRV and VSEL bits select the drive strength and Vddio voltage respectively.

8.2.41 PWRCTL(70)

Bit #	Name	DIR	Default	Function
7:1		R	0	Reserved
0	IMGDIS	RW	0	0 = Normal Operation 1 = Disable Image Sensor Logic

The PWRCTL register controls the power consumption of the CYIWOSC3000AA Imager. The Imager powers-up in normal active mode ready to begin full operation once the registers have been initialized. The default state of PWRCTL corresponds to power Mode 1 (Active).

Power Mode 2 (Standby) is achieved by setting the TRIIO bits in the PCLKIO and PIXIO registers. This tri-states the IO pins and reduces power consumption. Power consumption is only slightly reduced however the imager is continuing to accumulate statistics and ready to take an image on the very next frame.

Power Mode 3 (Full Standby) is achieved by setting the IMGDIS bit to a 1. In this mode, the imager is turned off and no video data is produced and no statistics are computed. All registers retain their current state and are ready to begin image capture once IMGDIS is cleared to 0. Power consumption is reduced as the timing signals to the image array are static and no data is flowing through the digital logic. The PIX bus IOs are static as well. Note that since no statistics are being computed, the exposure control and FPN algorithms will need several frames to stabilize before a valid image is ready to capture.

8.2.42 RESET(7E)

Bit #	Name	DIR	Default	Function
7:0	RESET	W		Write a 0x52 to reset the entire chip.

Writing a 0x52 to the RESET register causes the entire chip to be reset. Writing any value other than 0x52 (ASCII ‘R’) has no effect. Note that the reset takes place as soon as the I^2C ACK bit is started. Thus, the imager will not ACK the data byte of the I2C command as it is now in reset and waiting for an I^2C START command.

8.2.43 SYNC(7F)

Bit #	Name	DIR	Default	Function
7	ENB	RW	0	0 = Immediate access to all registers 1 = Enable Synchronization mode This bit is automatically cleared once the VSYNC has updated the registers
6	NextVsync	RW	0	0 = No updates to the registers 1 = Update all registers on the next VSYNC. This bit is automatically cleared once the VSYNC has updated the registers.
5	VBLANK	R		0 = Not currently in VBLANK 1 = Imager is currently in VBLANK

Critical configuration registers have a shadow register in their write path. This allows these registers to be loaded with a new value but it won't take effect until just before the next frame begins. When ENB is 0, the shadow register is disabled and access is direct to the register. Note that changing many of the row/column registers during an active frame time will cause a bad frame to be output. When ENB is 1, then any write to a register with a shadow register causes the write to be stored but not take effect until the NextVsync bit is a 1 and VSYNC begins.

Note that register reads always come from the currently active register. When ENB = 1, after you write to a register, if you immediately read the register you will get the old value, not the value you just wrote. Once NextVsync = 1 and VSYNC has occurred, then the new value can be read from the register.

The VBLANK bit may be used to update a small number of registers during the vertical blanking time. This is a read only bit. Software can simply poll this bit and wait until it is a one (or transitions to a one) and then write a few registers directly without causing bad frames.

Once the ENB and the NextVsync bit are set, no register writes should be performed until the registers have been updated. The ENB bit will be cleared to 0 when the registers are updated. There is a small chance that a write to a register will happen just as the other registers are being updated at VSYNC and the write conflict will result in unpredictable operation.

Usage examples:

1. Initial power-up
   a. The imager is currently off and we wish to configure the registers as quickly as possible.
   b. ENB = 0, NextVsync = X (don't care but usually 0).
   c. Write all configuration registers
   d. Enable the back-end processor to begin searching for a VSYNC pulse to begin processing frame data. The first frame may be a partial frame with bad data.

2. Change from video sub-windowed mode to full image capture mode
   a. ENB = 1, NextVsync = 0
   b. Write all registers that need to be updated for the new capture mode
   c. NextVsync = 1
   d. Wait until NextVsync = 0, which indicates that the registers have been updated. The next frame should begin immediately and be in the new format. Do not write to any other registers while waiting for NextVsync to change to 0.

NOTE: Registers in *Table 8-1* labeled with a 1 are controlled by the SYNC bit. Note that many of the other registers are effectively SYNCed as they are only used by internal logic at specific times during a frame. See the individual register descriptions for more details.

8.3 Status Registers

8.3.1 GrAVGH(80) & GrAVGL(81)

Bit #	Name	DIR	Default	Function
15:0	GrAVG	R		Green-Red pixel value average

The GrAVG registers make up a sixteen-bit register split across two 8-bit registers. The value is the average intensity value in a 12.4 fixed point format for all green pixels on the red row in the area defined by the ROI registers. The upper twelve bits are the integer portion and the lower four bits provide a fractional value. This register is updated at the end of the active pixels and before vertical blanking. The register always contains a valid value of the most recent frame.

8.3.2 GbAVGH(82) & GbAVGL(83)

Bit #	Name	DIR	Default	Function
15:0	GbAVG	R		Green-Blue pixel value average

The GbAVG registers are the average intensity value for all green pixels on the blue row in the area defined by the ROI registers. This register is updated at the end of the active pixels and before vertical blanking. The register always contains a valid value of the most recent frame.

8.3.3 RAVGH(84) & RAVGL(85)

Bit #	Name	DIR	Default	Function
15:0	RAVG	R		Red pixel value average

The RAVG registers are the average intensity value for all red pixels in the area defined by the ROI registers. This register is updated at the end of the active pixels and before vertical blanking. The register always contains a valid value of the most recent frame.

8.3.4 BAVGH(86) & BAVGL(87)

Bit #	Name	DIR	Default	Function
15:0	BAVG	R		Blue pixel value average

The BAVG registers are the average intensity value for all blue pixels in the area defined by the ROI registers. This register is updated at the end of the active pixels and before vertical blanking. The register always contains a valid value of the most recent frame.

8.3.5 LUMAVGH(88) & LUMAVGL(89)

Bit #	Name	DIR	Default	Function
15:0	LUMAVG	R		Pixel value average

The LUMAVG registers are the average intensity value for all pixels in the area defined by the ROI registers. This register is updated at the end of the active pixels and before vertical blanking. The register always contains a valid value of the most recent frame.

8.3.6 REPLPIX(A0)

Bit #	Name	DIR	Default	Function
7:0	REPLPIX	R		Number of Pixels Replaced

The REPLPIX register is a count of the number of pixels that have been replaced by the Pixel Replacement algorithm. If more than 255 pixels have been replaced, the value is clipped to 255.

8.3.7 CURROW(A1)

Bit #	Name	DIR	Default	Function
7:0	CURROW	R		Eight MSBs of the Current row

The CURROW register contains the eight most-significant bits of the 11-bit Row counter. Thus, CURROW indicates where the imager is currently reading data from the image array. Note that this value may jump quickly from one part of the image to the

other when sub-windowed. A value of zero indicates that a new frame has just started. A value above 196 indicates we are in vertical blanking.

8.3.8 NOISEVARH(A2) & NOISEVARL(A3)

Bit #	Name	DIR	Default	Function
15:0	NOISEVAR	R		Variance of the noise in the Top Dark pixels.

The NOISEVAR register is a 16-bit register which holds the noise variance of the current frame. The noise variance is the square of the difference of a pixel and the previous frames BLKLVL. The noise variance is accumulated for 214 pixels in the Top Dark Rows. The noise variance is typically used to assist the image processing software in setting limits on gain to maintain a reasonable signal-to-noise ratio.

8.3.9 ACTROWSH(A4) & ACTROWSL(A5)

Bit #	Name	DIR	Default	Function
11:0	ACTROWS	R		Number of active pixels per row

The ACTROWS register provides a count of the number of Active Rows per frame. The number of Active Rows per frame depends on the setting of many registers and may be difficult to compute. This register provides an easy way to determine the number of Active Rows per frame for the current operating mode.

8.3.10 ACTCOLSH(A6) & ACTCOLSL(A7)

Bit #	Name	DIR	Default	Function
11:0	ACTCOLS	R		Number of active pixels per column

The ACTCOLS register provides a count of the number of Active Pixels per row. The number of Active pixels per row depends on the setting of many registers and may be difficult to compute. This register provides an easy way to determine the number of Active pixels per row for the current operating mode.

8.3.11 COLCNT(A8) & COLCNT(A9)

Bit #	Name	DIR	Default	Function
11:0	COLCOUNT	R		Number of clocks per row

The COLCNT register is a read-only register that provides the number of clocks per row. It is a twelve bit register and hence if more than 4096 clocks/row are programmed the register will reset to 0 and begin the next count.

8.3.12 TINTAEH(AA) & TINTAEL(AB)

Bit #	Name	DIR	Default	Function
11:0	TINTAE	R		Integration time in rows when AutoExposure is enabled

The TINTAE register is a read-only register that provides the current Integration time when the AutoExposure unit is enabled. The Integration time typically changes every frame when the Auto Exposure unit is enabled. This register is updated just before the start of a new frame and is the value being used while the frame is being captured.

9.0 Feature Descriptions

9.1 HiSENS™

This circuit provides reduced readout noise using circuitry both inside and peripheral to the imaging area.

9.2 Power Saver Settings

There are three power modes on the sensor to provide a balance of imager performance and power consumption, as described in *Table 9-1*.

The imager default (power-up) setting is in Power Mode 1 but will inhibit output video until it has stabilized to avoid displaying bad frame data. Significant power savings can be obtained by running the imager at a slower clock frequency, reducing the active pixel area (subwindowing) or by sub-sampling the image. This allows the imager to run in an active preview mode at substantially reduced power levels but return briefly to a high power mode when taking a full 3MP capture.

9.3 Selectable Frame Rate

Frame rate can be adjusted by a number of factors. The CLK frequency sets the basic frame rate and can be as high as 48 MHz. To readout a full 3MP image in 1/14th of a second requires a 48-MHz CLK. The frame rate can also be adjusted by varying the number of Vblank rows. The number of Vblank rows can be up to 4095, allowing for a wide range of frame rates. Subwindowing will also increase the frame rate as fewer rows need to be read out. Note that binning does not increase the frame rate as the imager must still collect all of the pixels but the data rate out of the pixel data bus is significantly lower in these modes.

Windowing into a relatively small number of rows can increase the frame rate for high-speed auto-focus applications. Reading out just the middle third of the image area will increase the frame rate by 3X. Decreasing the number of columns does not change the frame rate as all pixels in a row must be read out to keep the row timing consistent.

Table 9-1. Power Modes

Mode	Video Operation	Serial Communication Operation
Active (Power Mode 1)	Full functionality Digital video output	Full functionality Registers retain settings
Standby with exposure (Power Mode 2)	Imager maintains exposure No video is output	Read all registers Write to Power Register only Registers retain settings
Full Standby (Power Mode 3)	No Imager operation No video is output	Read all registers Write to Power Register only Registers retain settings

Table 9-2. Typical Power Consumption in Common Operating Modes

Power Mode	Operation	Analog and Digital Power Consumption (V_{DDD} = 1.8V, V_{DDA} = 2.8V)
Full Frame Full Speed Capture	2048 x 1536 14 fps with 48-MHz Clk	I_{DDA} = 59 mA I_{DDD} = 27 mA P = 215 mW
Preview Mode	640 x 480 30 fps with 18-MHz Clk	I_{DDA} = 15 mA I_{DDD} = 9 mA P = 60 mW
Standby/Idle Mode	Reset Low CLK = 0 Hz	I_{DDA} = 1μA I_{DDD} = 3 μA P = 8 μW

9.4 FPN Reduction

Column Fixed Pattern Noise Reduction: The imager collects pattern data generated in the dark rows for fixed pattern noise and computes correction values to reduce this noise. A test voltage is applied to the ADCs during 16 rows of VBLANK and the results are accumulated and stored in a special Row Buffer. This offset is then subtracted digitally. This subtraction is done to all pixels including the dark pixels.

Point Defect Correction: Pixels operating outside of the response of their neighbors may be defective. The CYIWOSC3000AA imager will compare the response of the neighbor pixels and will replace the defective pixel with the nearest same color. All of these modes can be disabled via software.

9.5 Black Level Setting and Averaging

The electronic and dark current induced offsets that cause black level errors will be removed on-chip. The imager will collect statistics on the electronic black level from optically shielded pixels. These statistics will provide an average value for subtracting from active pixels. The first 8096 pixels in the top 12 dark rows are accumulated and an average is calculated. The remaining pixels in the image have this value subtracted from them. This algorithm has the advantage of collecting statistics for the current frame and applying them immediately which will improve quality as it will track changes in Tint. Pixels that have the upper 4 MSbs set are not included in the black level calculation. This insures that “hot” pixels are ignored which might otherwise cause the average to be unusually high. There is a mask register that allows any of the 12 rows to be not used in the black level calculation. This allows certain rows to be excluded which are found to not be truly black. Only four rows are typically needed for the black level calculation.

9.6 Digital Gain per Color

A 12x12 multiplier can be applied to each of the four color channels (R, Gr, Gb and B) individually via registers. The default is to multiply by 1 which has no effect. These multipliers provide digital gain typically used correct the responsivity of the color masks. If the color value exceeds 12 bits after the multiplication, then the color is saturated to the maximum value. The multiplication factor is in a 12-bit register with a 4.8 fixed point format. The value is rounded to the nearest by adding 128 to the result before shifting right by 8.

9.7 Exposure Control

The imager provides for both automatic and manual control of the exposure or integration period. The exposure control algorithm sets the imager base integration period to set the average pixel value at a default or user specified level. In addition to setting the desired image average, the user may limit the integration period available to the automatic control. These registers may be used to prevent the integration from exceeding motion blur limits in dark environments.

9.8 Resolution Control

The imager contains several blocks to control the output resolution and field of view (FOV). By combining these blocks, many combinations of resolution/FOV are available to the user via register setting.

9.9 Sub-window Control

The imager can be read out at any sub-frame resolution on Bayer boundaries (odd columns and even rows) down to 2H X 2V pixels. The blanking time minimums are required. The size of the sub-window is specified in the registers by setting the coordinates of the corners. The location of the sub-window can start at any Bayer boundary.

9.10 Analog On-chip Binning

Binning can be performed in the analog domain to independently combine pixels in the horizontal and vertical dimensions with factors of 2, 3 (Vertical only) and 4 adjacent Bayer pixels. By combining pixels the low-light signal-to-noise ratio is increased. The imager architecture was tuned for on-chip binning factors of 2, 3, and 4. Binning by 3 can only be done in the vertical dimension. Analog Binning has the advantage that it increases the frame rate. However, binning by more than 2X is not as flexible in analog as it is in digital. Analog binning is also lower power than digital binning. Generally, analog binning by 2 should be used whenever possible.

9.11 Digital On-chip Binning

The imager provides additional digital binning to support reduced resolution output modes. Digital binning can be performed in both the horizontal and vertical dimensions. Vertical binning is limited to 2X and 4X. Horizontal binning can be any combination of 2, 3, or 4X in two stages. Thus, horizontal binning can be 2, 3, 4, 6, 8, 9, 12, or 16X. There are two pixel weighting modes for digital binning. The weighting for each pixel can either be the normal 1:1 weighting, or a special mode where the appropriate color of the Bayer pattern is weighted more favorably based on the location in the super-pixel. Subsampling can be performed instead of binning, which increases the frame rate and lowers power consumption, however the image may tend to “sparkle” due to aliasing artifacts. Subsampling in the vertical dimension will increase the frame rate however subsampling in the horizontal dimension will not. It is recommended to subsample vertically wherever possible and always use binning in the horizontal dimension.

9.12 50-/60-Hz Flicker Reduction

Flicker reduction involves setting the Integration Time to be a multiple of either 100 or 120 Hz. This will insure that in relatively low-light situations where the lighting is likely to be from fluorescent bulbs, the image does not “beat” with the flicker of the fluorescent bulbs. Software must perform this function and properly set the Integration Time to be a multiple of 100 or 120 Hz.

9.13 Blanking Time, PCLK and Sync Polarity

The polarity of the HSYNC, VSYNC, and PCLK signals can be inverted by setting the proper register. Additional HBlank pixels and VBlank rows can be added to the image frame by setting the appropriate registers.

9.14 Power-on Reset

The CYIWOSC3000AA powers up automatically to default register mode operation as specified in this document. No serial communications are required on power-up to initiate image capture, the imager will output video imagery at full resolution with associated sync signals. The RESET_N signal should be asserted until both power supplies have reached their proper voltage level and the CLK is stable.

9.15 On-chip Test Pattern Generation

A test pattern will be output from the imager when set by the registers to provide a standard SMPTE color bar pattern. This is to assist with system development and testing. A representation of the test pattern is shown in *Figure 9-1* with RGB values of 8-bit depth. The output of the test pattern will be in raw Bayer form and each sample may be adjusted on chip using the digital gain per color channel registers. A configuration row of data may optionally be inserted into row 0 of the image. This configuration row contains data such as the Frame Number. Tint value and other parameters. This mode is only used for testing and debug.

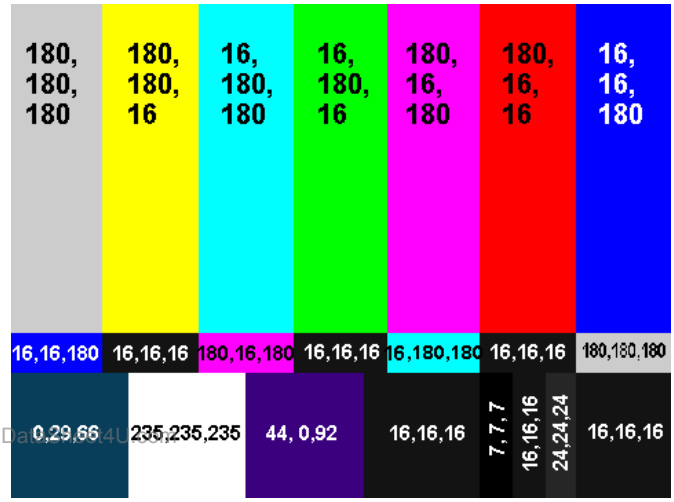


Figure 9-1. SMPTE Color Bars

9.16 Exposure Control Region of Interest (ROI)

The camera includes a region of interest feature that can be used to influence the automatic control of the integration period. The region is defined by specifying the upper left and lower right corners of a rectangle using pixel row and column numbers. The exposure calculations can generated with pixels within the region or on those that lie outside the region.

9.17 Register Setting Sync Control

Most of the configuration registers have a shadow register that will hold the new value until the next VSYNC. This insures that all of the registers are updated at the same time and no bad frames are output. See the definition of the SYNC register for more details.

9.18 Preview and Video Mode

The imager generates a video signal at up to 14 fps (full frame) with internally generated clocks and synchronization signals. These synchronization signals are output to other devices together with the processed image data.

9.19 Parallel Digital Interface

The CYIWOSC3000AA image sensor offers 8 and 12-bit parallel digital interfaces. This interface is configured to operate in a variety of modes to maximize compatibility with a variety of DSP interfaces and other custom applications.

The imager samples and processes 12-bit data. If an 8-bit output is selected, the 12-bit data is mapped to 8-bit either with a fixed non-linear curve or linear mapping.

The Parallel Digital Output option will have the following output modes:

1. 12-bit data out, with HSYNC, VSYNC, PCLK
2. 8-bit data out with HSYNC, VSYNC, PCLK
3. Each of the previously mentioned modes with embedded sync. The HSYNC and VSYNC are embedded by substituting raw pixel values of assigned sync levels. This will allow client devices to sync up to the timing codes in the data stream.

10.0 Electrical Specifications

10.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Storage Temperature: ..... .–30°C to 85°C

Input Voltage: ..... –0.2V to V_{CC} +0.2V

ESD Susceptibility (HBM): 2000V

10.2 Operating Conditions

Supply Voltage: ..... 2.8 and 1.8VDC

Operating Temperature: ..... –30°C to +70°C

11.0 Electrical Characteristics

The following specifications apply for T_A = 25°C Environmental Specifications

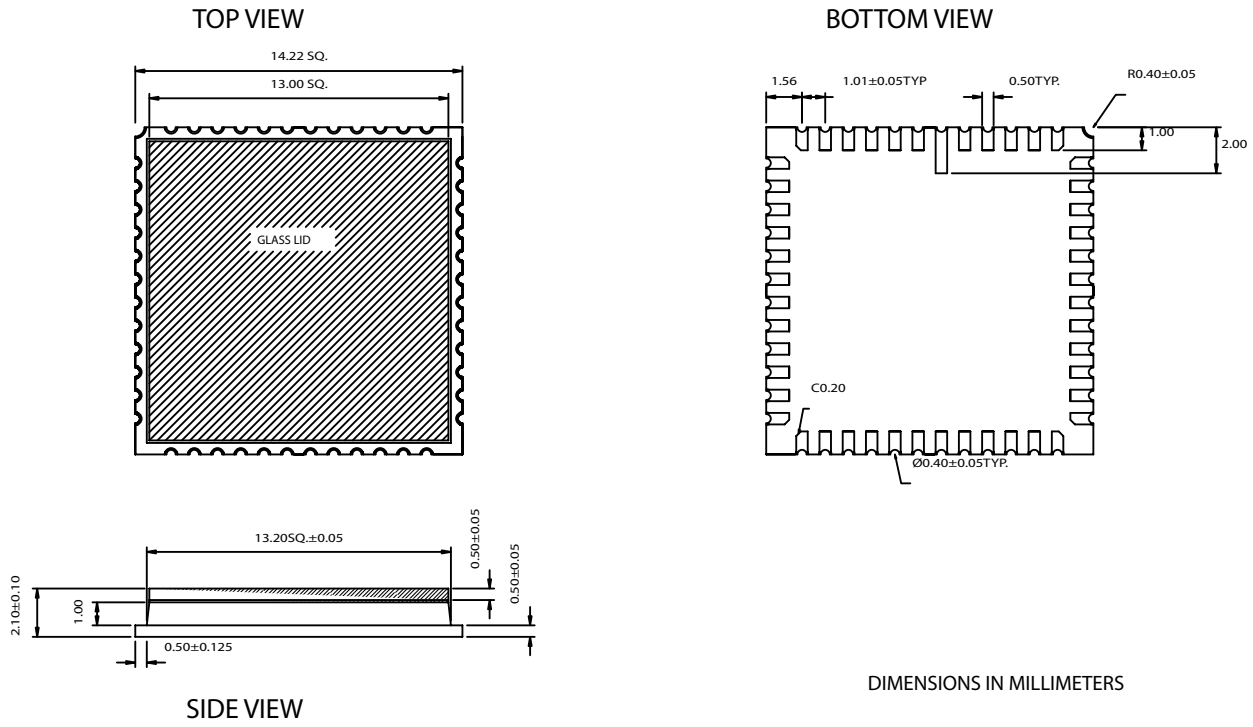
Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Vdd	Digital Supply voltage		1.65	1.8	2.0	V
Vaa	Analog Supply voltage		2.5	2.8	3.1	V
P	Analog and Digital Power Consumption	@ 30 fps (640 x 480)		60		mW
		@ 14 fps (2048 x1536)		215		mW
Digital I/O						
V_{OH28}	Output level [high]	I_{OH} = –4.0 mA	Vaa – 0.2			V
V_{OL28}	Output level [low]	I_{OL} = 4.0 mA	0.2			V
V_{OH18}	Output level [high]		Vdd – 0.2			V
V_{OL18}	Output level [low]		0.2			V
V_{IH28}	Input level [high]		Vaa – 0.3		Vaa + 0.3	V
V_{IL28}	Input level [low]		–0.3		0.3	V
V_{IH18}	Input level [high]		Vdd – 0.3		Vdd + 0.3	V
V_{IL18}	Input level [low]		–0.3		0.3	V
I_{LOAD}	Input leakage current	V_I = 0V to 3.0V			10	µA
C_{IN}	Input capacitance	V_{IN} = 0V, f = 1.0 MHz			10	pF
C_{OUT}	Output capacitance	V_{IN} = 0V, f = 1.0 MHz			12	pF
PCLK max	Pixel Output rate				48	MHz

Table 11-1. Environmental Specifications

Specification	Value	Comment
Operating Junction Temperature	–30°C to +70°C	See performance specifications for sensitivity de-rating over temperature
Storage Temperature	–30°C to 85°C	Junction
Dust	100 mg/m^3	-

12.0 48-Pin PLCC Package Diagram



PART # TABLE	
QP48A	WINDOWED PLASTIC LEADLESS CHIP CARRIER (STANDARD)
QY48A	WINDOWED PLASTIC LEADLESS CHIP CARRIER (LEAD FREE)

Figure 12-1. 48-Pin PLCC Package Diagram

12.1 Ordering Information

Table 12-1. Ordering Information

Ordering Code	Package Name	Package Type
CYIWOSC3000AA - QYC	QY48A	48-Pin PLCC Package

Purchase of I^2C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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Document History Page

Document Title: CYIWOSC3000AA 3.1 Megapixel CMOS Sensor Document Number: 38-19009				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	355657	See ECN	HBH	New data sheet
*A	384066	See ECN	HBH	Added detail to meet final product specifications
*B	414413	See ECN	SYT	Converted from Preliminary to Final Changed Optical Format from 1.3” to 1.28 “ Removed 10-bit Parallel Data Port Information Added Analog and Digital Power Consumption specs Changed the True Output Dynamic Range from 72 dB to 60 dB Removed the SNR_{MAX} for XGA and QVGA resolutions Changed the SNR_{MAX} spec from 42 to 39 and 51.5 to 43 for the QXGA and the VGA resolutions respectively. Changed Analog Supply Voltage from 2.65V - 3.1V to 2.5V - 3.1V I^2C made consistent in the whole of the document Corrected typo in the ROWNUMH/ROWNUML and COLNUMH/COLUMNL descriptions on Page #: 14 and 15 Appended information for RESET(7E) register description on Page# 27 Edited the COLCNT register descriptions on Page # 30 Changed the contents of Table 8.2 Changed Vaa min from 2.52 to 2.5 V in Table #9.1 Included “Frames per Second and Integration Time Calculation” section. Removed Salt Mist Atmosphere, Chemical Resistance and Humidity specifications from Table # 10.0
*C	416566	See ECN	SYT	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed the Max Data Rate/Master Clock Rate from 100 MPS/100 MHz to 48 MPS/48 MHz Changed Frame Rate from 30 fps to 14 fps for 2048 x 1536 mode and from 83 fps to 80 fps for 640 x 480 mode. Changed the Dynamic Range from 55 dB to 60 dB Included unit for SNR_{MAX} Changed SNR_{MAX} from 39 to 35 dB for QXGA and from 43 to 40 db for VGA Changed the Analog and Digital Power consumption spec from 55mW @ 30 fps (640 x 480) to 60 mW and 195 mW @ 15 fps (2048x1536) to 215 mW @ 14 fps. Changed the clock frequency for Preview mode from 12Mhz to 18 Mhz on Table 8-2 on Page # 31
*D	431055	See ECN	SYT	Added 48-PLCC Package Diagram
*E	436607	See ECN	QGS	Updated Bond Diagram for 48-PLCC Package on Page # 5. Added Note on Page # 5. Changed time required to read out a single row to COLCNT / CLK FREQ from CLK FREQ / COLCNT on Page # 10. Added HBLANK register number (0x8, 0x9) on Page 10.