# CYM1946

# 512K x 32 Static RAM Module

## Features

- **High-density 16-megabit SRAM module**
- **32-bit Standard Footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed SRAMs**
  - **— Access time of 35 ns**
- **Low active power**
  - **— 7.3W (max.) at 35ns**
- **Compatible with CYM1821, CYM1831, CYM1836, CYM1841, and CYM1851 JDEC Modules**

## Functional Description

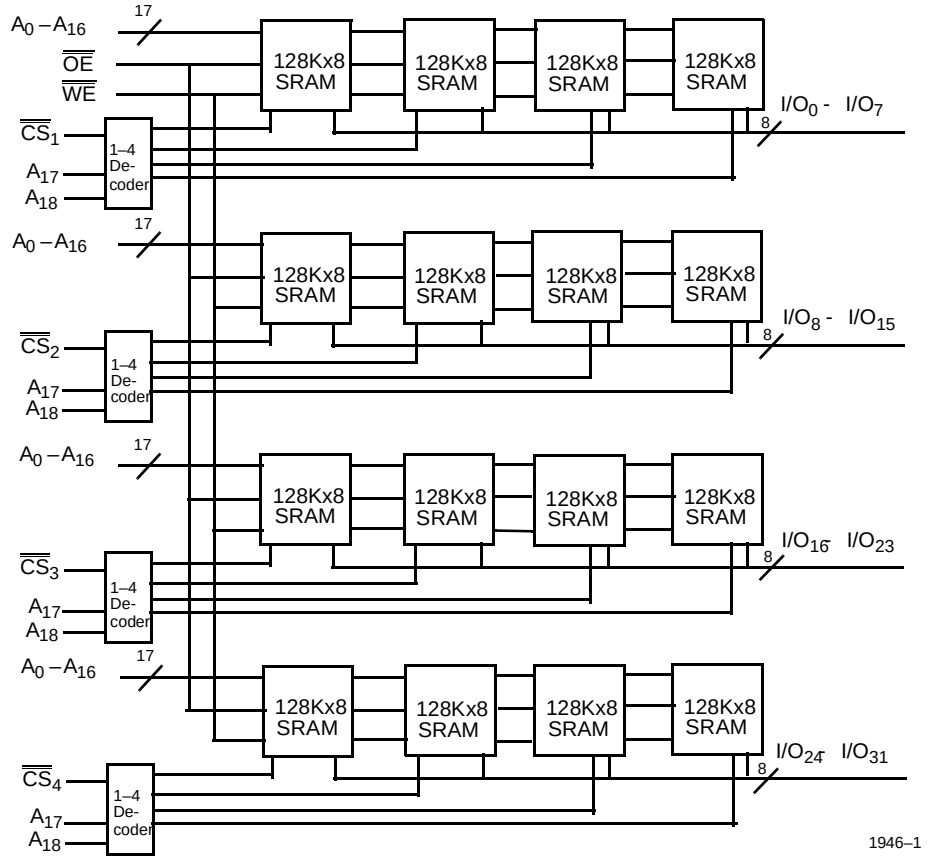
The CYM1946 is a high-performance 16-megabit static RAM module organized as 512K words by 32 bits. This module is constructed from 16 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The CYM1946 is designed for use with standard 72-pin SIMM sockets. The pinout is downward compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841). Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1,024K words (CYM1851).

Presence detect pins ($PD_0$–$PD_3$) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.

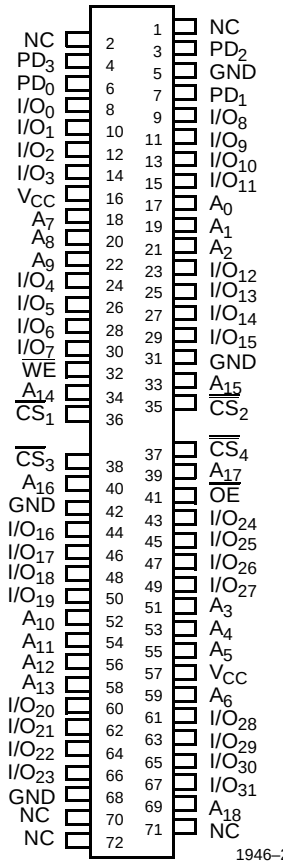
## Logic Block Diagram

$PD_0$ - OPEN
$PD_1$ - OPEN
$PD_2$ - GND
$PD_3$ - OPEN




## Pin Configuration

**ZIP/SIMM Top View**



## Selection Guide

| | 1946-35 | 1946-45 | 1946-55 |
|---|---|---|---|
| Maximum Access Time (ns) | 35 | 45 | 55 |
| Maximum Operating Current (mA) | 1100 | 1100 | 1100 |
| Maximum Standby Current (mA) | 585 | 585 | 585 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–55°C to +125°C

Ambient Temperature with Power Applied.....–10°C to +85°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +$V_{CC}$

DC Input Voltage .....–0.5V to +7.0V

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.3 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –32 | +32 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | | –20 | +20 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, $\overline{CS}_N$ ≤ $V_{IL}$ | –35, –45, –55 | | 1100 | mA |
| $I_{SB1}$ | Automatic $\overline{CS}$ Power-Down Current[1] | Max. $V_{CC}$, $\overline{CS}$ ≥ $V_{IH}$, Min. Duty Cycle = 100% | | | 585 | mA |
| $I_{SB2}$ | Automatic $\overline{CS}$ Power-Down Current[1] | Max. $V_{CC}$, $\overline{CS}$ ≥ $V_{CC}$ – 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V, or $V_{IN}$ ≤ 0.2V | –35, –45, –55 | | 200 | mA |

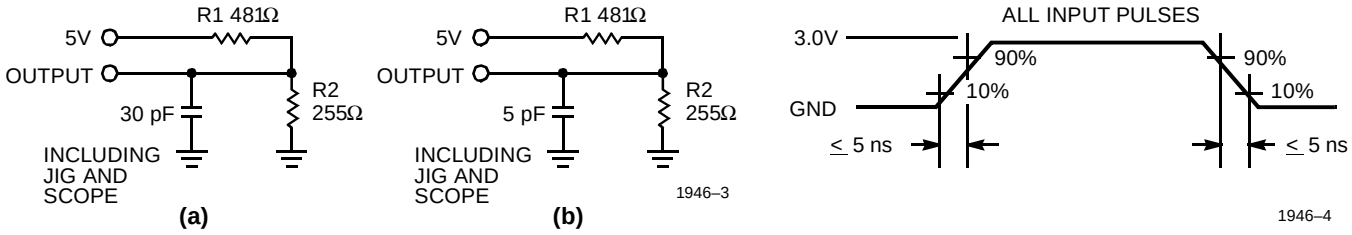
## Capacitance[2]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{INA}$ | Input Capacitance ($\overline{WE}$, $\overline{OE}$, $A_{0–16}$) | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 175 | pF |
| $C_{INB}$ | Input Capacitance ($\overline{CS}$) | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 45 | pF |
| $C_{INA17–18}$ | Input Capacitance $A_{17–18}$ | | 45 | pF |

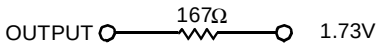
**Notes:**

1. A pull-up resistor to $V_{CC}$ on the $\overline{CS}$ input is required to keep the device deselected during $V_{CC}$ power-up, otherwise $I_{SB}$ will exceed values given.
2. Tested on a sample basis.

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT




## Switching Characteristics Over the Operating Range[3]

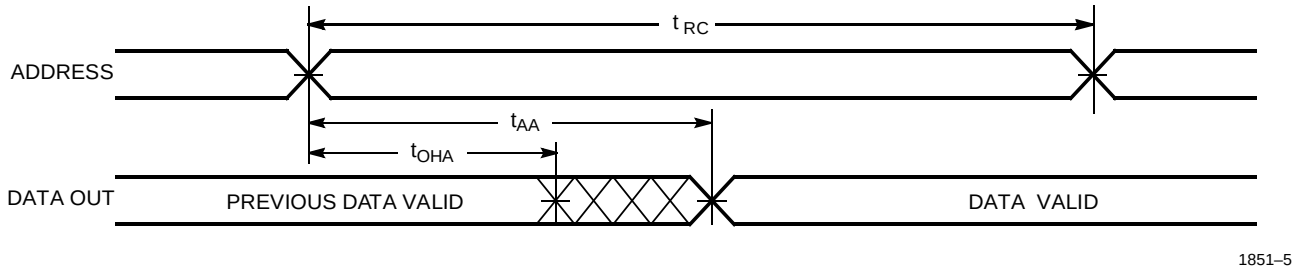
| Parameter | Description | 1946-35 | | 1946-45 | | 1946-55 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 35 | | 45 | | 55 | | ns |
| $t_{AA}$ | Address to Data Valid | | 35 | | 45 | | 55 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 5 | | 5 | | 5 | | ns |
| $t_{ACS}$ | $\overline{CS}$ LOW to Data Valid | | 35 | | 45 | | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 15 | | 17 | | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 0 | | 0 | | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z | | 12 | | 17 | | 22 | ns |
| $t_{LZCS}$ | $\overline{CS}$ LOW to Low Z[4] | 10 | | 10 | | 10 | | ns |
| $t_{HZCS}$ | $\overline{CS}$ HIGH to High Z[4, 5] | | 17 | | 22 | | 27 | ns |
| $t_{PD}$ | $\overline{CS}$ HIGH to Power-Down | | 35 | | 45 | | 55 | ns |
| **WRITE CYCLE**[6] | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 35 | | 45 | | 55 | | ns |
| $t_{SCS}$ | $\overline{CS}$ LOW to Write End | 30 | | 40 | | 50 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 30 | | 40 | | 50 | | ns |
| $t_{HA}$ | Address Hold from Write End | 5 | | 5 | | 5 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 2 | | 2 | | 2 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 30 | | 35 | | 45 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 20 | | 25 | | 35 | | ns |
| $t_{HD}$ | Data Hold from Write End | 7 | | 7 | | 7 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 5 | | 5 | | 5 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[5] | | 15 | | 15 | | 15 | ns |

**Notes:**

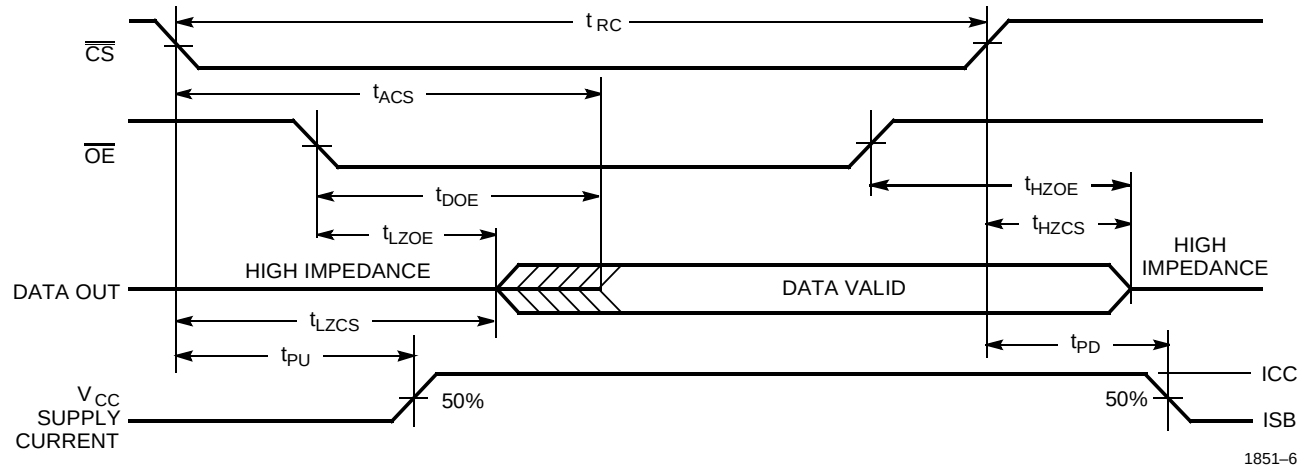
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
4. At any given temperature and voltage condition, $t_{HZCS}$ is less than $t_{LZCS}$ for any given device. These parameters are guaranteed and not 100% tested.
5. $t_{HZCS}$ and $t_{HZWE}$ are specified with $C_L$ = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Waveforms

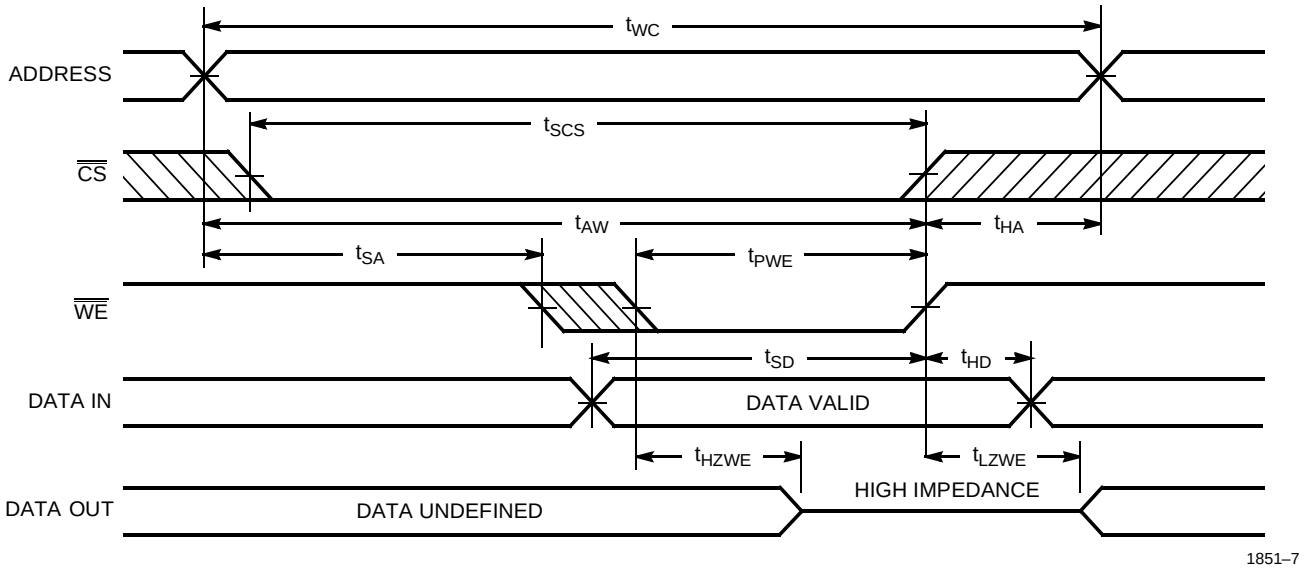
**Read Cycle No. 1** [7,8]




**Read Cycle No. 2** [7,9]



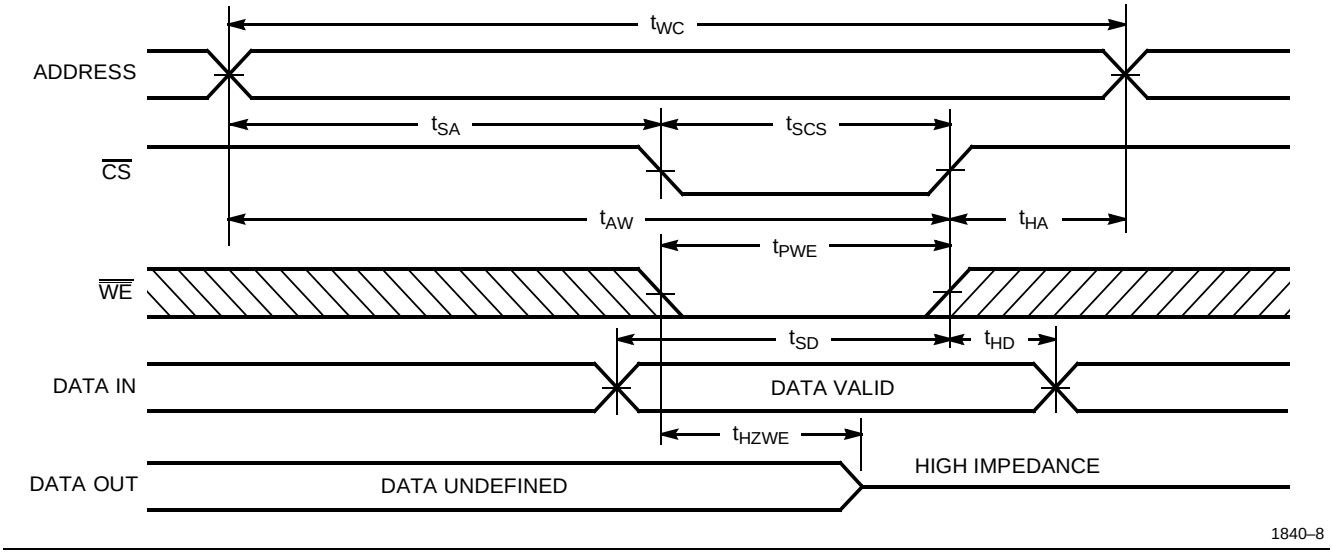

**Write Cycle No. 1 ($\overline{WE}$ Controlled)** [6]




**Notes:**
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = $V_{IL}$, and $\overline{OE}$= $V_{IL}$.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

## Switching Waveforms (continued)

**Write Cycle No. 2 ($\overline{CS}$ Controlled)** [6,10]




**Note:**
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

## Truth Table

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Output | Mode |
|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power-Down |
| L | H | L | Data Out | Read |
| L | L | X | Data In | Write |
| L | H | H | High Z | Deselect |

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|---|---|---|---|---|
| 35 | CYM1946PM-35C | PM47 | 72-Pin Plastic SIMM Module | Commercial |
| 45 | CYM1946PM-45C | PM47 | 72-Pin Plastic SIMM Module | Commercial |
| 55 | CYM1946PM-55C | PM47 | 72-Pin Plastic SIMM Module | Commercial |

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## Package Diagram

**72-Pin Plastic SIMM Module PM47**