CYNSE70032
Network Search Engine

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1.0 Overview

Cypress Semiconductor Corporation's (Cypress's) CYNSE70032 network search engine (NSE) incorporates patent-pending Associative Processing Technology™ (APT) and is designed to be a high-performance, pipelined, synchronous, 16K-entry NSE. The CYNSE70032 database entry size can be 68, 136, or 272 bits. In the 68-bit entry mode, the size of the database is 16K entries. In the 136-bit mode, the size of the database is 8K entries, and in the 272-bit mode, the size of the database is 4K entries. The CYNSE70032 is configurable to support multiple databases with different entry sizes. The 36-bit entry table can be implemented using the global mask registers (GMRs) building-database size of 32K entries with a single device.

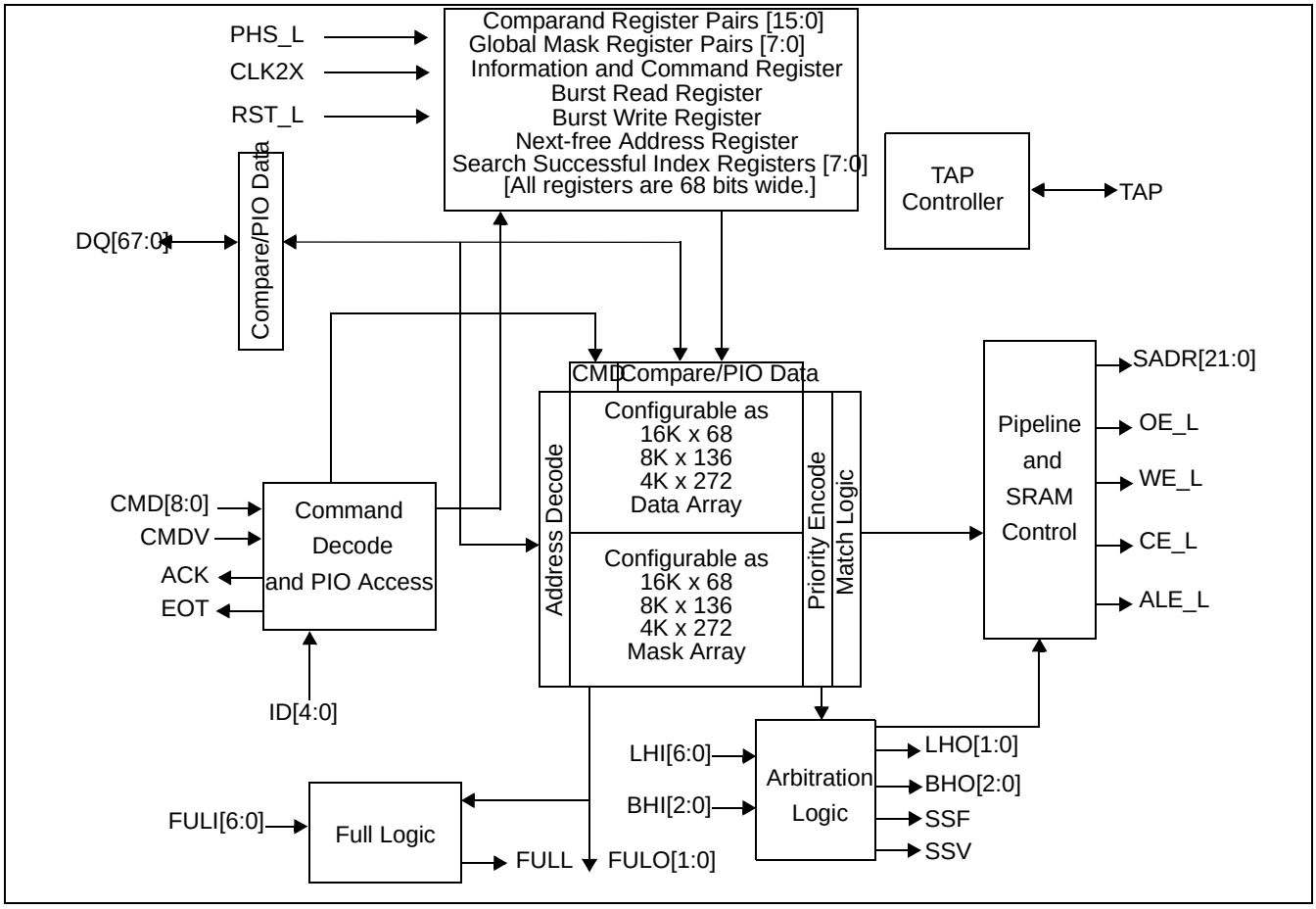
The search engine can sustain 83 million transactions per second when the database is programmed or configured as 68 or 136 bits. When the database is programmed to have an entry size of 34 or 272 bits, the search engine will perform at 41.5 million transactions per second. The CYNSE70032 can be used to accelerate network protocols such as longest-prefix match (CIDR), address-resolution protocol (ARP), multiprotocol label switching (MPLS), and other layer 2, 3, and 4 protocols.

This high-speed, high-capacity NSE can be deployed in a variety of networking and communications applications. The performance and features of the CYNSE70032 device make it attractive in applications such as Enterprise local-area network (LAN) switches and routers and broadband switching and/or routing equipment supporting multiple data rates at OC-48 and beyond. The NSE is designed to be scalable in order to support network database sizes of up to 992K entries specifically for environments that require large network policy databases. The block diagram for the CYNSE70032 device is shown on page 10.

2.0 CYNSE70032 Features

- **32K 34-bit entries in a single device**
- **16K entries in 68-bit mode, 8K entries in 136-bit mode, 4K entries in 272-bit mode**
- **83 million transactions per second in 68- and 136-bit configurations**
- **41.5 million transactions in 34- and 272-bit configurations**
- **Searches any subfield in a single cycle**
- **Synchronous pipelined operation**
- **Up to 31 NSEs can be cascaded**
- **When cascaded, the database entries can range to 992K 36-bit entries**
- **Multiple width tables in a single database bank**
- **Glueless interface to industry standard SRAMs and/or SSRAMs**
- **Simple hardware instruction interface**
- **IEEE 1149.1 test access port**
- **1.8V core voltage supply**
- **2.5/3.3V I/O voltage supply**
- **272-pin BGA package**.

3.0 Block Diagram



4.0 Functional Description

The following subsections contain the following descriptions: command (CMD) and DQ bus (command and databus), database entry, arbitration logic, pipeline and SRAM control, and full logic.

4.1 Command Bus and DQ Bus

CMD[8:0] carries the command and its associated parameter. DQ[67:0] is used for data transfer to and from the database entries, which is made up of data and mask fields that are organized as data and mask arrays. The DQ bus carries the Search data (of the data and mask arrays and internal registers) during the Search command, as well as the address and data during Read or Write operations. The DQ bus can also carry address information for the flow-through accesses to the external SRAMs or SSRAMs.

4.2 Database Entry (Data Array and Mask Array)

Each database entry comprises a data and a mask field. The resultant value of the entry is “1,” “0,” or “X (don’t care),” depending on the value in the data mask bit. The on-chip priority encoder selects the first matching entry in the database that is nearest to location 0.

4.3 Arbitration Logic

When multiple search engines are cascaded to create large databases, the data being searched is presented simultaneously to all search engines in the cascaded system. If multiple matches occur within the cascaded devices, arbitration logic on the search engines will enable the winning device (with a matching entry that is closest to address 0 of the cascaded database) to drive the SRAM bus.

4.4 Pipeline and SRAM Control

Pipeline latency is added to give enough time to a cascaded system's arbitration logic to determine the device that will drive the index of the matching entry on the SRAM bus. Pipeline logic adds latency to both the SRAM access cycles and the SSF and SSV signals in order to align them to the host ASIC that receives the associated data.

4.5 Full Logic

Bit[0] in each of the 68-bit entries has a special purpose for the Learn command (0 = empty, 1 = full). When all the data entries have bit[0] set to 1, the database asserts the FULL flag, indicating that all the search engines in the depth-cascaded array are full.

5.0 Signal Descriptions

Table 5-1 lists and describes all CYNSE70032 signals.

Table 5-1. CYNSE70032 Signal Description

Parameter	Type[1]	Description
Clocks and Reset		
CLK2X	I	**Master Clock**. CYNSE70032 samples all the data and control pins on the positive edge of CLK2X. All signals are driven out of the device on the rising edge of CLK2X (when PHS_L is low).
PHS_L	I	**Phase**. This signal runs at half the frequency of CLK2X and generates an internal clock from CLK2X. See Section 6.0, "Clocks" on page 13.
RST_L	I	**Reset**. Driving RST_L low initializes the device to a known state.
Command and DQ Bus		
CMD[8:0]	I	**Command Bus**. [1:0] specifies the command and [8:2] contains the command parameters. The descriptions of individual commands explains the details of the parameters. The encoding of commands based on the [1:0] field are: 00: PIO Read 01: PIO Write 10: Search 11: Learn.
CMDV	I	**Command Valid**. This signal qualifies the command bus: 0: No command 1: Command.
DQ[67:0]	I/O	**Address/Data Bus**. This signal carries the Read and Write address and data during register, data, and mask array operations. It carries the compare data during Search operations. It also carries the SRAM address during SRAM PIO accesses.
ACK[2]	T	**Read Acknowledge**. This signal indicates that valid data is available on the DQ bus during register, data, and mask array Read operations, or that the data is available on the SRAM data bus during SRAM Read operations.
EOT[2]	T	**End of Transfer**. This signal indicates the end of burst transfer to the data or mask array during Read or Write burst operations.
SSF	T	**Search Successful Flag**. When asserted, this signal indicates that the device is the global winner in a Search operation.
SSV	T	**Search Successful Flag Valid**. When asserted, this signal qualifies the SSF signal.
SRAM Interface		
SADR[21:0]	T	**SRAM Address**. This bus contains address lines to access off-chip SRAMs that contain associative data. See *Table 15-1* for the details of the generated SRAM address. In a database of multiple CYNSE70032 devices, each corresponding bit of the SRAM address from all cascaded devices must be connected.
CE_L	T	**SRAM Chip Enable**. This is the chip-enable control for external SRAMs. In a database of multiple CYNSE70032 devices, CE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.
WE_L	T	**SRAM Write Enable**. This is the write-enable control for external SRAMs. In a database of multiple CYNSE70032 devices, WE_L of all cascaded devices must be connected together. This signal is then driven by only one of the devices.

Notes:
1. I = Input only, I/O = Input or Output, O = Output only, T = three-state output.
2. ACK and EOT require a weak external pull-down such as 47KΩ or 100KΩ.

Table 5-1. CYNSE70032 Signal Description (continued)

Parameter	Type[1]	Description
OE_L	T	**SRAM Output Enable**. This is the output-enable control for external SRAMs. Only the last device drives this signal (with the LRAM bit set).
ALE_L	T	**Address Latch Enable**. When this signal is low, the addresses are valid on the SRAM address bus. In a database of multiple CYNSE70032s, the ALE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.
Cascade Interface		
LHI[6:0]	I	**Local Hit In**. These pins depth cascade the device to form a larger table. One signal of this bus is connected to the LHO[1] or LHO[0] of each of the upstream devices in a block. All unused LHI pins are connected to a logic 0. (For more information, see Section 14.0, “Depth-Cascading” on page 96.)
LHO[1:0]	O	**Local Hit Out**. LHO[1] and LHO[0] are the same logical signal. Either the LHO[1] or the LHO[0] is connected to one input of the LHI bus of up to four downstream devices in a block of up to eight. (For more information see Section 14.0, “Depth-Cascading” on page 96.)
BHI[2:0]	I	**Block Hit In**. Inputs from the previous block BHO[2:0] are tied to the BHI[2:0] of the current device. In a four-block system, the last block can contain only seven devices because the identification code 11111 is used for broadcast access.
BHO[2:0]	O	**Block Hit Out**. These outputs from the last device in a block are connected to the BHI[2:0] inputs of the devices in the downstream blocks.
FULI[6:0]	I	**Full In**. Each signal in this bus is connected to FULO[0] or FULO[1] of an upstream device to generate the FULL flag for the depth-cascaded block.
FULO[1:0]	O	**Full Out**. FULO[1] and FULO[0] are the same logical signal. One of these two signals must be connected to the FULI of up to four downstream devices in a depth-cascaded table. Bit[0] in the data array indicates whether the entry is full (1) or empty (0).This signal is asserted if all bits in the data array are 1s. (Refer to Section 14.0, “Depth-Cascading” on page 96, for information on how to generate the FULL flag.)
FULL	O	**Full Flag**. When asserted, this signal indicates that the table of multiple depth-cascaded devices is full.
Device Identification		
ID[4:0]	I	**Device Identification**. The binary-encoded device identification for a depth-cascaded system starts at 00000 and goes up to 11110. 11111 is reserved for a special broadcast address that selects all cascaded search engines in the system. On a broadcast Read-only, the device with the LDEV bit set to 1 responds.
Supplies		
V_{DD}	n/a	**Chip Core Supply**. 1.8V.
V_{DDQ}	n/a	**Chip I/O Supply**. 2.5V or 3.3V.
Test Access Port		
TDI	I	Test Access Port’s Test Data In.
TCK	I	Test Access Port’s Test Clock.
TDO	T	Test Access Port’s Test Data Out.
TMS	I	Test Access Port’s Test Mode Select.
TRST_L	I	Test Access Port’s Reset.

6.0 Clocks

The CYNSE70032 device receives the CLK2X and PHS_L signals. It uses the PHS_L signal to divide CLK2X and generate an internal clock (CLK[3]), as shown in *Figure 6-1*. The CYNSE70032 device uses CLK2X and CLK for internal operations.

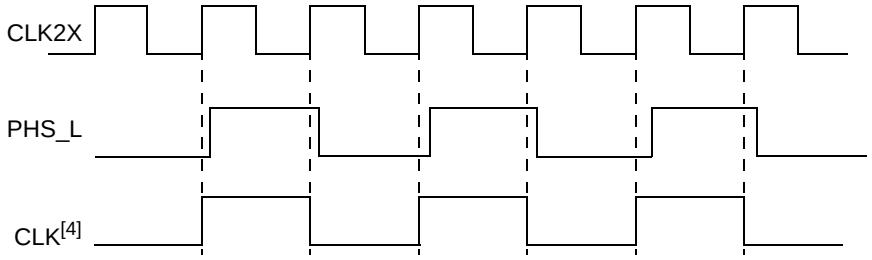


Figure 6-1. CYNSE70032 Clocks (CLK2X and PHS_L)

7.0 Registers

All registers in the CYNSE70032 are 68 bits wide. The CYNSE70032 device contains sixteen pairs of comparand storage registers, eight pairs of GMRs, eight search successful index registers and one each of command, information, burst Read, burst Write, and next-free address registers. *Table 7-1* provides an overview of all the CYNSE70032 registers. The registers are listed in ascending address order. Each register group is then described in the subsections that follow.

Table 7-1. Register Overview

Address	Abbreviation	Type	Name
0–31	COMP0–31	R	Sixteen pairs of comparand registers that store comparands from the DQ bus for learning later.
32–47	MASKS	RW	Eight GMR pairs.
48–55	SSR0–7	R	Eight search successful index registers.
56	COMMAND	RW	Command register.
57	INFO	R	Information register.
58	RBURREG	RW	Burst Read register.
59	WBURREG	RW	Burst Write register.
60	NFA	R	Next-free address register.
61–63	–	–	Reserved.

7.1 Comparand Registers

The device contains 32 68-bit comparand registers (sixteen pairs) dynamically selected in every Search operation to store the comparand presented on the DQ bus. The Learn command will later use these registers when it is executed. The CYNSE70032 device stores the Search command's cycle A comparand in the even-numbered register and its cycle B comparand in the odd-numbered register, as shown in *Figure 7-1*.

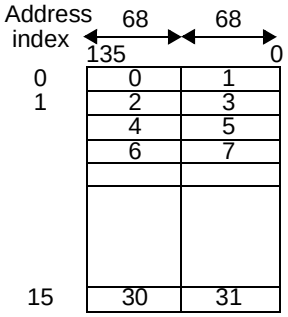


Figure 7-1. Comparand Register Selection during Search and Learn Instructions

Notes:
3. Any reference to "CLK" cycles means one cycle of CLK.
4. ."CLK" is an internal clock signal.

7.2 Mask Registers

The device contains sixteen 68-bit global mask registers (eight pairs) dynamically selected in every Search operation to select the search subfield. The addressing of these registers is explained in *Figure 7-2*. The three-bit GMR Index supplied on the CMD bus can apply eight pairs of global masks during the Search and Write operations, as shown below. ***Note***. In 68-bit Search and Write operations, the host ASIC must program both the even and odd mask registers with the same values.

Index	68 (135)	68 (0)
0	0	1
1	2	3
2	4	5
3	6	7
4	8	9
5	10	11
6	12	13
7	14	15

Search and Write Command Global Mask Selection

Figure 7-2. Addressing the Global Mask Register Array

Each mask bit in the GMRs is used during Search and Write operations. In Search operations, setting the mask bit to 1 enables compares; setting the mask bit to 0 disables compares (forced match) at the corresponding bit position. In Write operations to the data or mask array, setting the mask bit to 1 enables writes; setting the mask bit to 0 disables writes at the corresponding bit position.

7.3 Search Successful Registers (SSR[0:7])

The device contains eight SSRs to hold the index of the location where a successful search occurred. The format of each register is described in *Table 7-2*. The Search command specifies which SSR stores the index of a specific Search command in cycle B of the Search instruction. Subsequently, the host ASIC can use this register to access that data array, mask array, or external SRAM using the index as part of the indirect access address (see *Table 7-2* and *Table 8-1*). The device with a valid bit set performs a Read or Write operation. All other devices suppress the operation.

Table 7-2. Search Successful Register Description

Field	Range	Initial Value	Description
INDEX	[13:0]	X	**Index**. This is the address of the 68-bit entry where a successful Search occurs. The device updates this field only when the Search is successful. If a hit occurs in a 136-bit entry-size quadrant, the least significant bit (LSB) is 0. If a hit occurs in a 272-bit entry-size quadrant, the two LSBs are 00. This index updates if the device is either a local or global winner in a Search operation.
–	[30:14]	0	**Reserved**.
VALID	[31]	0	**Valid**. During a Search operation in a depth-cascaded configuration, the device that is a global winner in a match sets this bit to 1. It updates only when the device is a global winner in a Search operation.
–	[67:32]	0	**Reserved**.

8.0 Command Register

Table 8-1 describes the command register fields.

Table 8-1. Command Register Description

Field	Range	Initial Value	Description
SRST	[0]	0	**Software Reset**. If 1, this bit resets the device with the same effect as a hardware reset. Internally, it generates a reset pulse lasting for eight CLK cycles. This bit automatically resets to 0 after the reset has completed.
DEVE	[1]	0	**Device Enable**. If 0, it keeps the SRAM bus (SADR, WE_L, CE_L, OE_L, and ALE_L), SSF, and SSV signals in a three-state condition and forces the cascade interface output signals LHO[1:0] and BHO[2:0] to 0. It also keeps the DQ bus in input mode. The purpose of this bit is to make sure that there are no bus contentions when the devices power up in the system.

Table 8-1. Command Register Description (continued)

Field	Range	Initial Value	Description
TLSZ	[3:2]	01	**Table Size**. The host ASIC must program this field to configure the chips into a table of a certain size. This field affects the pipeline latency of the Search and Learn operations as well as the Read and Write accesses to the SRAM (SADR[21:0], CE_L, OE_L, WE_L, ALE_L, SSV, SSF, and ACK). Once programmed, the Search latency stays constant. The latency by number of CLK cycles is as follows: 00: One device 4 01: Up to eight devices 5 10: Up to 31 devices 6 11: Reserved.
HLAT	[6:4]	000	**Latency of Hit Signals**. This field further adds latency to the SSF and SSV signals by the following number of CLK cycles during searches and ACKs in an SRAM Read access: 000: 0 100: 4 001: 1 101: 5 010: 2 110: 6 011: 3 111: 7.
LDEV	[7]	0	**Last Device in the Cascade**. When set, this is the last device in the depth-cascaded table and is the default driver for the SSF and SSV signals. In the event of a Search failure, the device with this bit set drives the hit signals as follows: SSF = 0, SSV = 1. During nonSearch cycles, the device with this bit set drives the signals as follows: SSF = 0, SSV = 0.
LRAM	[8]	0	**Last Device on the SRAM Bus**. When set, this device is the last device on the SRAM bus in the depth-cascaded table and is the default driver for the SADR, CE_L, WE_L, and ALE_L signals. In cycles where no CYNSE70032 device (in a depth-cascaded table) drives these signals, the signals are driven as follows: SADR = 22'h3FFFFF, CE_L = 1, WE_L = 1, and ALE_L = 1. OE_L is always driven by the device for which this bit is set.
CFG	[16:9]	00000000	**Database Configuration**. The device is divided internally into four partitions of 8K × 68 bits, each of which can be configured as 8K × 68 bits, 4K × 136 bits, or 2K × 272 bits, as follows: 00: 4K × 68 bits 01: 2K × 136 bits 10: 1K × 272 bits 11: Reserved. Bits[10:9] apply to configuring the first partition in the address space. Bits[12:11] apply to configuring the second partition in the address space. Bits[14:13] apply to configuring the third partition in the address space. Bits[16:15] apply to configuring the fourth partition in the address space.
	[67:17]	0	**Reserved**.

9.0 Information Register

Table 9-1 describes the information register fields.

Table 9-1. Information Register Description

Field	Range	Initial Value	Description
Revision	[3:0]	0001	**Revision Number**. This is the current device revision number. Numbers start at one and increment by one for each revision of the device.
Implementation	[6:4]	000	This is the device implementation number.
Reserved	[7]	0	**Reserved**.
Device ID	[11:8]	0001	This is the device identification number.
Device ID	[12]	0 or 1	**Reserved**.
Device ID	[15:13]	000	These are the three most significant bits of the device identification number.
MFID	[31:16]	1101_1100_0111_1111	**Manufacturer ID**. This field is the same as the manufacturer identification number and continuation bits in the TAP controller.
Reserved	[67:32]		**Reserved**.

9.1 Read Burst Address Register

Table 9-2 shows the Read burst address register (RBURREG) fields that must be programmed before a burst Read.

Table 9-2. Read Burst Register Description

Field	Range	Initial Value	Description
ADR	[13:0]	0	**Address**. This is the starting address of the data or mask array during a burst Read operation. It automatically increments by one for each successive Read of the data or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:14]		**Reserved**.
BLEN	[27:19]	0	**Length of Burst Access**. The device provides the capability to Read from 4–511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[67:28]		**Reserved**.

9.2 Write Burst Address Register Description

Table 9-3 describes the Write burst address register (WBURREG) fields that must be programmed before a burst Write.

Table 9-3. Write Burst Register Description

Field	Range	Initial Value	Description
ADR	[13:0]	0	**Address**. This is the starting address of the data or mask array during a burst Write operation. It automatically increments by one for each successive write of the data or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:14]		**Reserved**.
BLEN	[27:19]	0	**Length of Burst Access**. The device provides the capability to write from 4–511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[67:28]		**Reserved**.

9.3 NFA Register

Bit[0] of each 68-bit data entry is specially designated for use in the operation of the Learn command. For 68-bit-configured quadrants, this bit indicates whether a location is full (bit set to 1) or empty (bit set to 0). Every Write or Learn command loads the address of the first 68-bit location containing a 0 into the entry's bit[0]. This is stored in the NFA register (see *Table 9-4*). If all the bits[0] in a device are set to 1, the CYNSE70032 asserts FULO[1:0] to 1.

For a 136-bit-configured quadrants, the LSB of the NFA register is always set to 0. The host ASIC must set both bit[0] and bit[68] in a 136-bit word to either 0 or 1 to indicate full or empty status. Both bit[0] and bit[68] must be set to either 0 or 1, (that is, the 10 or 01 settings are invalid).

Table 9-4. NFA Register

Address	67–14	13–0
60	Reserved	Index

10.0 NSE Architecture and Operation Overview

The CYNSE70032 device consists of 16K × 68-bit storage cells referred to as data bits. There is a mask cell corresponding to each data cell. *Figure 10-1* shows the three organizations of the device based on the value of the CFG bits in the command register.

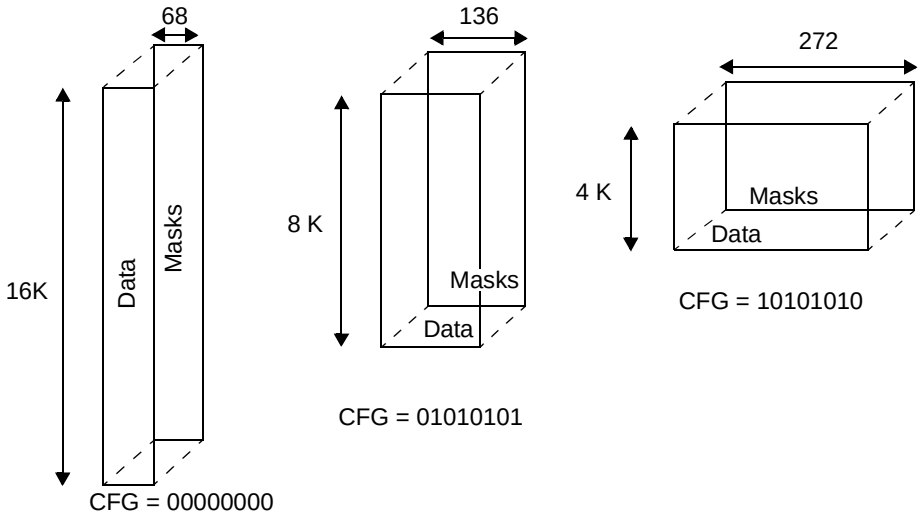


Figure 10-1. CYNSE70032 Database Width Configuration

During a Search operation, the Search data bit (S), the data array bit (D), the mask array bit (M), and the global mask bit (G) are used in the following manner to generate a match at that bit position (see *Table 10-1*). The entry with a match on every bit position results in a successful Search during a Search operation.

Table 10-1. Bit Position Match

G	M	D	S	Match
0	X	X	X	1
1	0	X	X	1
1	1	0	0	1
1	1	1	0	0
1	1	0	1	0
1	1	1	1	1

In order for a successful Search to make the device the local winner in the Search operation, all 68-bit positions within a device must generate a match for a 68-bit entry in 68-bit-configured quadrants, or all 136-bit positions must generate a match for two consecutive even and odd 68-bit entries in quadrants configured as 136 bits, or all 272-bit positions must generate a match for four consecutive entries aligned to four entry-page boundaries of 68-bit entries in quadrants configured as 272 bits.

An arbitration mechanism using a cascade bus determines the global winning device among the local winning devices in a Search cycle. The global winning device drives the SRAM bus, SSV, and the SSF signals. In the case of a Search failure, the device(s) with LDEV and LRAM bits set drive the SRAM bus, SSF, and SSV signals.

The CYNSE70032 device can be configured to contain tables of different widths, even within the same chip. *Figure 10-2* shows a sample configuration of different widths.

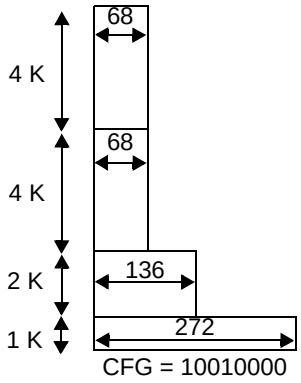


Figure 10-2. Multiwidth Database Configurations

11.0 Data and Mask Addressing

Figure 11-1 shows CYNSE70032 data and mask array addressing.

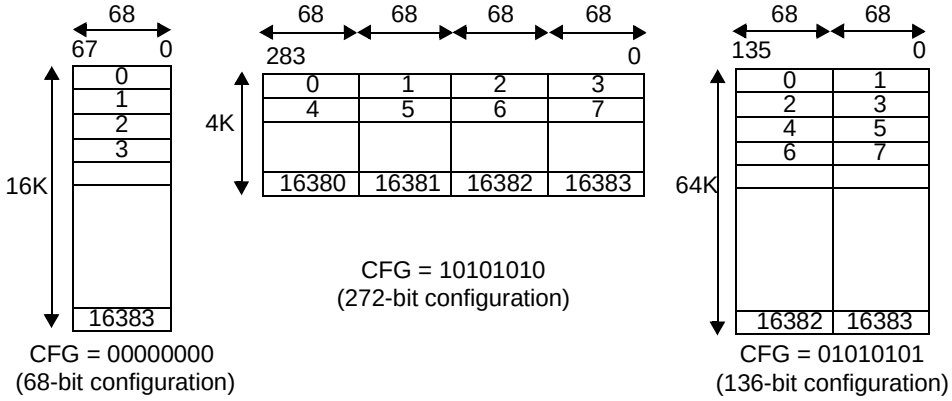


Figure 11-1. Addressing CYNSE70032 Data and Mask Arrays

12.0 Commands

A master device such as an ASIC controller issues commands to the CYNSE70032 device using the command valid (CMDV) signal and the CMD bus. The following subsections describe the operation of the commands.

12.1 Command Codes

The CYNSE70032 device implements four basic commands, shown in *Table 12-1*. The command code must be presented to CMD[1:0] while keeping the CMDV signal high for two CLK2X cycles (cycles A and B). The controller ASIC must align the instructions using the PHS_L signal. The CMD[8:2] field passes the parameters of the command in cycles A and B.

Table 12-1. Command Codes

Command Code	Command	Description
00	Read	Reads one of the following: data array, mask array, device registers, or external SRAM.
01	Write	Writes one of the following: data array, mask array, device registers, or external SRAM.
10	Search	Searches the data array for a desired pattern using the specified register from the GMR array and local mask associated with each data cell.
11	Learn	The device has internal storage for up to 16 comparands that it can learn. The device controller can insert these entries at the next free address (as specified by the NFA register) using the Learn instruction.

12.2 Commands and Command Parameters

Table 12-2 lists the CMD bus fields that contain the CYNSE70032 command parameters and their respective cycles. Each command is described separately in the subsections that follow.

Table 12-2. Command Parameters

Command	CYC	8	7	6	5	4	3	2	1	0
Read	A	SADR[21]	SADR[20]	SADR[19]	0	0	0	0 = Single 1 = Burst	0	0
	B	0	0	0	0	0	0	0 = Single 1 = Burst	0	0
Write	A	SADR[21]	SADR[20]	SADR[19]	GMR Index [2:0]			0 = Single 1 = Burst	0	1
	B	0	0	0	GMR Index [2:0]			0 = Single 1 = Burst	0	1
Search	A	SADR[21]	SADR[20]	SADR[19]	GMR Index 2:0]			68-bit or 136-bit: 0 272-bit: 1 in first cycle 0 in second cycle	1	0
	B	SSR Index[2:0]			Comparand Register Index				1	0
Learn[5]	A	SADR[21]	SADR[20]	SADR[19]	Comparand Register Index				1	1
	B	0	0	Mode 0: 68-bit 1: 136-bit	Comparand Register Index				1	1

12.3 Read Command

The Read can be a single Read of a data array, a mask array, an SRAM, or a register location (CMD[2] = 0). It can be a burst Read of the data (CMD[2] = 1) or mask array locations using an internal autoincrementing address register (RBURADR). A description of each type is provided in *Table 12-3*. A single-location Read operation lasts six cycles, as shown in *Figure 12-1*. The burst Read adds two cycles for each successive Read. The SADR[21:19] bits supplied in Read instruction cycle A drive SADR[21:19] signals during the Read of an SRAM location.

Table 12-3. Read Command Parameters

Command Parameter CMD[2]	Read Command	Description
0	Single Read	Reads a single location of the data array, mask array, external SRAM, or device registers. All access information is applied on the DQ bus.
1	Burst Read	Reads a block of locations from the data or mask arrays as a burst. The RBURADR specifies the starting address and the length of the data transfer from the data or mask array, and it autoincrements the address for each access. All other access information is applied on the DQ bus. ***Note***. The device registers and external SRAM can only be read in single-Read mode.

Note:
5. The 272-bit-configured devices or 272-bit-configured quadrants within devices do not support the Learn instruction.

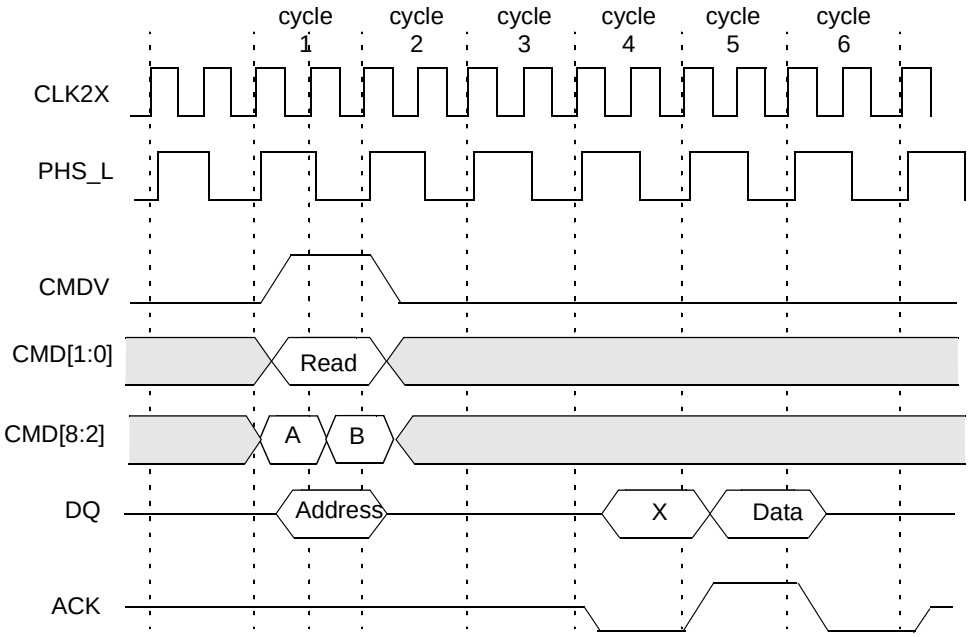


Figure 12-1. Single-Location Read Cycle Timing

The single Read operation takes six clock cycles that are performed in the following sequence.

- **Cycle 1**: The host ASIC applies the Read instruction on CMD[1:0] (CMD[2] = 0) using CMDV = 1, and the DQ bus supplies the address as shown in *Table 12-4* and *Table 12-5*. The host ASIC selects the CYNSE70032 device for which ID[4:0] matches the DQ[25:21] lines. If DQ[25:21] = 11111, the host ASIC selects the CYNSE70032 with the LDEV bit set. The host ASIC also supplies SADR[21:19] on CMD[8:6] in cycle A of the Read instruction if the Read is directed to the external SRAM.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive the DQ[67:0] bus, and drives the ACK signal from Z to low.
- **Cycle 5**: The selected device drives the Read data from the addressed location on the DQ[67:0] bus, and drives the ACK signal high.
- **Cycle 6**: The selected device floats the DQ[67:0] to a three-state condition and drives the ACK signal low.

At the termination of cycle 6, the selected device releases the ACK line to a three-state condition. The Read instruction is complete, and a new operation can begin. ***Note***. The latency of the SRAM Read will be different than the one described above (see Subsection 15.2, “SRAM PIO Access” on page 99). *Table 12-4* lists and describes the format of the Read address for a data array, mask array, or SRAM.

Table 12-5 describes the Read address format for the internal registers. *Figure 12-2* illustrates the timing diagram for the burst Read of the data or mask array.

Table 12-4. Read Address Format for Data Array, Mask Array, or SRAM

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20:19]	DQ [18:14]	DQ[13:0]
Reserved	0: Direct 1: Indirect	SSR Index (applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is 0, this field carries the address of the data array location. If DQ[29] is 1, the SSR Index specified on DQ[28:26] is used to generate the address of the data array location: {SSR[13:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSR Index (applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is 0, this field carries the address of the mask array location. If DQ[29] is 1, the SSR Index specified on DQ[28:26] is used to generate the address of the mask array location: {SSR[13:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSR Index (applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is 0, this field carries the address of the SRAM location. If DQ[29] is 1, the SSR Index specified on DQ[28:26] is used to generate the address of the SRAM location: {SSR[13:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]

Note:
6. “ | ” stands for logical OR operation. “{}” stands for concatenation operator.

Table 12-5. Read Address Format for Internal Registers

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	ID	11: Register	Reserved	Register Address

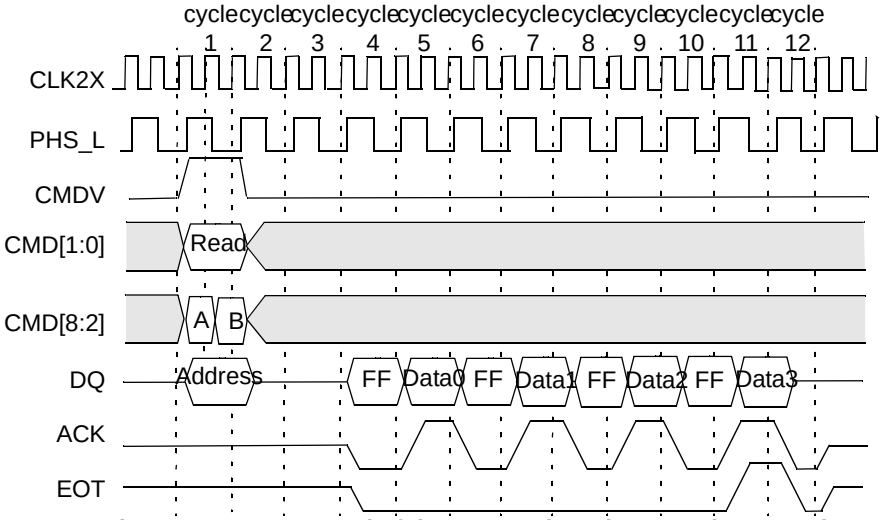


Figure 12-2. Burst Read of the Data and Mask Arrays (BLEN = 4)

The read operation lasts 4 + 2n CLK cycles (where n is the number of accesses in the burst specified by the BLEN field of the RBURREG) in the sequence shown below. This operation assumes that the host ASIC has programmed the RBURREG with the ADR and the BLEN before initiating a burst Read command.

- **Cycle 1**: The host ASIC applies the Read instruction on CMD[1:0] (CMD[2] = 1) using CMDV = 1 and the address supplied on the DQ bus as shown in *Table 12-6*. The host ASIC selects the CYNSE70032 device where ID[4:0] matches the DQ[25:21] lines. If DQ[25:21] = 11111, the host ASIC selects the CYNSE70032 device with the LDEV bit set.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive the DQ[67:0] bus, and drives ACK and EOT from Z to low.
- **Cycle 5**: The selected device drives the Read data from the addressed location on the DQ[67:0] bus and drives the ACK signal high.

Cycles 4 and 5 repeat for each additional access until all the accesses specified in the BLEN field of the RBURREG are complete. On the last transfer, the CYNSE70032 device drives the EOT signal high.

- **Cycle (4 + 2n)**: The selected device drives the DQ[67:0] to a three-state condition, and drives the ACK and EOT signals low.

At the termination of cycle (4 + 2n), the selected device floats the ACK line to a three-state condition. The burst Read instruction is complete, and a new operation can begin. *Table 12-6* describes the Read address format for data and mask arrays for burst Read operations.

Table 12-6. Read Address Format for Data and Mask Arrays

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:14]	DQ[13:0]
Reserved	ID	00: Data Array	Reserved	**Do not care**. These fifteen bits come from the internal RBURADR, which increments for each access.
Reserved	ID	01: Mask Array	Reserved	**Do not care**. These fifteen bits come from the internal RBURADR, which increments for each access.

12.4 Write Command

The Write command can be a single Write of a data array, mask array, register, or an external SRAM location (CMD[2] = 0). It can also be a burst Write (CMD[2] = 1) using an internal auto-incrementing address register (WBURADR) of the data or mask array locations. A single-location Write is a three-cycle operation as shown in *Figure 12-3*. The burst Write adds one extra cycle for each successive location Write.

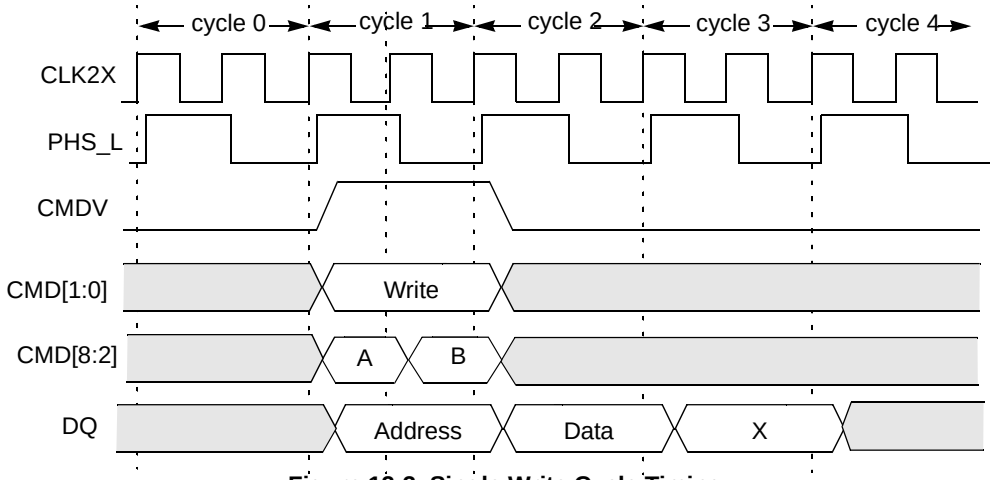


Figure 12-3. Single Write Cycle Timing

The following is the Write operation sequence, and *Table 12-7* shows the Write address format for the data array, the mask array, or the single-Write SRAM. *Table 12-8* shows the Write address format for the internal registers.

- **Cycle 1A**: The host ASIC applies the Write instruction to CMD[1:0] (CMD[2] = 0) using CMDV = 1 and the address supplied on the DQ bus. The host ASIC also supplies the GMR Index to mask the write to the data or mask array location on CMD[5:3]. For SRAM Writes, the host ASIC must supply SADR[21:19] on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Write instruction to CMD[1:0] (CMD[2] = 0) using CMDV = 1 and the address supplied on the DQ bus. The host ASIC continues to supply the GMR Index to mask the Write to the data or mask array locations in CMD[5:3]. The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.
- **Cycle 2**: The host ASIC drives the DQ[67:0] with the data to be written to the data array, the mask array, or the register location of the selected device.
- **Cycle 3**: Idle cycle.

At the termination of cycle 3, another operation can begin. ***Note***. The latency of the SRAM Write will be different than the one described above (see Subsection 15.2, “SRAM PIO Access” on page 99).

Figure 12-4 shows the timing diagram of a burst Write operation of the data or mask array.

Table 12-7. Write Address Format for Data Array, Mask Array, or SRAM (Single Write)

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20:19]	DQ [18:14]	DQ[13:0]
Reserved	0: Direct 1: Indirect	SSR (applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is 0, this field carries the address of the data array location. If DQ[29] is 1, the SSR specified on DQ[28:26] is used to generate the address of the data array location: {SSR[13:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSR (applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is 0, this field carries the address of the mask array location. If DQ[29] is 1, the SSR specified on DQ[28:26] is used to generate the address of the mask array location: {SSR[13:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSR (applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is 0, this field carries the address of the SRAM location. If DQ[29] is 1, the SSR specified on DQ[28:26] is used to generate the address of the SRAM location: {SSR[13:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]

Table 12-8. Write Address Format for Internal Registers

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	ID	11: Register	Reserved	Register address

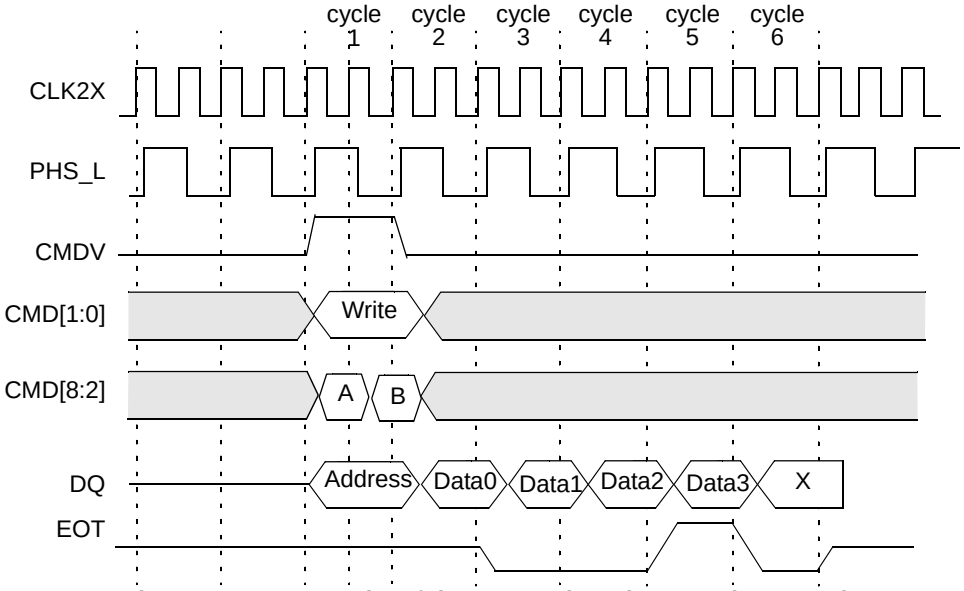


Figure 12-4. Burst Write of the Data and Mask Arrays (BLEN = 4)

The burst Write operation lasts for (n + 2) CLK cycles. n signifies the number of accesses in the burst as specified in the BLEN field of the WBURREG. The following is the block Write operation sequence. This operation assumes that the host ASIC has programmed the WBURREG with the ADR and the BLEN before initiating a burst Write command.

- **Cycle 1A**: The host ASIC applies the Write instruction to CMD[1:0] (CMD[2] = 1) using CMDV = 1, and the address supplied on the DQ bus, as shown in *Table 12-9*. The host ASIC also supplies the GMR Index to mask the Write to the data or mask array locations in CMD[5:3].
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] (CMD[2] = 1) using CMDV = 1 and the address supplied on the DQ bus. The host ASIC continues to supply the GMR Index to mask the Write to the data or mask array locations in CMD[5:3]. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. It selects all the devices when DQ[25:21] = 11111.
- **Cycle 2**: The host ASIC drives the DQ[67:0] with the data to be written to the data or mask array location of the selected device. The CYNSE70032 device writes the data from the DQ[67:0] bus only to the subfield that has the corresponding mask bit set to 1 in the GMR specified by the index CMD[5:3]supplied in cycle 1.
- **Cycles 3 to n + 1**: The host ASIC drives DQ[67:0] with the data to be written to the next data or mask array location of the selected device (addressed by the auto-increment ADR field of the WBURREG register).

The CYNSE70032 device writes the data on the DQ[67:0] bus only to the subfield that has the corresponding mask bit set to 1 in the GMR that is specified by the index CMD[5:3] supplied in cycle 1. The CYNSE70032 device drives the EOT signal low from cycle 3 to cycle n; the CYNSE70032 device drives the EOT signal high in cycle n + 1 (n is specified in the BLEN field of the WBURREG).

- **Cycle n + 2**: TheCYNSE70032 drives the EOT signal low.

At the termination of cycle n + 2, the CYNSE70032 device floats the EOT signal to a three-state operation, and a new instruction can begin.

Table 12-9. Write Address Format for Data and Mask Array (Burst Write)

DQ [67:26]	DQ [25:21]	DQ [20:19]	DQ [18:14]	DQ[13:0]
Reserved	ID	00: Data array	Reserved	***Do not care***. These fifteen bits come from the internal WBURADR, which increments with each access.
Reserved	ID	01: Mask array	Reserved	***Do not care***. These fifteen bits come from the internal WBURADR, which increments with each access.

13.0 Search Command

This subsection will describe the following searches.

- **68-bit Search on tables configured as ×68 using one device**
- **68-bit Search on tables configured as ×68 using up to eight devices**
- **68-bit Search on tables configured as ×68 using up to 31 devices**
- **136-bit Search on tables configured as ×136 using one device**
- **136-bit Search on tables configured as ×136 using up to eight devices**
- **136-bit Search on tables configured as ×136 using up to 31 devices**
- **272-bit Search on tables configured as ×272 using one device**
- **272-bit Search on tables configured as ×272 using up to eight devices**
- **272-bit Search on tables configured as ×272 using up to 31 devices**
- **Mixed-size searches on tables configured with different widths using an CYNSE70032**.

13.1 68-bit Search on Tables Configured as ×68 using a Single CYNSE70032 Device

Figure 13-1 shows the timing diagram for a Search command in a 68-bit-configured table (CFG = 00000000) consisting of a single device for one set of parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. The hardware diagram for this Search subsystem is shown in *Figure 13-2*.

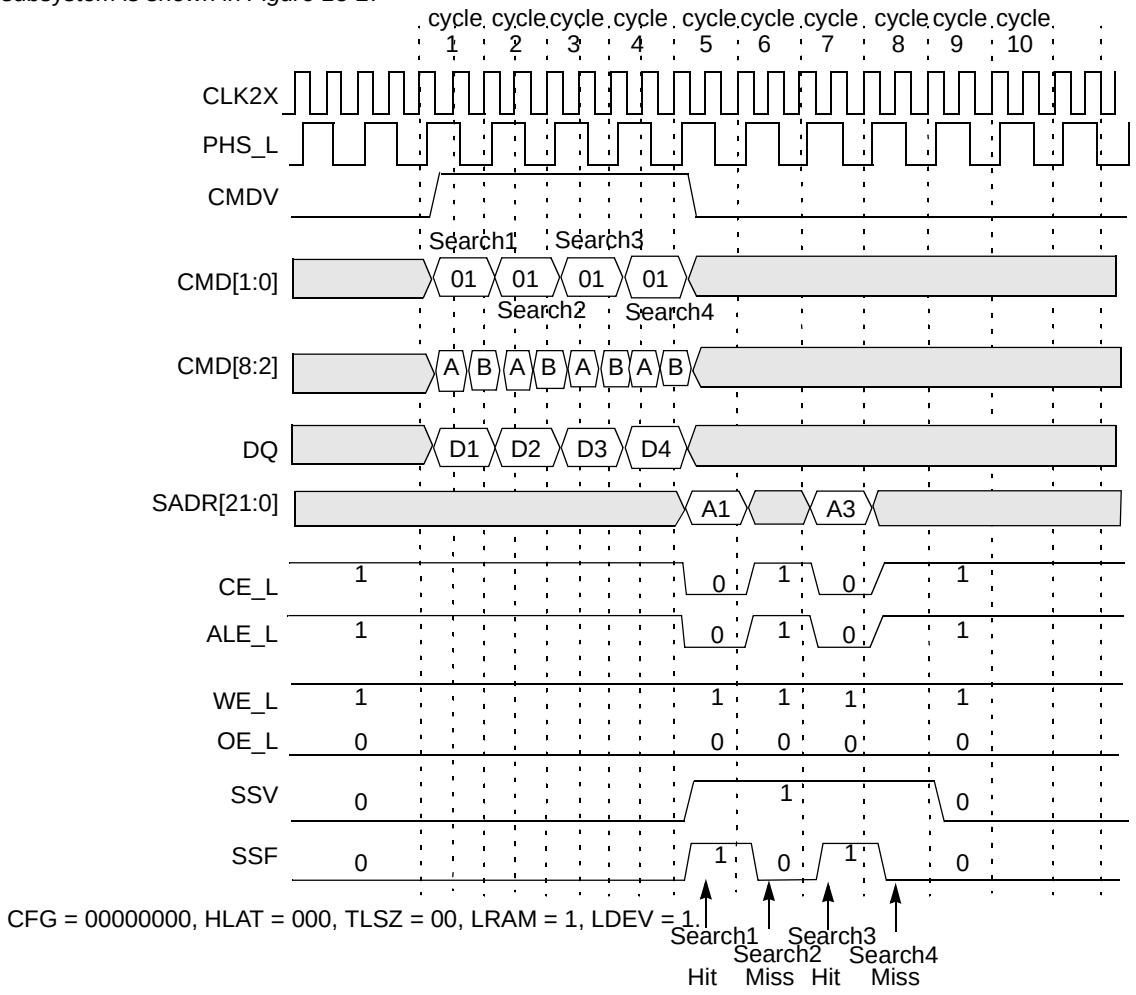


Figure 13-1. Timing Diagram for 68-bit Search in ×68 Table (One Device)

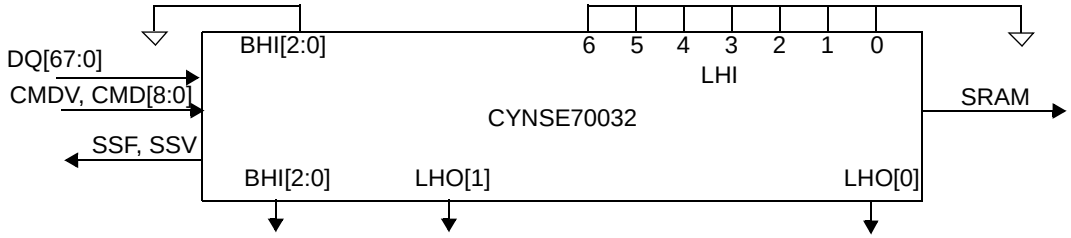


Figure 13-2. Hardware Diagram for a Table with a Single Device

The following is the sequence of operation for a single 68-bit Search command (also refer to “Command and Command Parameters,” Subsection 12.2 on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven by the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive CMDV high and to apply Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for information on SSR[0:7]). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note. For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both cycles A and B. The even and odd GMR pairs selected for the compare must be programmed with the same value.

The logical 68-bit Search operation is shown in *Figure 13-3*. The entire table of 68-bit entries is compared to a 68-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs selected by the GMR Index in the command’s cycle A. The 68-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command’s cycle B. In a ×68 configuration, only the even comparand register can subsequently be used by the Learn command. The word K (presented on the DQ bus in both cycles A and B of the command) is compared with each entry in the table, starting at location 0. The first matching entry’s location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see “SRAM Addressing” on page 98).

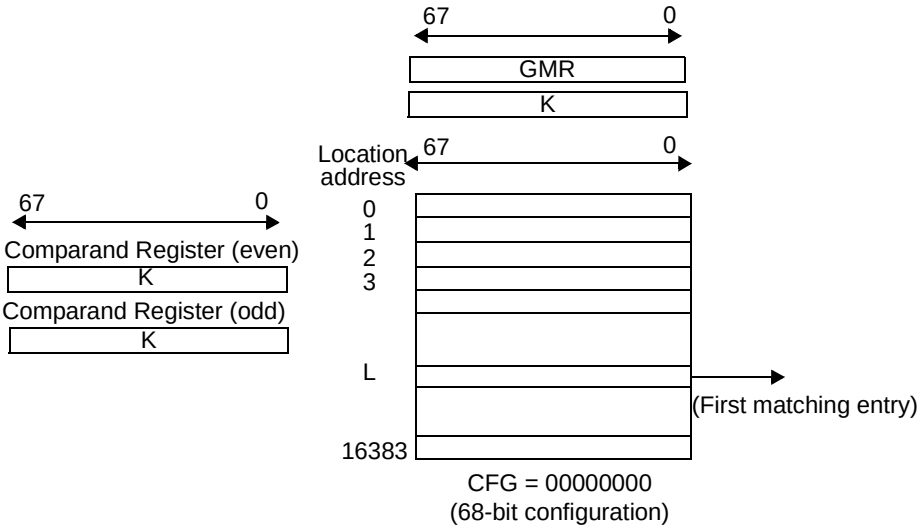


Figure 13-3. ×68 Table with One Device

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 68-bit searches in ×68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit Search command cycle (which is two CLK2X cycles) is shown in *Table 13-1*.

Table 13-1. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K × 68 bits	4
1–8 (TLSZ = 01)	128K × 68 bits	5
1–31 (TLSZ = 10)	496K × 68 bits	6

Search latency from command to SRAM access cycle is 4 for a single device in the table with TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT as specified in *Table 13-2*.

Table 13-2. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.2 68-bit Search on Tables Configured as ×68 Using up to Eight CYNSE70032 Devices

The hardware diagram of the Search subsystem of eight devices is shown in *Figure 13-4*. The following are the parameters programmed into the eight devices.

- First seven devices (devices 0–6): CFG = 00000000, TLSZ = 01, HLAT = 010, LRAM = 0, and LDEV = 0.
- Eighth device (device 7): CFG = 00000000, TLSZ = 01, HLAT = 010, LRAM = 1, and LDEV = 1.

Note. All eight devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table (device number 7 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (devices 0 through 6 in this case) must be programmed with LRAM = 0 and LDEV = 0.

Figure 13-5 shows the timing diagram for a Search command in the 68-bit-configured table of eight devices for device number 0. *Figure 13-6* shows the timing diagram for a Search command in the 68-bit-configured table of eight devices for device number 1. *Figure 13-7* shows the timing diagram for a Search command in the 68-bit-configured table of eight devices for device number 7 (the last device in this specific table). For these timing diagrams four 68-bit searches are performed sequentially. HIT/MISS assumptions were made as shown below in *Table 13-3*.

Table 13-3. HIT/MISS Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Devices 2–6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

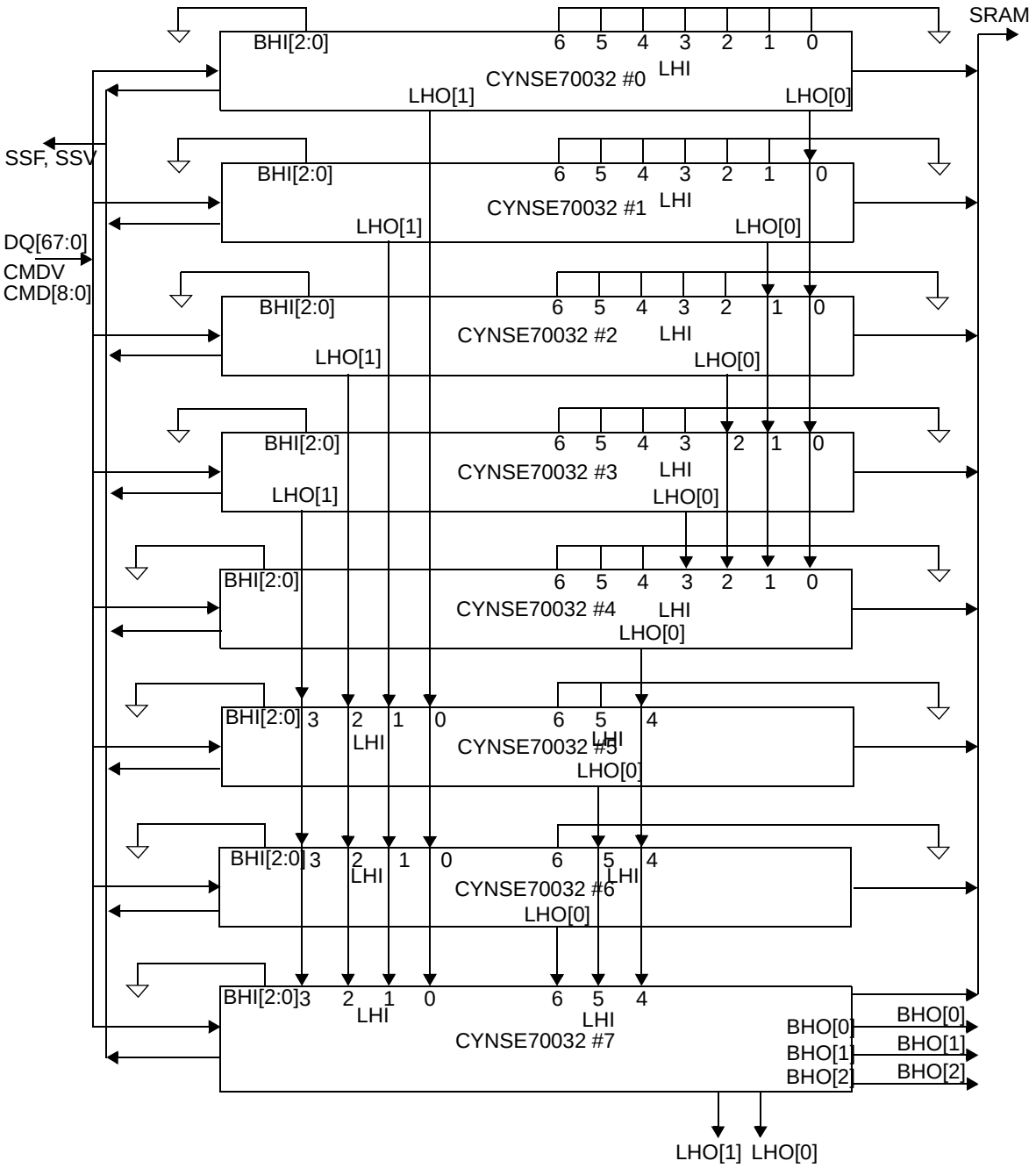
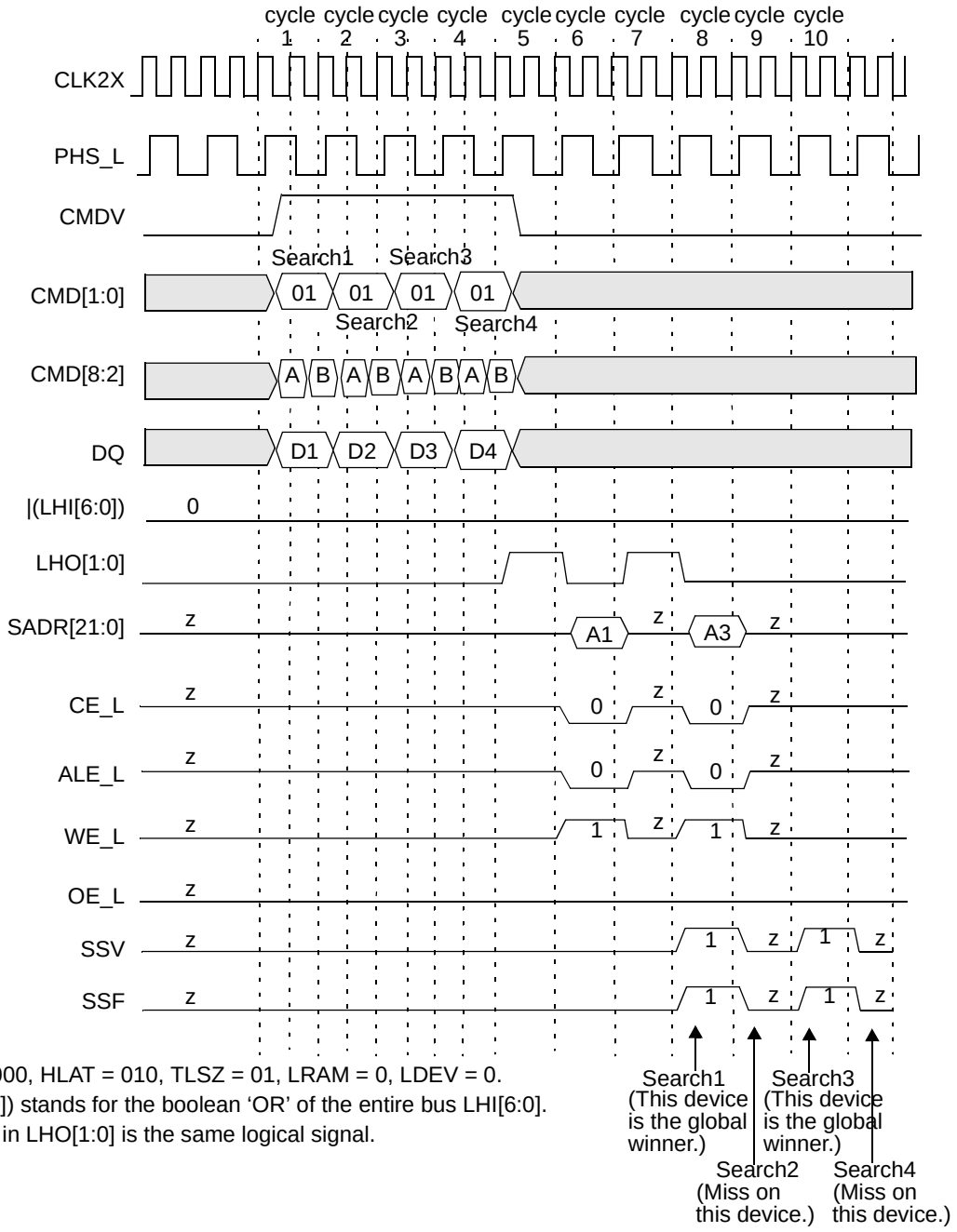
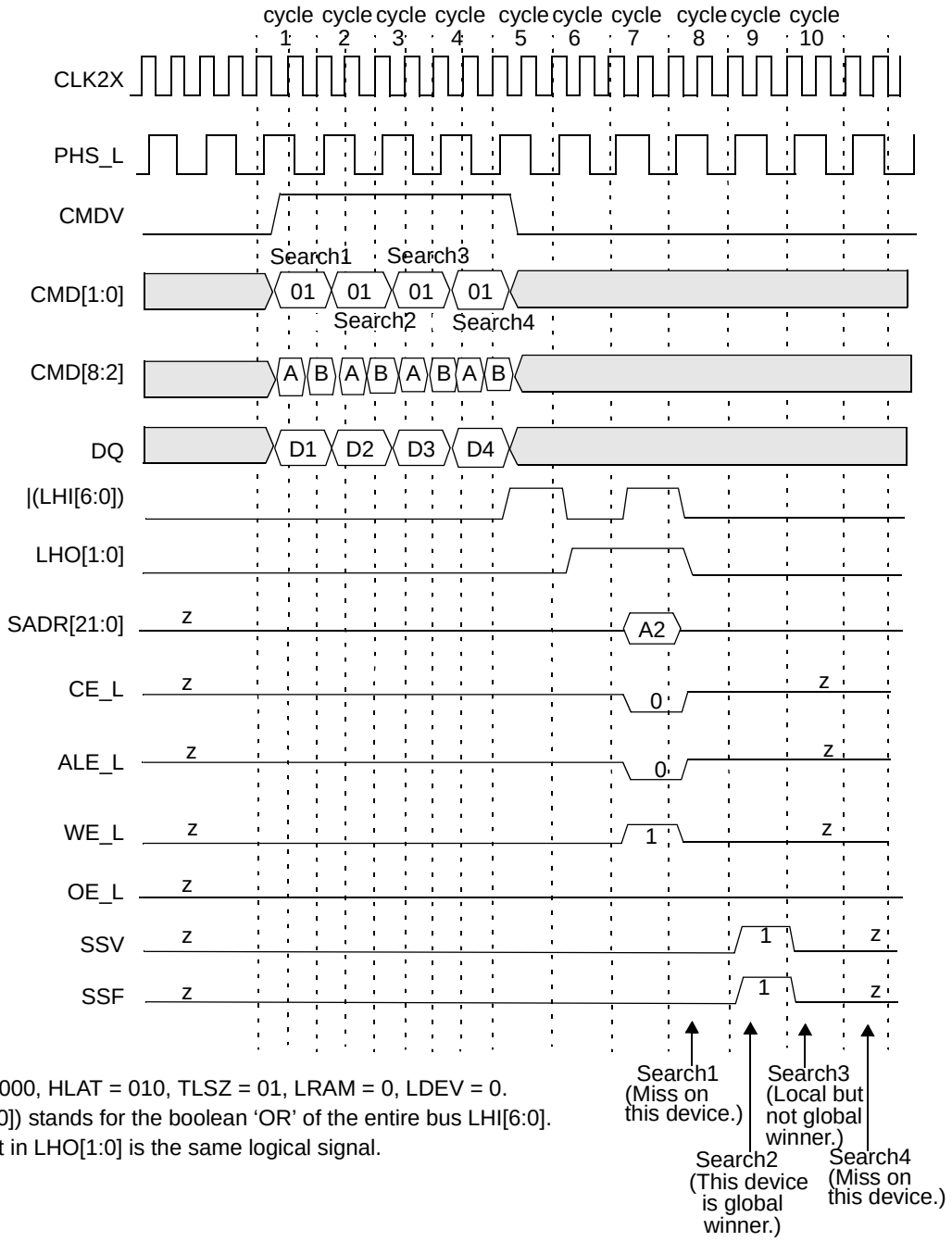


Figure 13-4. Hardware Diagram for a Table with Eight Devices



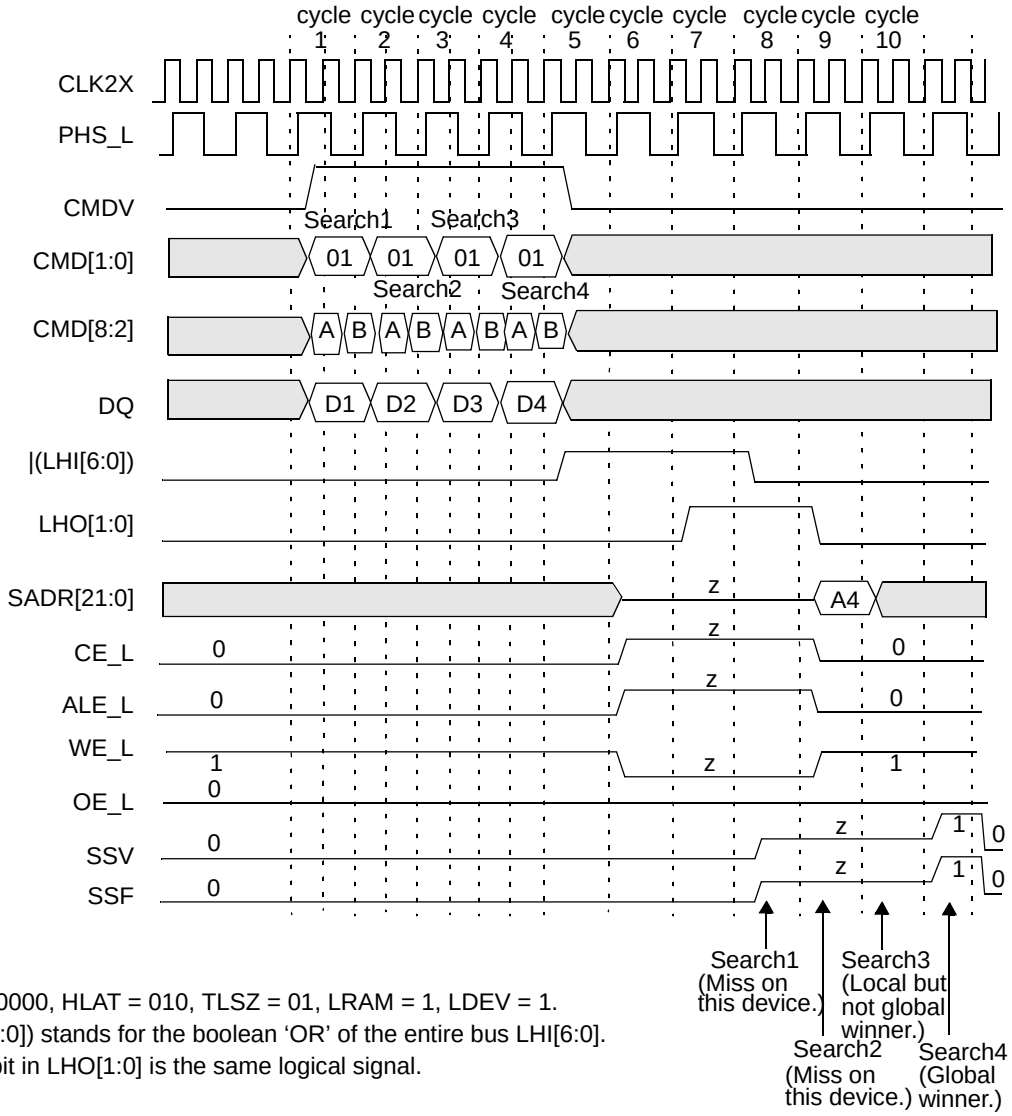
CFG = 00000000, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-5. Timing Diagram for 68-bit Search Device Number 0



CFG = 00000000, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-6. Timing Diagram for 68-bit Search Device Number 1



CFG = 00000000, HLAT = 010, TLSZ = 01, LRAM = 1, LDEV = 1.

Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].

Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-7. Timing Diagram for 68-bit Search Device Number 7 (Last Device)

The following is the sequence of operation for a single 68-bit Search command (also refer to "Command and Command Parameters," Subsection 12.2 on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) to CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive CMDV high and to apply Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 14 for a description of SSR[0:7]). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note. For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both cycles A and B. The even and odd GMR pairs selected for the comparison must also be programmed with the same value.

The logical 68-bit Search operation is shown in *Figure 13-8*. The entire table of eight devices of 68-bit entries is compared to a 68-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's cycle A. The 68-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs (selected by the Comparand Register Index in command cycle B) in each of the eight devices. In the ×68 configuration, only the even comparand register can subsequently be used by the Learn command in one of the devices (the first non-full device only). The word K (presented on the DQ bus in both cycles A and B of

the command) is compared with each entry in the table, starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 98). The global winning device will drive the bus in a specific cycle. On a global miss cycle the device with LRAM = 1 (default driving device for the SRAM bus) and LDEV = 1 (default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

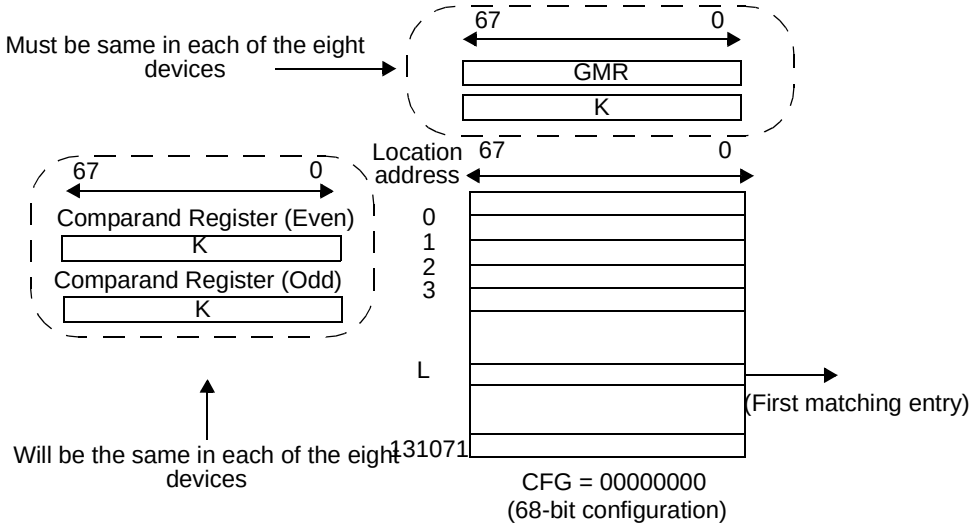


Figure 13-8. ×68 Table with Eight Devices

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 68-bit searches in ×68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit Search command cycle (two CLK2X cycles) is shown in *Table 13-4*.

Table 13-4. Search latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K × 68 bits	4
1–8 (TLSZ = 01)	128K × 68 bits	5
1–31 (TLSZ = 10)	496K × 68 bits	6

Search latency from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ = 01). SSV and SSF also shift further to the right for different values of HLAT as specified in *Table 13-5*.

Table 13-5. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.3 68-bit Search on Tables Configured as ×68 Using up to 31 CYNSE70032 Devices

The hardware diagram of the Search subsystem of 31 devices is shown in *Figure 13-9*. Each of the four blocks in the diagram represents eight CYNSE70032 devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in *Figure 13-10*. The following are the parameters that are programmed into the 31 devices.

- First thirty devices (devices 0–29): CFG = 00000000, TLSZ = 10, HLAT = 001, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30): CFG = 00000000, TLSZ = 10, HLAT = 001, LRAM = 1, and LDEV = 1.

Note. All devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table (device number 30 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (devices 0 through 29 in this case) must be programmed with LRAM = 0 and LDEV = 0.

The timing diagrams referred to in this paragraph reference the Hit/Miss assumptions defined in *Table 13-6*. For the purpose of illustrating timings, it is further assumed that the there is only one device with a matching entry in each of the blocks. *Figure 13-11* shows the timing diagram for a Search command in the 68-bit-configured table of 31 devices for each of the eight devices in block number 0. *Figure 13-12* shows a timing diagram for a Search command in the 68-bit-configured table of 31 devices for all the devices in block number 1 (above the winning device in that block). *Figure 13-13* shows the timing diagram for the globally winning device (defined as the final winner within its own and all blocks) in block number 1. *Figure 13-14* shows the timing diagram for all the devices below the globally winning device in block number 1. *Figure 13-15*, *Figure 13-16*, and *Figure 13-17*, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device for block number 2. *Figure 13-18*, *Figure 13-19*, *Figure 13-20*, and *Figure 13-21*, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device except the last device (device 30) for block number 3.

The 68-bit Search operation is pipelined and executed as follows. Four cycles from the Search command, each of the devices knows the outcome internal to it for that operation. In the fifth cycle after the Search command, the devices in a block arbitrate for a winner amongst them (a “block” being defined as less than or equal to eight devices resolving the winner between them using the LHI[6:0] and LHO[1:0] signalling mechanisms). In the sixth cycle after the Search command, the blocks resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanisms. The winning device within the winning block is the global winning device for a Search operation.

Table 13-6. Hit/Miss Assumption

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

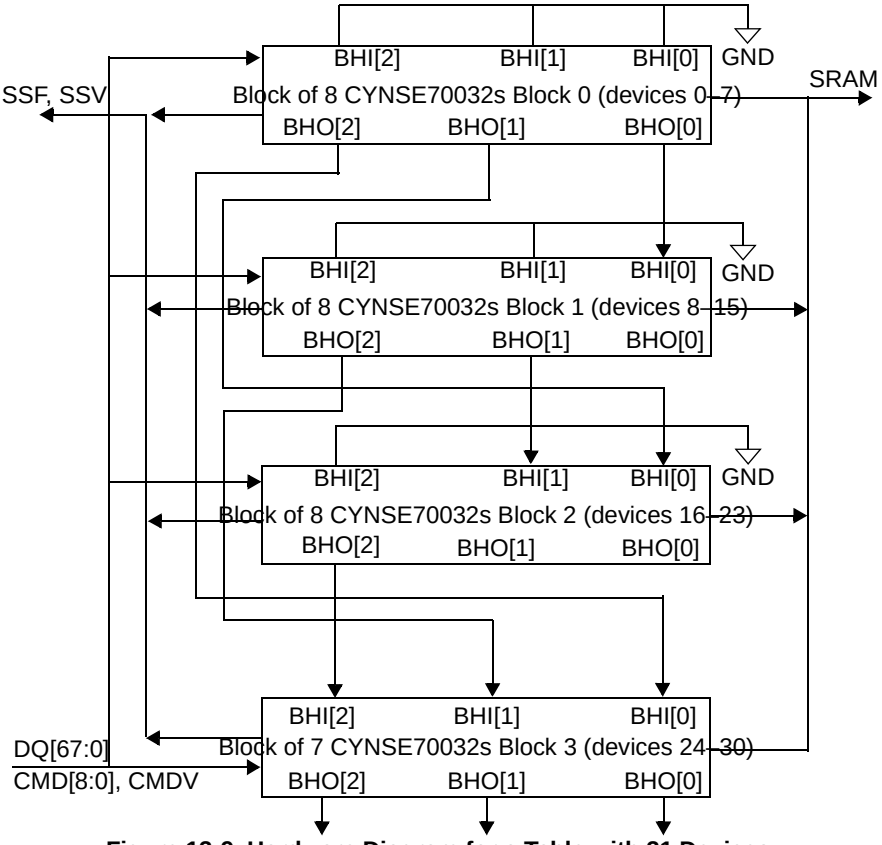


Figure 13-9. Hardware Diagram for a Table with 31 Devices

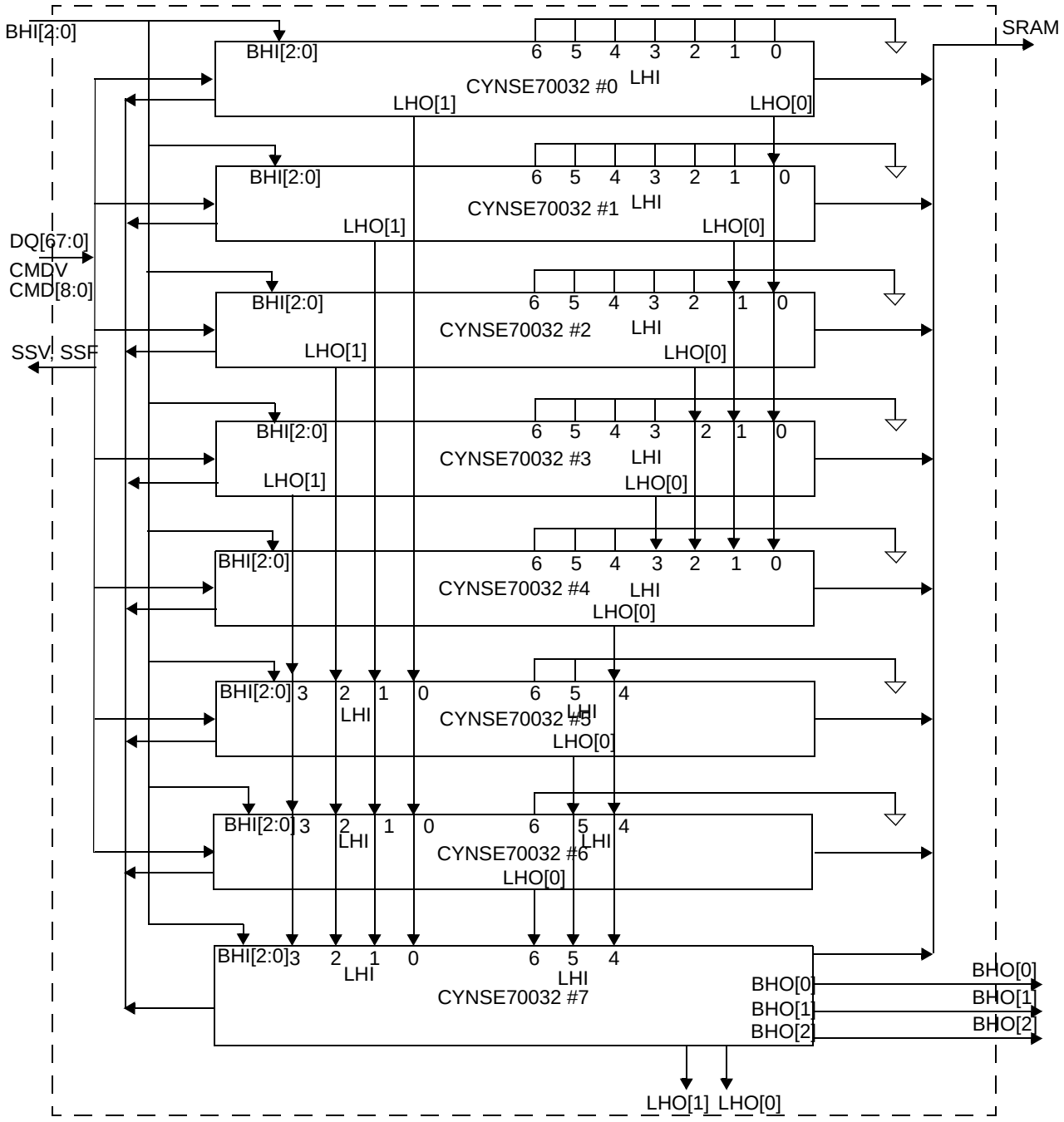
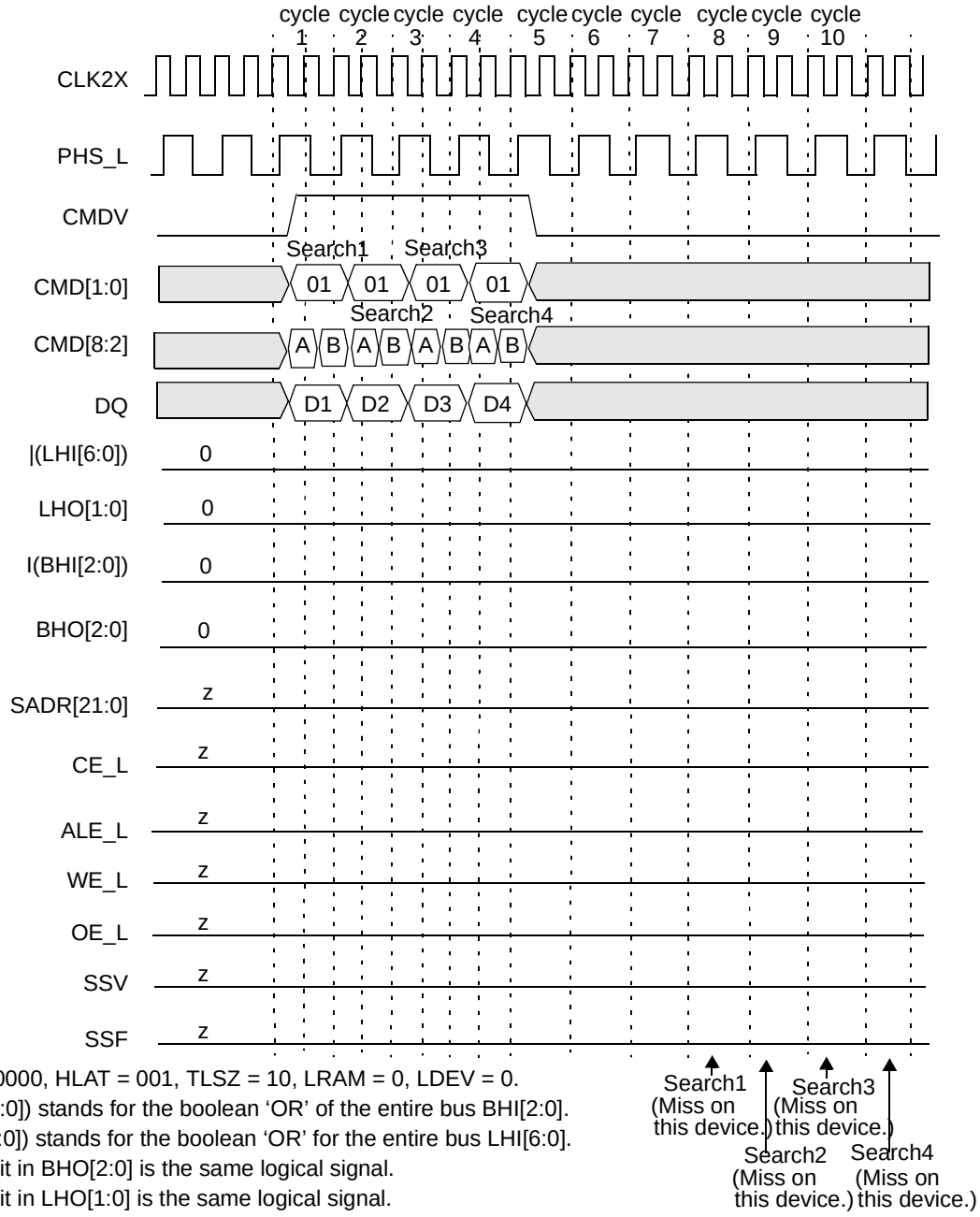
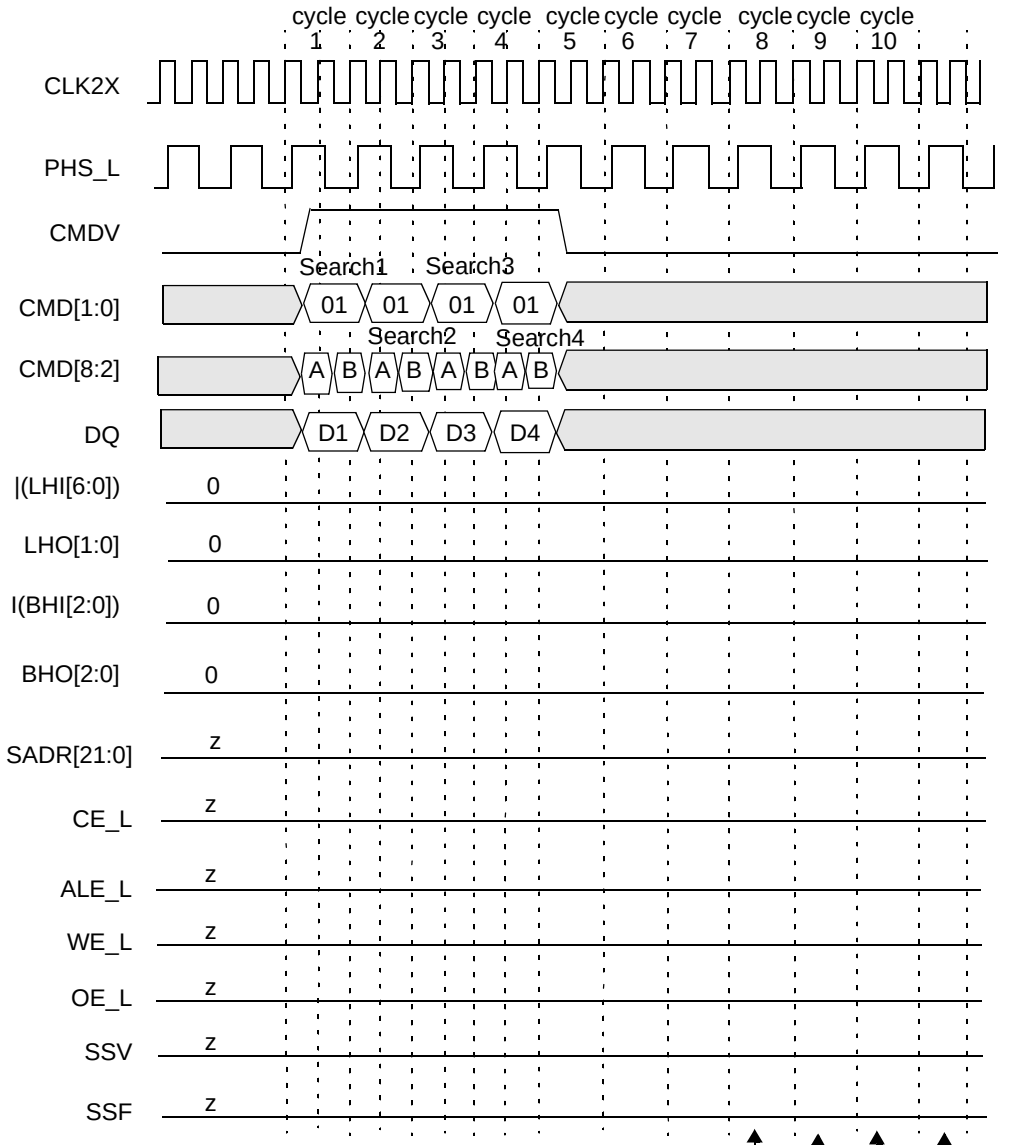


Figure 13-10. Hardware Diagram for a Block of up to Eight Devices



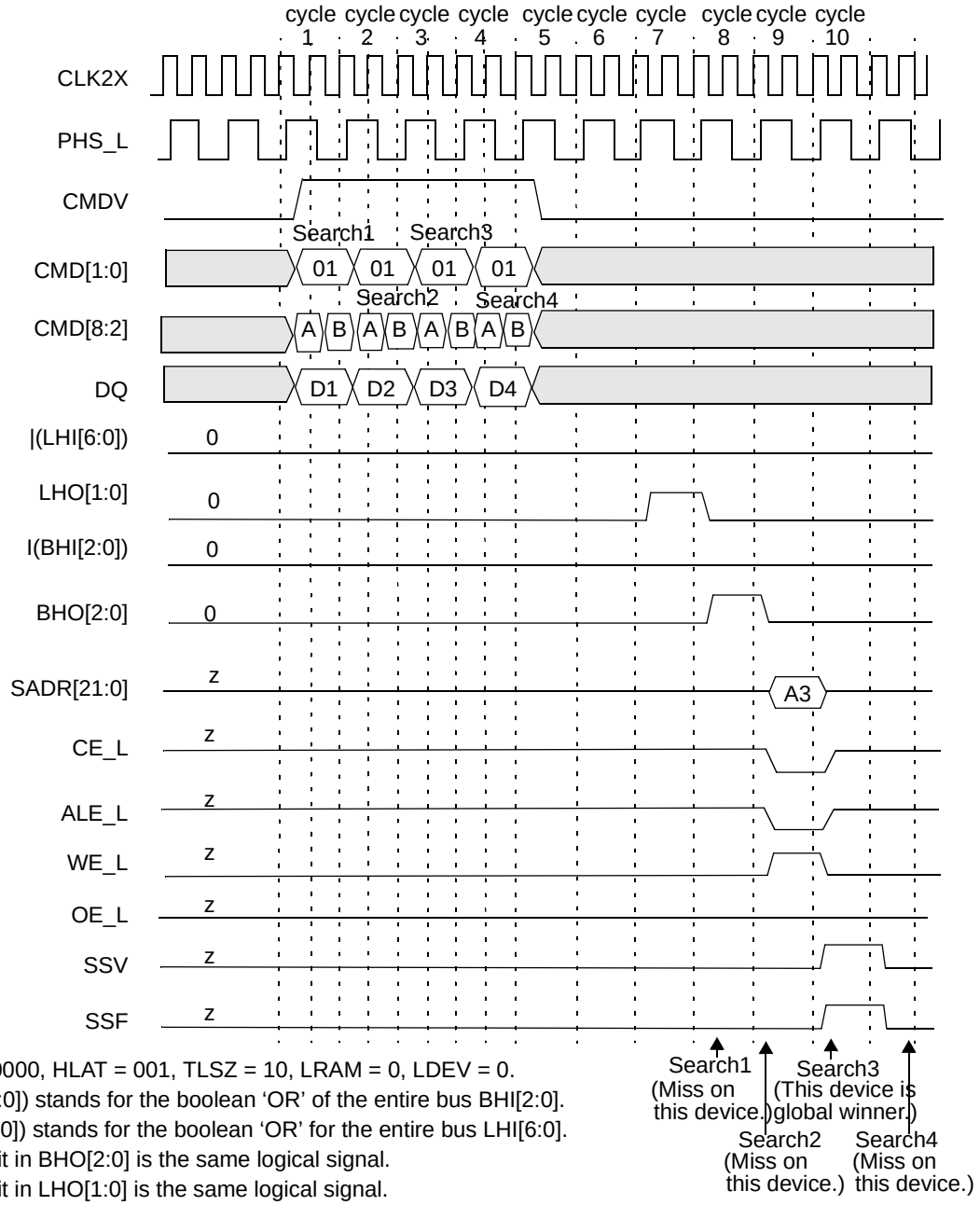
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-11. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



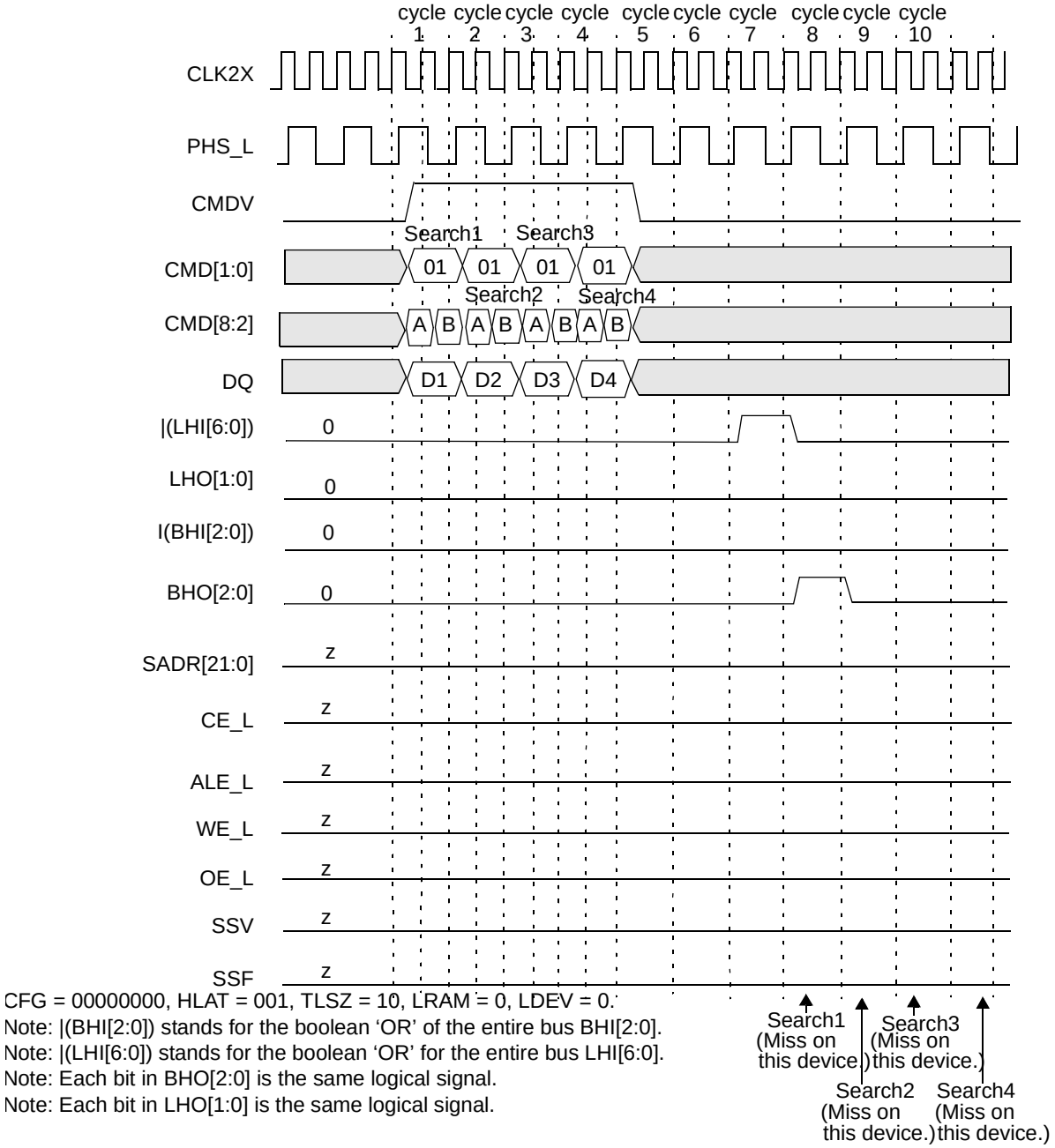
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0)] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-12. Timing Diagram for Each Device Above the Winning Device in Block Number 1



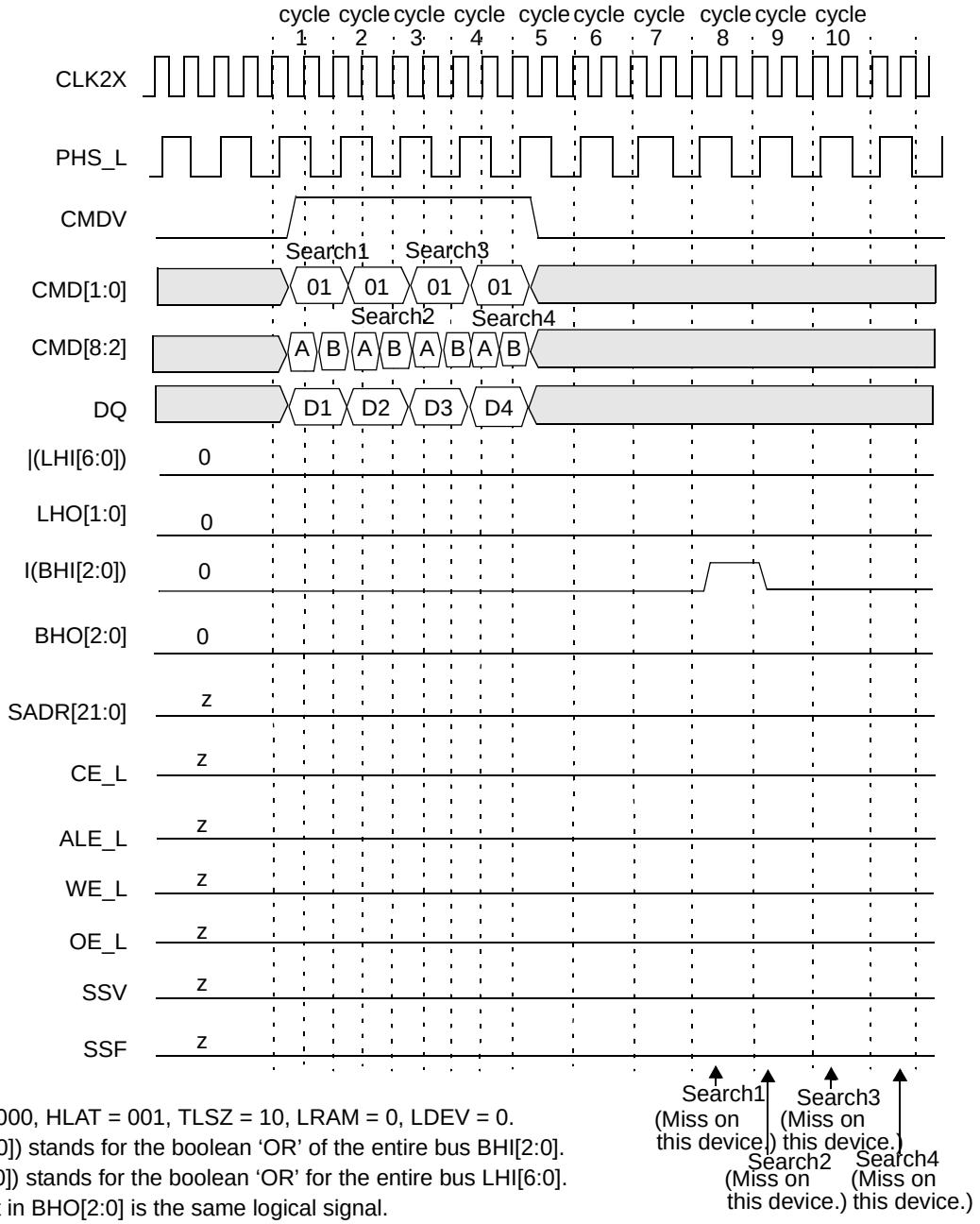
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-13. Timing Diagram for Globally Winning Device in Block Number 1



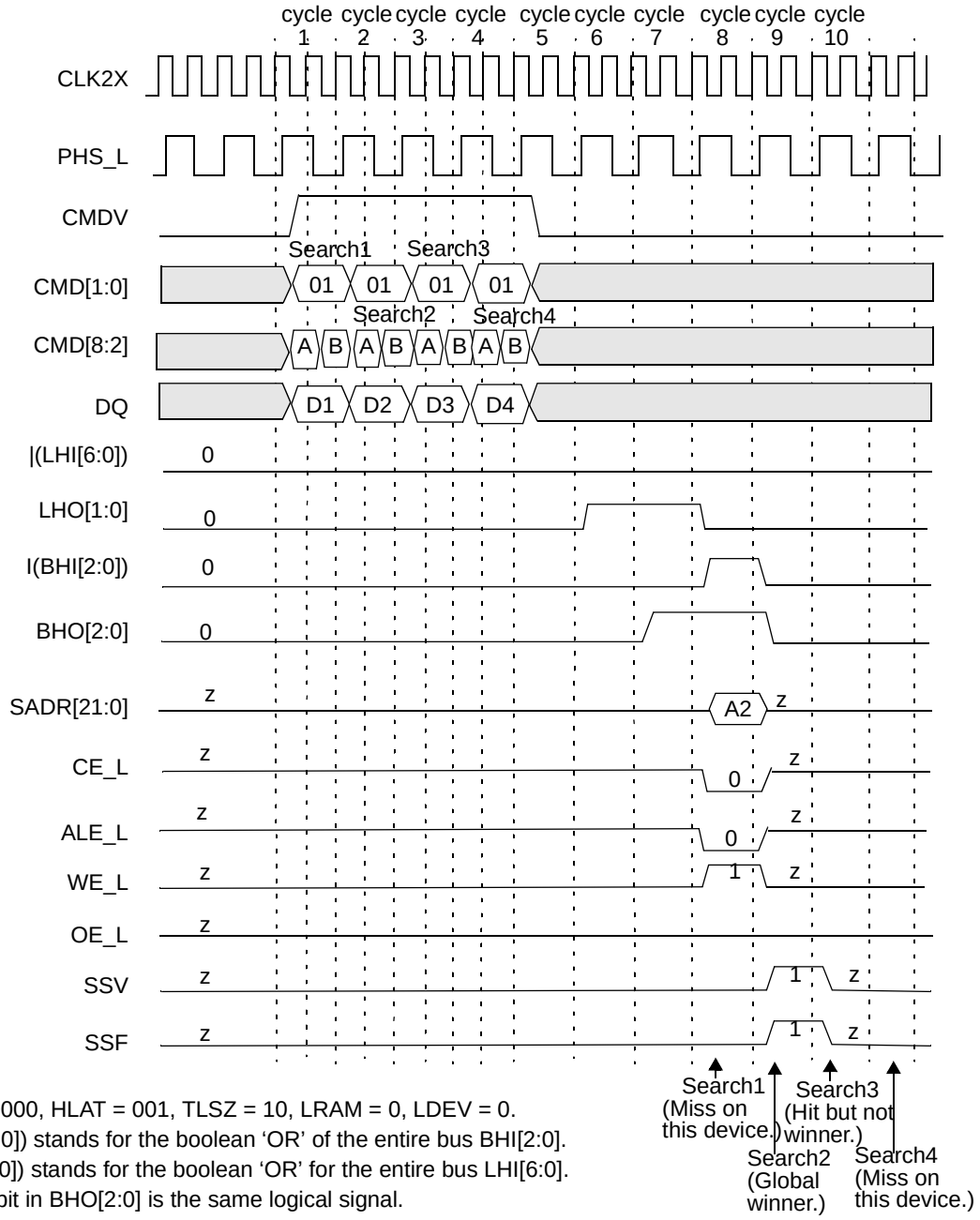
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-14. Timing Diagram for Devices Below the Winning Device in Block Number 1



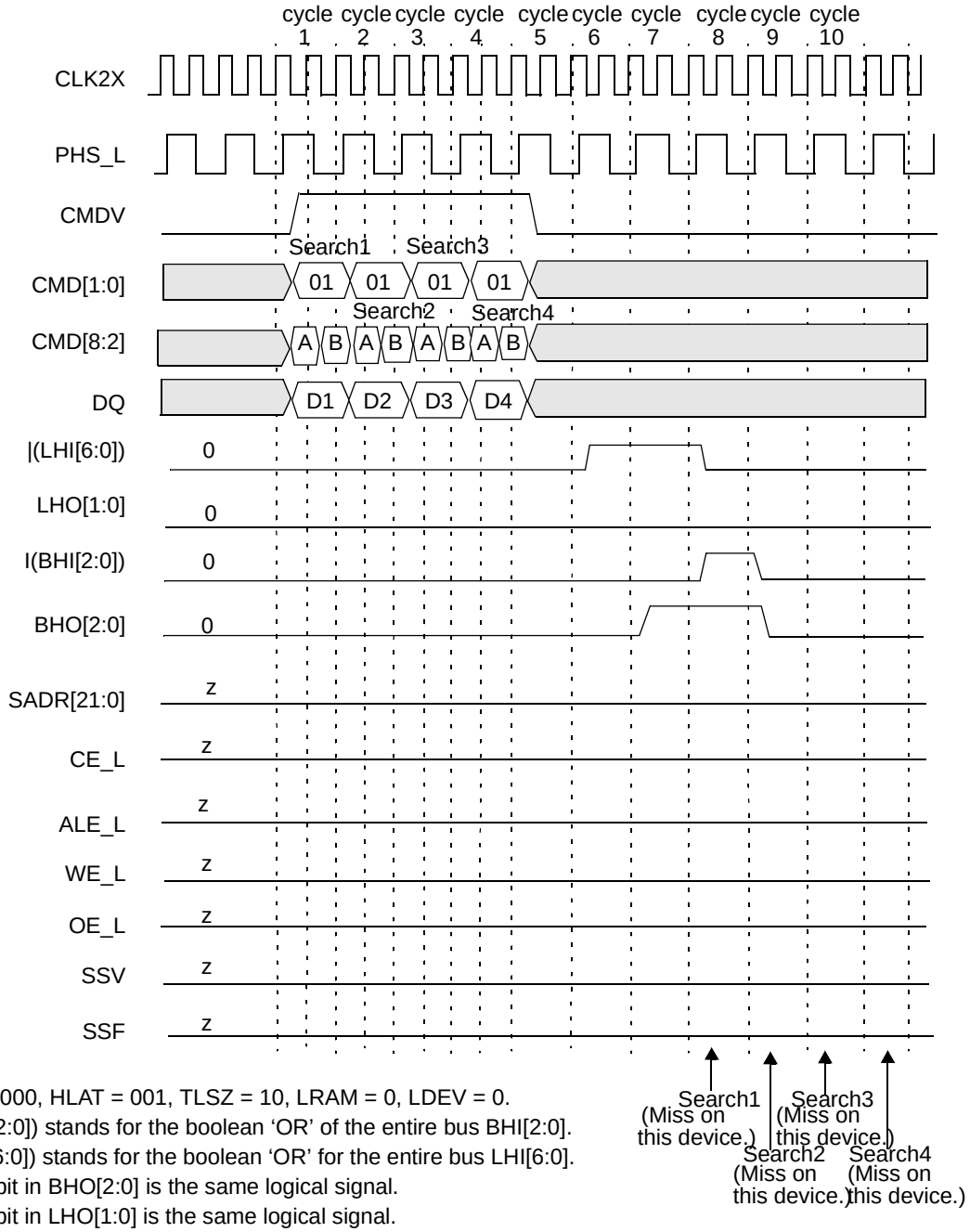
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-15. Timing Diagram for Devices Above the Winning Device in Block Number 2



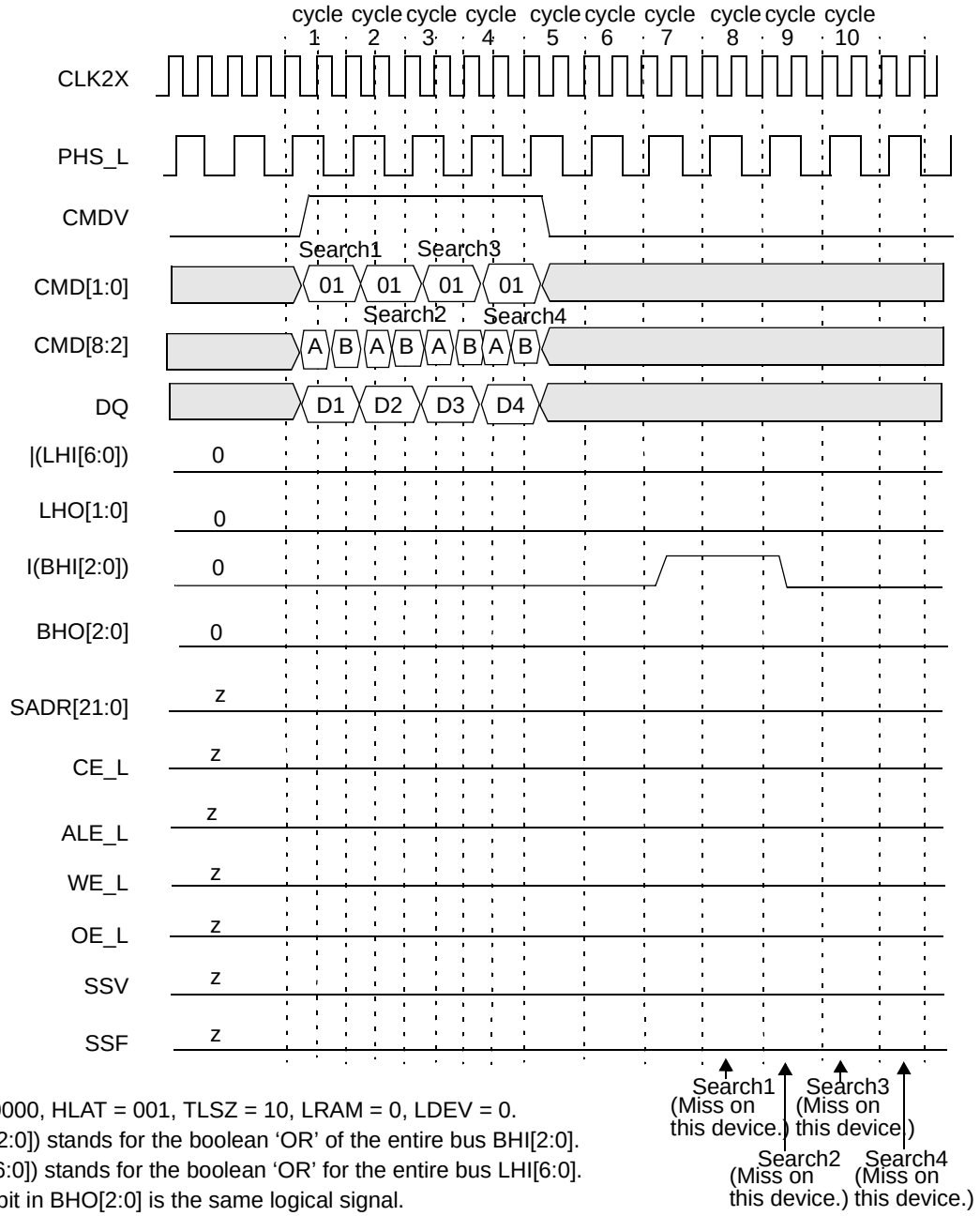
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-16. Timing Diagram for Globally Winning Device in Block Number 2



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-17. Timing Diagram for Devices Below the Winning Device in Block Number 2



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.

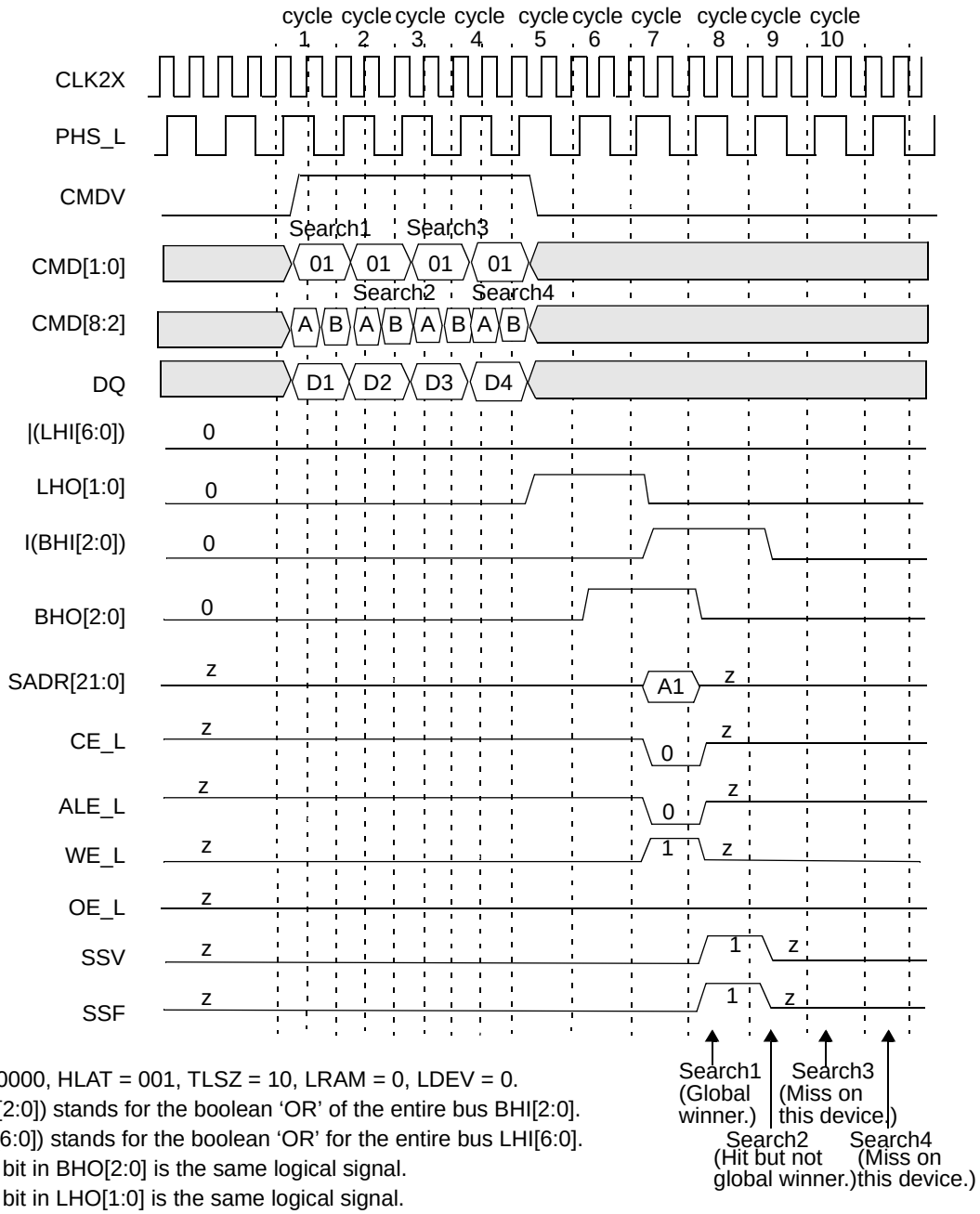
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].

Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].

Note: Each bit in BHO[2:0] is the same logical signal.

Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-18. Timing Diagram for Devices Above the Winning Device in Block Number 3



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.

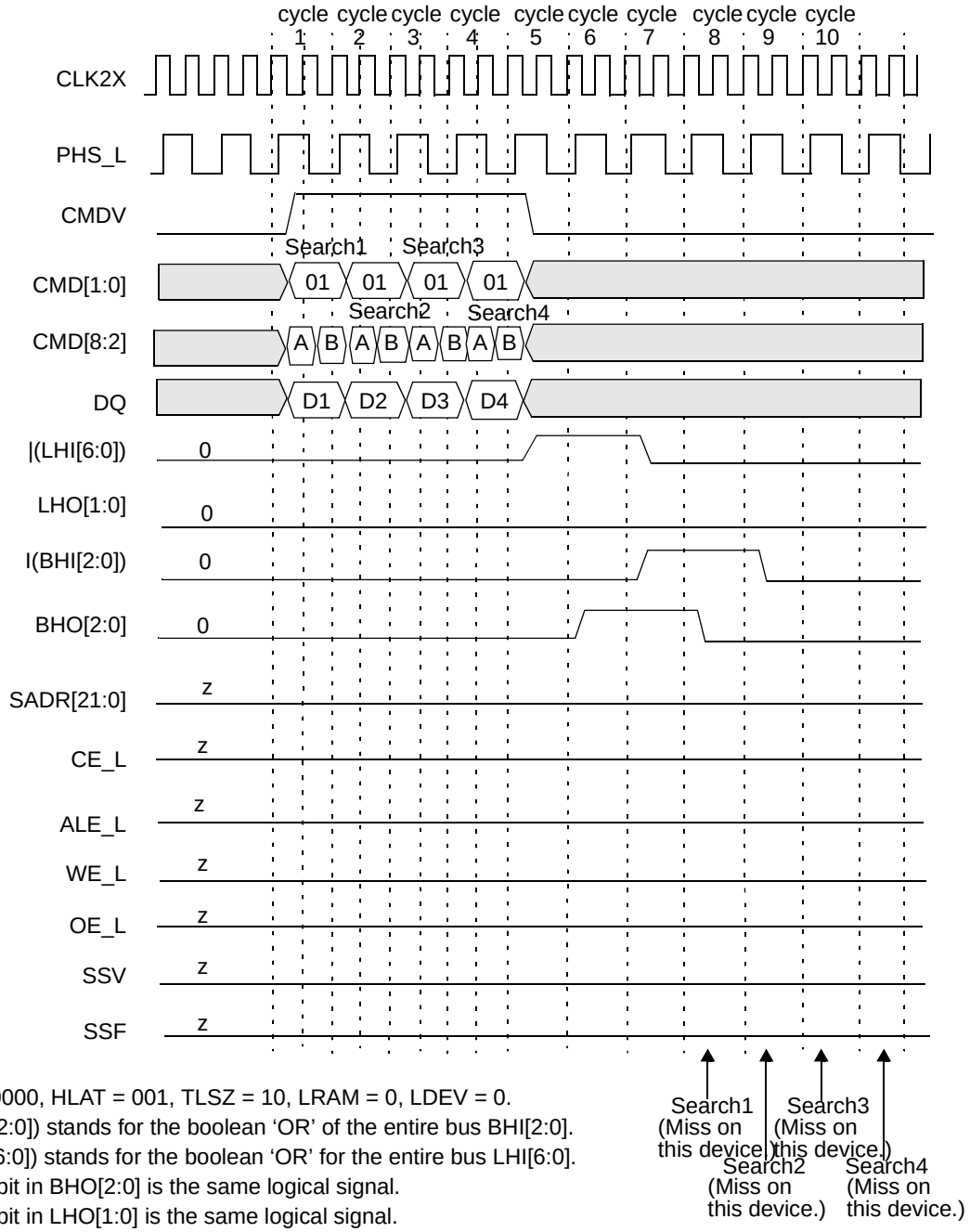
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].

Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].

Note: Each bit in BHO[2:0] is the same logical signal.

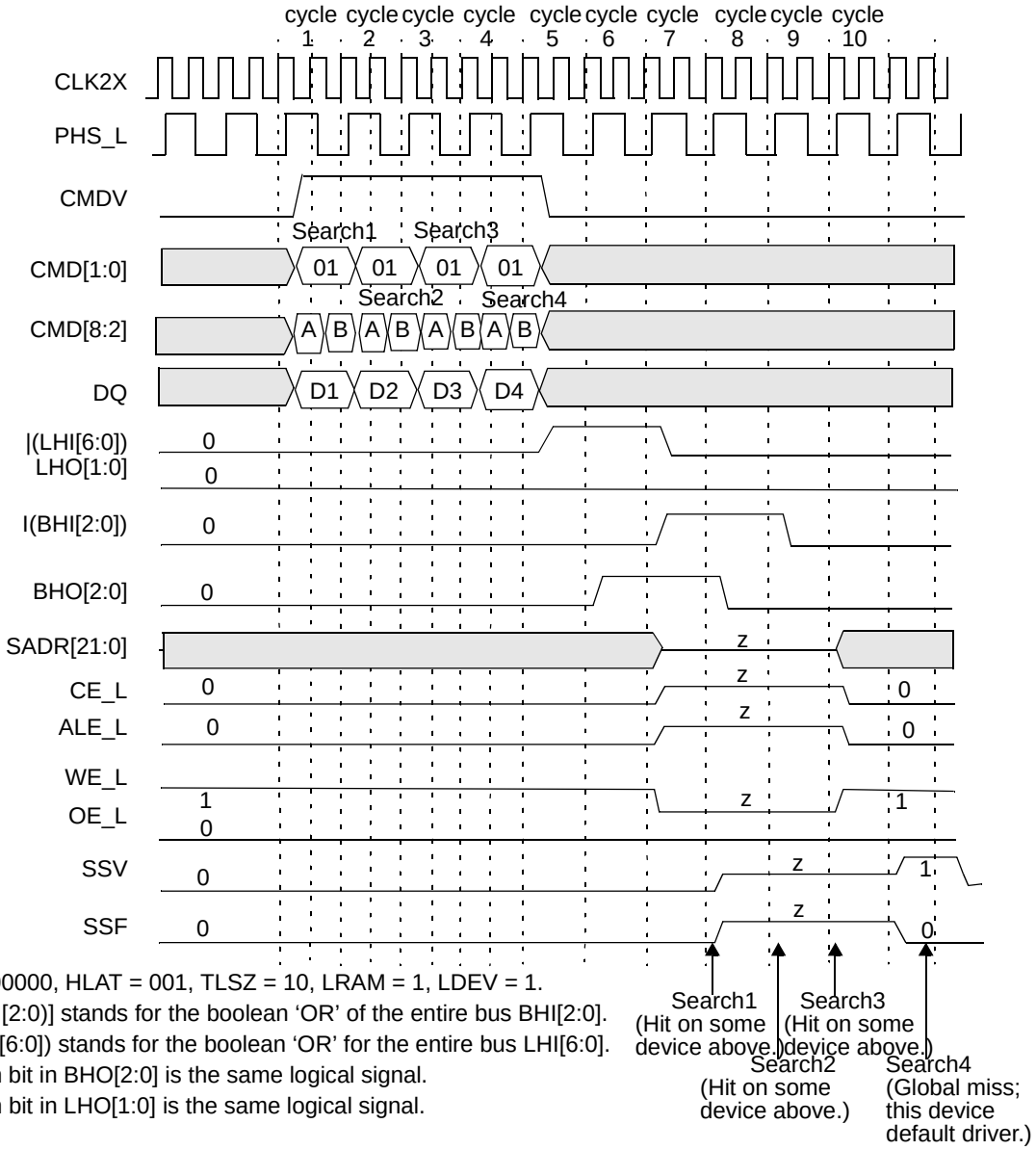
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-19. Timing Diagram for Globally Winning Device in Block Number 3



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-20. Timing Diagram for Devices Below the Winning Device in Block Number 3 (Except the Last Device [Device Number 30])



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 1, LDEV = 1.

Note: |(BHI[2:0)] stands for the boolean 'OR' of the entire bus BHI[2:0].

Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].

Note: Each bit in BHO[2:0] is the same logical signal.

Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-21. Timing Diagram for Device Number 6 in Block Number 3 (Device Number 30 in Depth-Cascaded Table)

The following is the sequence of operation for a single 68-bit Search command (also refer to "Command and Command Parameters," Subsection 12.2 on page 19).

- Cycle A: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to logic 0.
- Cycle B: The host ASIC continues to drive CMDV high and applies Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note. For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both cycles A and B. The even and odd GMR pairs selected for the compare must be programmed with the same value.

The logical 68-bit Search operation is shown in *Figure 13-22*. The entire table (31 devices of 68-bit entries) is compared to a 68-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected

by the GMR Index in the command's cycle A. The 68-bit word K (presented on the DQ bus in cycles A and B of the command) is also stored in both even and odd comparand register pairs in each of the eight devices (and selected by the Comparand Register Index in command's cycle B). In the x68 configuration, the even comparand register can subsequently be used by the Learn command, but only in the first non-full device. The word K (presented on the DQ bus in cycles A and B of the command) is compared with each entry in the table, starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 98). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 and LDEV = 1 will be the default driver for such missed cycles.

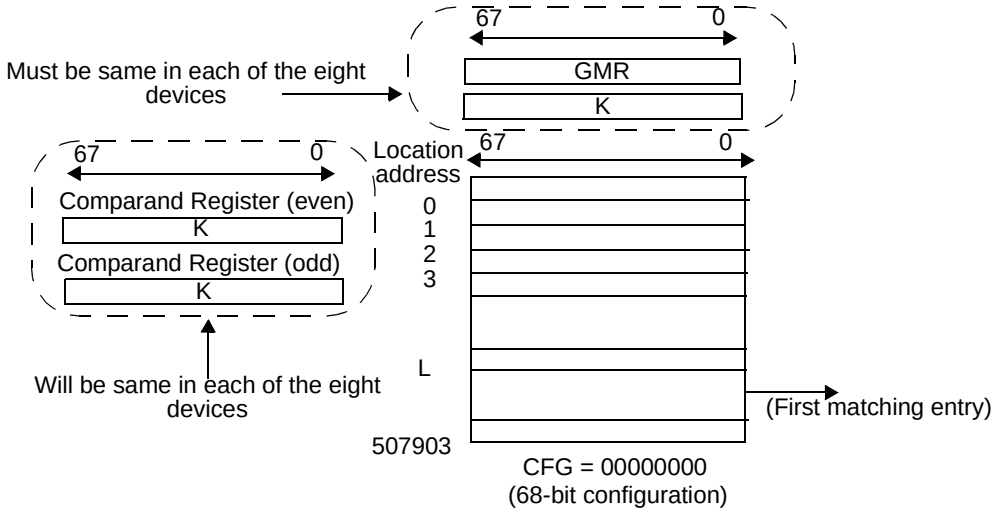


Figure 13-22. ×68 Table with 31 Devices

The Search command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 68-bit searches in ×68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit Search command cycle (two CLK2X cycles) is shown in *Table 13-7*.

Table 13-7. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K × 68 bits	4
1–8 (TLSZ = 01)	128K × 68 bits	5
1–31 (TLSZ = 10)	496K × 68 bits	6

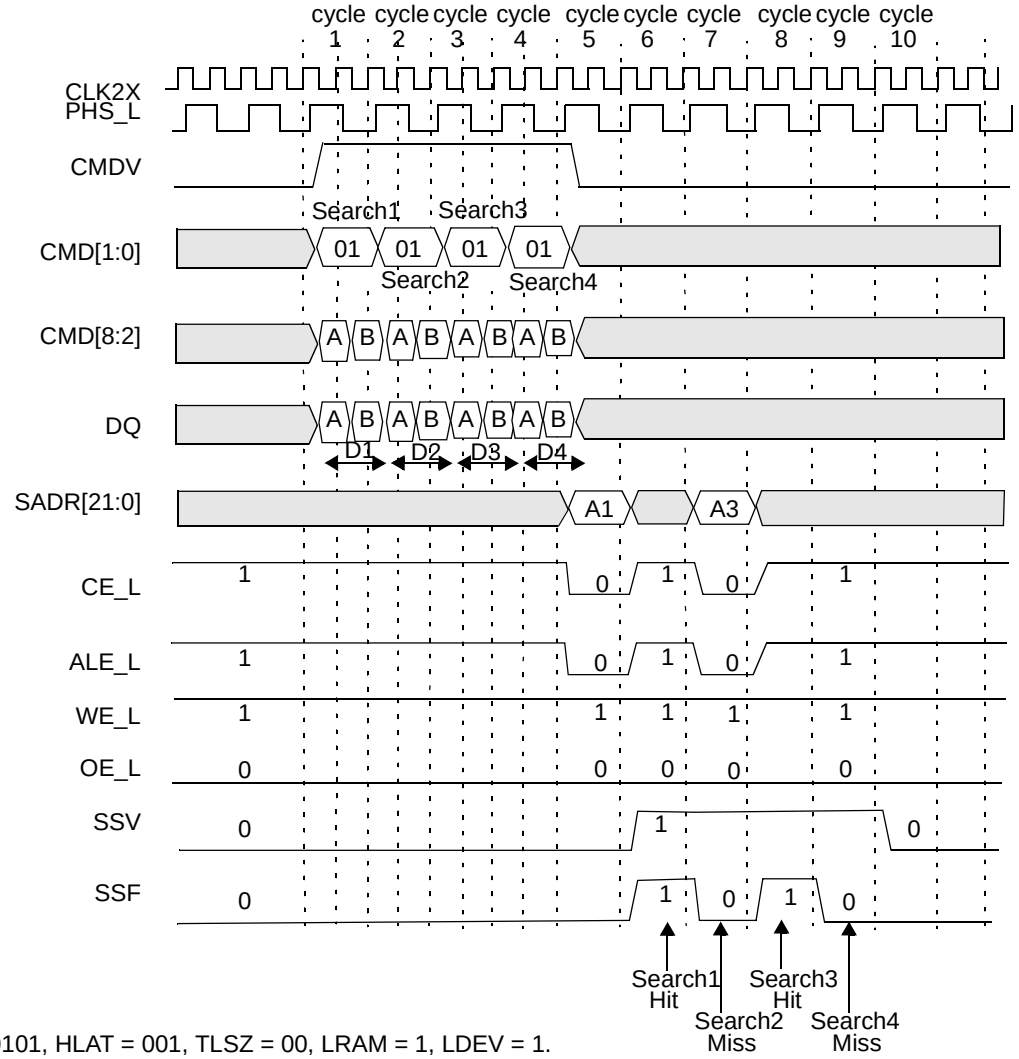
For up to 31 devices in the table (TLSZ = 10), search latency from command to SRAM access cycle is 6. In addition, SSV and SSF shift further to the right for different values of HLAT as specified in *Table 13-8*.

Table 13-8. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.4 136-bit Search on Tables Configured as ×136 Using a Single CYNSE70032 Device

Figure 13-23 shows the timing diagram for a Search command in the 136-bit-configured table (CFG = 01010101) consisting of a single device for one set of parameters: TLSZ = 00, HLAT = 001, LRAM = 1, LDEV = 1. The hardware diagram for this Search subsystem is shown in *Figure 13-24*.



CFG = 01010101, HLAT = 001, TLSZ = 00, LRAM = 1, LDEV = 1.

Figure 13-23. Timing Diagram for 136-bit Search (One Device)

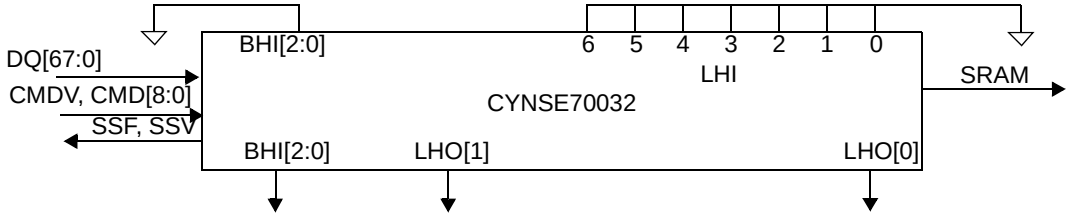


Figure 13-24. Hardware Diagram for a Table With One Device

The following is the operation sequence for a single 136-bit Search command (also refer to “Command and Command Parameters,” Subsection 12.2 on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) to CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared against all even locations. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive CMDV high and applies Search command code (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0]), compared to all odd locations.

Note. For 136-bit searches, the host ASIC must supply two distinct 68-bit data words on DQ[67:0] during cycles A and B. The even-numbered GMR of the pair specified by the GMR Index is used for masking the word in cycle A. The odd-numbered GMR of the pair specified by the GMR Index is used for masking the word in cycle B.

The logical 136-bit search operation is shown in *Figure 13-25*. The entire table of 136-bit entries is compared to a 136-bit word K (presented on the DQ bus in cycles A and B of the command) using the GMR and local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's cycle A. The 136-bit word K (presented on the DQ bus in cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's cycle B. The two comparand registers can subsequently be used by the Learn command with the even comparand register stored in an even location, and the odd comparand register stored in an adjacent odd location. The word K (presented on the DQ bus in cycles A and B of the command) is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on SADR[21:0] lines (see "SRAM Addressing" on page 98). ***Note***. The matching address is always going to be an even address for a 136-bit Search.

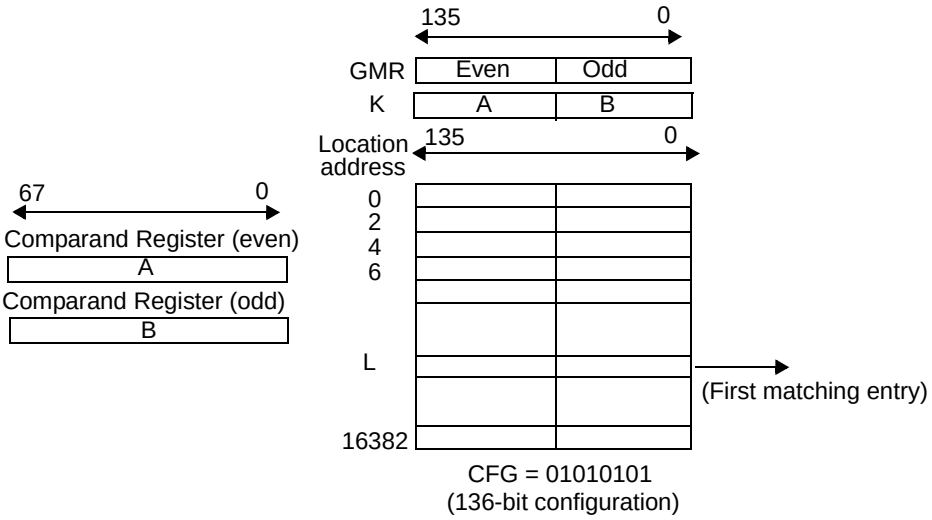


Figure 13-25. ×136 Table with One Device

The Search command is a pipelined operation that executes searches at half the rate of the frequency of CLK2X for 136-bit searches in ×136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit Search command cycle (two CLK2X cycles) is shown in *Table 13-9*.

Table 13-9. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K × 136 bits	4
1–8 (TLSZ = 01)	64K × 136 bits	5
1–31 (TLSZ = 10)	248K × 136 bits	6

For a single device in the table with TLSZ = 00, the Search latency from command to SRAM access cycle is 4. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 13-10*.

Table 13-10. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.5 136-bit Search on Tables Configured as ×136 Using up to Eight CYNSE70032 Devices

The hardware diagram of the Search subsystem of eight devices is shown in *Figure 13-26*. The following are parameters programmed into the eight devices.

- First seven devices (devices 0–6): CFG = 01010101, TLSZ = 01, HLAT = 010, LRAM = 0, and LDEV = 0.
- Eighth device (device 7): CFG = 01010101, TLSZ = 01, HLAT = 010, LRAM = 1, and LDEV = 1.

Note. All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table (device number 7 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (devices 0 through 6 in this case) must be programmed with LRAM = 0 and LDEV = 0.

Figure 13-27 shows the timing diagram for a Search command in the 136-bit-configured table of eight devices for device number 0. *Figure 13-28* shows the timing diagram for a Search command in the 136-bit-configured table consisting of eight devices for device number 1. *Figure 13-29* shows the timing diagram for a Search command in the 136-bit configured table consisting of eight devices for device number 7 (the last device in this specific table). For these timing diagrams, four 136-bit searches are performed sequentially, and the following Hit/Miss assumptions were made (see *Table 13-11*).

Table 13-11. Hit/Miss Assumptions

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Device 2–6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

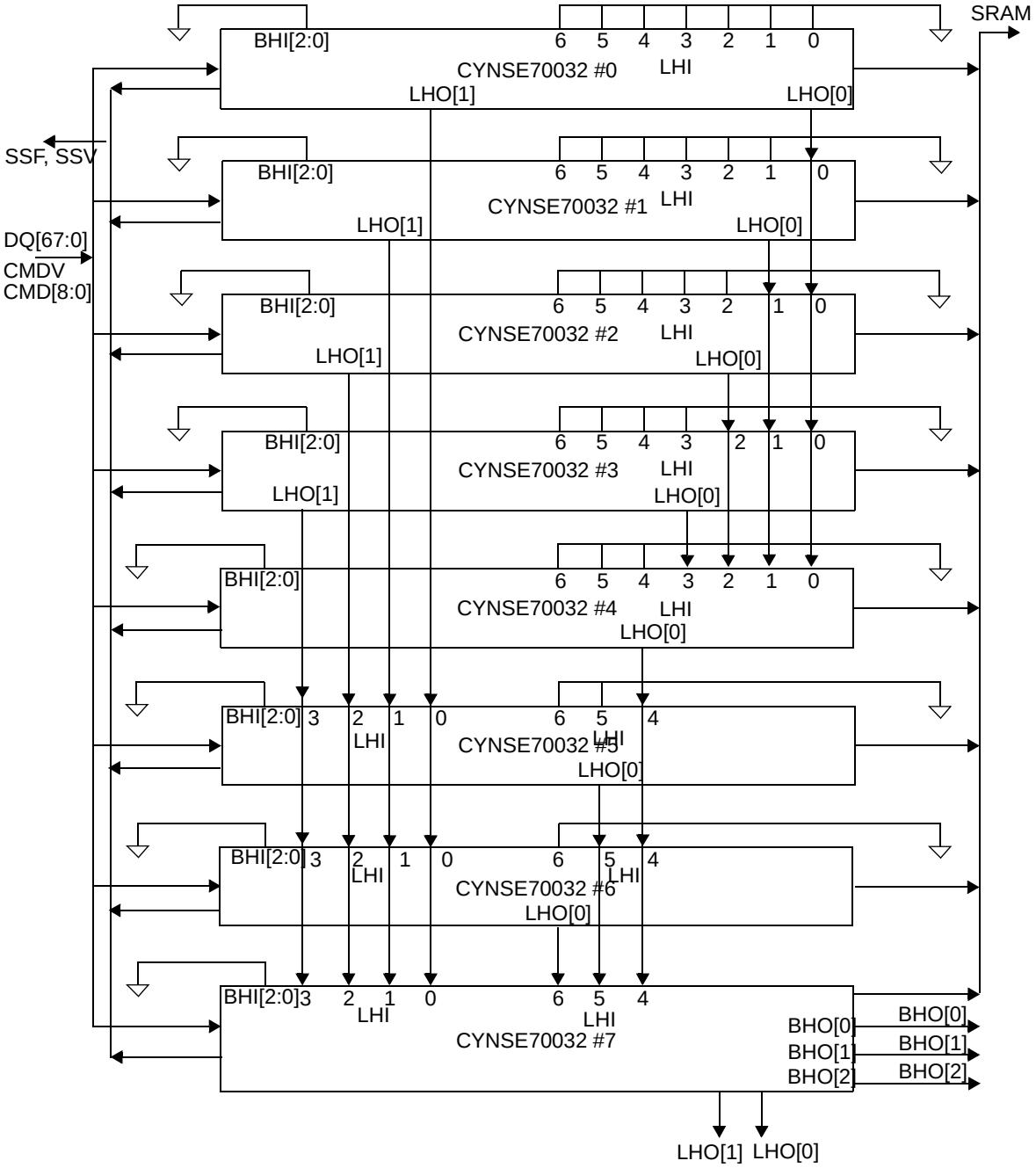
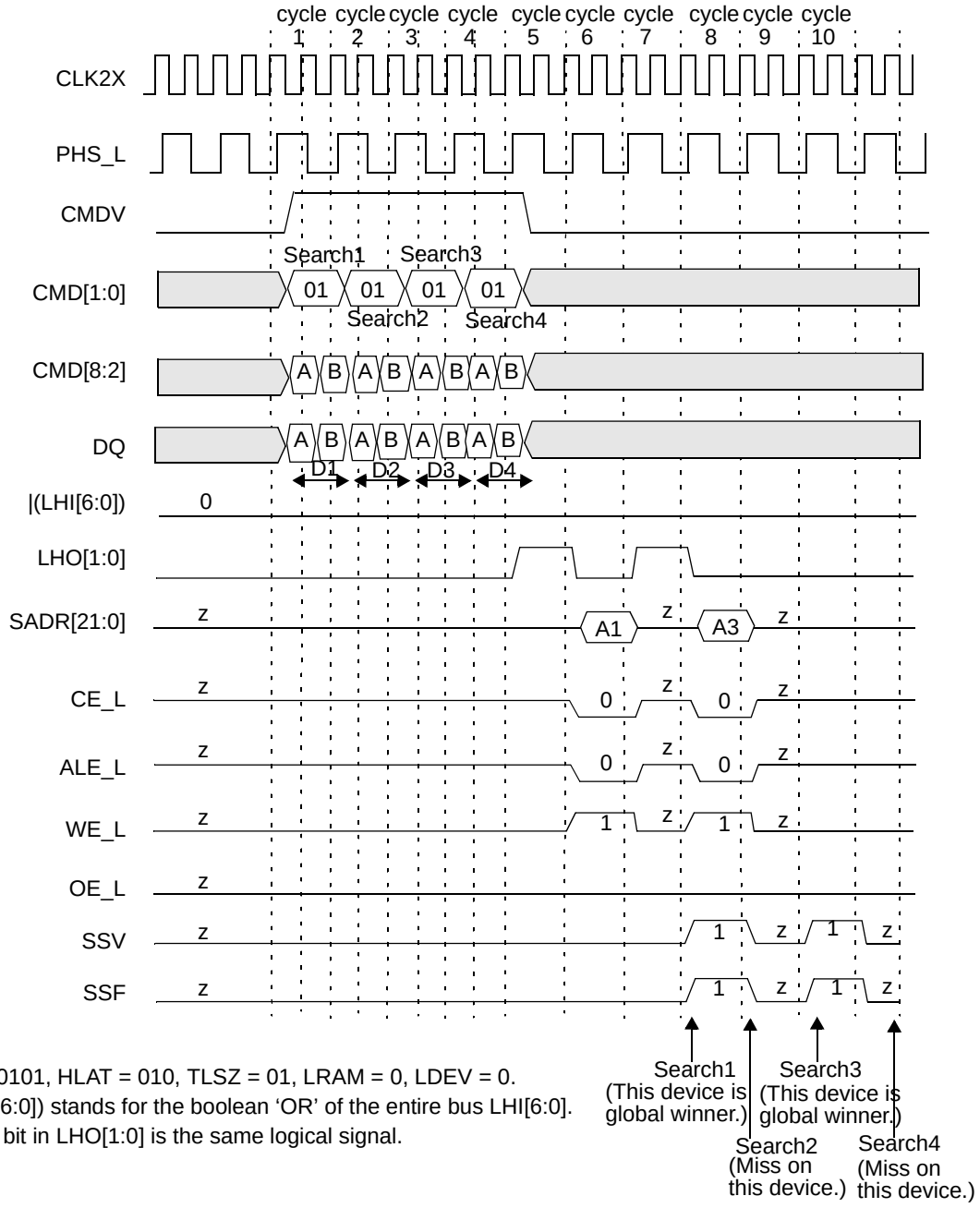
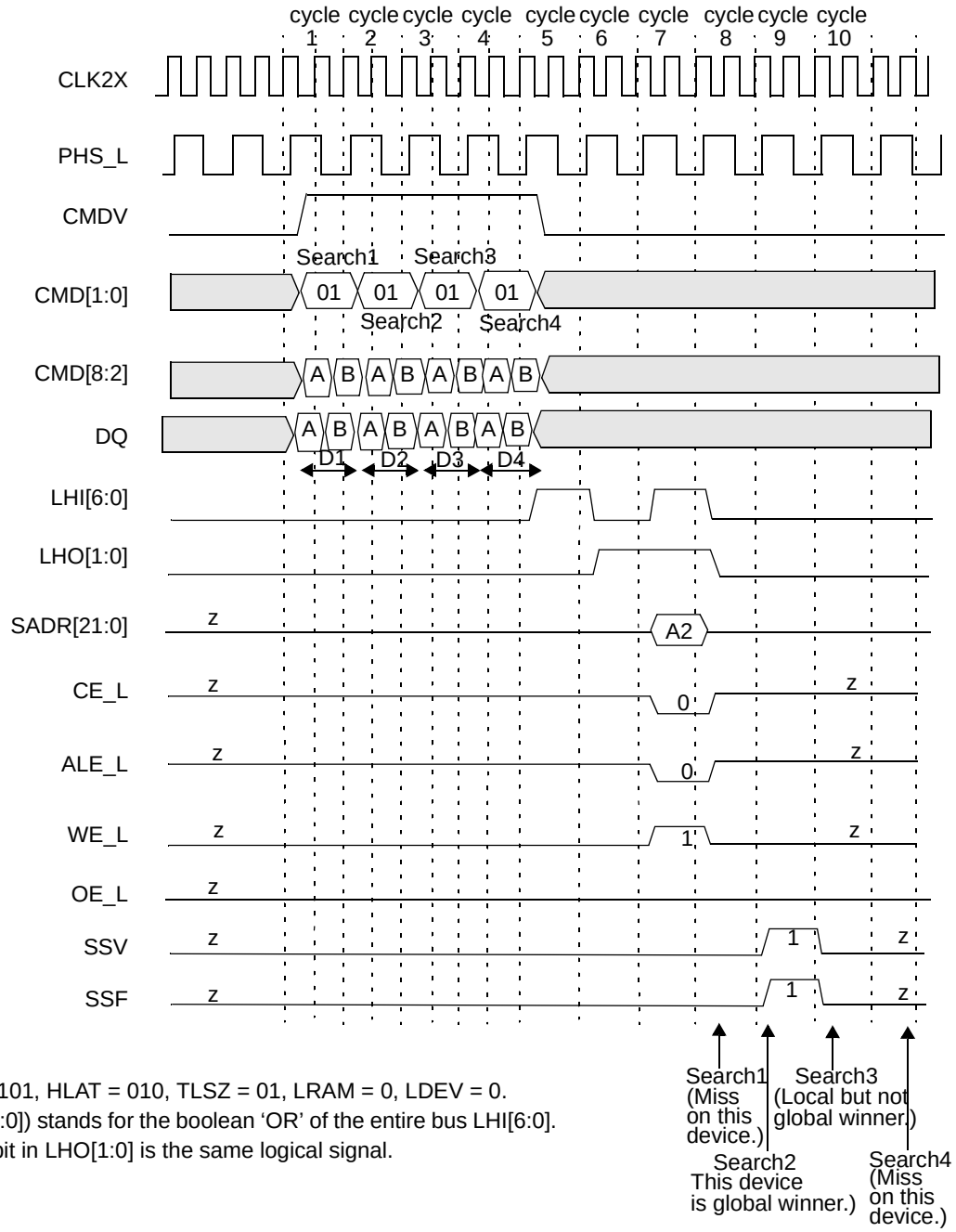


Figure 13-26. Hardware Diagram for a Table with Eight Devices



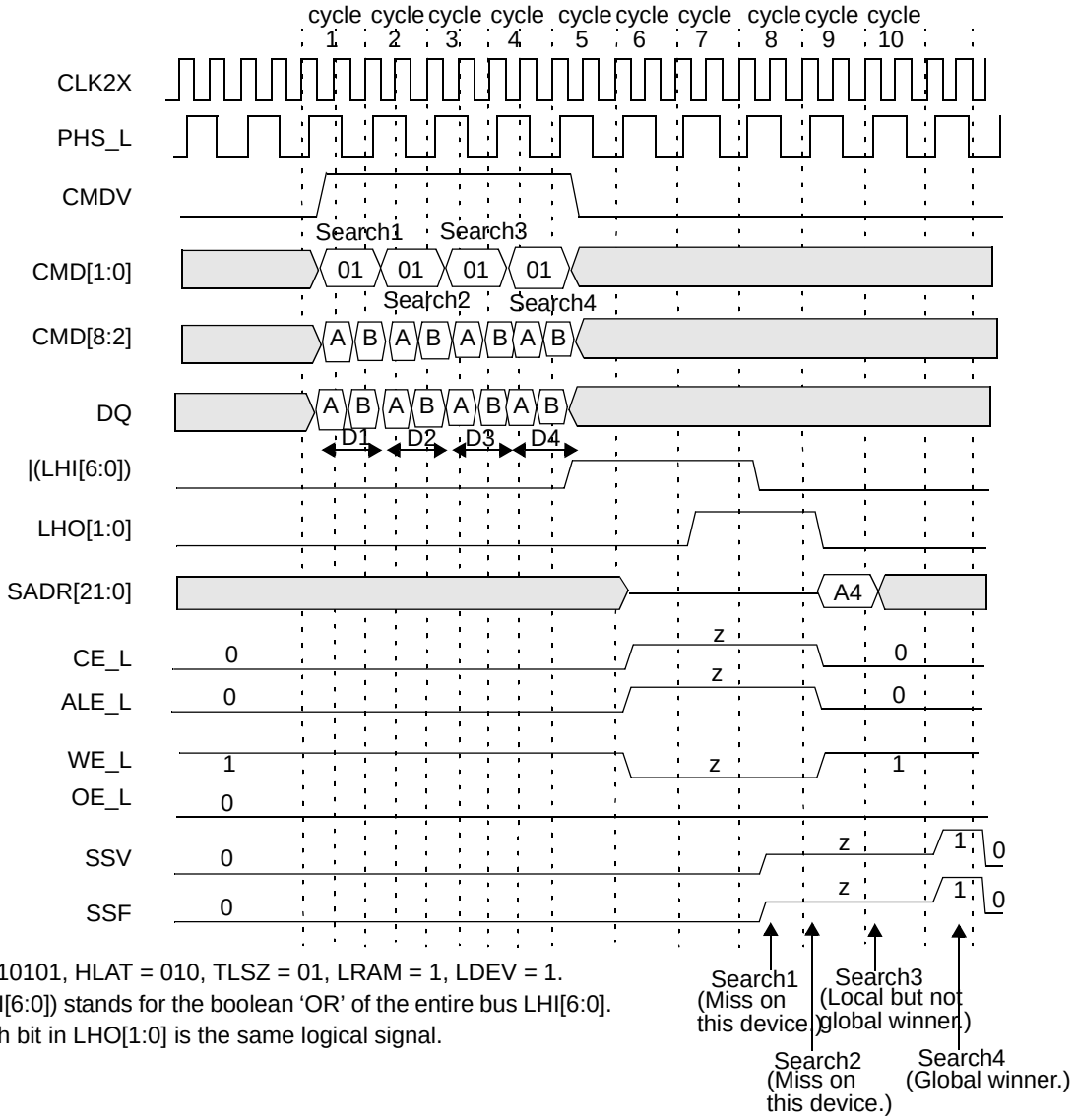
CFG = 01010101, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-27. Timing Diagram for 136-bit Search Device Number 0



CFG = 01010101, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-28. Timing Diagram for 136-bit Search Device Number 1



CFG = 01010101, HLAT = 010, TLSZ = 01, LRAM = 1, LDEV = 1.

Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].

Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-29. Timing Diagram for 136-bit Search Device Number 7 (Last Device)

The following is the sequence of operation for a single 136-bit Search command (also see Subsection 12.2, "Commands and Command Parameters" on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the same bits that will be driven by this device on SADR[21:19] if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) in order to be compared against all even locations. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive CMDV high and to apply Search command code (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the SSR index that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0]) compared against all odd locations.

The host ASIC continues to drive CMDV high and to apply Search command code (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the SSR index that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0]) compared against all odd locations.

The logical 136-bit Search operation is shown in *Figure 13-30*. The entire table (eight devices of 136-bit entries) is compared to a 136-bit word K (presented on the DQ bus in cycles A and B of the command) using the GMR and local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's cycle A.

The 136-bit word K (presented on the DQ bus in cycles A and B of the command) is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's cycle B. In ×136 configurations, the even and odd comparand register can subsequently be used by the Learn command in only one of the devices (the first non-full device). The word K (presented on the DQ bus in cycles A and B of the command) is compared to each entry in the table, starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 98). The global winning device will drive the bus in a specific cycle. On global miss cycles, the device with LRAM = 1 (the default driving device for the SRAM bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles. ***Note***. During 136-bit searches of 136-bit-configured tables, the Search hit will always be at an even address.

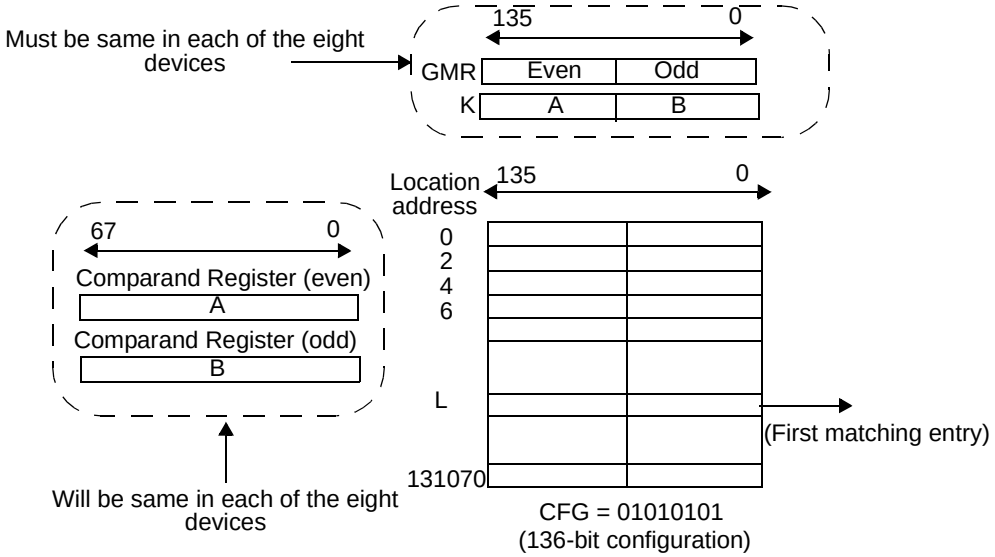


Figure 13-30. ×136 Table with Eight Devices

The Search command is a pipelined operation and executes a Search at half the rate of the CLK2X frequency for 136-bit searches in ×136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit Search command cycle (two CLK2X cycles) is shown in *Table 13-12*.

Table 13-12. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K × 136 bits	4
1–8 (TLSZ = 01)	64K × 136 bits	5
1–31 (TLSZ = 10)	248K × 136 bits	6

For one to eight devices in the table and TLSZ = 01, Search latency from command to SRAM access cycle is 5. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 13-13*.

Table 13-13. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.6 136-bit Search on Tables Configured as ×136 using up to 31 CYNSE70032 Devices

The hardware diagram of the Search subsystem of 31 devices is shown in *Figure 13-31*. Each of the four blocks in the diagram represents a block of eight CYNSE70032 devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in *Figure 13-32*. The following are the parameters programmed into the 31 devices.

- First 30 devices (devices 0–29): CFG = 01010101, TLSZ = 10, HLAT = 001, LRAM = 0, and LDEV = 0.
- 31st device (device 30): CFG = 01010101, TLSZ = 10, HLAT = 001, LRAM = 1, and LDEV = 1.

Note. All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table (device number 30 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (devices 0 through 29 in this case) must be programmed with LRAM = 0 and LDEV = 0.

The timing diagrams referred to in this paragraph reference the Hit/Miss assumptions listed in *Table 13-14*. For the purpose of illustrating timings, it is further assumed that the there is only one device with a matching entry in each of the blocks. *Figure 13-33* shows the timing diagram for a Search command in the 136-bit-configured table (31 devices) for each of the eight devices in block number 0. *Figure 13-34* shows the timing diagram for Search command in the 68-bit-configured table (31 devices) for all devices above the winning device in block number 1. *Figure 13-35* shows the timing diagram for the globally winning device (the winner within its own and all blocks) in block number 1. *Figure 13-36* shows the timing diagram for all devices below the globally winning device in block number 1. *Figure 13-37*, *Figure 13-38*, and *Figure 13-39*, respectively, show the timing diagrams of the devices above globally winning device, the globally winning device, and the devices below the globally winning device for block number 2. *Figure 13-40*, *Figure 13-41*, *Figure 13-42*, and *Figure 13-43*, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device except the last device (device 30) for block number 3, and then the last device (device 30) for block number 3.

The 136-bit Search operation is pipelined and executes as follows. Four cycles from the Search command, each of the devices knows the outcome internal to it for that operation. In the fifth cycle after the Search command, the devices in a block arbitrate for a winner from among them (a “block” being less than or equal to eight devices resolving the winner by using LHI[6:0] and LHO[1:0] signalling mechanisms). In the sixth cycle after the Search command, the blocks of devices resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanisms. The winning device in the winning block is the global winning device for a Search operation.

Table 13-14. Hit/Miss Assumptions

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

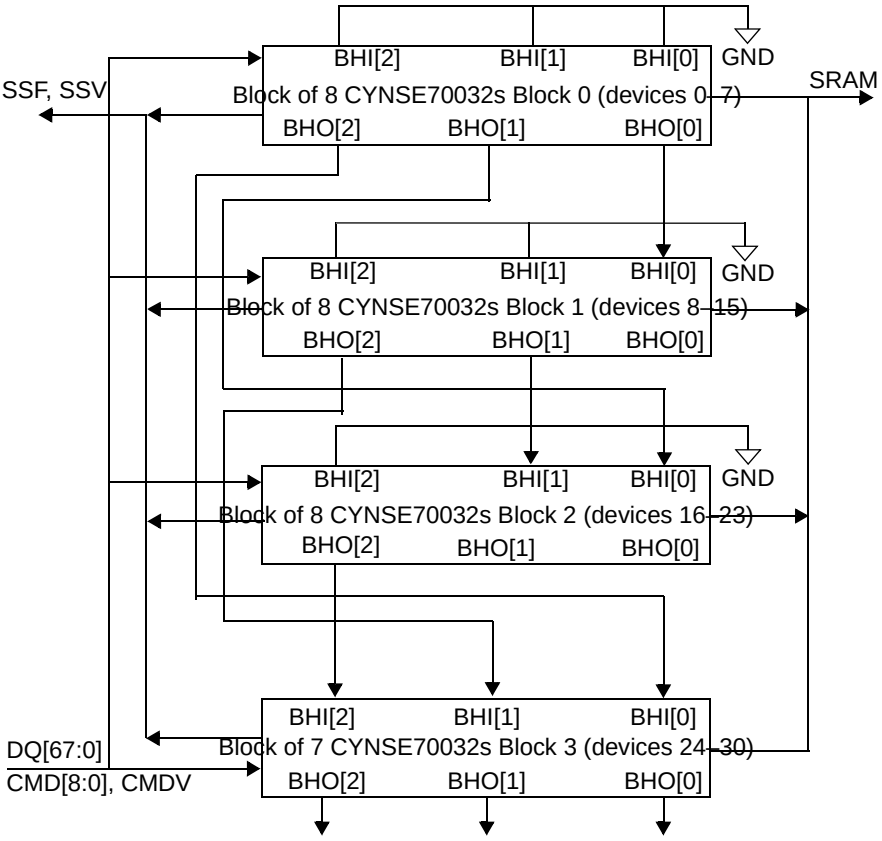


Figure 13-31. Hardware Diagram for a Table with 31 Devices

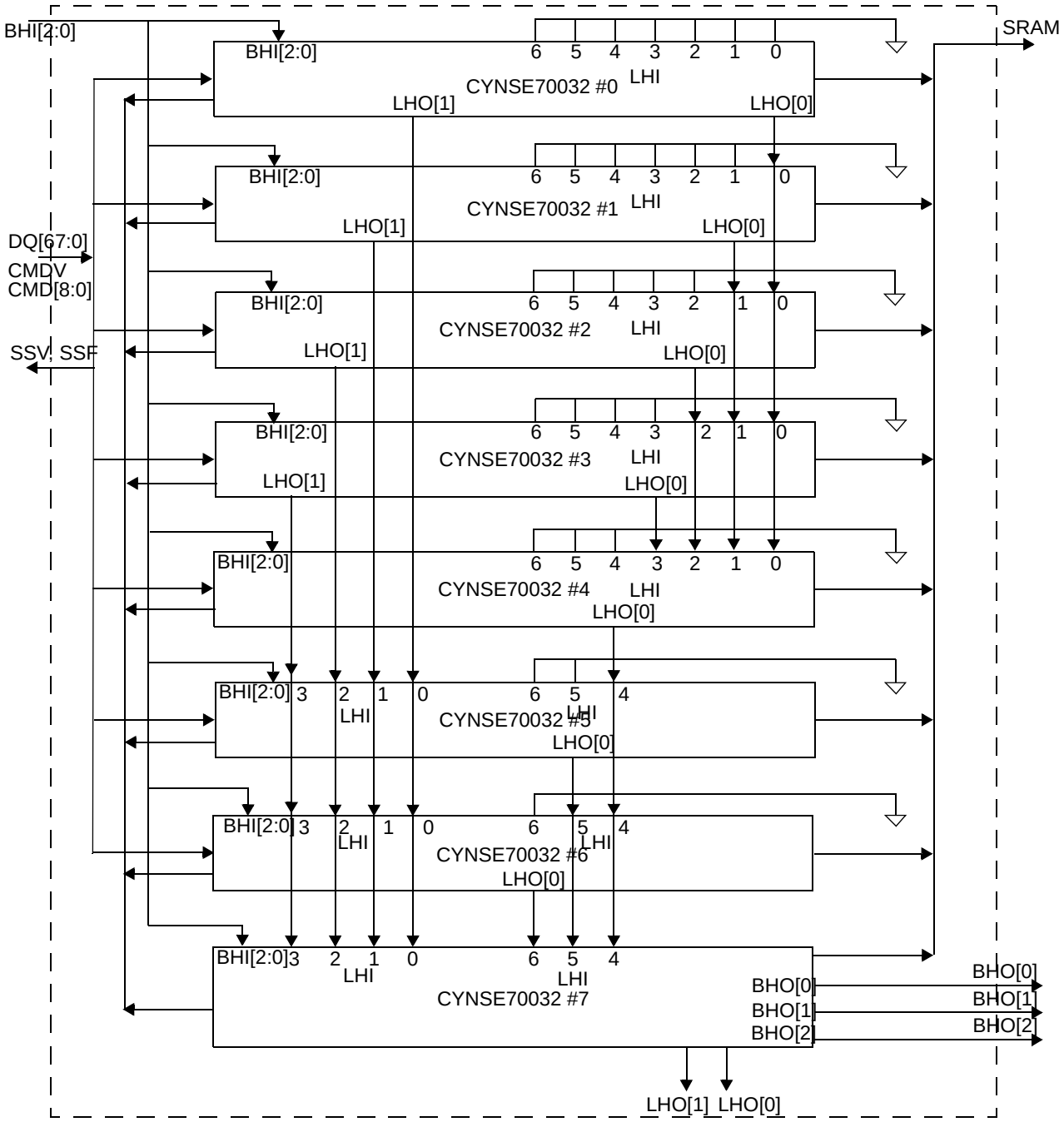
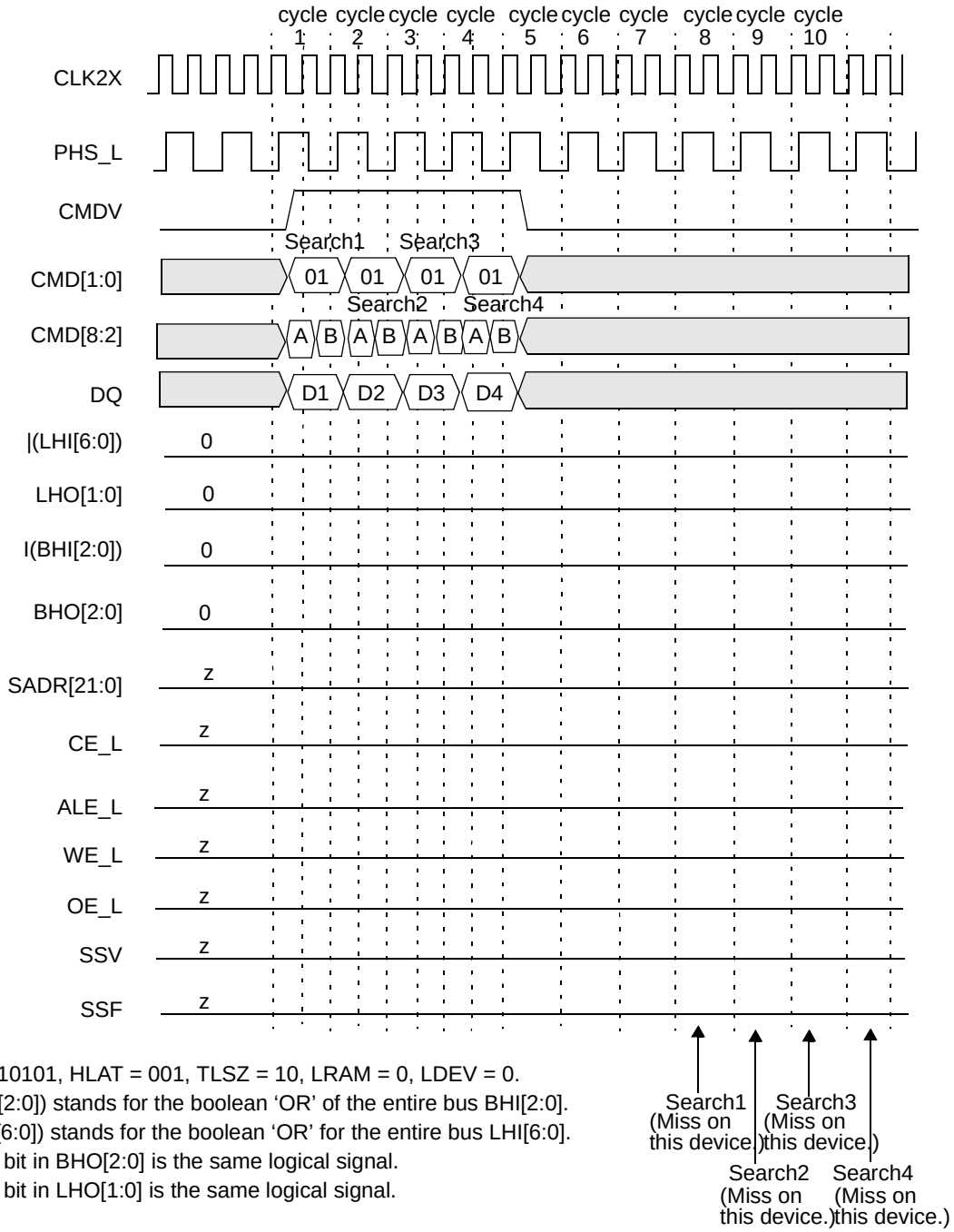
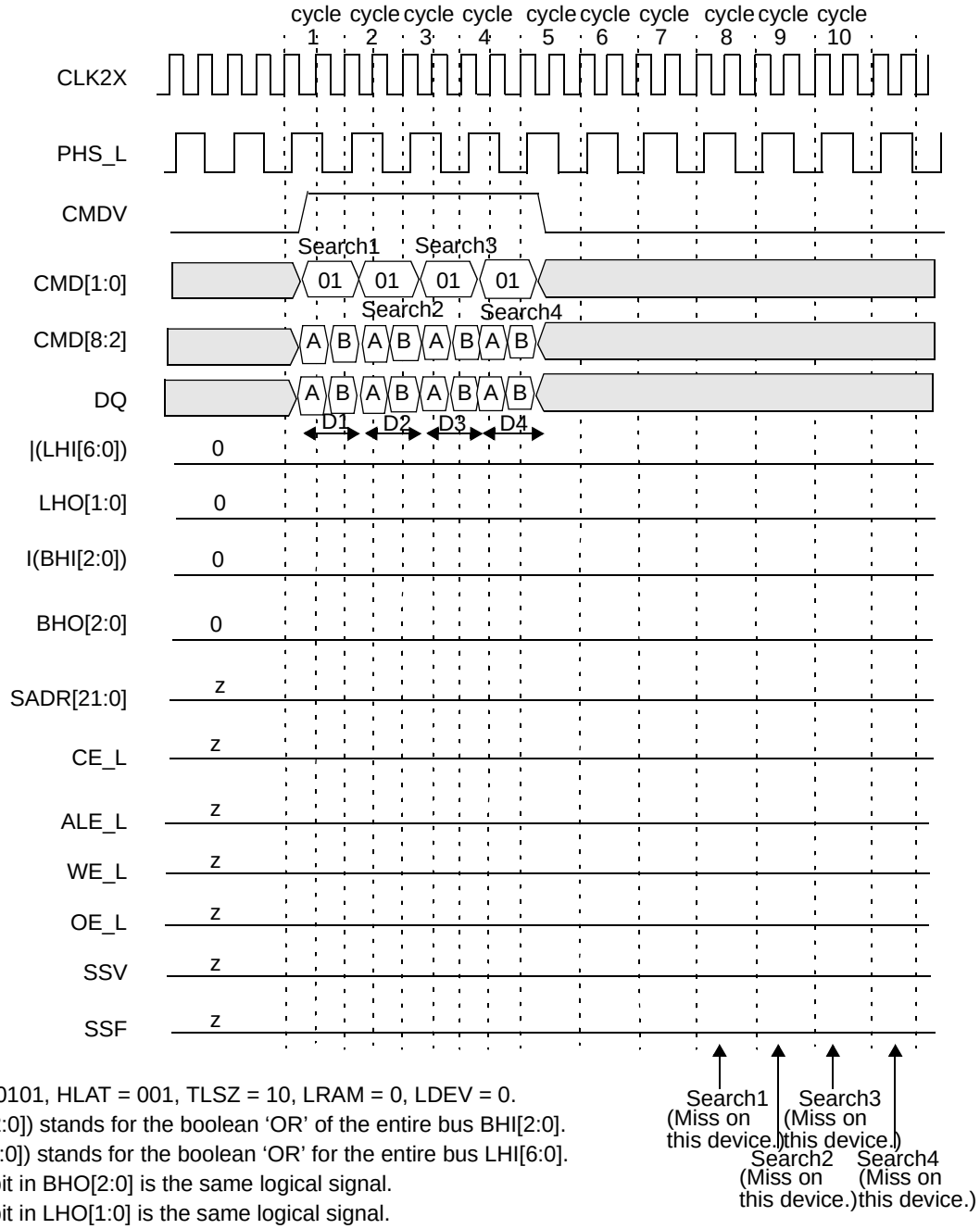


Figure 13-32. Hardware Diagram for a Block of up to Eight Devices



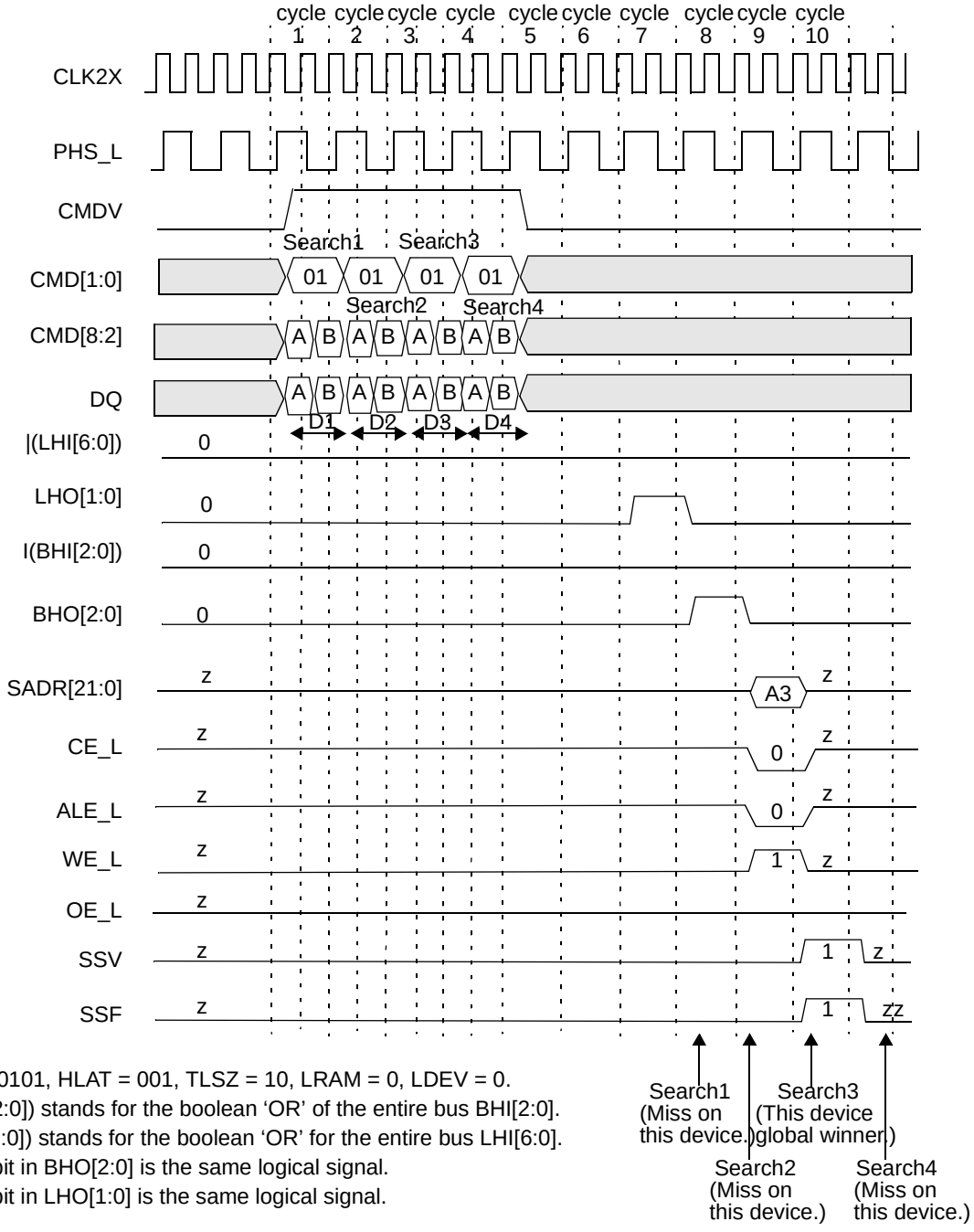
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-33. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



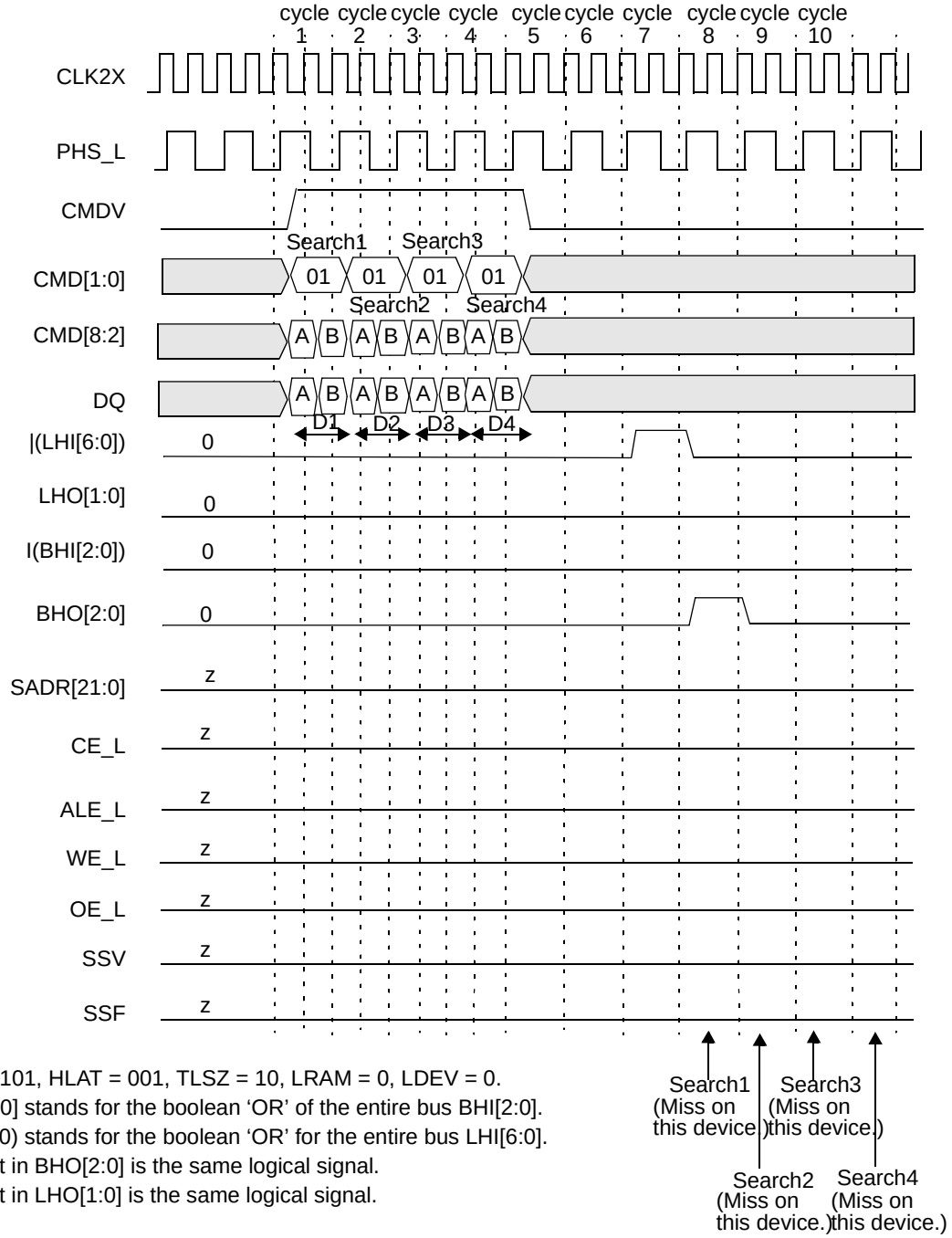
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-34. Timing Diagram for Each Device Above the Winning Device in Block Number 1



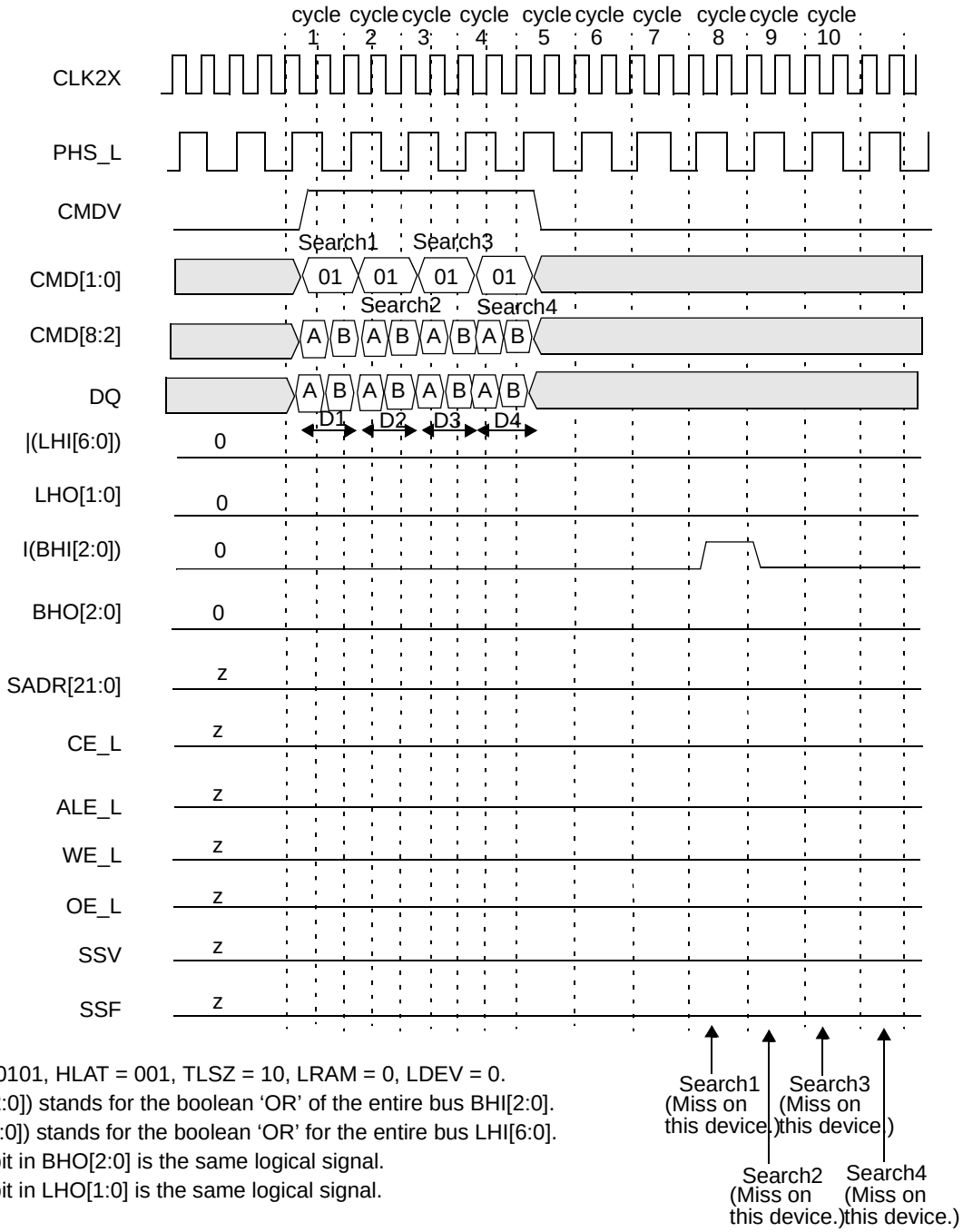
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-35. Timing Diagram for Globally Winning Device in Block Number 1



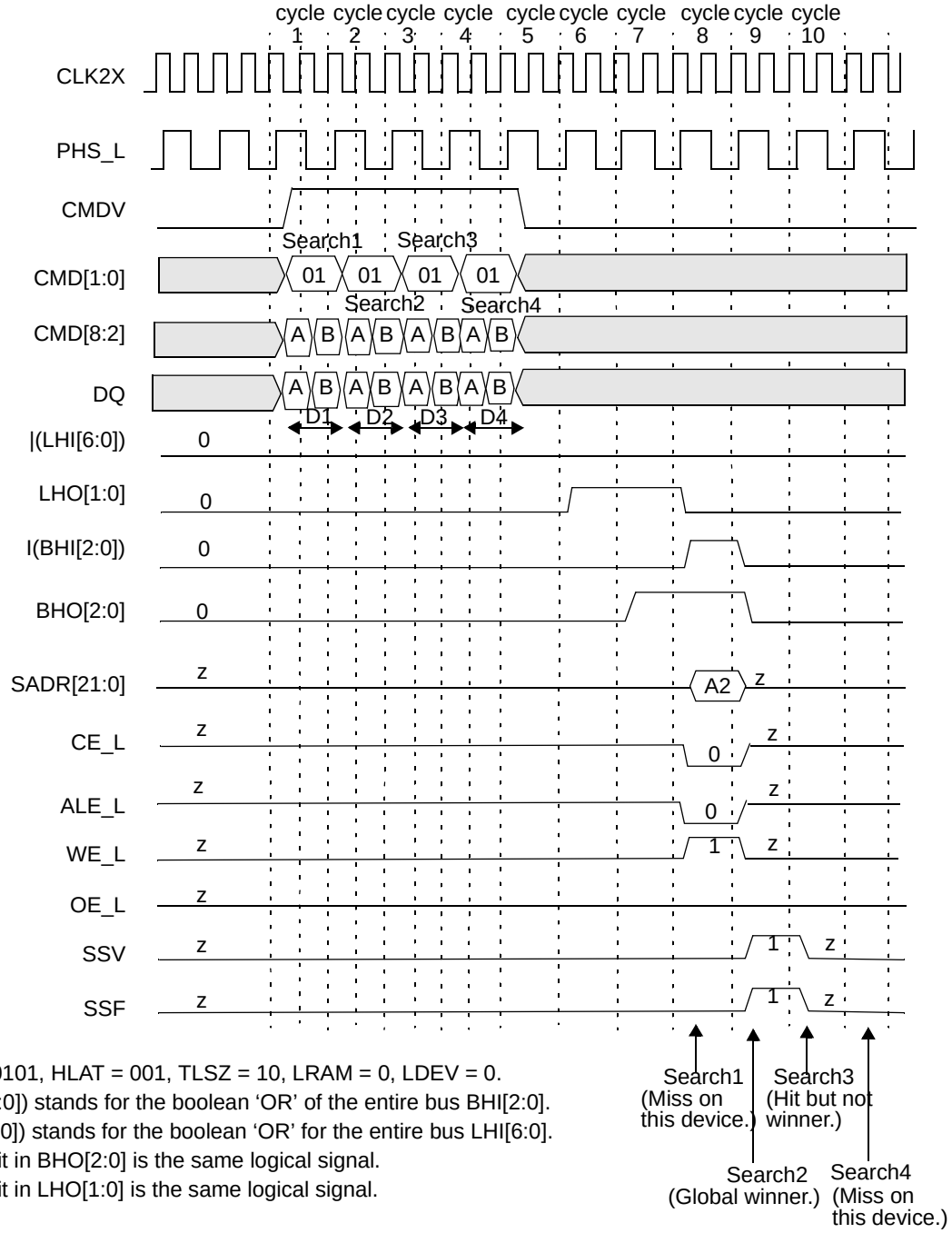
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI(6:0) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-36. Timing Diagram for Devices Below the Winning Device in Block Number 1



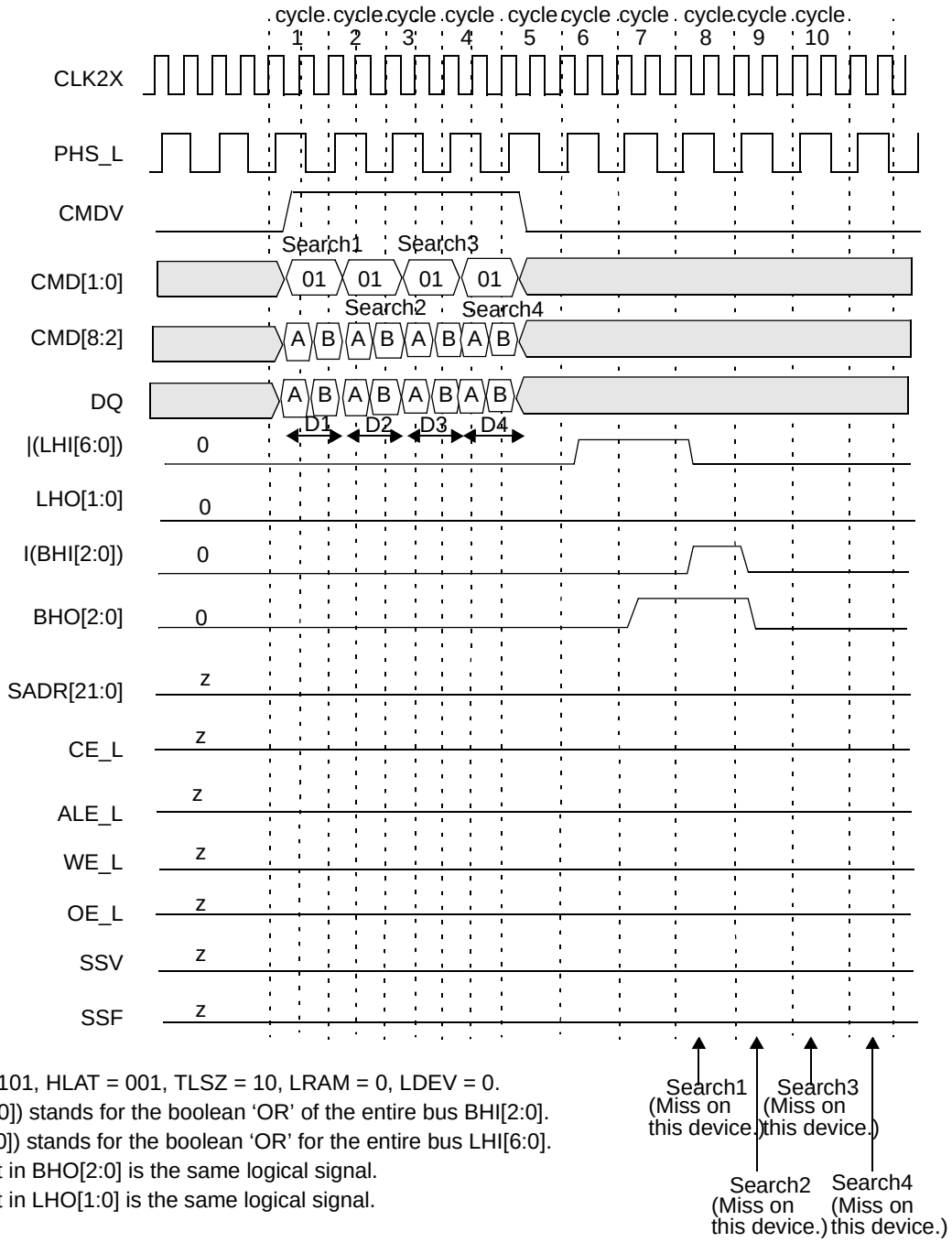
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-37. Timing Diagram for Devices Above the Winning Device in Block Number 2



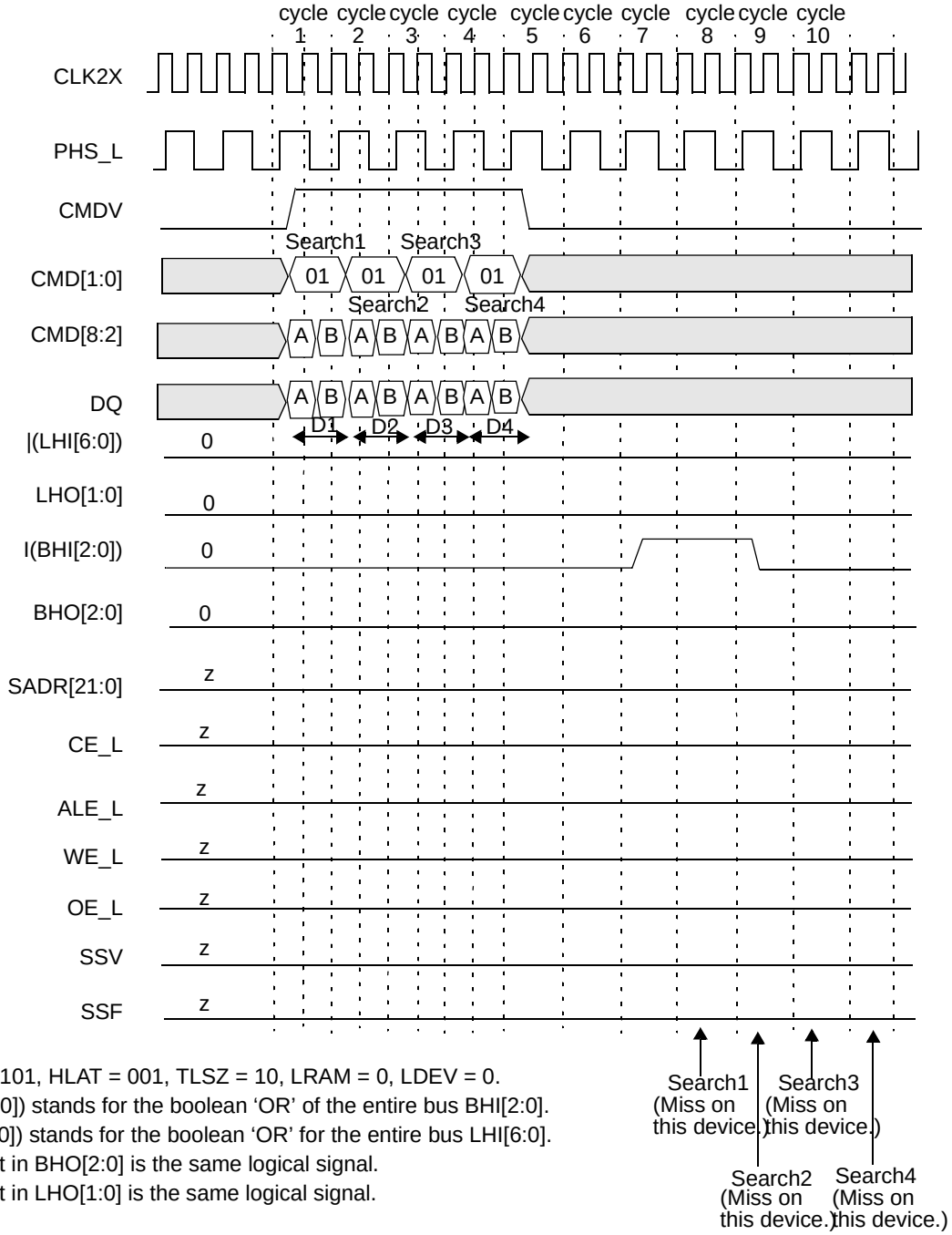
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-38. Timing Diagram for Globally Winning Device in Block Number 2



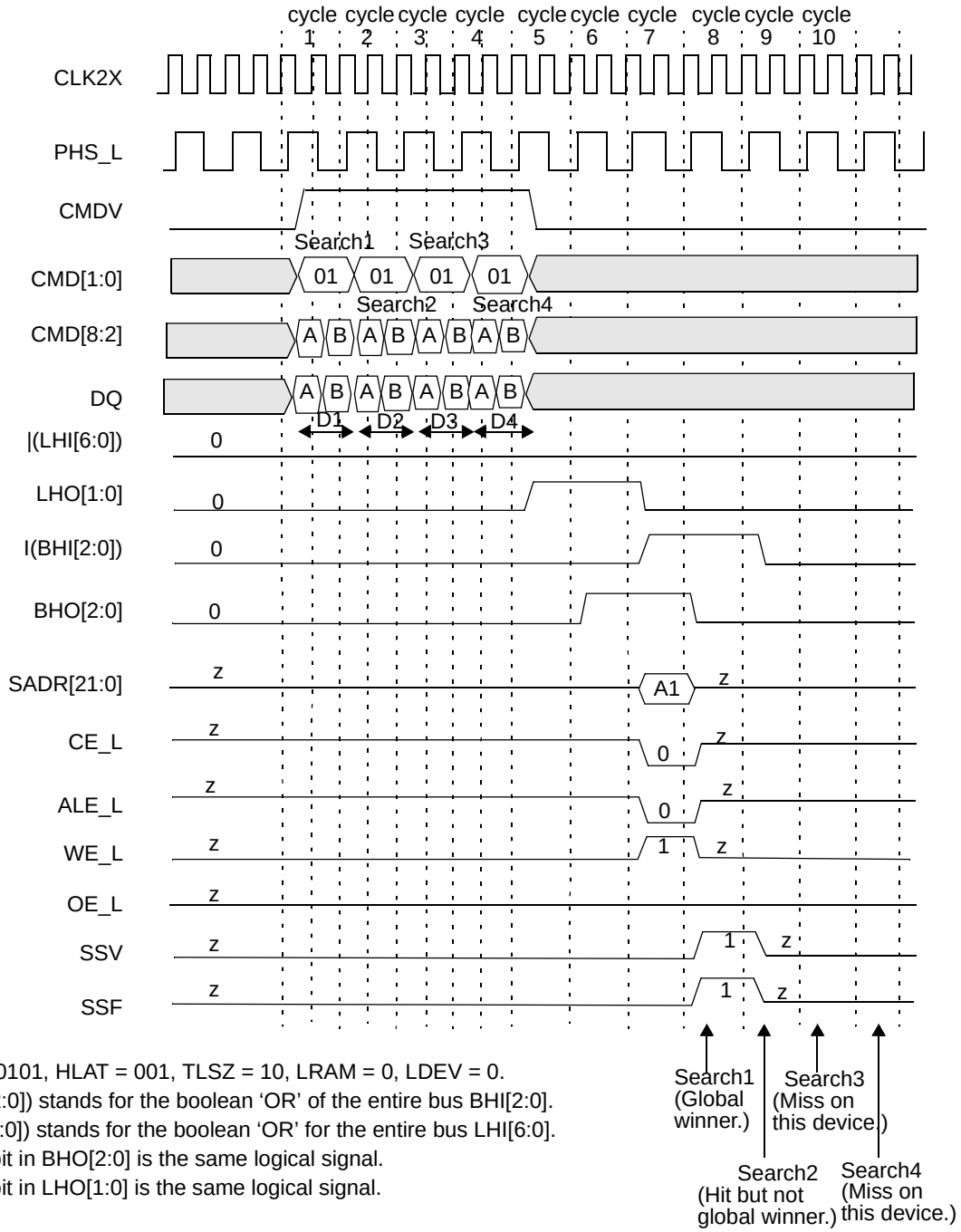
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-39. Timing Diagram for Devices Below the Winning Device in Block Number 2



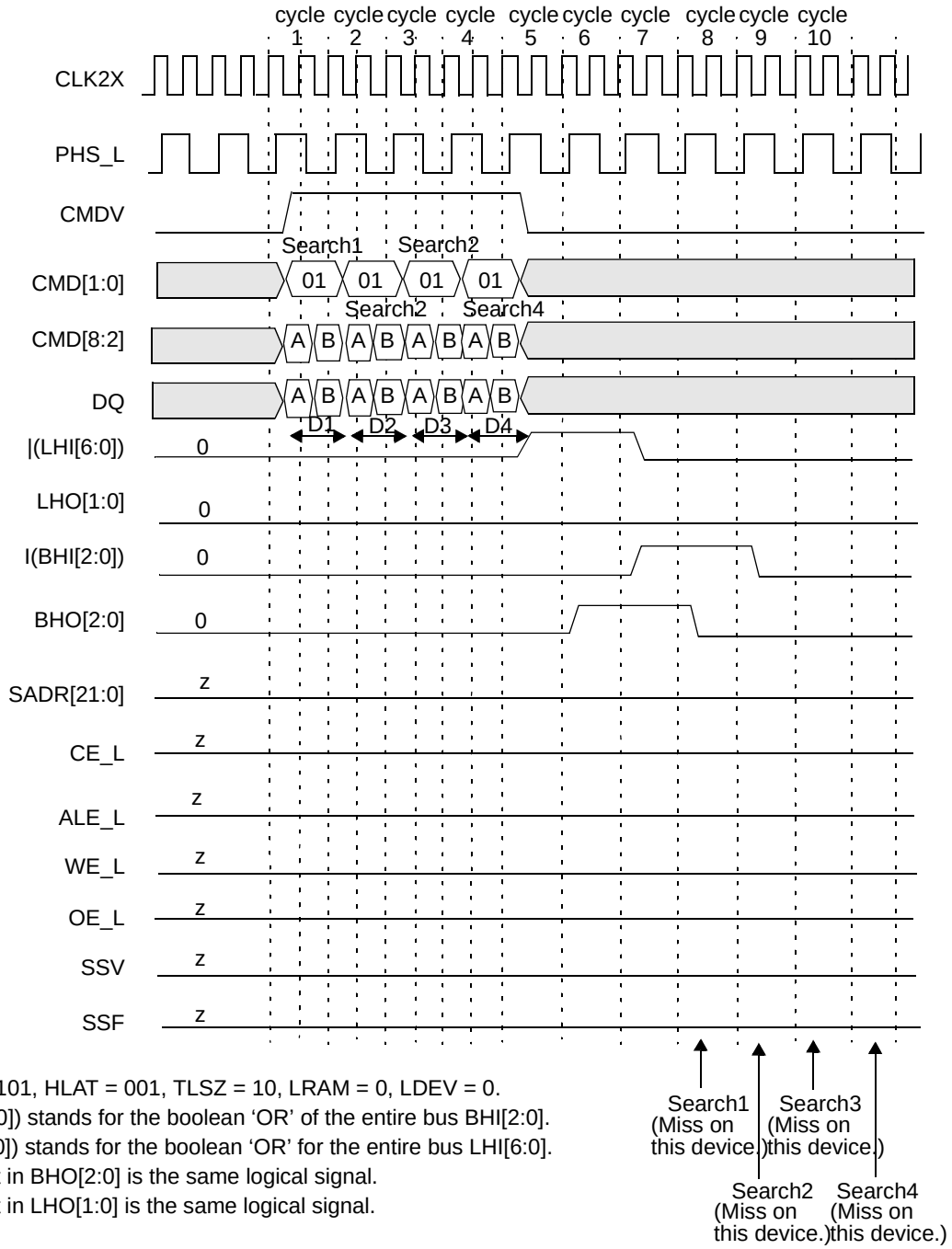
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-40. Timing Diagram for Devices Above the Winning Device in Block Number 3



CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-41. Timing Diagram for Globally Winning Device in Block Number 3



CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-42. Timing Diagram for Devices Below the Winning Device in Block Number 3 Except Device Number 30 (the Last Device)

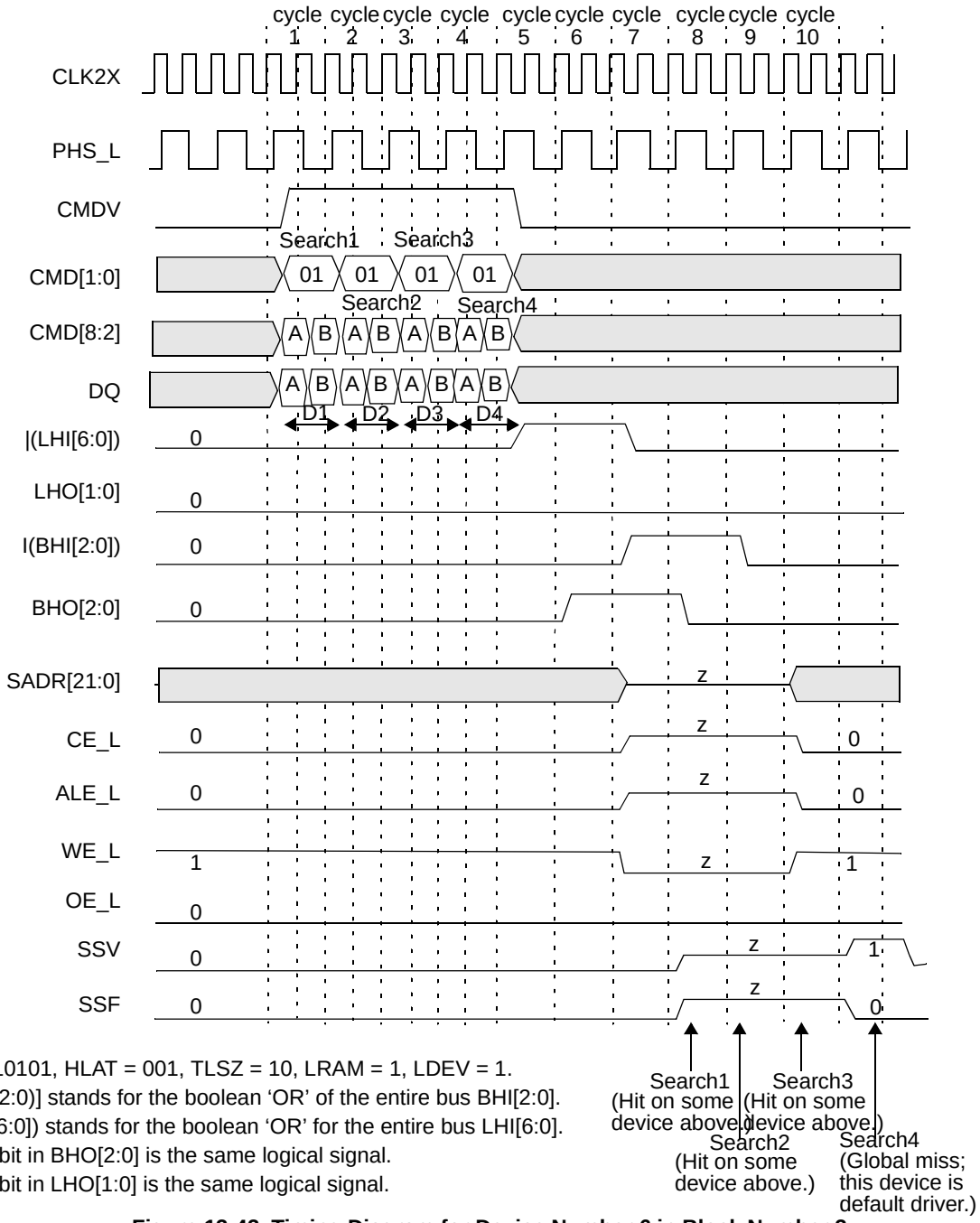


Figure 13-43. Timing Diagram for Device Number 6 in Block Number 3 (Device Number 30 in Depth-Cascaded Table)

The following is the sequence of operation for a single 136-bit Search command (also refer to "Command and Command Parameters," Subsection 12.2 on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:6] signals must be driven with the bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) in order to be compared against all even locations. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive CMDV high and to apply Search command code (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching

entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0])to be compared against all odd locations.

A logical 136-bit Search operation is shown in *Figure 13-44*. The entire table made up of 31 devices and consisting of 136-bit entries is compared against a 136-bit word K that is presented on the DQ bus (using the GMR and local mask bits) in cycles A and B of the command. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's cycle A.

The 136-bit word K that is presented on the DQ bus in cycles A and B of the command is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's cycle B. In ×136 configurations, the even and odd comparand registers can subsequently be used by the Learn command in the first non-full device only. ***Note***. The Learn command is supported for only one of the blocks consisting of up to eight devices in a depth-cascaded table of more than one block. The word K that is presented on the DQ bus in cycles A and B of the command is compared with each entry in the table, starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see Section 15.0, "SRAM Addressing" on page 98). The global winning device will drive the bus in a specific cycle. In global miss cycles, the device with LRAM = 1 (the default driving device for the SRAM bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles. ***Note***. During 136-bit searches of 136-bit-configured tables, the Search hit will always be at an even address.

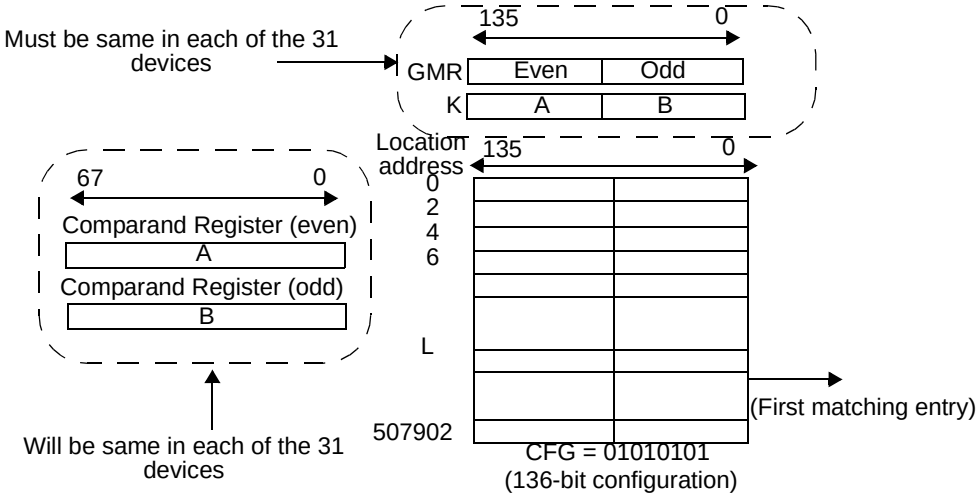


Figure 13-44. x136 Table with 31 Devices

The Search command is a pipelined operation. It executes a Search at half the rate of the frequency of CLK2X for 136-bit searches in ×136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit Search command cycle (two CLK2X cycles) is shown in *Table 13-15*.

Table 13-15. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K × 136 bits	4
1–8 (TLSZ = 01)	64K × 136 bits	5
1–31 (TLSZ = 10)	248K × 136 bits	6

Search latency from command to SRAM access cycle is 6 for 1–31 devices in the table and TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 13-16*.

Table 13-16. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.7 272-bit Search on Tables Configured as ×272 using a Single CYNSE70032 Device

Figure 13-45 shows the timing diagram for a Search command in the 272-bit-configured table (CFG = 10101010) consisting of a single device for one set of parameters: TLSZ = 00, HLAT = 001, LRAM = 1, and LDEV = 1. The hardware diagram for this search subsystem is shown in *Figure 13-46*.

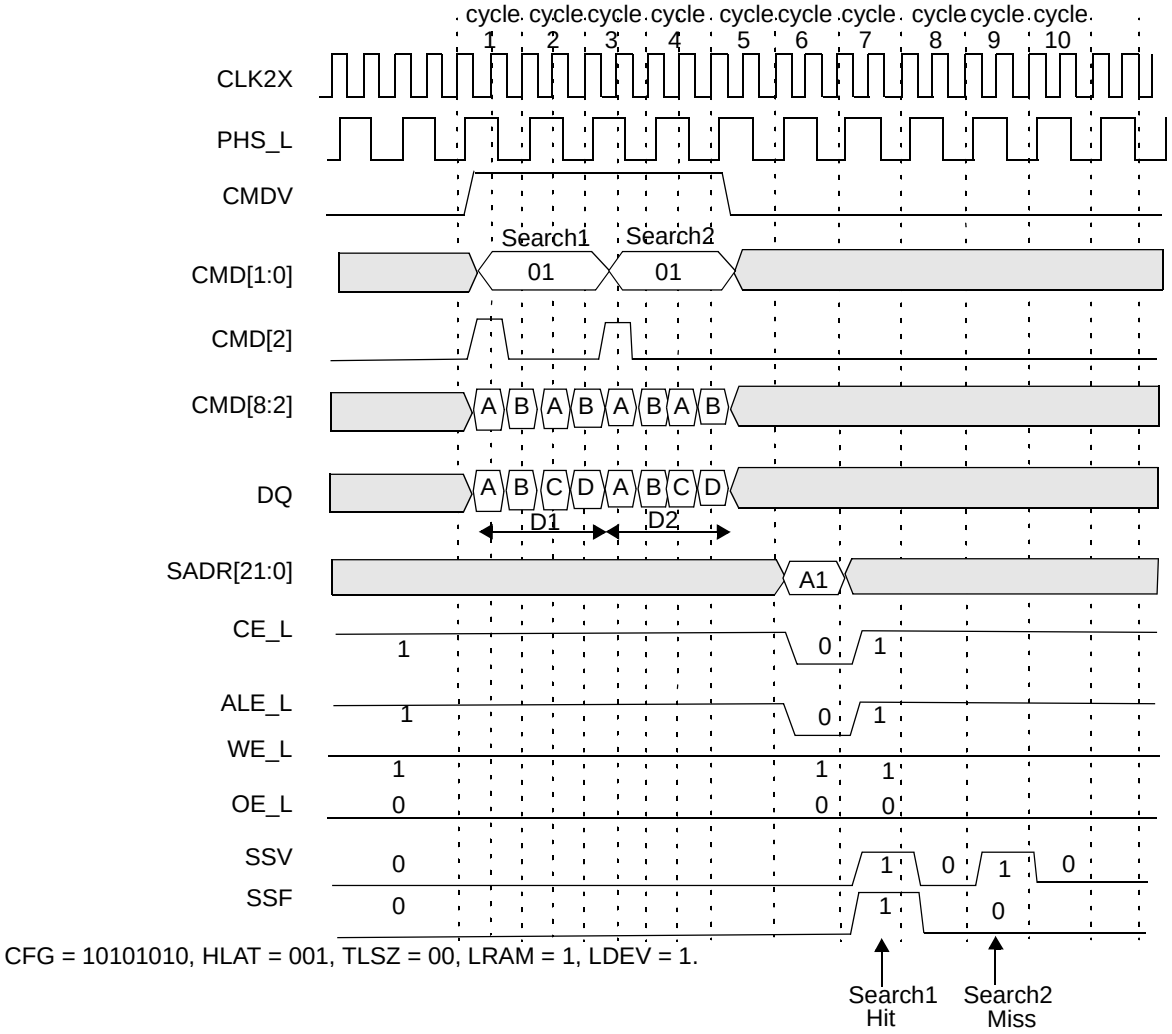


Figure 13-45. Timing Diagram for 272-bit Search (One Device)

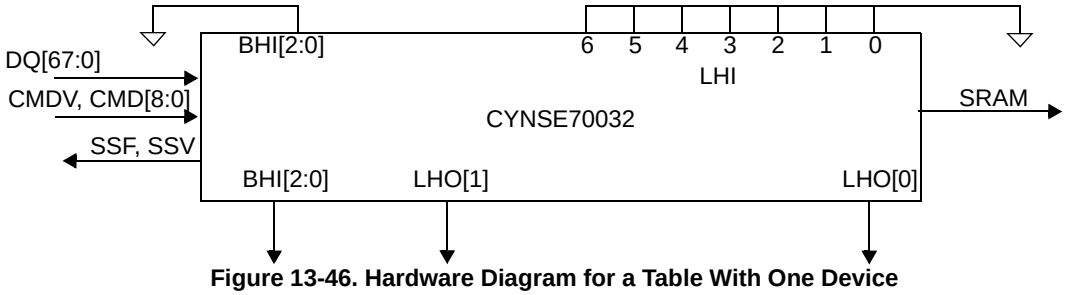


Figure 13-46. Hardware Diagram for a Table With One Device

The following is the sequence of operation for a single 136-bit Search command (also refer to Subsection 12.2, “Commands and Command Parameters” on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared to all locations 0 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 1. ***Note***. CMD[2] = 1 signals that the search is a x272-bit search. CMD[8:3] in this cycle is ignored.

- **Cycle B**: The host ASIC continues to drive CMDV high and continues to apply Search command code (10) on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared to all locations 1 in the four 68-bits-word page.
- **Cycle C**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [135:0] of the data being searched. CMD[8:6] signals must be driven with the bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared to all locations 2 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 0.
- **Cycle D**: The host ASIC continues to drive the CMDV high and applies Search command code (10) on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations 3 in the four 68-bits-word page. CMD[5:2] is ignored because the Learn instruction is not supported for x272 tables.

Note. For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during cycles A, B, C, and D. The GMR index in cycle A selects a pair of GMRs that apply to DQ data in cycles A and B. The GMR index in cycle C selects a pair of GMRs that apply to DQ data in cycles C and D.

The logical 272-bit Search operation is shown in *Figure 13-47*. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's cycles A and C. The 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on SADR[21:0] lines (see "SRAM Addressing" on page 98). ***Note***. The matching address is always going to be location 0 in a four-entry page for a 272-bit Search (two LSBs of the matching index will be 00).

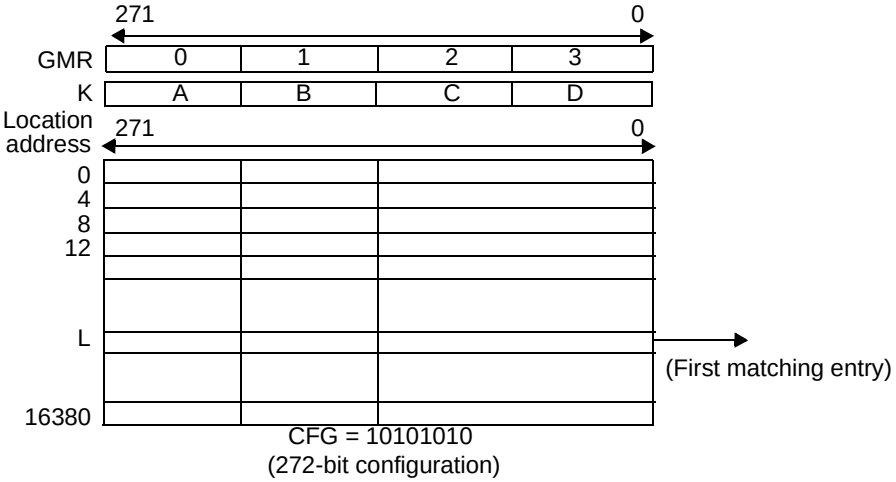


Figure 13-47. x272 Table with One Device

The Search command is a pipelined operation and executes at one-fourth the rate of the frequency of CLK2X for 272-bit searches in ×272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit Search command (measured in CLK cycles) from the CLK2X cycle that contains the C and D cycles is shown in *Table 13-17*.

Table 13-17. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	4K × 272 bits	4
1–8 (TLSZ = 01)	32K × 272 bits	5
1–31 (TLSZ = 10)	124K × 272 bits	6

Search latency from command to SRAM access cycle is 4 for a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 13-18*.

Table 13-18. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3

Table 13-18. Shift of SSF and SSV from SADR (continued)

HLAT	Number of CLK Cycles
100	4
101	5
110	6
111	7

13.8 272-bit Search on Tables Configured as ×272 and Using up to Eight CYNSE70032 Devices

The hardware diagram of the Search subsystem of eight devices is shown in *Figure 13-48*. The following are the parameters programmed into the eight devices.

- First seven devices (devices 0–6): CFG = 10101010, TLSZ = 01, HLAT = 000, LRAM = 0, and LDEV = 0.
- Eighth device (device 7): CFG = 10101010, TLSZ = 01, HLAT = 000, LRAM = 1, and LDEV = 1.

Note. All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 6 in this case).

Figure 13-49 shows the timing diagram for a Search command in the 272-bit-configured table of eight devices for device number 0. *Figure 13-50* shows the timing diagram for a Search command in the 272-bit-configured table of eight devices for device number 1. *Figure 13-51* shows the timing diagram for a Search command in the 272-bit-configured table of eight devices for device number 7 (the last device in this specific table). For these timing diagrams, three 272-bit searches are performed sequentially. The following Hit/Miss assumptions were made, as shown in *Table 13-19*.

Table 13-19. Hit/Miss Assumptions

Search Number	1	2	3
Device 0	Hit	Miss	Miss
Device 1	Miss	Hit	Miss
Devices 2–6	Miss	Miss	Miss
Device 7	Miss	Miss	Miss

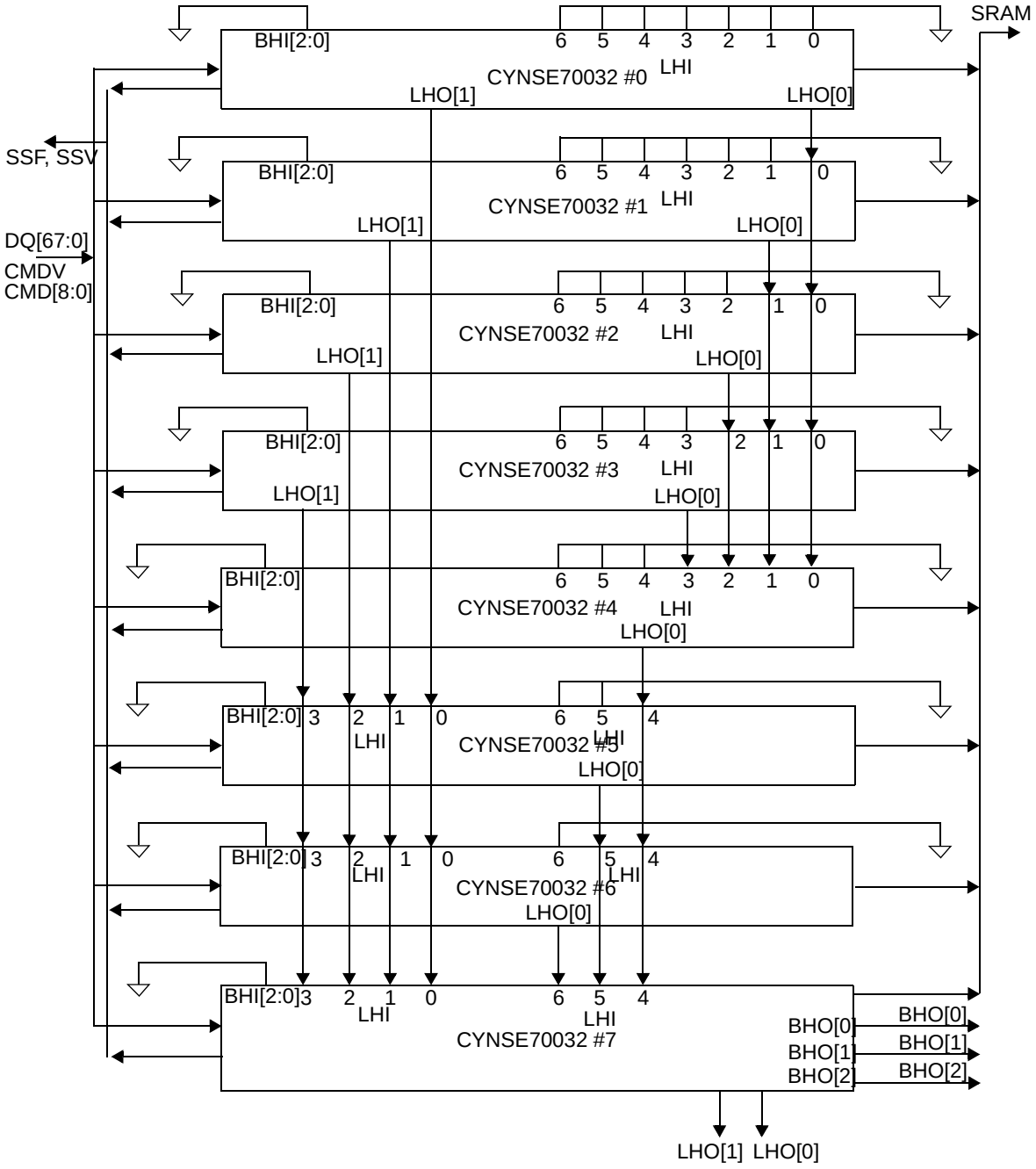
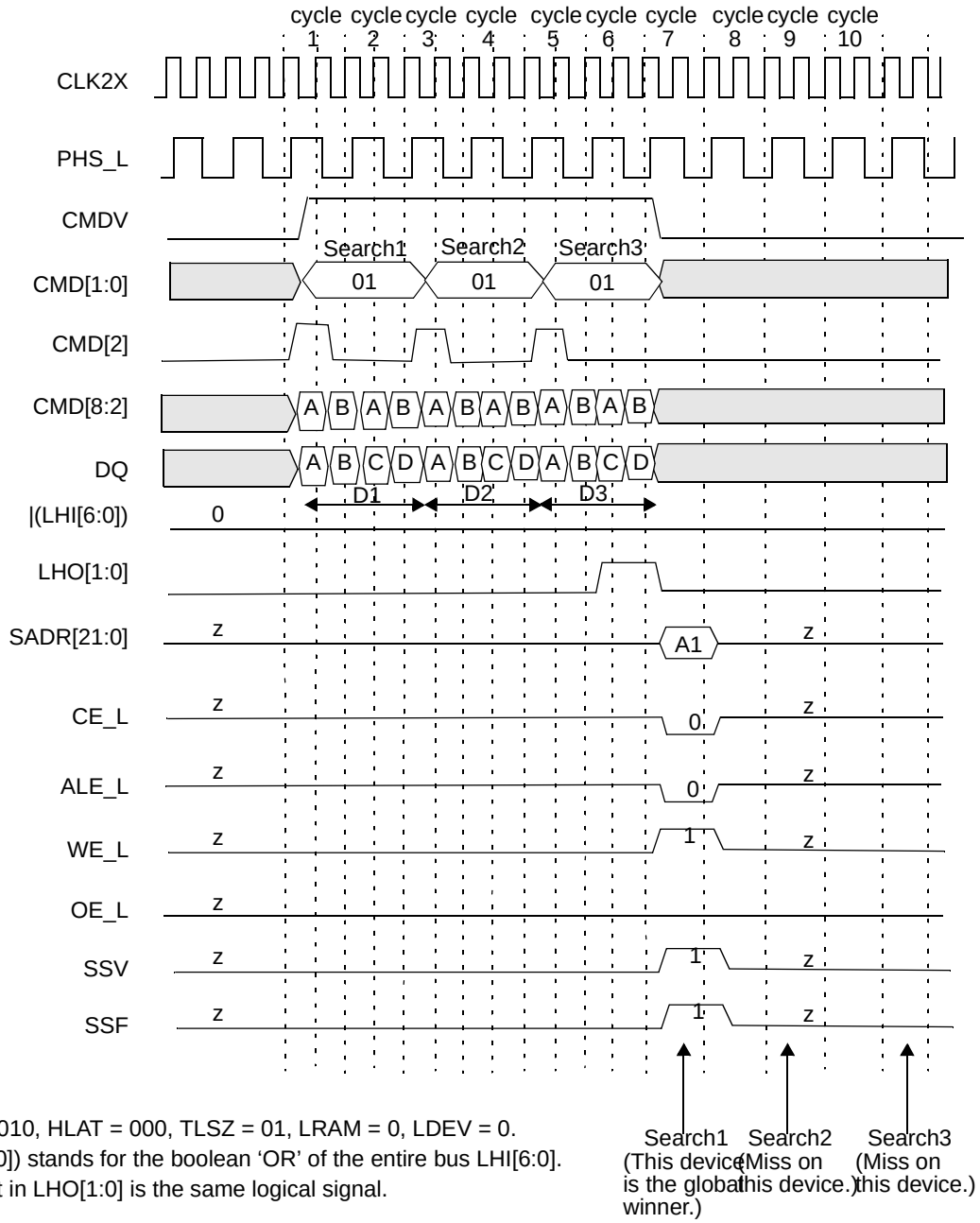
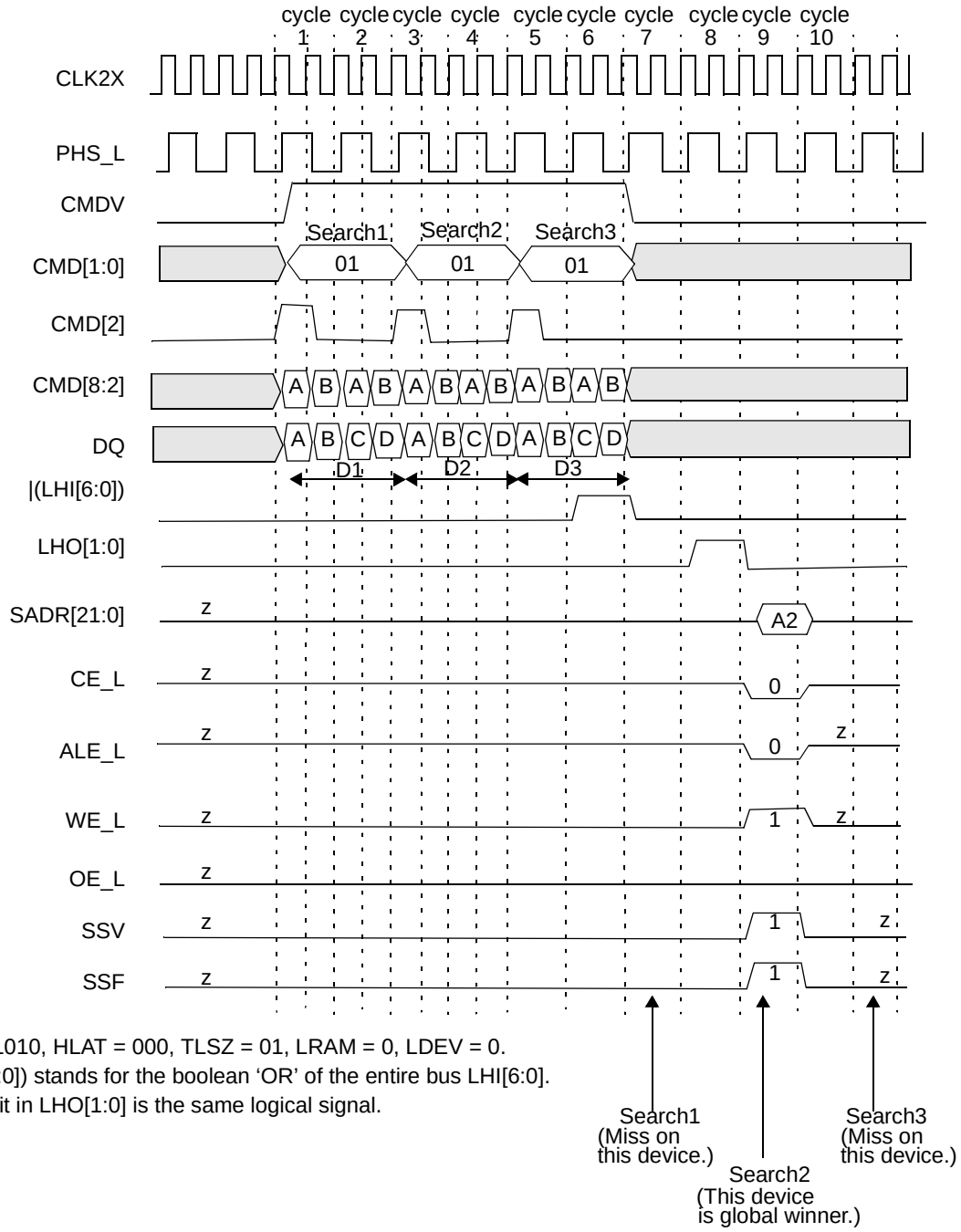


Figure 13-48. Hardware Diagram for a Table with Eight Devices



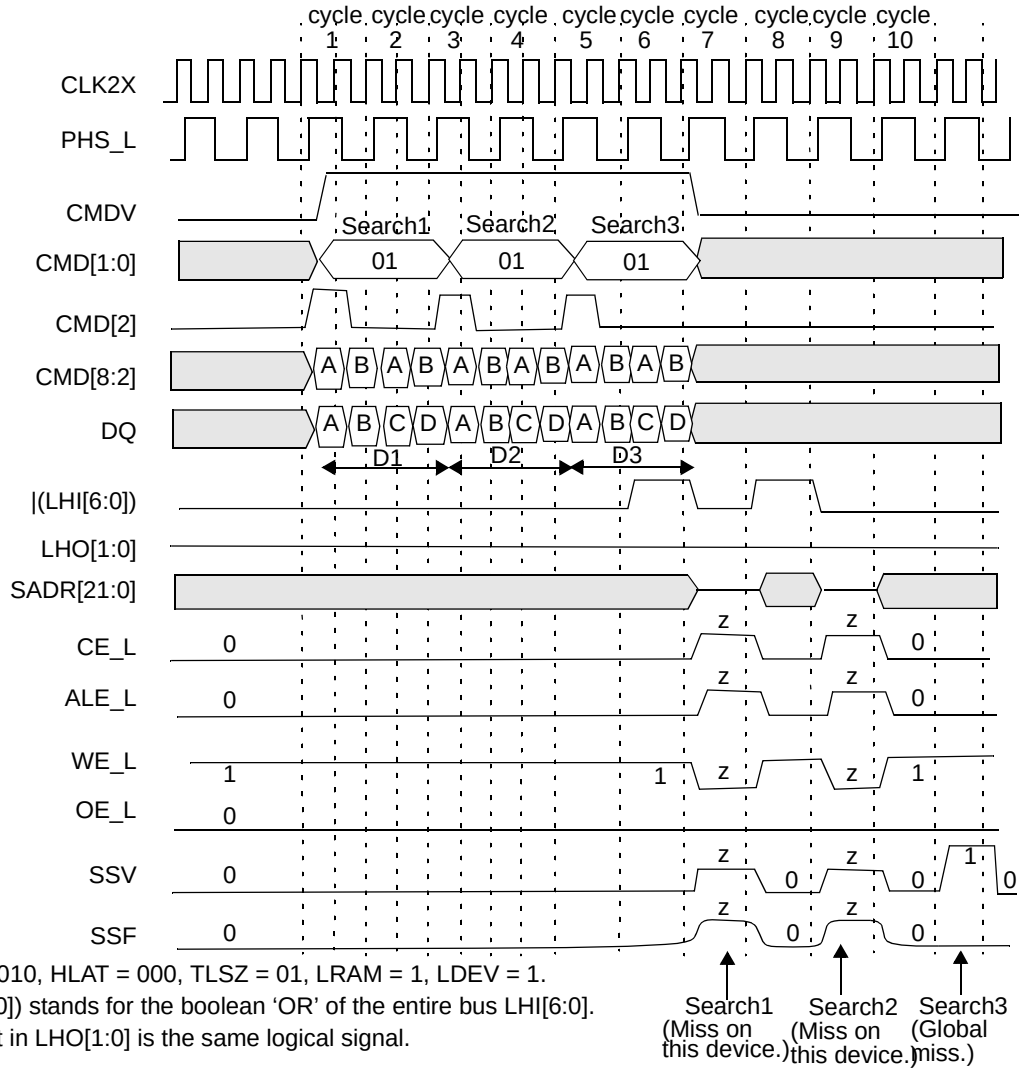
CFG = 10101010, HLAT = 000, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-49. Timing Diagram for 272-bit Search Device Number 0



CFG = 10101010, HLAT = 000, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-50. Timing Diagram for 272-bit Search Device Number 1



CFG = 10101010, HLAT = 000, TLSZ = 01, LRAM = 1, LDEV = 1.

Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].

Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-51. Timing Diagram for 272-bit Search Device Number 7 (Last Device)

The following is the sequence of operation for a single 272-bit Search command (also see "Commands and Command Parameters" on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched in this operation. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared against all locations 0 in the four-word 68-bit page. The CMD[2] signal must be driven to logic 1. ***Note***. CMD[2] = 1 signals that the search is a x272 bit search. CMD[8:3] in this cycle is ignored.
- **Cycle B**: The host ASIC continues to drive CMDV high and applies Search command code (10) on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared against all locations 1 in the four 68-bits-word page.
- **Cycle C**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [135:0] of the data being searched. CMD[8:6] signals must be driven with the bits that will be driven on SADR[21:19] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared against all locations 2 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 0.
- **Cycle D**: The host ASIC continues to drive CMDV high and applies Search command code (10) on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations 3 in the four 68-bits-word page. CMD[5:2] is ignored because the Learn instruction is not supported for ×272 tables.

Note. For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during cycles A, B, C, and D. The GMR index in cycle A selects a pair of GMRs in each of the eight devices that apply to DQ data in cycles A and B. The GMR index in cycle C selects a pair of GMRs in each of the eight devices that apply to DQ data in cycles C and D.

The logical 272-bit Search operation is shown in *Figure 13-52*. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command using the GMR and the local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's cycles A and C in each of the eight devices. The 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command is compared to each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 98). ***Note***. The matching address is always going to be a location 0 in a four-entry page for 272-bit Search (two LSBs of the matching index will be 00).

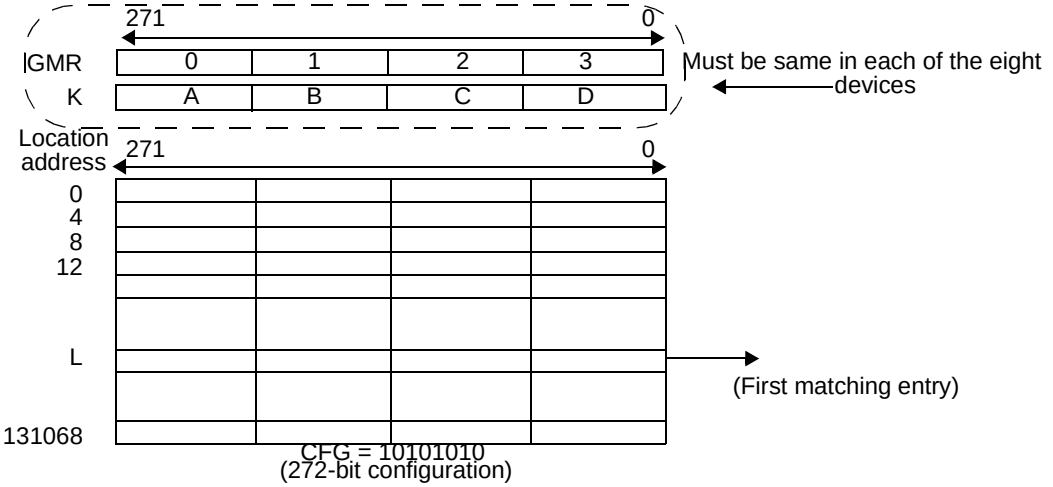


Figure 13-52. x272 Table with Eight Devices

The Search command is a pipelined operation and executes a Search at one-fourth the rate of the frequency of CLK2X for 272-bit searches in ×272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit Search command (measured in CLK cycles) from the CLK2X cycle that contains the C and D cycles is shown in *Table 13-20*.

Table 13-20. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	4K × 272 bits	4
1–8 (TLSZ = 01)	32K × 272 bits	5
1–31 (TLSZ = 10)	124K × 272 bits	6

Search latency from command to SRAM access cycle is 5 for only a single device in the table and TLSZ = 01. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 13-21*.

Table 13-21. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.9 272-bit Search on Tables Configured as ×272 using up to 31 CYNSE70032 Devices

The hardware diagram of the search subsystem of 31 devices is shown in *Figure 13-53*. Each of the four blocks in the diagram represents a block of eight CYNSE70032 devices, except the last which has seven devices. The diagram for a block of eight devices is shown in *Figure 13-54*. The following are the parameters programmed into the 31 devices.

- First thirty devices (devices 0–29): CFG = 10101010, TLSZ = 10, HLAT = 000, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30): CFG = 10101010, TLSZ = 10, HLAT = 000, LRAM = 1, and LDEV = 1.

Note. All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in *Table 13-22*. For the purpose of illustrating the timings, it is further assumed that there is only one device with the matching entry in each block. *Figure 13-55* shows the timing diagram for a Search command in the 272-bit-configured table consisting of 31 devices for each of the eight devices in block number 0. *Figure 13-56* shows the timing diagram for a Search command in the 272-bit-configured table of 31 devices for all devices above the winning device in block number 1. *Figure 13-57* shows the timing diagram for the globally winning device (the final winner within its own and all blocks) in block number 1. *Figure 13-58* shows the timing diagram for all the devices below the globally winning device in block number 1. *Figure 13-59*, *Figure 13-60*, and *Figure 13-61*, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device for block number 2. *Figure 13-62*, *Figure 13-63*, *Figure 13-64*, and *Figure 13-65*, respectively, show the timing diagrams of the device above the globally winning device, the globally winning device, the devices below the globally winning device (except device 30), and last device (device 30) for block number 3.

The 272-bit Search operation is pipelined and executes as follows. Four cycles from the last cycle of the Search command each of the devices knows the outcome internal to it for that operation. In the fifth cycle from the Search command, the devices in a block (less than or equal to eight devices resolving the winner within them using an LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner. In the sixth cycle after the Search command, the blocks of devices resolve the winning block through a BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for the Search operation.

Table 13-22. Hit/Miss Assumptions

Search Number	1	2	3
Block 0	Miss	Miss	Miss
Block 1	Miss	Miss	Hit
Block 2	Miss	Hit	Hit
Block 3	Hit	Hit	Miss

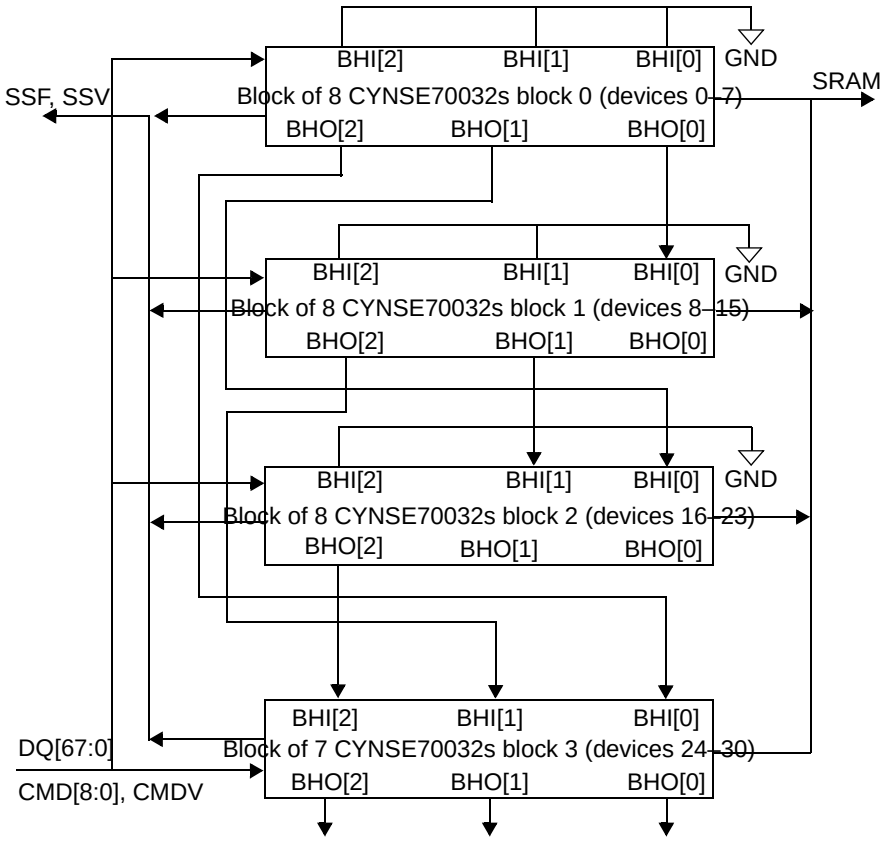


Figure 13-53. Hardware Diagram for a Table with 31 Devices

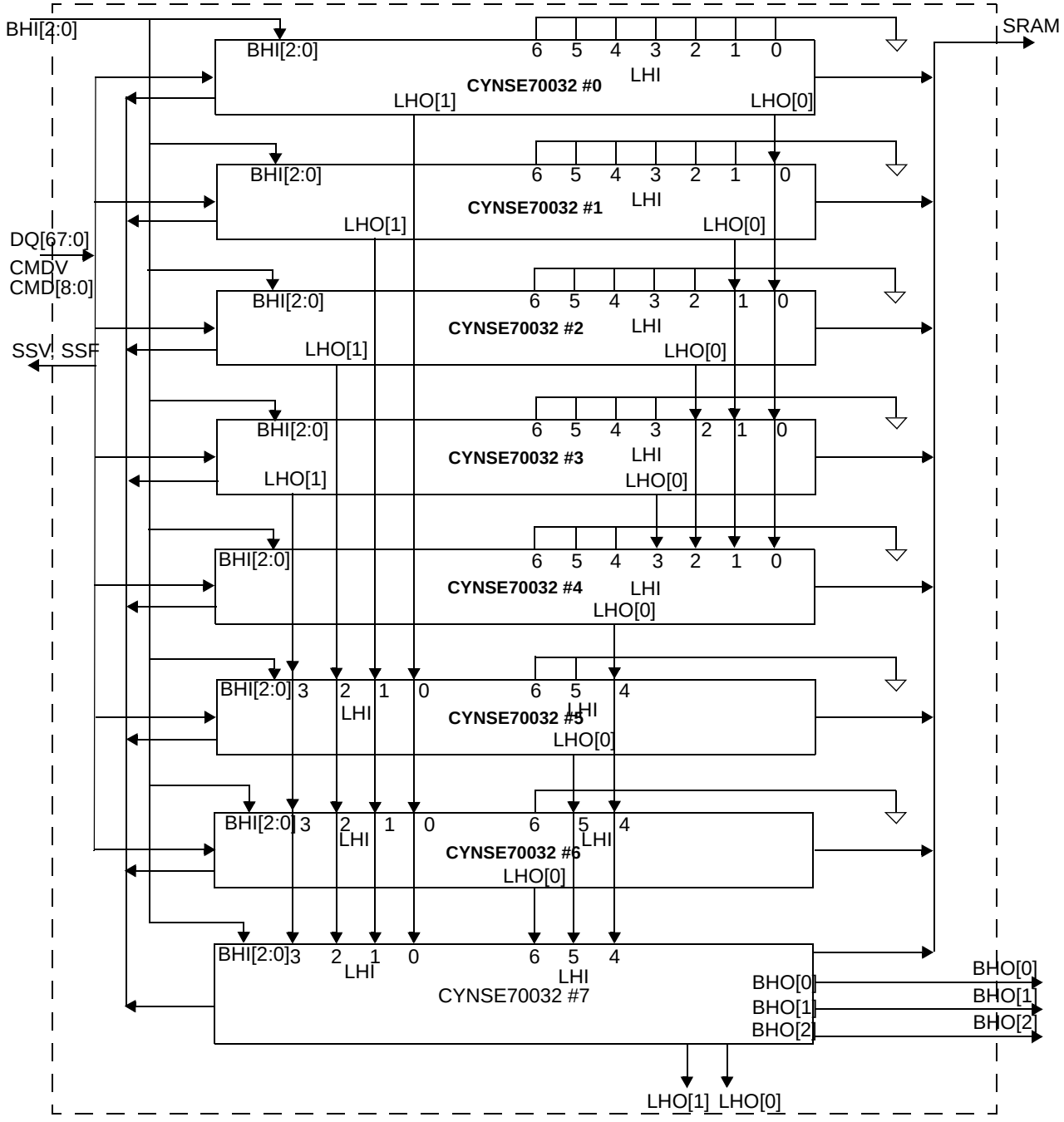
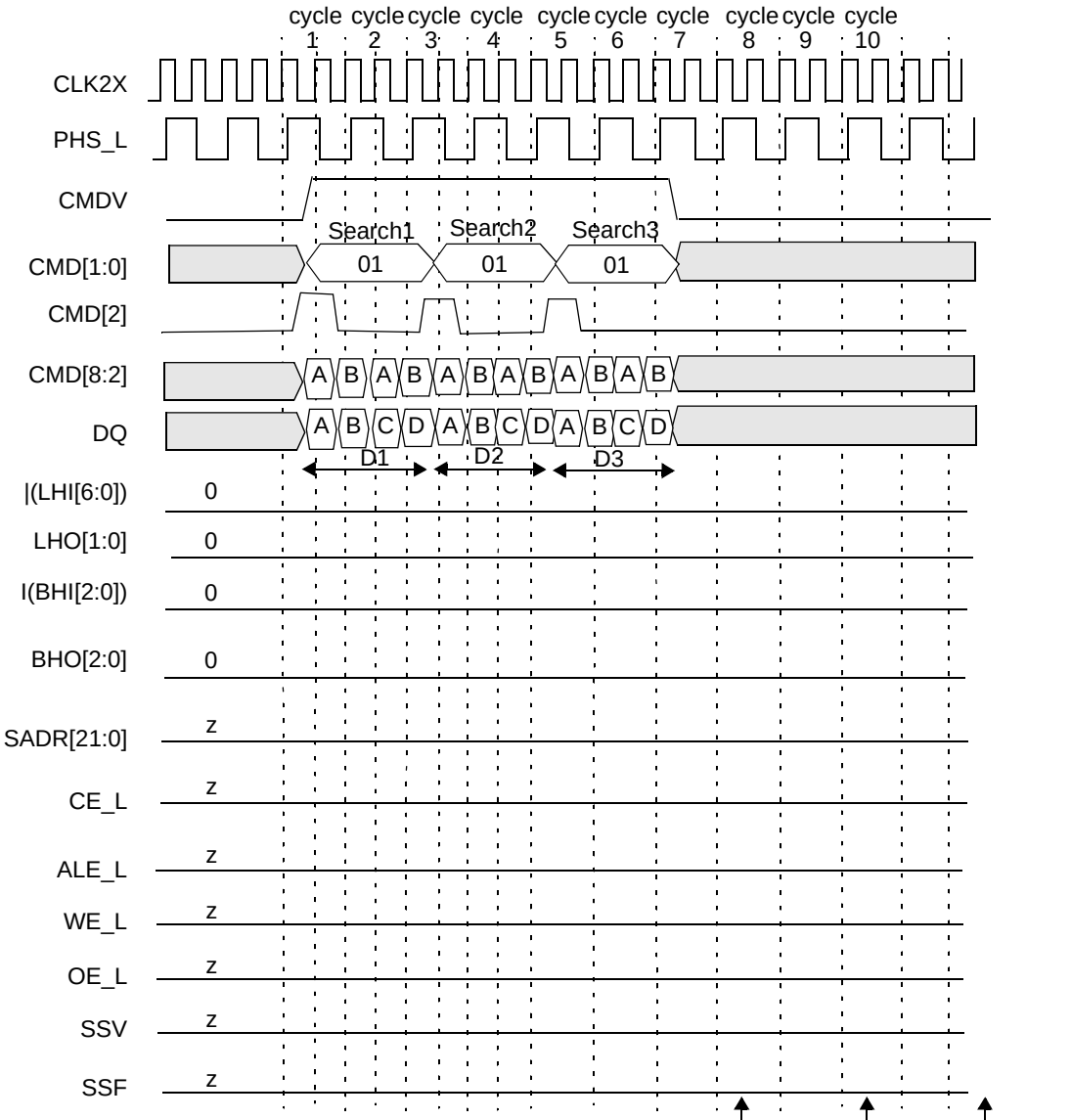
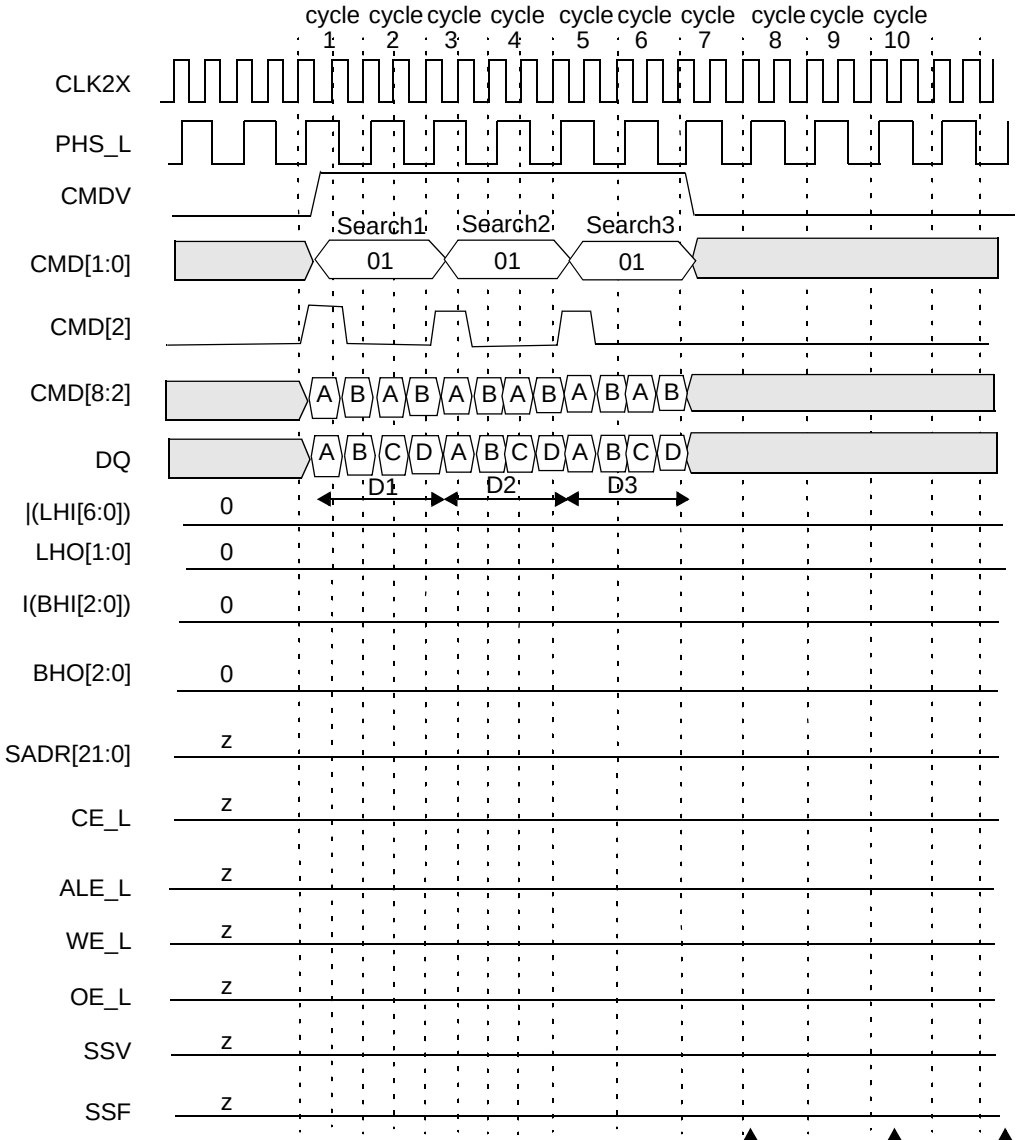


Figure 13-54. Hardware Diagram for a Block of up to Eight Devices



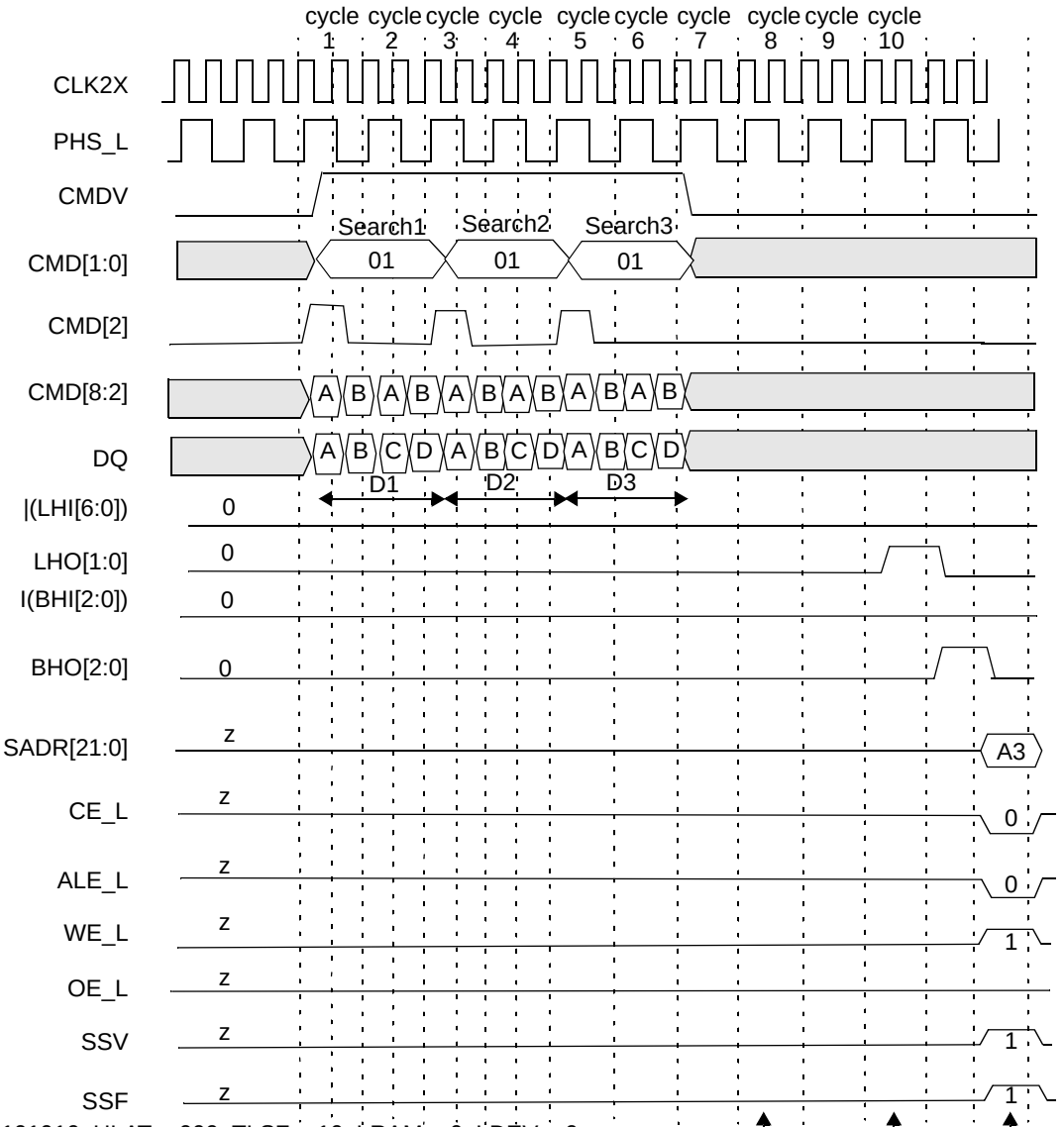
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-55. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



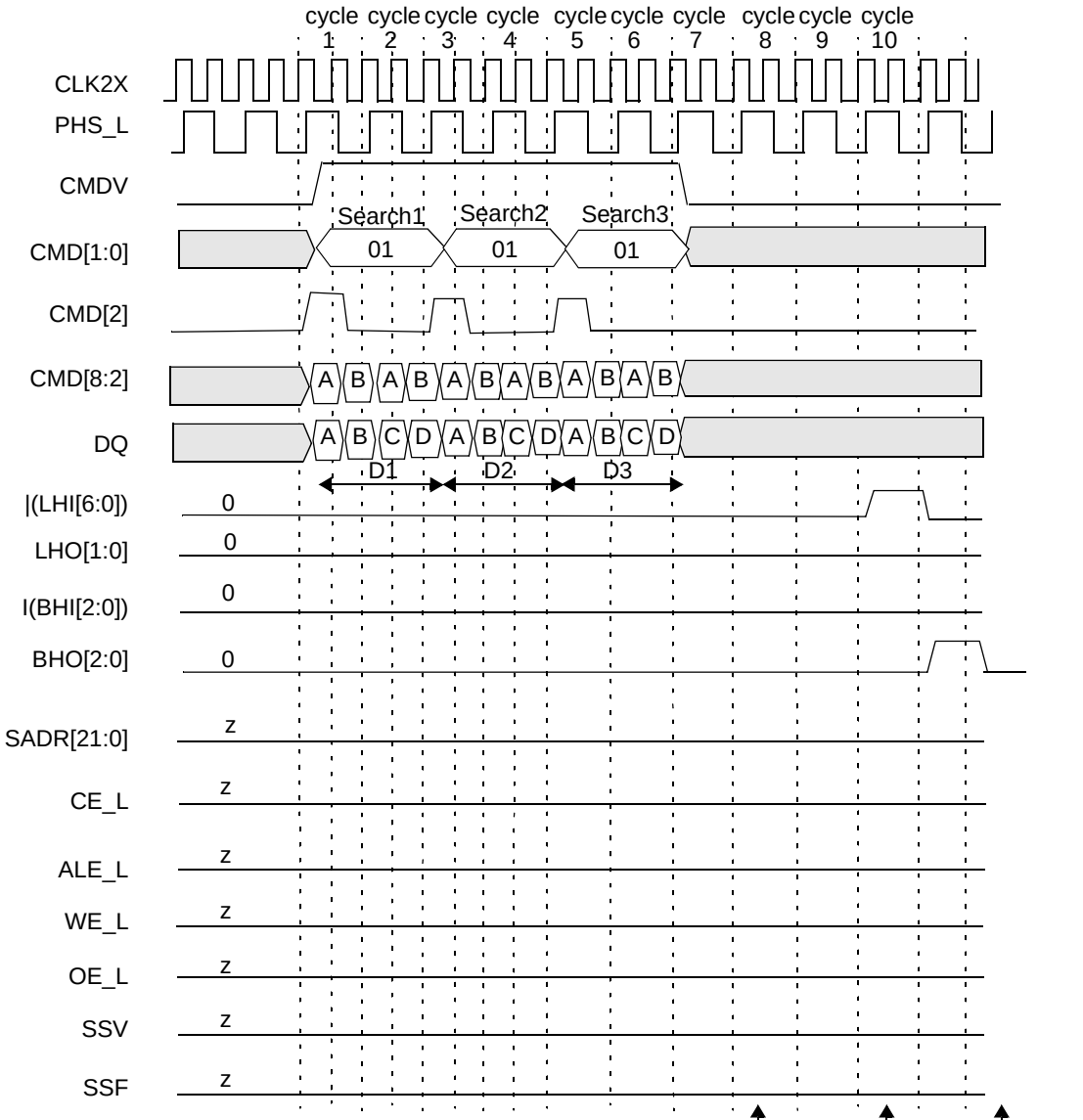
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-56. Timing Diagram for Each Device Above the Winning Device in Block Number 1



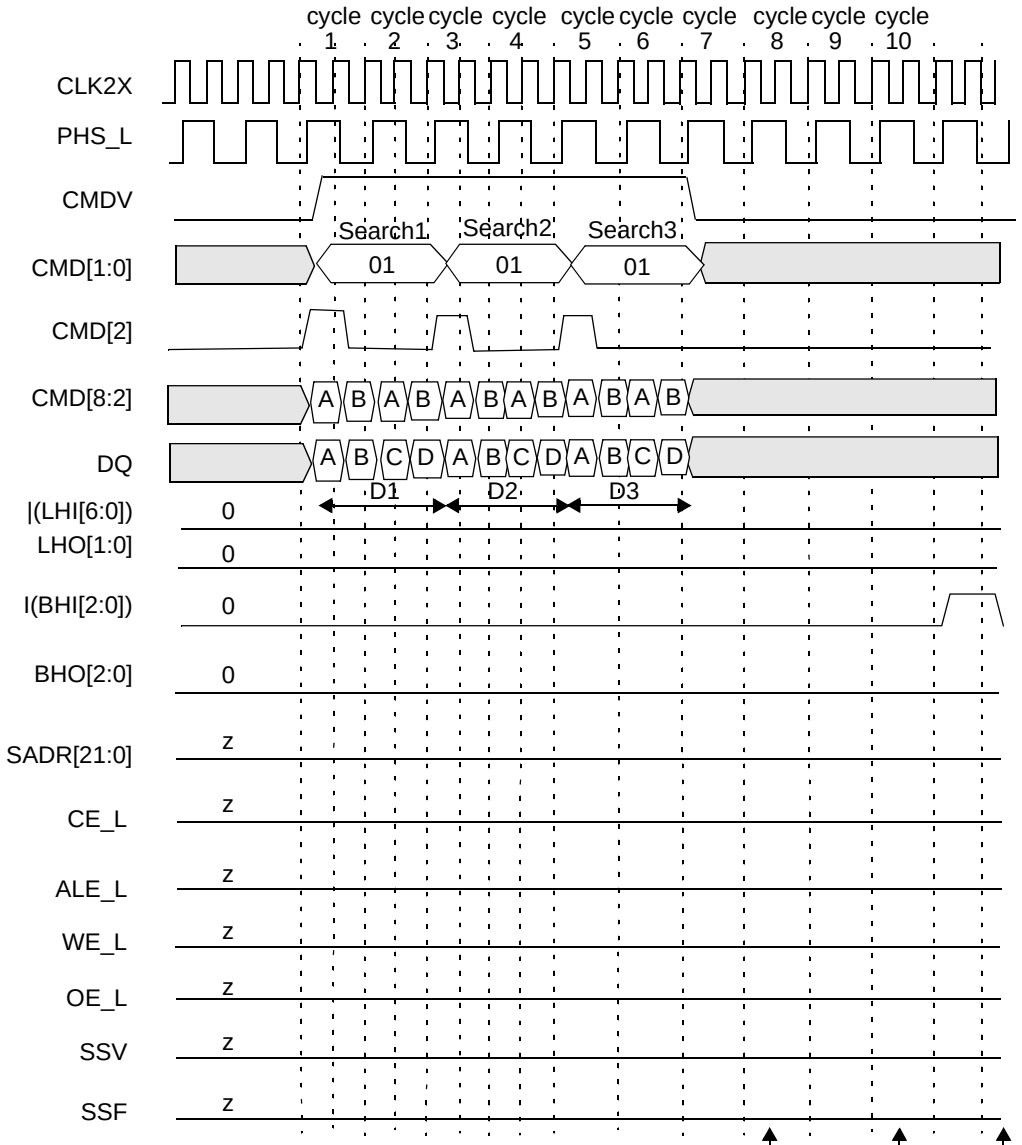
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-57. Timing Diagram for Globally Winning Device in Block Number 1



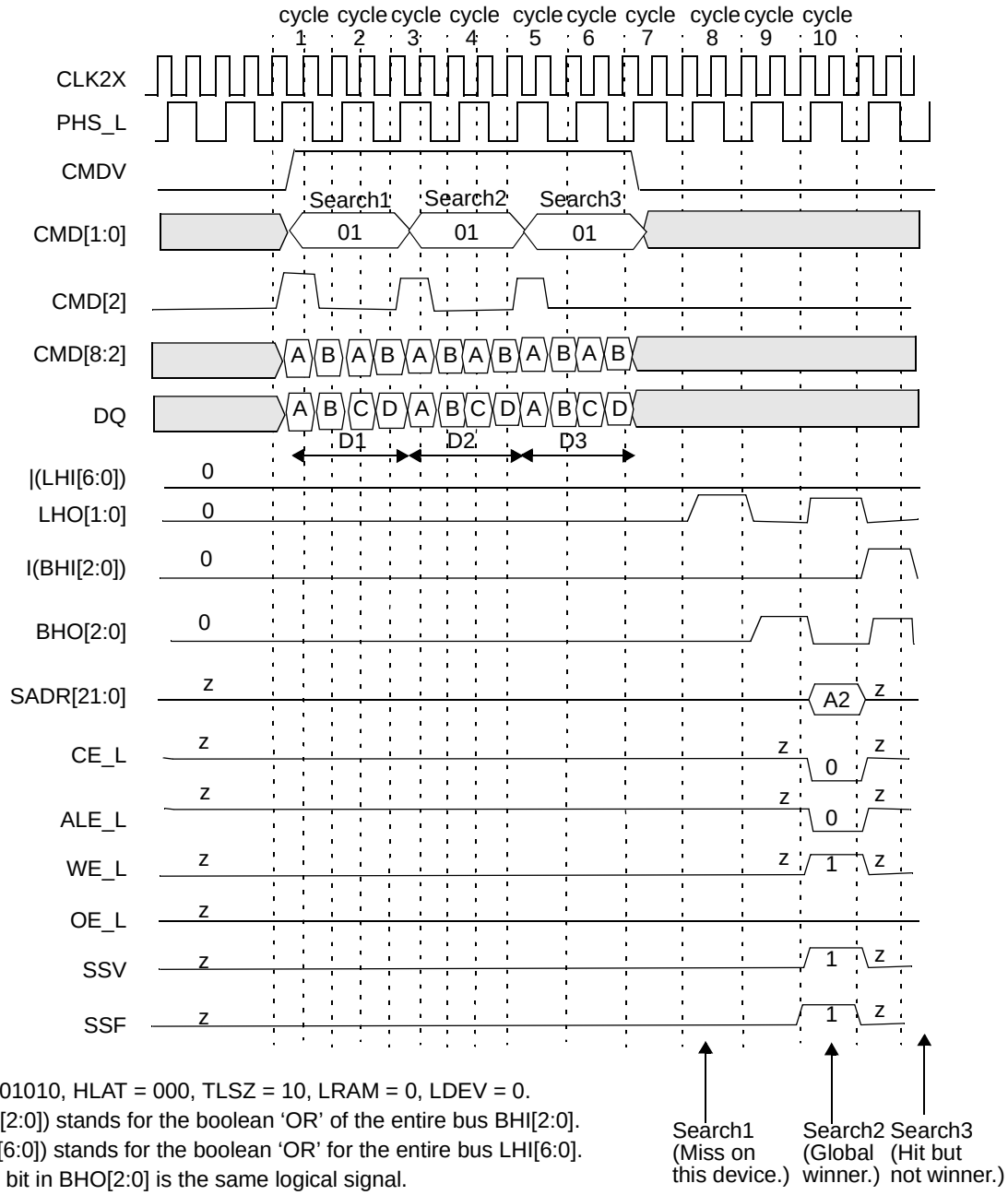
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-58. Timing Diagram for Devices Below the Winning Device in Block Number 1



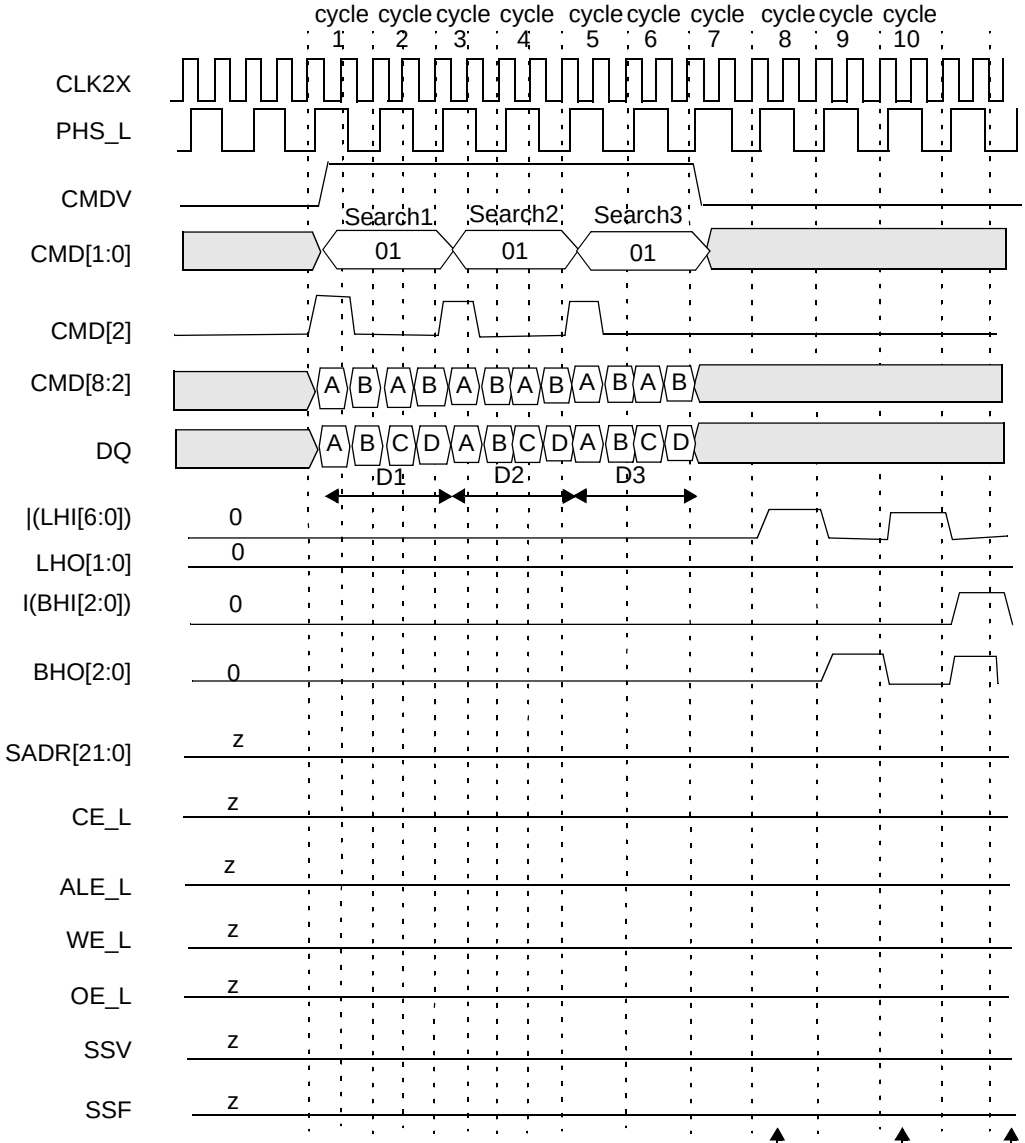
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-59. Timing Diagram for Devices Above the Winning Device in Block Number 2



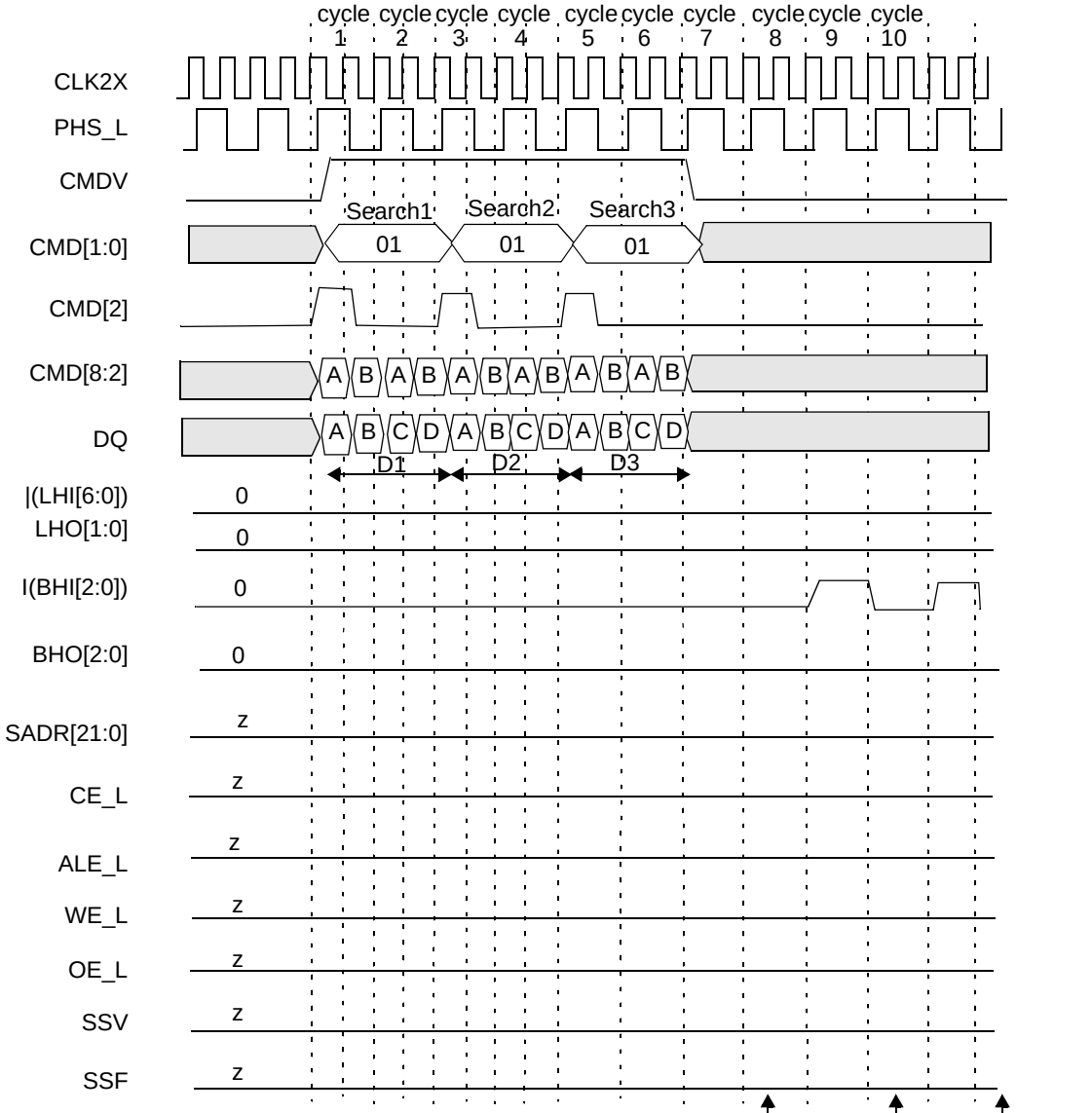
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-60. Timing Diagram for Globally Winning Device in Block Number 2



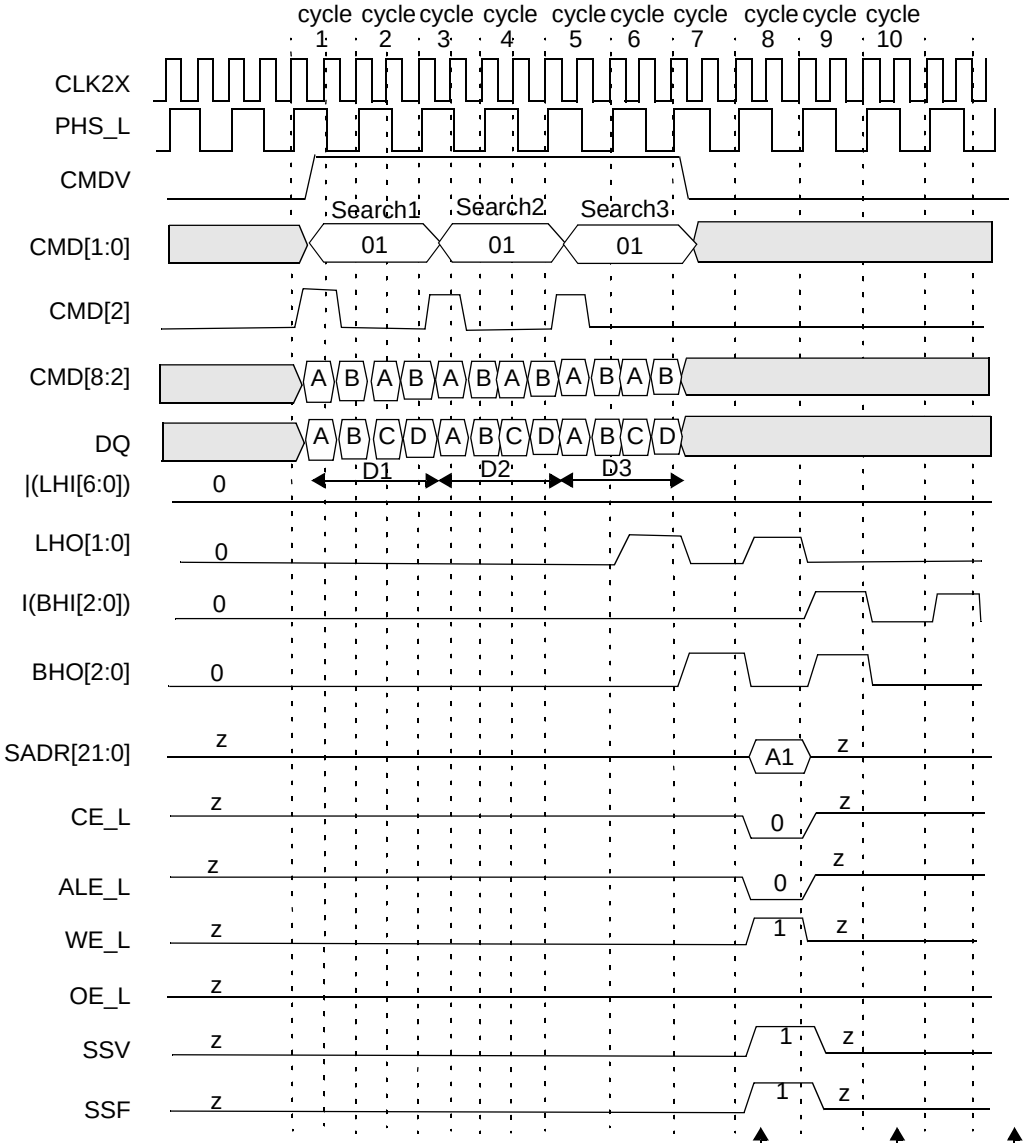
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-61. Timing Diagram for Devices Below the Winning Device in Block Number 2



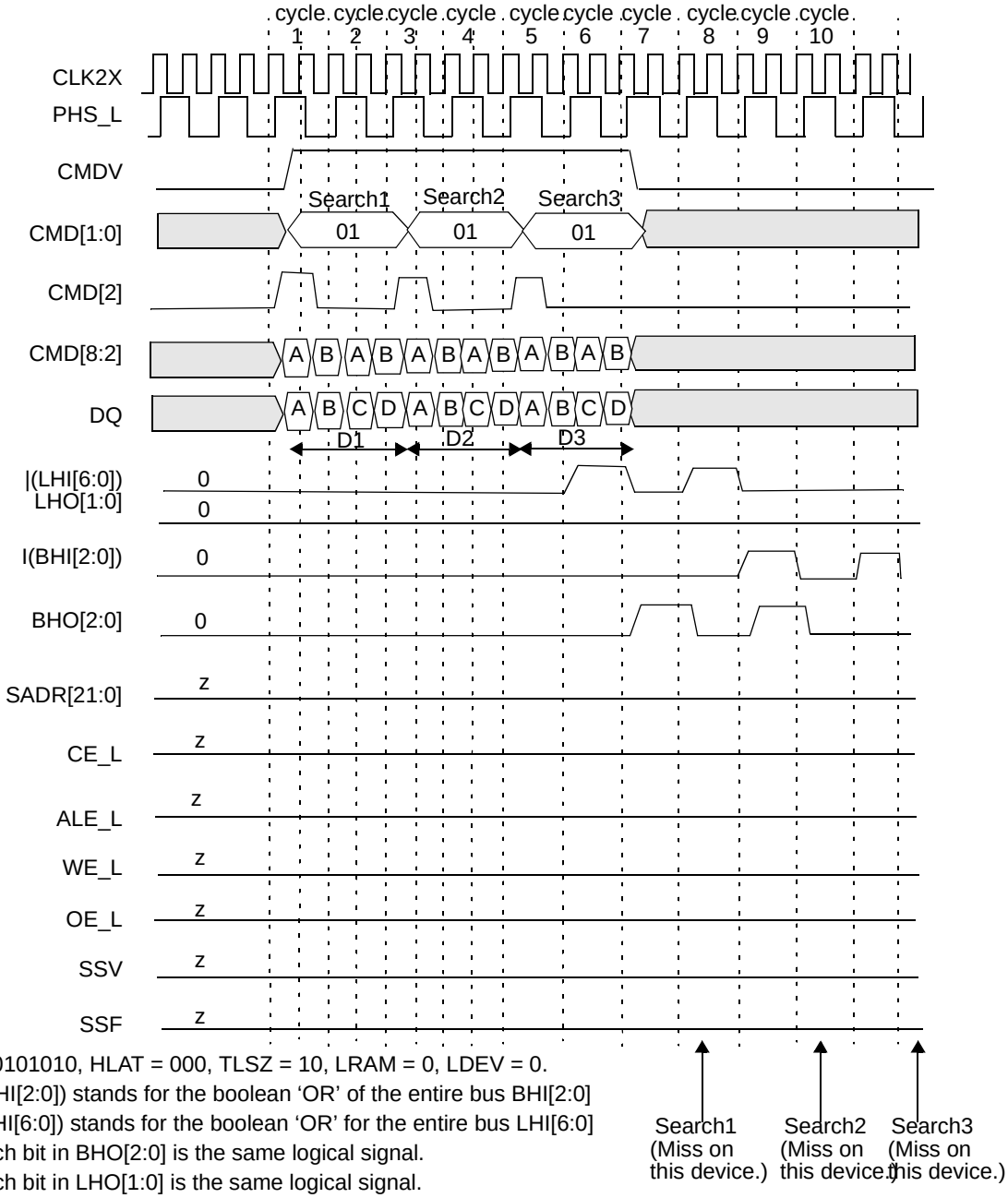
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-62. Timing Diagram for Devices Above the Winning Device in Block Number 3



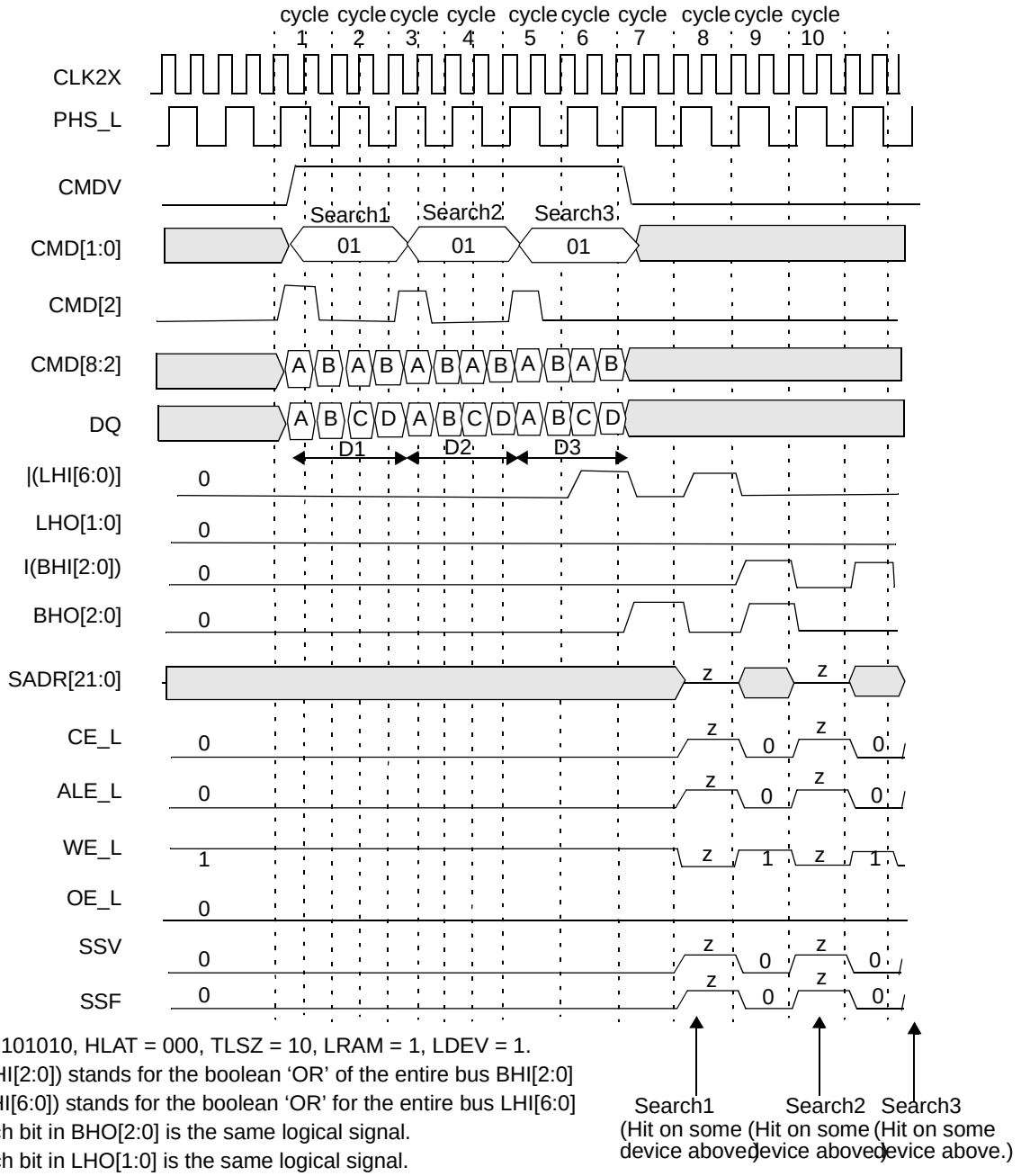
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-63. Timing Diagram for Globally WInning Device in Block Number 3



CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0]
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0]
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-64. Timing Diagram for Devices Below the Winning Device in Block Number 3 Except Device Number 30 (the Last Device)



CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 1, LDEV = 1.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0]
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0]
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 13-65. Timing Diagram of the Last Device in Block Number 3 (Device 30 in the Table)

The following is the sequence of operation for a single 272-bit Search command (also refer to Subsection 12.2, "Commands and Command Parameters" on page 19).

- **Cycle A**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits[271:136] of the data being searched. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared to all locations 0 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 1. ***Note***. CMD[2] = 1 signals that the search is a x272-bit Search. CMD[8:6] is ignored in this cycle.
- **Cycle B**: The host ASIC continues to drive CMDV high and applies Search command (10) on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared to all locations 1 in the four 68-bits-word page.
- **Cycle C**: The host ASIC drives CMDV high and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for the bits [135:0] of the data being searched. CMD[8:6] signals must be driven with the bits that will be driven by this device on SADR[21:19] if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared to all locations 2 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 0.

- **Cycle D**: The host ASIC continues to drive CMDV high and to apply Search command code (10) on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for a description of SSR[0:7]). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations 3 in the four 68-bits-word page. CMD[5:2] is ignored because the Learn instruction is not supported for ×272 tables.

Note. For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during cycles A, B, C, and D. The GMR Index in cycle A selects a pair of GMRs in each of the 31 devices that apply to DQ data in cycles A and B. The GMR Index in cycle C selects a pair of GMRs in each of the 31 devices that apply to DQ data in cycles C and D.

The logical 272-bit Search operation is as shown in *Figure 13-66*. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's cycles A and C in each of the 31 devices. The 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command is compared to each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 98). ***Note***. The matching address is always going to be location 0 in a four-entry page for 272-bit search (two LSBs of the matching index will be 00).

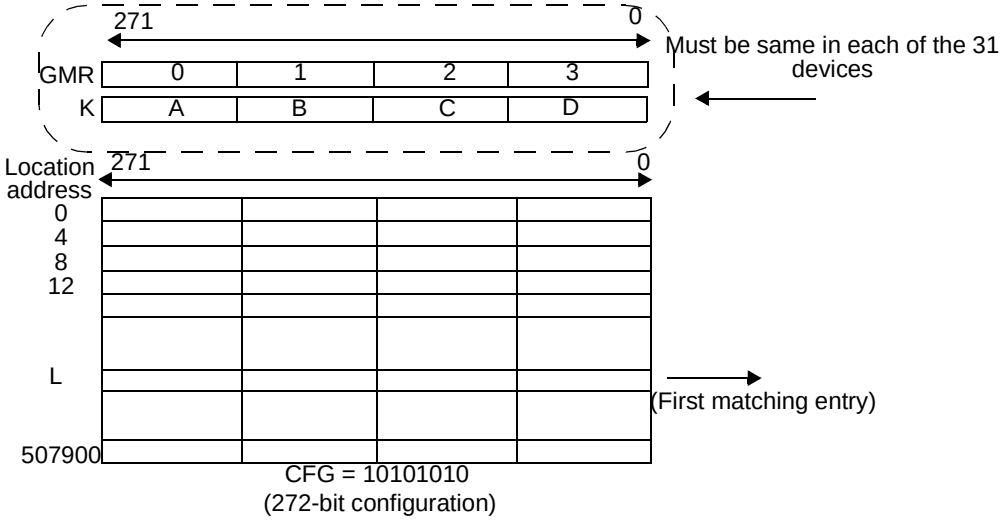


Figure 13-66. x272 Table with 31 Devices

The Search command is a pipelined operation that executes a Search at one-fourth the rate of the frequency of CLK2X for 272-bit searches in ×272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit Search command (measured in CLK cycles) from the CLK2X cycle containing the C and D cycles is shown in *Table 13-23*.

Table 13-23. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	4K × 272 bits	4
1–8 (TLSZ = 01)	32K × 272 bits	5
1–31 (TLSZ = 10)	124K × 272 bits	6

Search latency from command to SRAM access cycle is 6 only for a single device in the table with TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 13-24*.

Table 13-24. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

13.10 Mixed-Size Searches on Tables Configured with Different Widths Using an CYNSE70032 Device

This subsection will cover mixed searches (×68, ×136, and ×272) with tables of different widths (×68, ×136, ×272). The sample operation shown is for a single device with CFG = 10010000 containing three tables of ×68, ×136, and ×272 widths. The operation can be generalized to a block of 8–31 devices using four blocks; the timing and the pipeline operation is the same as described previously for fixed searches on a table of one-width-size.

Figure 13-67 shows three sequential searches: first, a 68-bit Search on the table configured as ×68, then a 136-bit search on a table configured as ×136, and finally a 272-bit search on the table configured as ×272 bits. Each results in a hit. ***Note***. The DQ[67:66] will be 00 in each of the two A and B cycles of the ×68-bit Search (Search1). DQ[67:66] is 01 in each of the A and B cycles of the ×136-bit Search (Search2). DQ[67:66] is 10 in each of the A, B, C, and D cycles of the ×272-bit Search (Search3). By having table designation bits, the CYNSE70032 device enables the creation of many tables of different widths in a bank of search engines.

Figure 13-68 shows the sample table. Two bits in each 68-bit entry need to designated as table number bits. One example choice might be: the 00 values for the table configured as ×68, 01 values for tables configured as ×136, and 10 values for tables configured as ×272. For the above explanation, it is further assumed that bits[67:66] for each entry will be designed as such table designation bits.

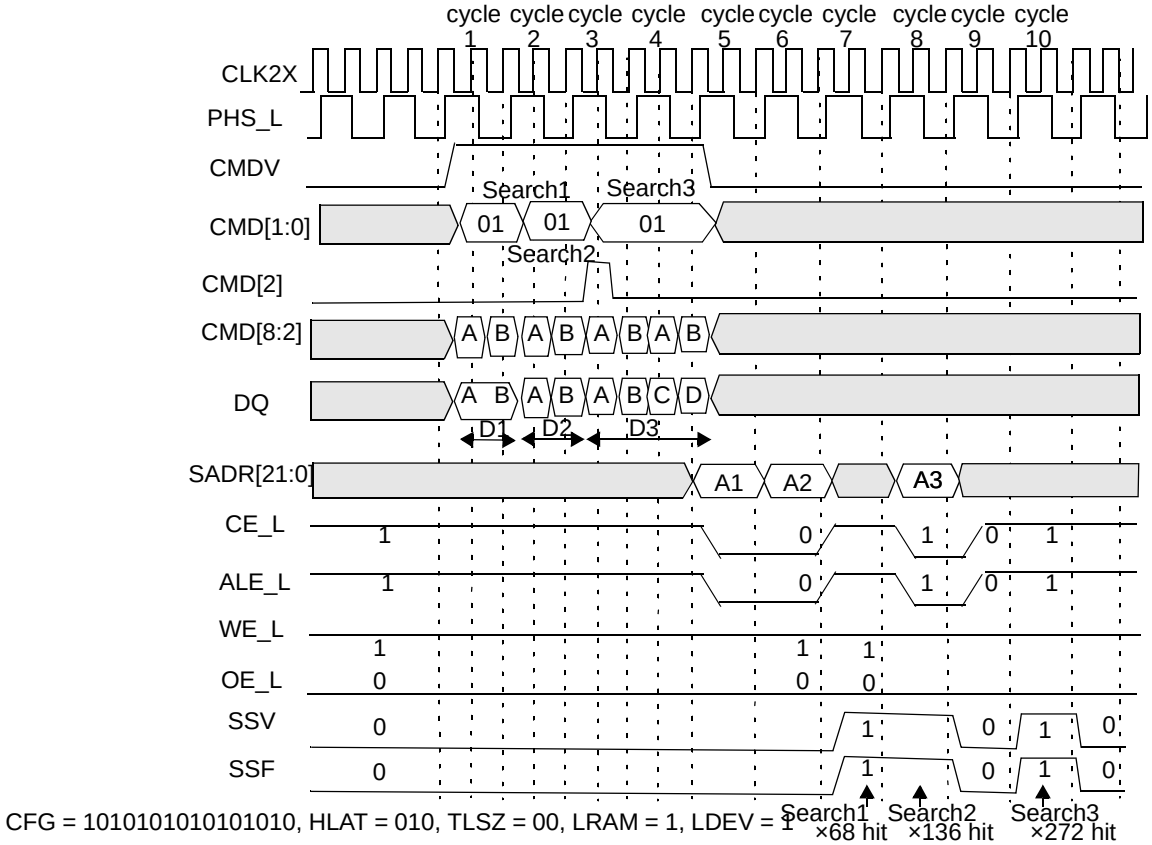


Figure 13-67. Timing Diagram for Mixed Search (One Device)

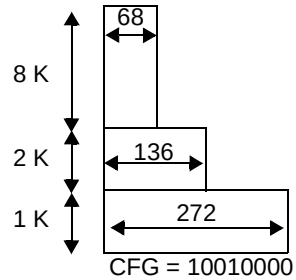


Figure 13-68. Multiwidth Configurations Example

13.11 LRAM and LDEV Description

When search engines are cascaded using multiple CYNSE70032 devices, the SADR, CE_L, and WE_L (three-state signals) are all tied together. To eliminate external pull-up and pull downs, one device in a bank is designated as the default driver. For non-Search or non-Learn cycles (see Subsection 13.12, “Learn Command” on page 92) or Search cycles with a global miss, the SADR, CE_L, and WE_L signals are driven by the device with the LRAM bit set. It is important that only one device in a bank of cascaded search engines have this bit set. Failure to do so will cause contention on SADR, CE_L, and WE_L, and can potentially cause damage to the device(s).

Similarly, when search engines using multiple CYNSE70032 devices are cascaded, SSF and SSV (also three-state signals) are tied together. To eliminate external pull-up and pull downs, one device in a bank is designated as the default driver. For nonSearch cycles or Search cycles with a global miss, the SSF and SSV signals are driven by the device with the LDEV bit set. It is important that only one device in a bank of cascaded search engines have this bit set. Failure to do so will cause contention on SSV and SSF and can potentially cause damage to the device(s).

13.12 Learn Command

Bit[0] of each 68-bit data location specifies whether an entry in the database is occupied. If all the entries in a device are occupied, the device asserts FULO signal to inform the downstream devices that it is full. The result of this communication between depth-cascaded devices determines the global FULL signal for the entire table. The FULL signal in the last device determines the fullness of the depth-cascaded table.

The device contains sixteen pairs of internal, 68-bit-wide comparand registers that store the comparands as the device executes searches. On a miss by the Search (signalled to ASIC through the SSV and SSF signals [SSV = 1, SSF = 0]), the host ASIC can apply the Learn command to Learn the entry from a comparand register to the next-free location (see Subsection 9.3, “NFA Register” on page 16). The NFA updates to the next-free location following each Write or Learn command.

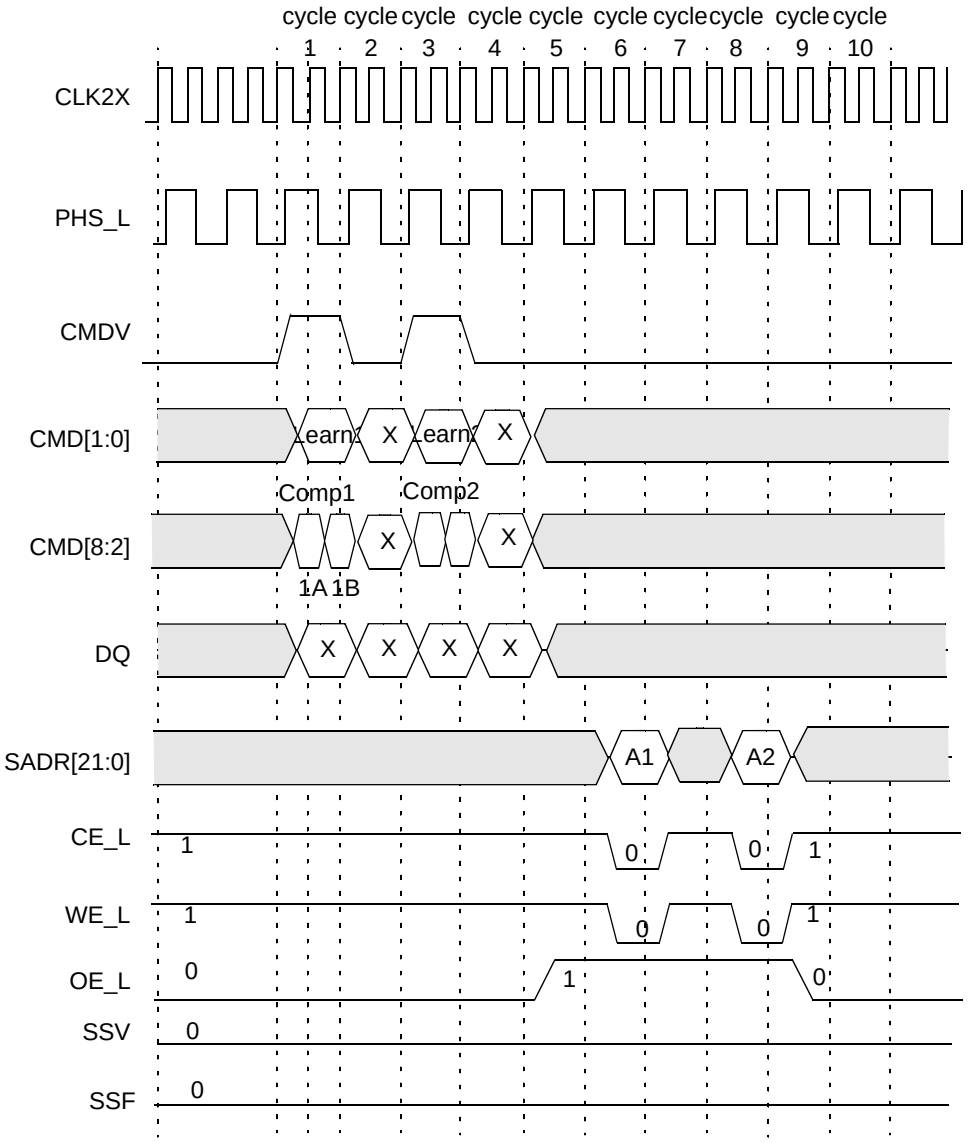
In a depth-cascaded table, only a single device will Learn the entry through the application of a Learn instruction. The determination of the Learn device is based on the FULI and FULO signalling between the devices. The first non-full device learns the entry by storing the contents of the specified comparand registers to the location(s) pointed to by NFA.

In a ×68-configured table the Learn command writes a single 68-bit location. In a ×136-configured table the Learn command writes the next even and odd 68-bit locations. In 136-bit mode, bit[0] of the even and odd 68-bit locations is 0, indicating that they are cascaded empty, or 1, which indicates that they are occupied.

The global FULL signal indicates to the table controller (the host ASIC) that all entries within a block are occupied and that no more entries can be learned. The CYNSE70032 device updates the signal to a data array after each Write or Learn command. Also using the NFA register as part of the SRAM address, the Learn command generates a Write cycle to the external SRAM (see Section 15.0, “SRAM Addressing” on page 98).

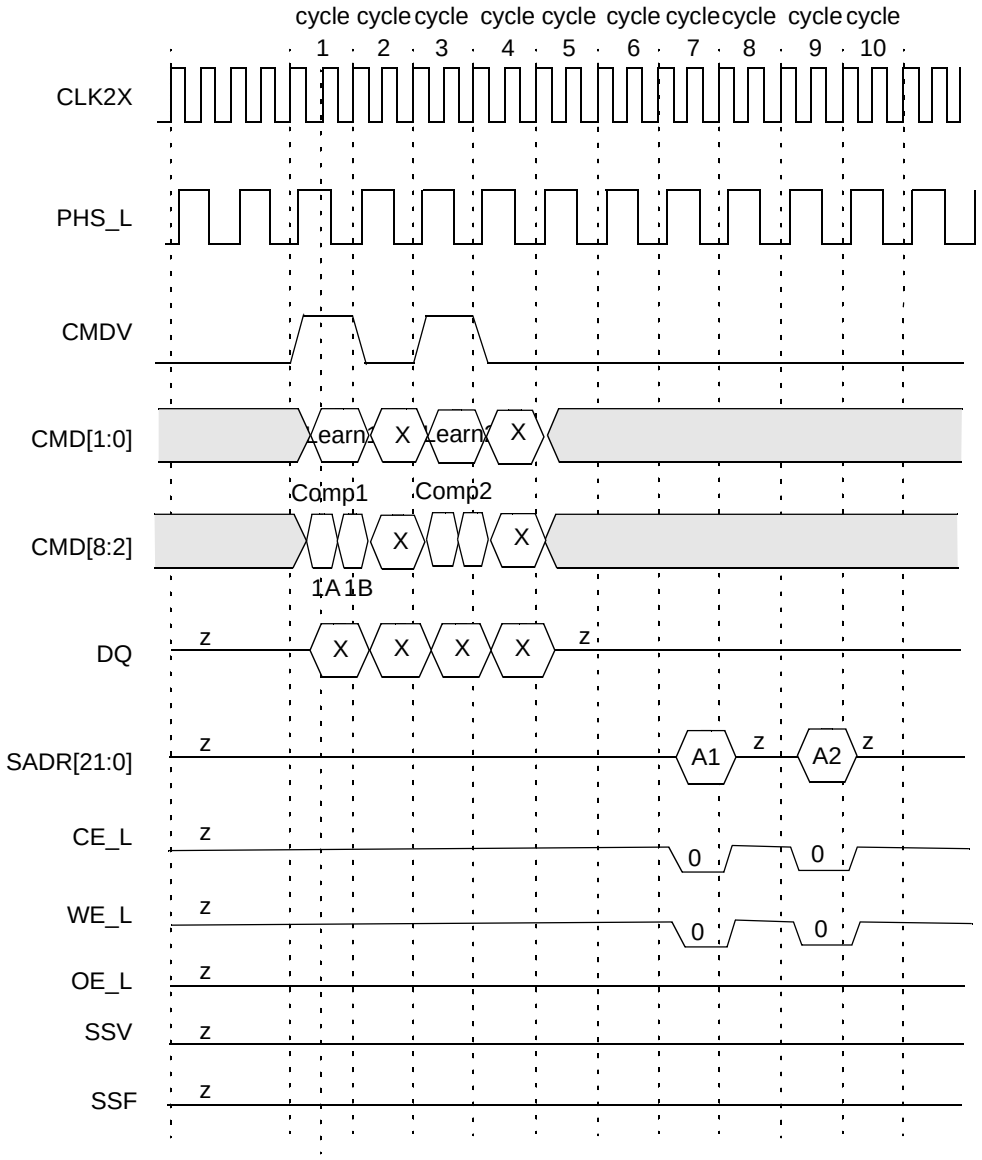
The Learn command is supported on a single block containing up to eight devices if the table is configured as either a ×68 or a ×136. The Learn command is not supported for ×272-configured tables.

Learn is a pipelined operation and lasts for two CLK cycles where TLSZ = 00, as shown in *Figure 13-69*, and TLSZ = 01 as shown in *Figure 13-70* and *Figure 13-71*. *Figure 13-70* and *Figure 13-71* assume that the device performing the Learn operation is not the last device in the table and has its LRAM bit set to 0. ***Note***. The OE_L for the device with the LRAM bit set goes high for two cycles for each Learn (one during the SRAM Write cycle, and one during the cycle before it). The latency of the SRAM Write cycle from the second cycle of the instruction is shown in *Table 13-25*.



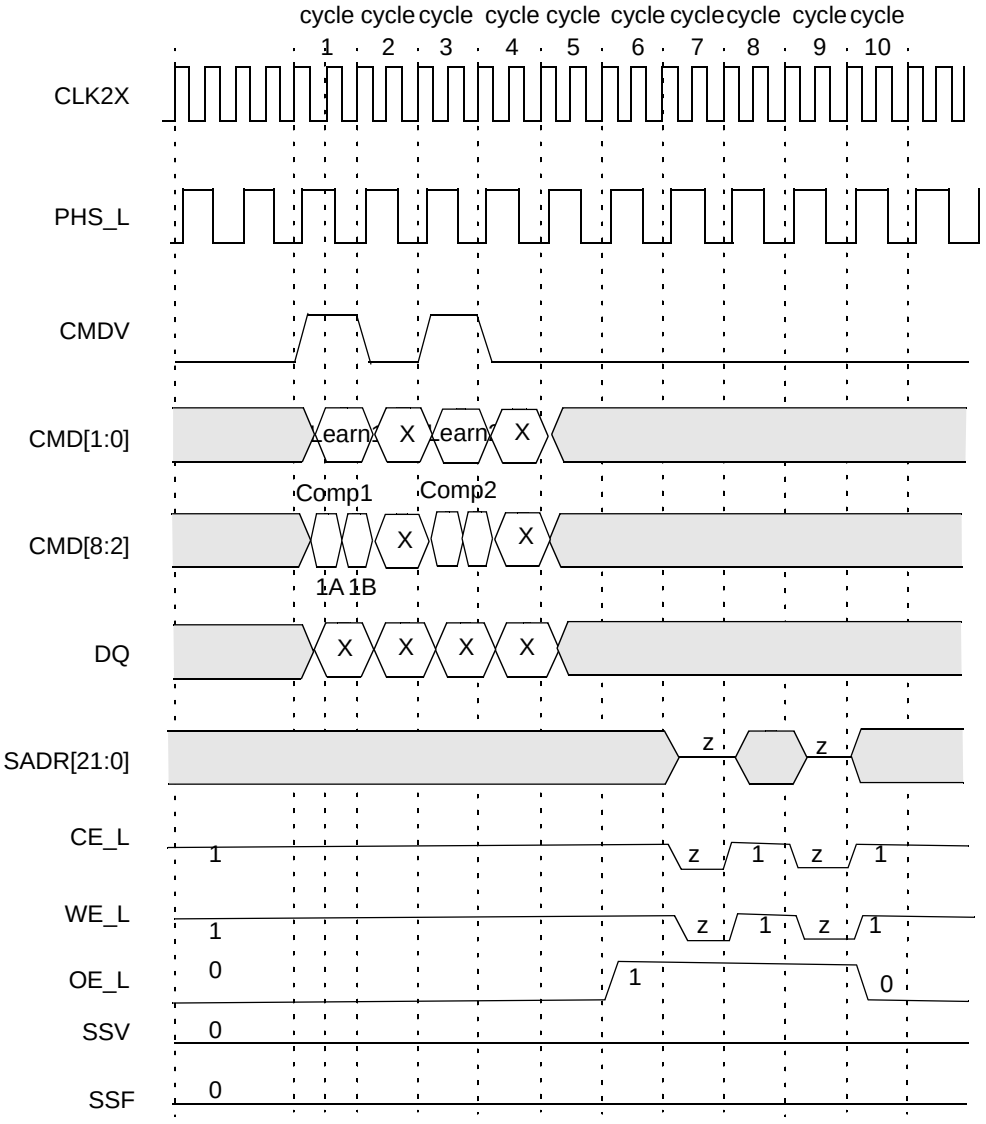
TLSZ = 00, LRAM = 1, LDEV = 1.

Figure 13-69. Learn Timing Diagram (TLSZ = 00)



TLSZ = 01, LRAM = 0, LDEV = 0.

Figure 13-70. Learn Timing Diagram (TLSZ = 01 [Except on the Last Device])



TLSZ = 01, LRAM = 1, LDEV = 1.

Figure 13-71. Learn Timing Diagram on Device Number 7 (TLSZ = 01)

Table 13-25. SRAM Write Cycle Latency from Second Cycle of Learn Instruction

Number of Devices	Latency in CLK Cycles
1 (TLSZ = 00)	4
1–8 (TLSZ = 01)	5
1–31 (TLSZ = 10)	6

The Learn operation lasts two CLK cycles. The sequence of operation is as follows.

- **Cycle 1A**: The host ASIC applies the Learn instruction on CMD[1:0] using CMDV = 1. The CMD[5:2] field specifies the index of the comparand register pair that will be written to the data array in the 136-bit-configured table. For a Learn in a 68-bit-configured table, the even-numbered comparand specified by this index will be written. CMD[8:6] carries the bits that will be driven on SADR[21:19] in the SRAM Write cycle.
- **Cycle 1B**: The host ASIC continues to drive CMDV to 1, CMD[1:0] to 11, and CMD[5:2] with the comparand pair index. CMD[6] must be set to 0 if the Learn is being performed on a 68-bit-configured table, and to 1 if the Learn is being performed on a 136-bit-configured table.
- **Cycle 2**: The host ASIC drives CMDV to 0.

At the end of cycle 2, a new instruction can begin. SRAM Write latency is the same as the Search to the SRAM read cycle (it is measured from the second cycle of the Learn instruction).

14.0 Depth-Cascading

The search engine application can depth-cascade the devices to various table sizes of different widths (68 bits, 136 bits, or 272 bits). The devices perform all the necessary arbitration to decide which device will drive the SRAM bus. Search latency increases as table size increases; the Search rate itself remains constant.

14.1 Depth-Cascading up to Eight Devices (One Block)

Figure 14-1 shows how up to eight devices can be cascaded to form 256K × 68-bit, 128K × 136-bit, or 64K × 272-bit tables. It also shows the interconnection between devices for depth-cascading. Each search engine asserts LHO[1] and LHO[0] signals to inform downstream devices of its results. The LHI[6:0] signals for a device are connected to LHO signals of the upstream devices. The host ASIC must program the TLSZ to 01 for each of up to eight devices in a block. A single device alone drives the SRAM bus in any single cycle.

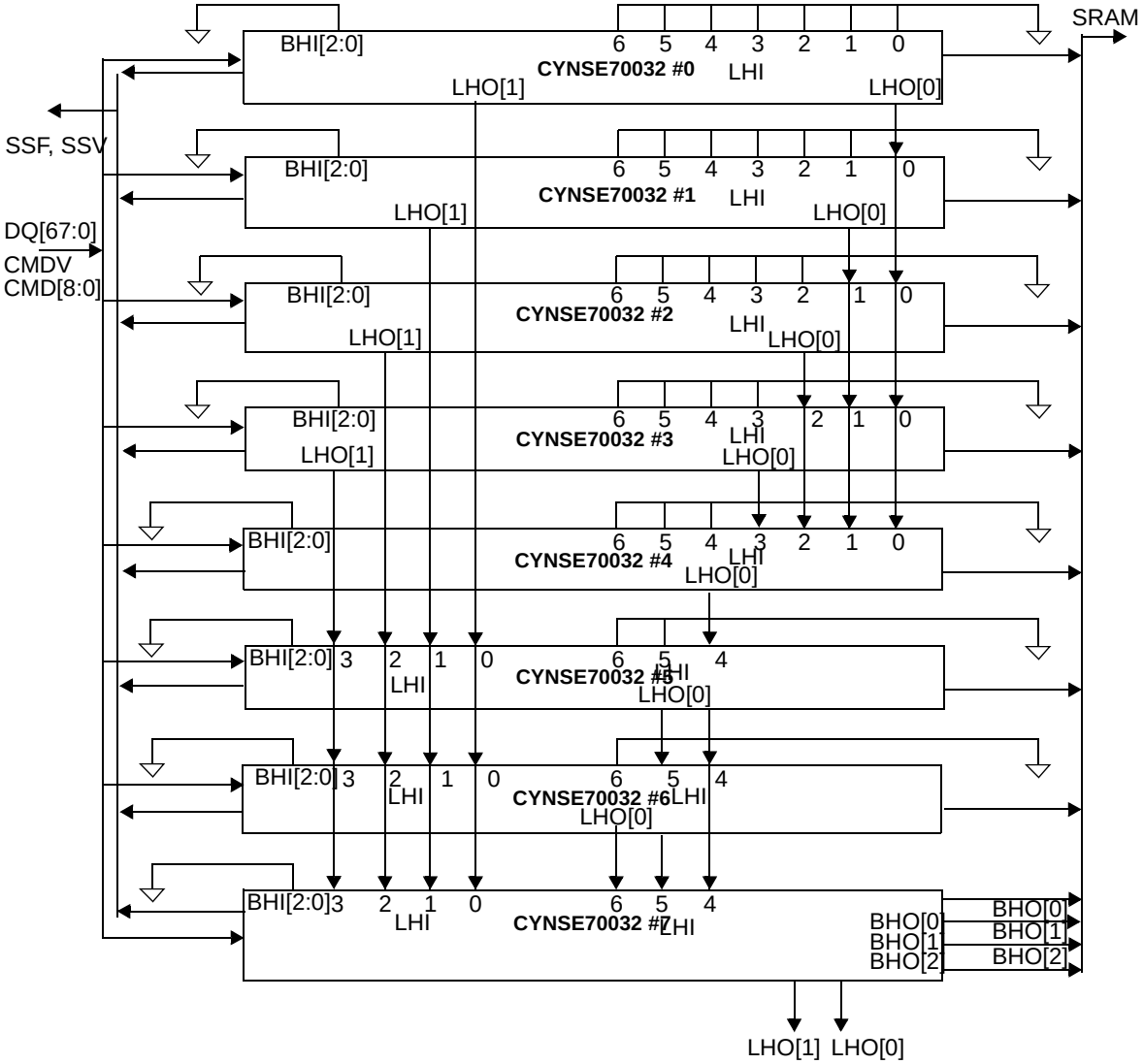


Figure 14-1. Depth-Cascading to Form a Single Block

14.2 Depth-Cascading up to 31 Devices (Four Blocks)

Figure 14-2 shows how to cascade up to four blocks. Each block except the last contains up to eight CYNSE70032 devices. The interconnection within each has been shown in the previous subsection with the cascading of up to eight devices in a block. ***Note***. The interconnection between blocks for depth-cascading is important. For each Search, a block asserts BHO[2], BHO[1], and BHO[0]. The BHO[2:0] signals for a block are taken only from the last device in the block. For all other devices within that block, these signals stay open and floating. The host ASIC must program the TLSZ field to 10 in each of the devices for cascading up to 31 devices (in up to four blocks).

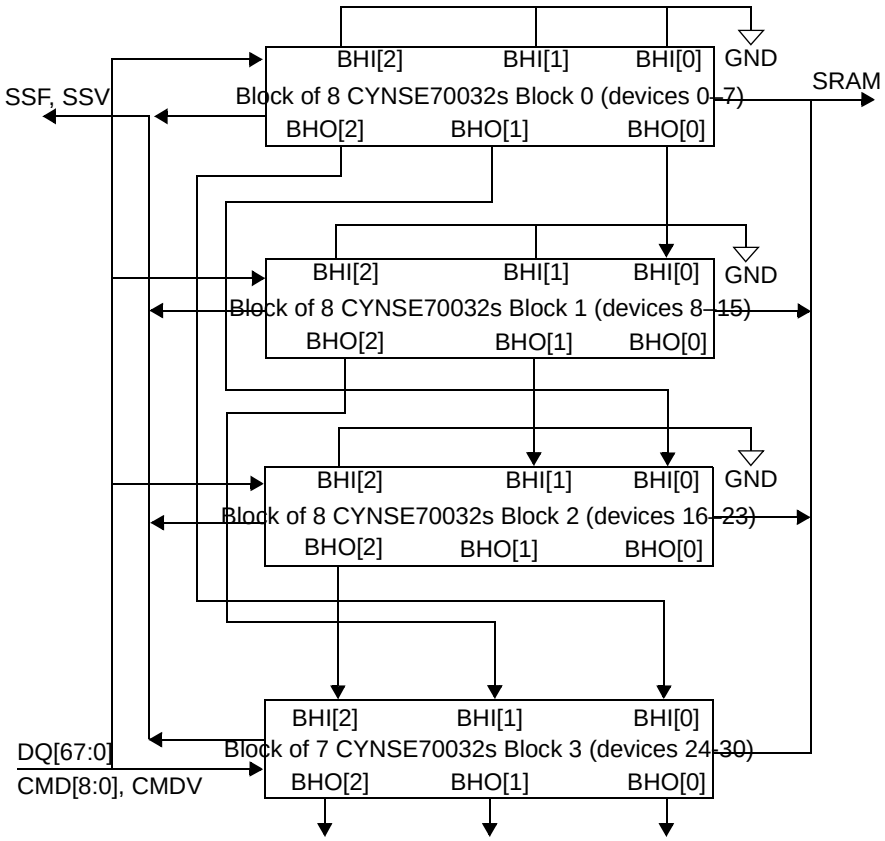


Figure 14-2. Depth-Cascading Four Blocks

14.3 Depth-Cascading for a FULL Signal

Bit[0] of each of the 68-bit entries is designated as a special bit (1 = occupied; 0 = empty). For each Learn or PIO Write to the data array, each device asserts FULO[1] and FULO[0] if it does not have any empty locations within it (see *Figure 14-3*). Each device combines the FULO signals from the devices above it with its own full status to generate a FULL signal, which will then give a full status of the table up to the device asserting the FULL signal. *Figure 14-3* shows the hardware connection diagram for generating the FULL signal that goes back to the ASIC. In a depth-cascaded block of up to eight devices, the FULL signal from the last device should be fed back to the ASIC controller to indicate the fullness of the table. The FULL signal of the other devices should be left open. ***Note***. The Learn instruction is supported for up to eight devices, whereas FULL cascading is allowed for one block in tables containing more than eight devices. In tables for which a Learn instruction will not be used, the bit[0] of each 68-bit entry should always be set to 1.

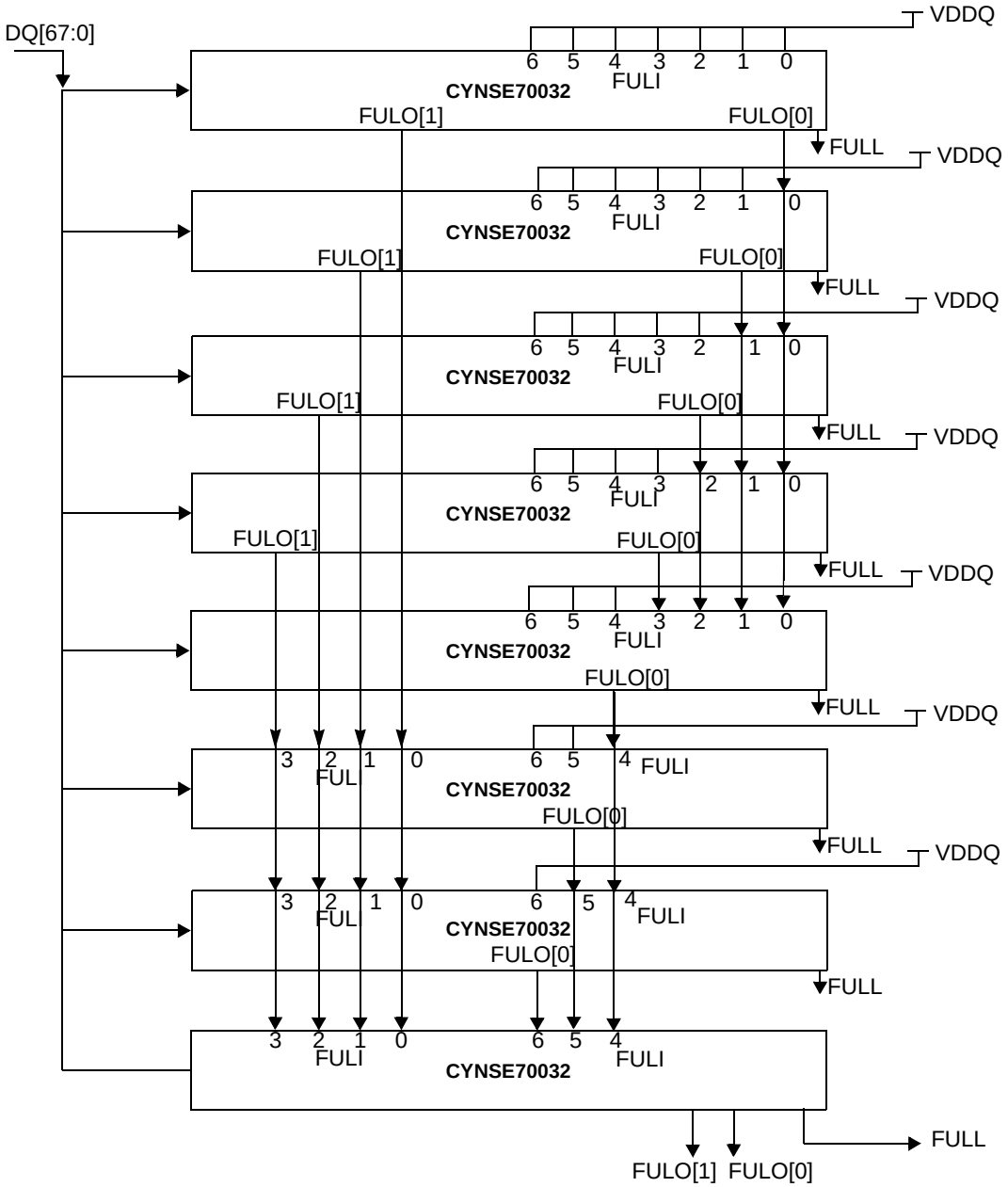


Figure 14-3. FULL Generation in a Cascaded Table

15.0 SRAM Addressing

Table 15-1 describes the commands used to generate addresses on the SRAM address bus. The index[13:0] field contains the address of a 68-bit entry that results in a hit in 68-bit-configured partition. It is the address of the 68-bit entry that lies at the 136-bit page, and the 272-bit page boundaries in 136-bit- and 272-bit-configured quadrants, respectively.

Section 7.0, “Registers” on page 13 of this specification, describes the NFA and SSR registers. ADR[13:0] contains the address supplied on the DQ bus during PIO access to the CYNSE70032. Command bits 8, and 7 {CMD[8:6]} are passed from the command to the SRAM address bus. See Section 12.0, “Commands” on page 18, for more information. ID[4:0] is the ID of the device driving the SRAM bus (see Section 21.0, “Pinout Descriptions and Package Diagrams” on page 120, for more information).

15.1 Generating an SRAM BUS Address

Table 15-1 details SRAM bus address generation.

Table 15-1. SRAM Bus Address

Command	SRAM Operation	21	20	19	[18:14]	[13:0]
Search	Read	C8	C7	C6	ID[4:0]	Index[13:0]
Learn	Write	C8	C7	C6	ID[4:0]	NFA[13:0]
PIO Read	Read	C8	C7	C6	ID[4:0]	ADR13:0]
PIO Write	Write	C8	C7	C6	ID[4:0]	ADR[13:0]
Indirect Access	Write/Read	C8	C7	C6	ID[4:0]	SSR[13:0]

15.2 SRAM PIO Access

The remainder of Section 15.0 describes SRAM Read and SRAM Write operations.

SRAM Read enables Read access to the off-chip SRAM that contains associative data. The latency from the issuance of the Read instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction, and will depend on the value programmed for the TLSZ parameter in the device configuration register. The latency of the ACK from the Read instruction is the same as the latency of the Search instruction to the SRAM address plus the HLAT programmed into the configuration register. ***Note***. SRAM Read is a blocking operation—no new instruction can begin until the ACK is returned by the selected device performing the access.

SRAM Write enables Write access to the off-chip SRAM containing associative data. The latency from the second cycle of the Write instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction, and will depend on the TLSZ value parameter programmed into the device configuration register. ***Note***. SRAM Write is a pipelined operation—new instruction can begin right after the previous command has ended.

15.3 SRAM Read with a Table of One Device

SRAM Read enables Read access to the off-chip SRAM that contains associative data. The latency from the issuance of the Read instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction and will depend on the TLSZ value parameter programmed into the device configuration register. The latency of the ACK from the Read instruction is the same as the latency of the Search instruction to the SRAM address plus the HLAT programmed into the configuration register. The following explains the SRAM Read operation in a table with only one device and having the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. *Figure 15-1* shows the associated timing diagram. For the following description, the selected device refers only to the device in the table because it is the only device to be accessed.

- **Cycle 1A**: The host ASIC applies the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[21:19] on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[67:0] and drives ACK from High-Z to LOW.
- **Cycle 5**: The selected device drives the Read address on SADR[21:0]; it also drives ACK HIGH, CE_L LOW, and ALE_L LOW.
- **Cycle 6**: The selected device drives CE_L HIGH, ALE_L HIGH, the SADR bus, the DQ bus in a three-state condition, and ACK LOW.

At the end of cycle 6, the selected device floats ACK in a three-state condition, and a new command can begin.

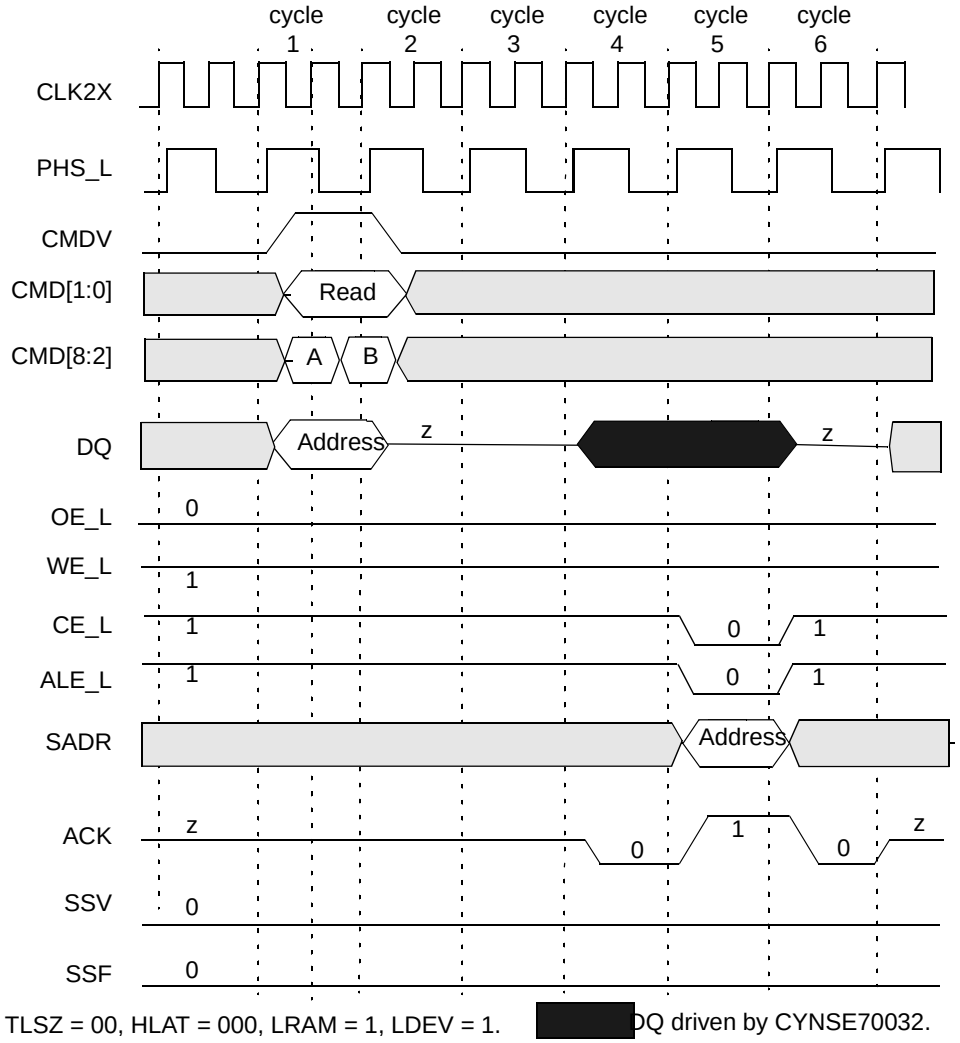


Figure 15-1. SRAM Read ACCESS (TLSZ = 00, HLAT = 000, LRAM = 1, LDEV = 1)

15.4 SRAM Read with a Table of up to Eight Devices

The following explains the SRAM Read operation completed through a table of up to eight devices using the following parameter: TLSZ = 01. *Figure 15-2* diagrams a block of eight devices. The following assumes that SRAM access is successfully achieved through CYNSE70032 device number 0. *Figure 15-3* and *Figure 15-4* show timing diagrams for device number 0 and device number 7, respectively.

- **Cycle 1A**: The host ASIC applies the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. During this cycle the host ASIC also supplies SADR[21:19] on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10 to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[67:0].
- **Cycle 5**: The selected device continues to drive DQ[67:0] and drives ACK from high-Z to low.
- **Cycle 6**: The selected device drives the Read address on SADR[21:0]. It also drives ACK high, CE_L low, WE_L high, and ALE_L low.
- **Cycle 7**: The selected device drives CE_L, ALE_L, WE_L, and DQ bus in a three-state condition. It continues to drive ACK low.

At the end of cycle 7, the selected device floats ACK in a three-state condition, and a new command can begin.

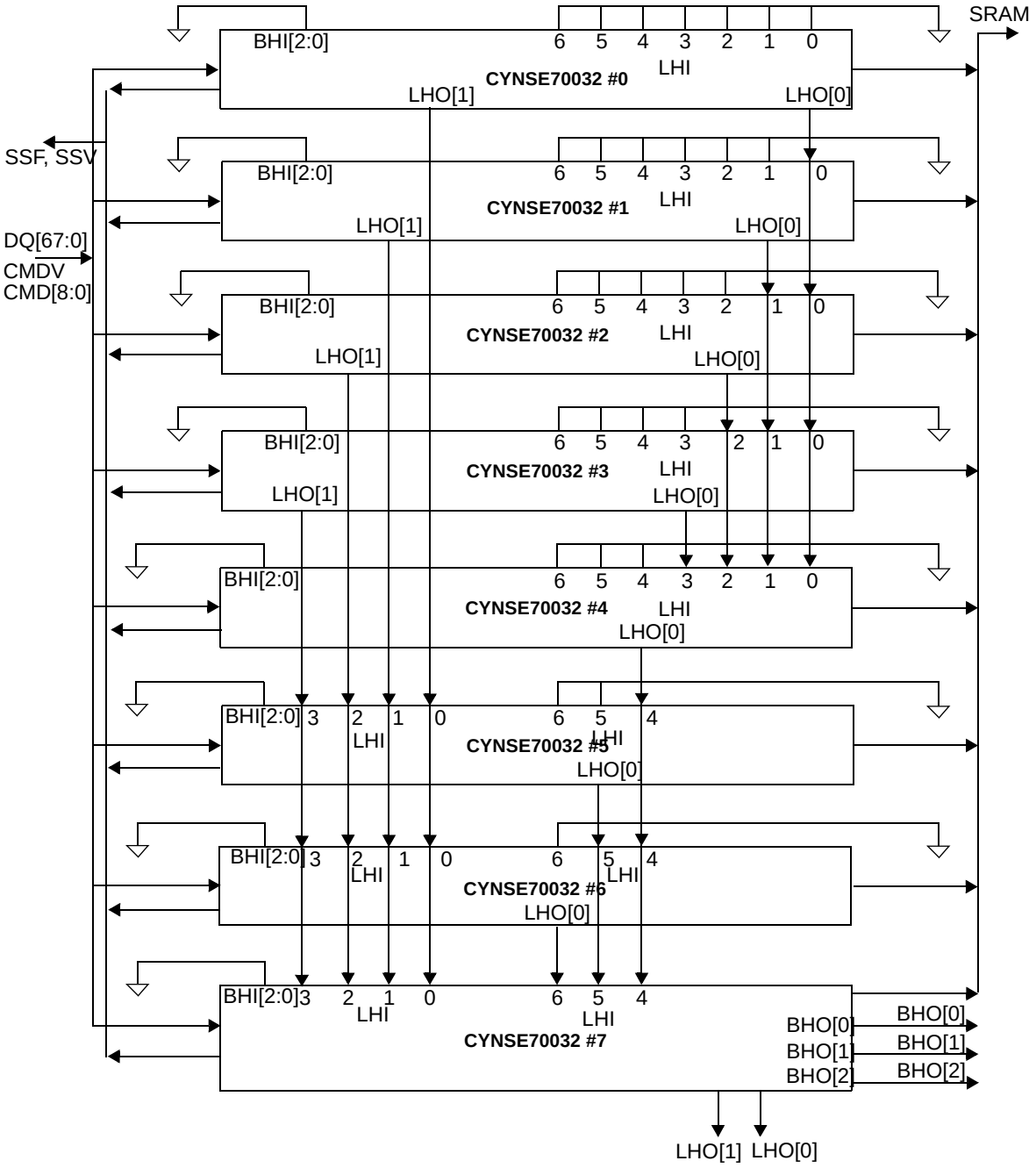


Figure 15-2. Table of a Block of Eight Devices

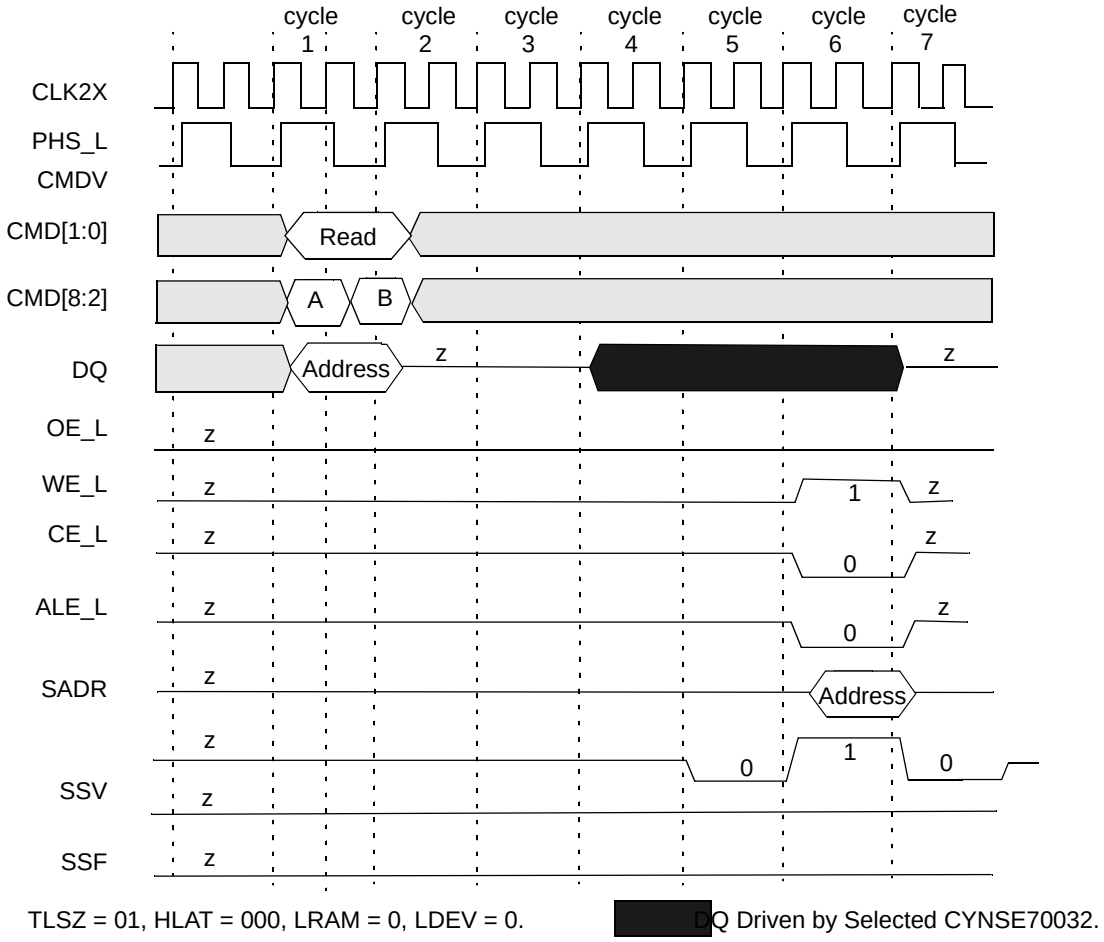
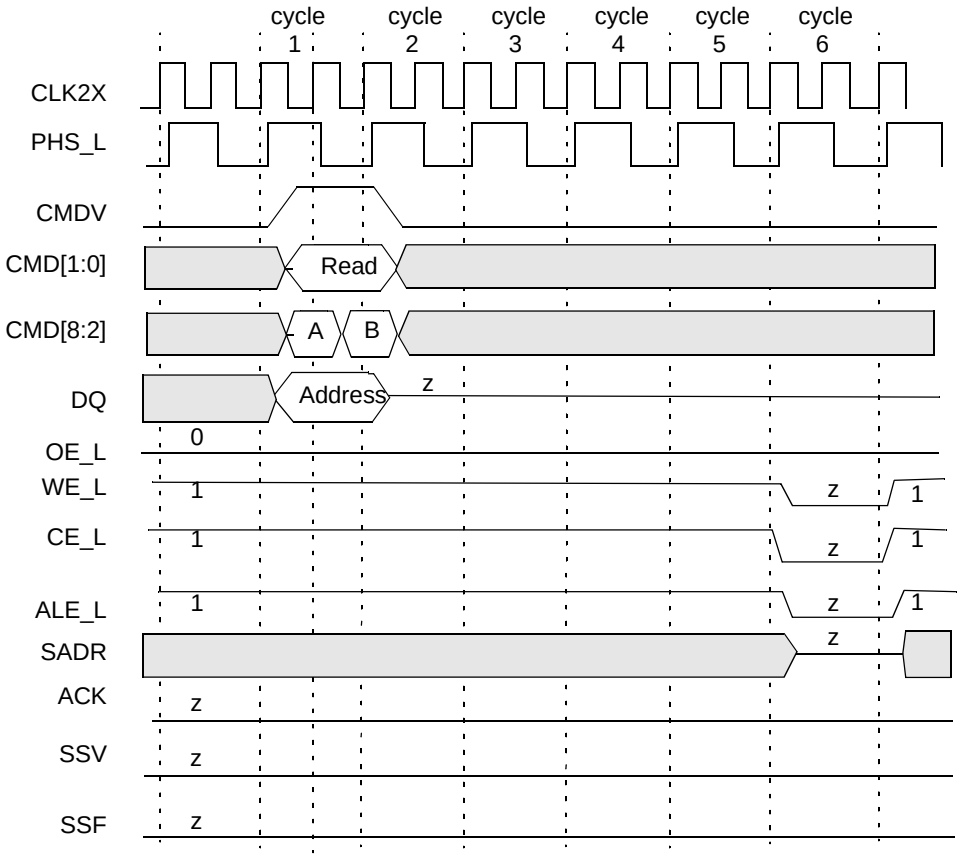


Figure 15-3. SRAM Read Through Device Number 0 in a Block of Eight Devices



TLSZ = 01, HLAT = 000, LRAM = 1, LDEV = 1.

Figure 15-4. SRAM Read Timing for Device Number 7 in a Block of Eight Devices

15.5 SRAM Read with a Table of up to 31 Devices

The following explains the SRAM Read operation accomplished through a table of up to 31 devices using the following parameters: TLSZ = 10. The diagram of this table is shown in *Figure 15-5*. The following assumes that SRAM access is being accomplished through CYNSE70032 device number 0 and that device number 0 is the selected device. *Figure 15-6* and *Figure 15-7* show the timing diagrams for device number 0 and device number 30, respectively.

- **Cycle 1A**: The host ASIC applies the Read instruction to CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[21:19] on CMD[8:6].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction to CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[67:0].
- **Cycles 5 to 6**: The selected device continues to drive DQ[67:0].
- **Cycle 7**: The selected device continues to drive DQ[67:0] and drives an SRAM Read cycle.
- **Cycle 8**: The selected device drives ACL from Z to LOW.
- **Cycle 9**: The selected device drives ACK to HIGH.
- **Cycle 10**: The selected device drives ACK from HIGH to LOW.

At the end of cycle 10, the selected device floats ACL in a three-state condition.

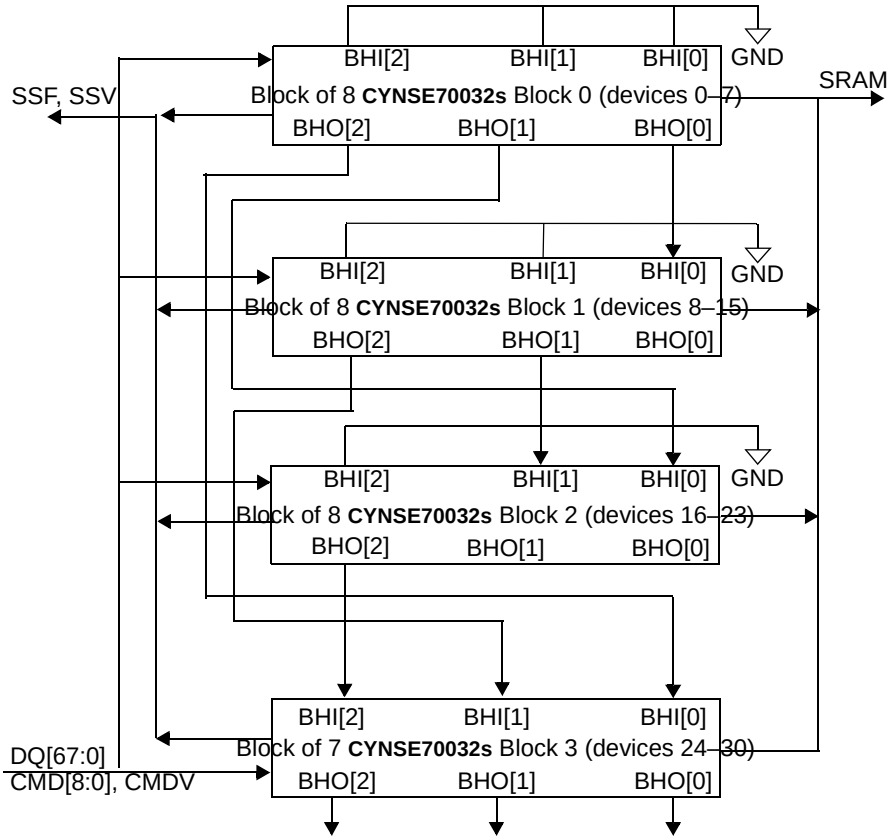


Figure 15-5. Table of 31 Devices Made of Four Blocks

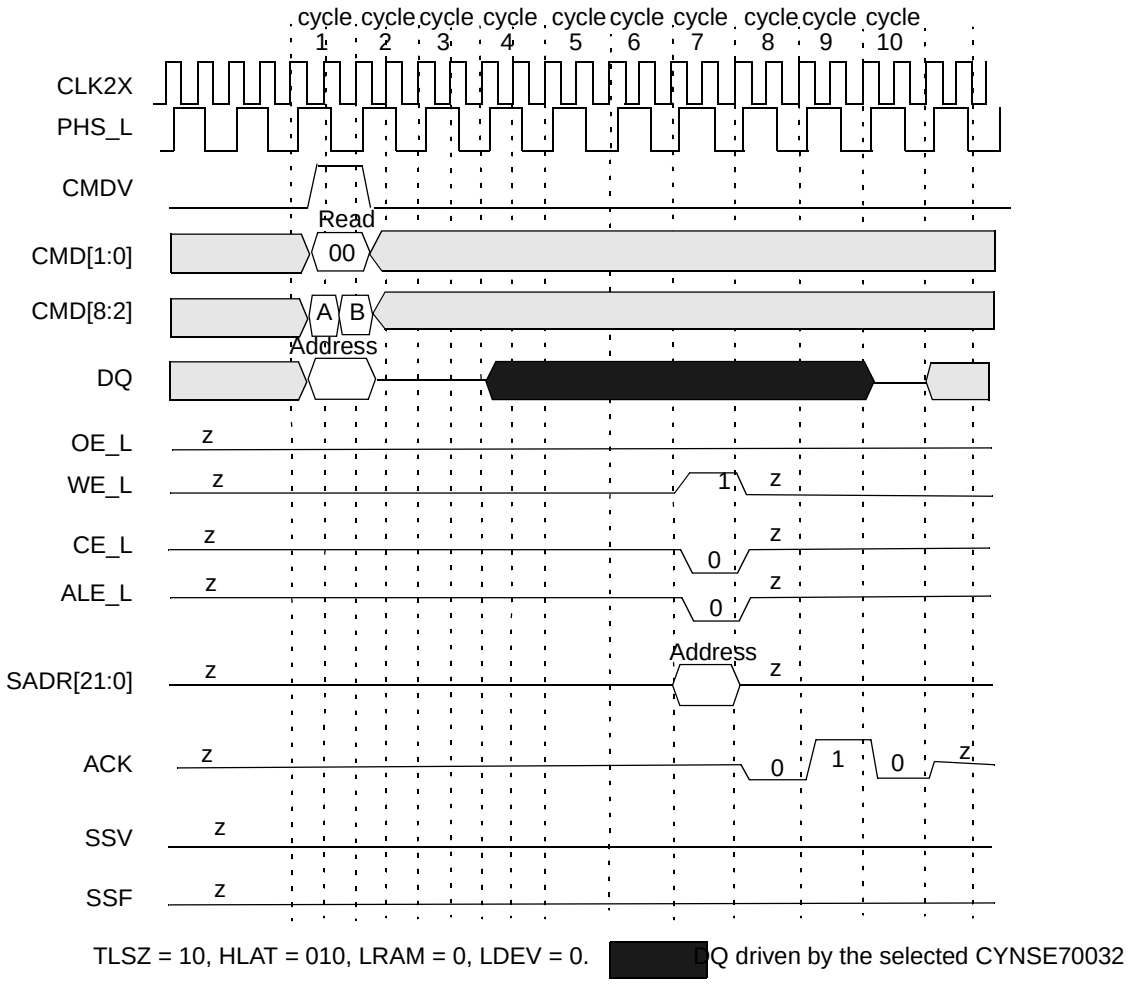


Figure 15-6. SRAM Read Through Device Number 0 in a Bank of 31 Devices (Device Number 0 Timing)

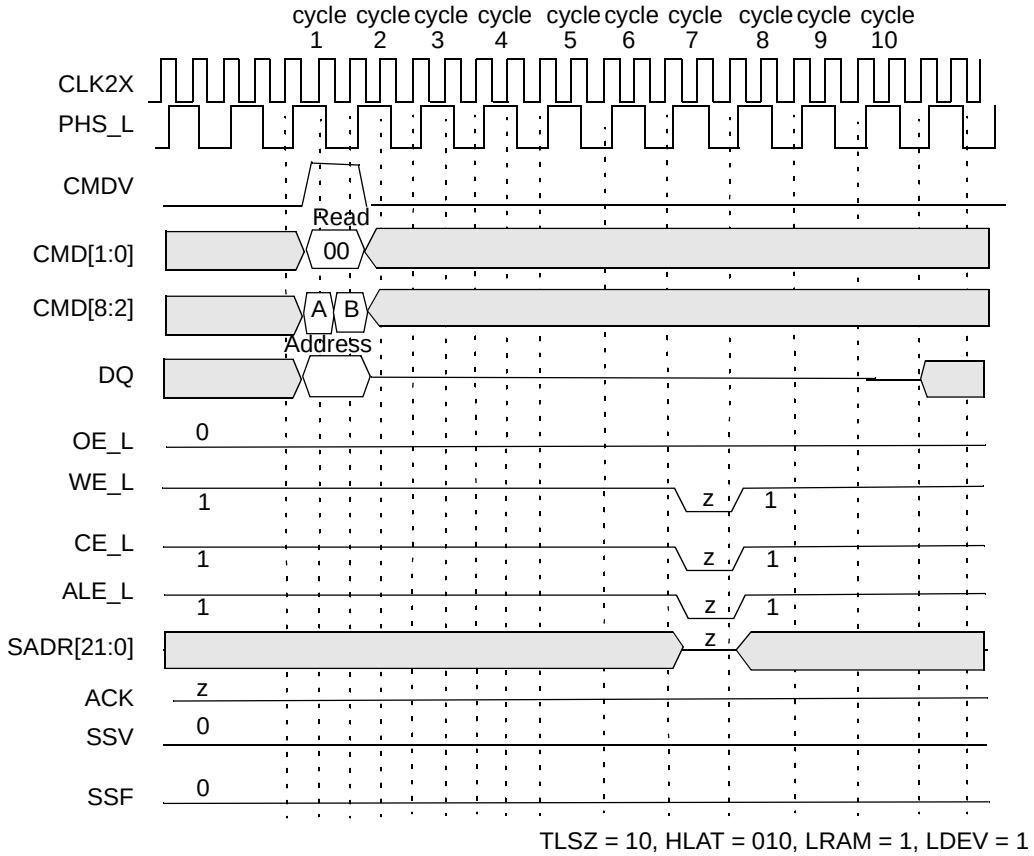


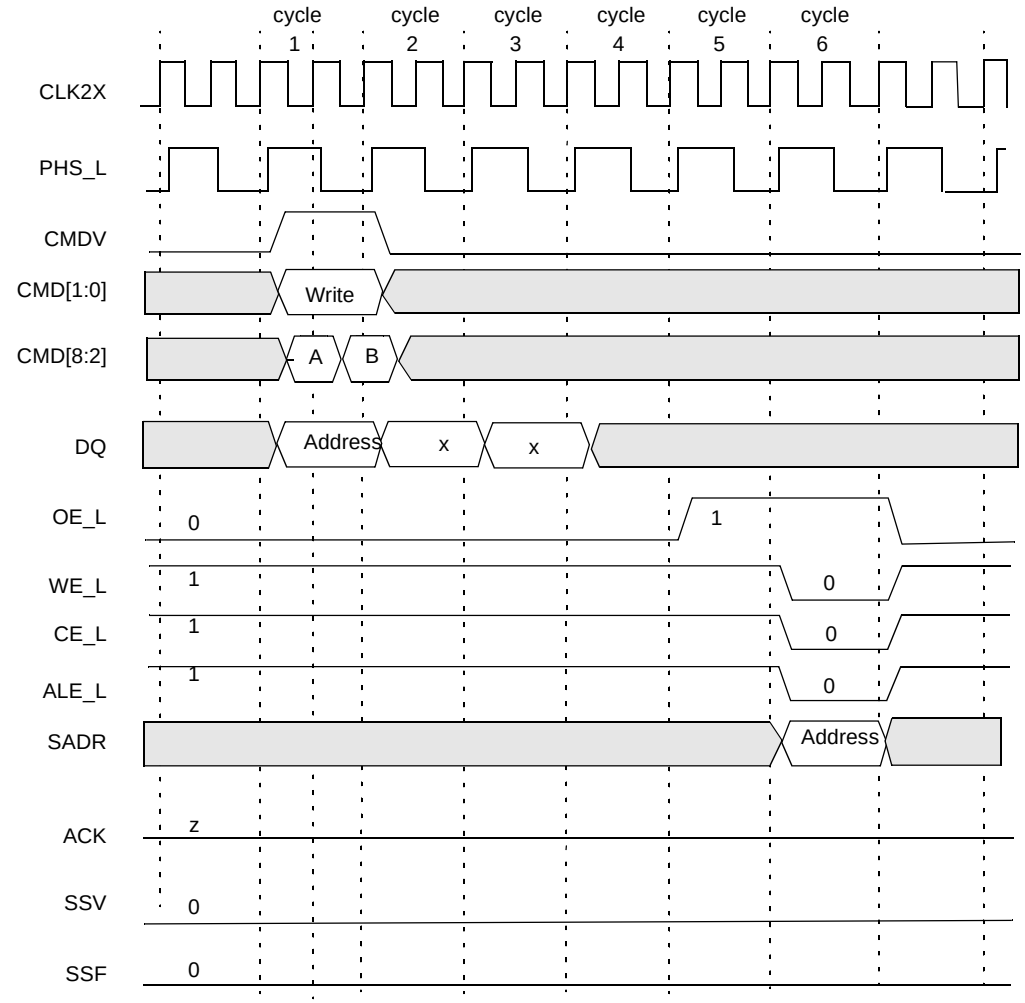
Figure 15-7. SRAM Readthrough Device Number 0 in a Bank of 31 Devices (Device Number 30 Timing)

15.6 SRAM Write with a Table of One Device

SRAM Write enables write access to the off-chip SRAM that contains associative data. The latency from the second cycle of the Write instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction, and will depend on the TLSZ value parameter programmed into the device configuration register. The following explains the SRAM Write operation accomplished through a table of only one device with the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. *Figure 15-8* shows the timing diagram. For the following description, the selected device refers to the only device in the table as this is the only device that will be accessed.

- **Cycle 1A**: The host ASIC applies the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:19] on CMD[8:6] in this cycle. ***Note***. CMD[2] must be set to 0 for SRAM Write, because burst Writes into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. ***Note***. CMD[2] must be set to 0 for SRAM Write, because burst Writes into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70032.
- **Cycle 3**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70032.

At the end of cycle 3, a new command can begin. The write is a pipelined operation; however, the Write cycle appears at the SRAM bus with the same latency as the Search instruction (as measured from the second cycle of the Write command).



TLSZ = 00, HLAT = 000, LRAM = 1, LDEV = 1

Figure 15-8. SRAM Write Access (TLSZ = 00, HLAT = 000, LRAM = 1, LDEV = 1)

15.7 SRAM Write with a Table of up to Eight Devices

The following explains the SRAM Write operation done via a table(s) of up to eight devices with the following parameters: TLSZ = 01. The diagram of this table is shown in *Figure 15-9*. The following assumes that SRAM access is getting done through CYNSE70032 device number 0. *Figure 15-10* and *Figure 15-11* show the timing diagram for the device number 0 and device number 7, respectively.

- **Cycle 1A**: The host ASIC applies the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:19] on CMD[8:6] in this cycle. ***Note***. CMD[2] must be set to 0 for SRAM Write, because burst Writes into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. ***Note***. CMD[2] must be set to 0 for SRAM Write, because burst Writes into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70032.
- **Cycle 3**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70032.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation; however, the Write cycle appears at the SRAM bus with the same latency as the Search instruction (as measured from the second cycle of the Write command).

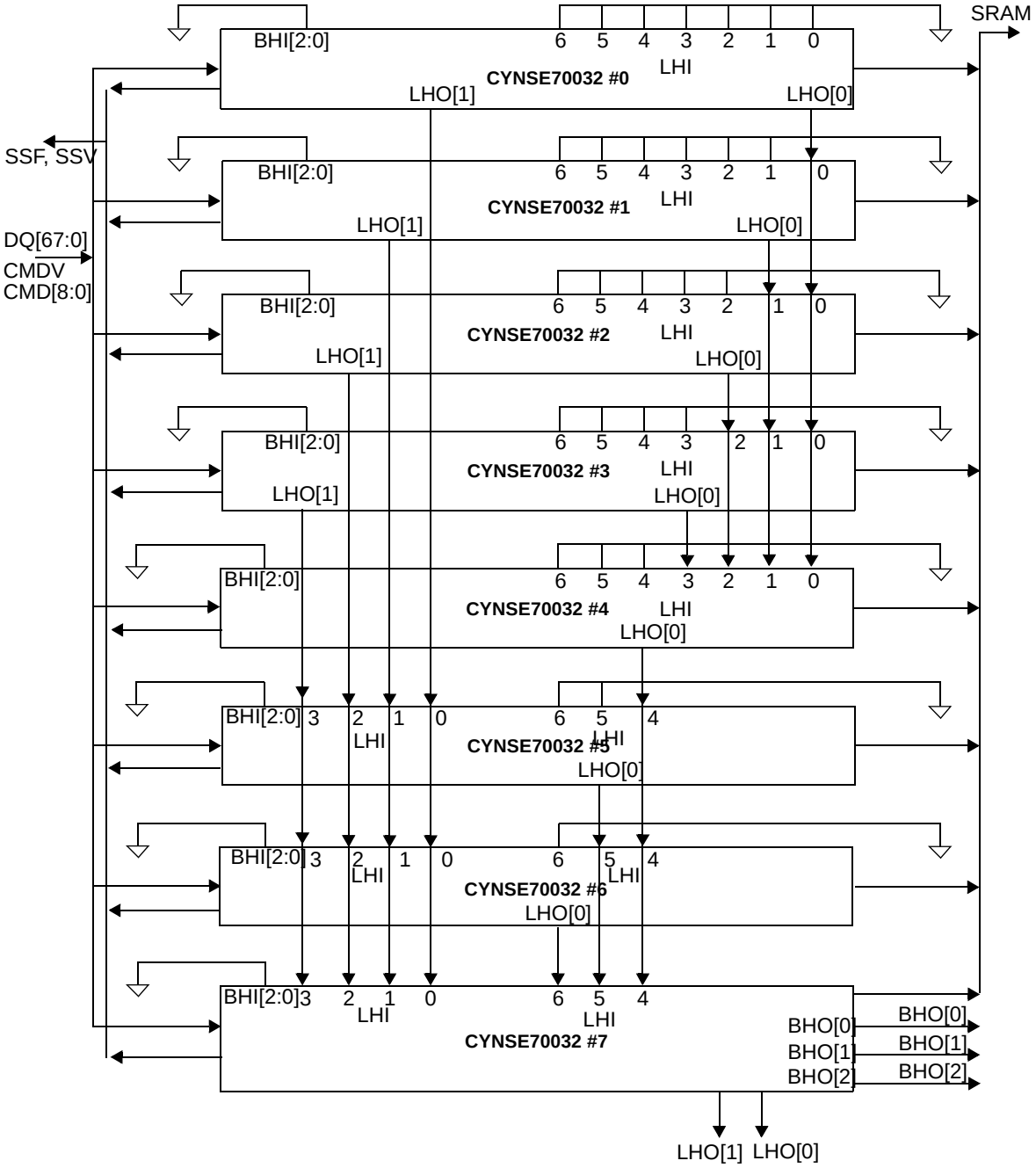


Figure 15-9. Table of a Block of Eight Devices

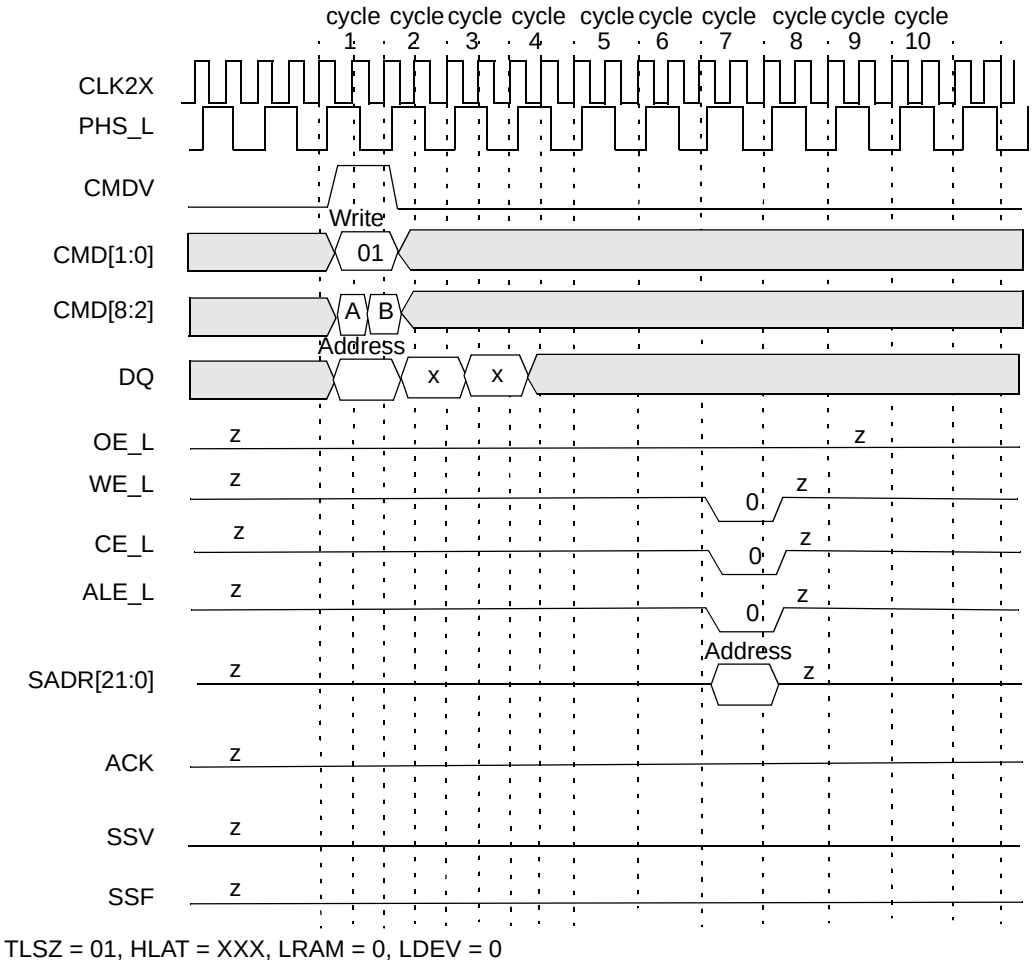
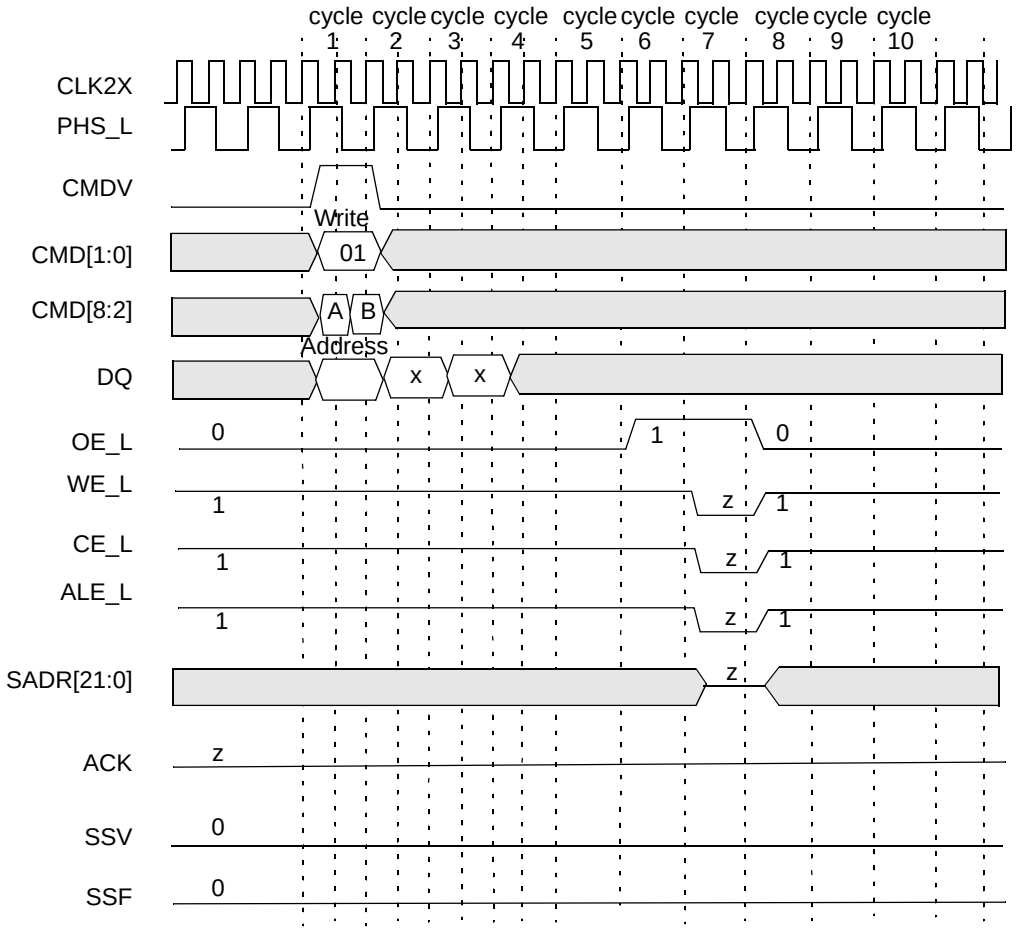


Figure 15-10. SRAM Write Through Device Number 0 in a Block of Eight Devices



TLSZ = 01, HLAT = XXX, LRAM = 1, LDEV = 1

Figure 15-11. SRAM Write Timing for Device Number 7 in a Block of Eight Devices

15.8 SRAM Write with Table(s) Consisting of up to 31 Devices

The following explains the SRAM Write operation done via a table(s) of up to 31 devices and with the following parameters: TLSZ = 10. The diagram of this table(s) is shown in *Figure 15-12*. The following assumes that SRAM access is accomplished through CYNSE70032 device number 0 (the selected device). *Figure 15-13* and *Figure 15-14* show the timing diagram for device number 0 and device number 30, respectively.

- **Cycle 1A**: The host ASIC applies the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:19] on CMD[8:6] in this cycle. ***Note***. CMD[2] must be set to 0 for SRAM Write, because burst Writes into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. ***Note***. CMD[2] must be set to 0 for SRAM Write, because burst Writes into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70032.
- **Cycle 3**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70032.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation; however, the Write cycle appears at the SRAM bus with the same latency as the Search instruction (as measured from the second cycle of the Write command).

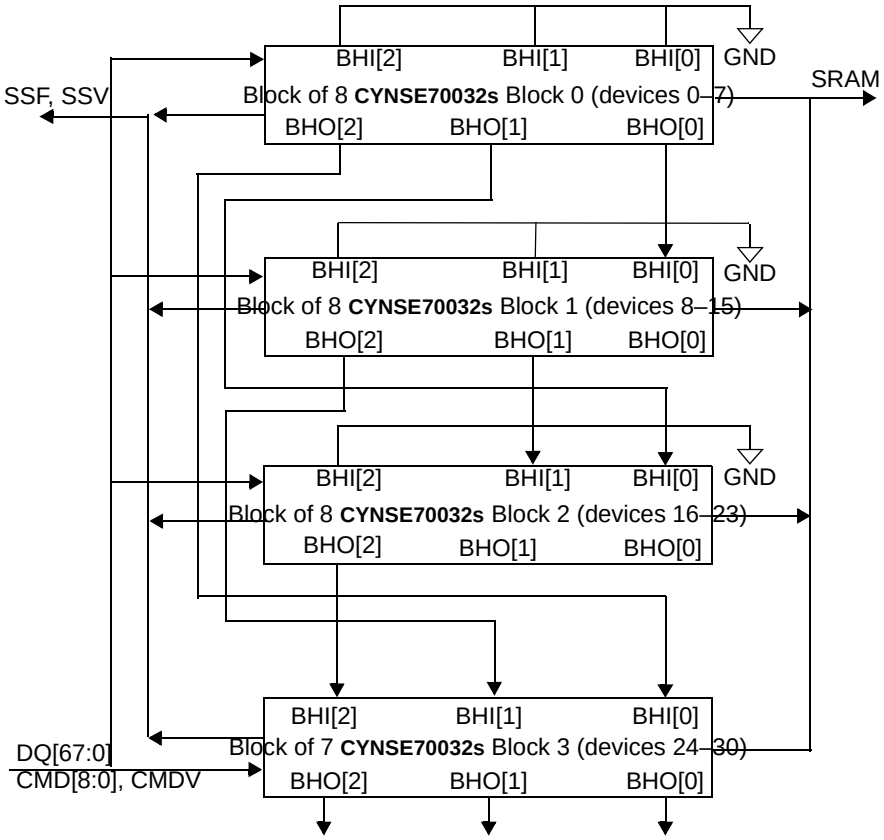
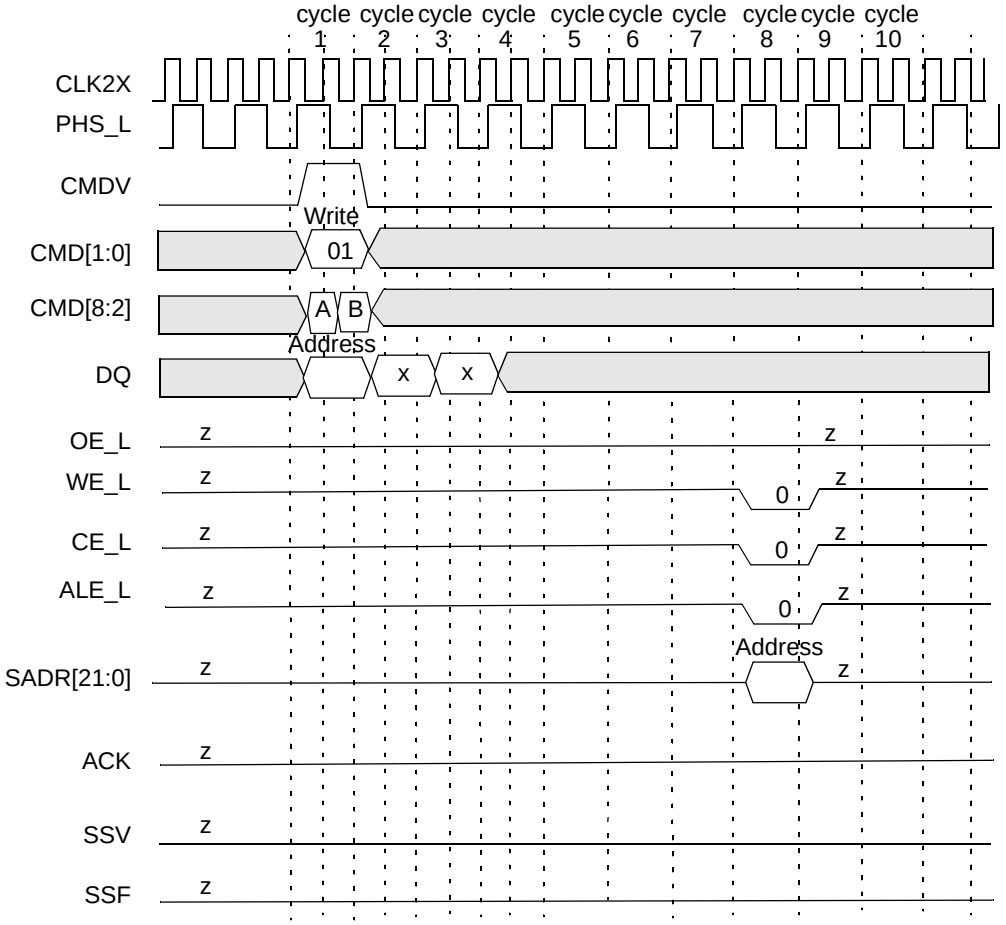
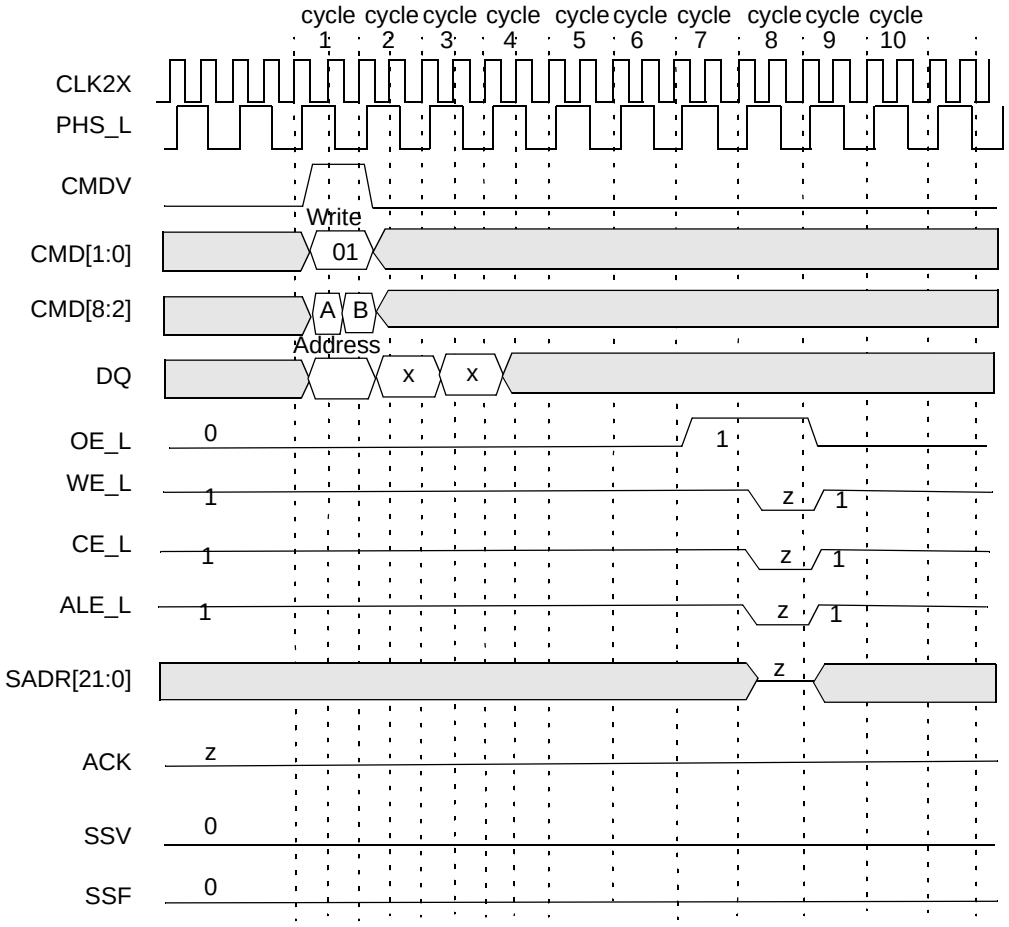


Figure 15-12. Table of 31 Devices (Four Blocks)



TLSZ = 01, HLAT = XXX, LRAM = 0, LDEV = 0.

Figure 15-13. SRAM Write Through Device Number 0 in a Bank of 31 Devices (Device 0 Timing)



TLSZ = 01, HLAT = XXX, LRAM = 1, LDEV = 1.

Figure 15-14. SRAM Write Through Device Number 0 in a Bank of 31 CYNSE70032 Devices (Device Number 30 Timing)

16.0 Power

16.1 The Proper Power-up Sequence

Proper power-up sequence is required to correctly initialize the Cypress Network Search Engines before functional access to the device can begin. RST_L and TRST_L should be held low before the power supplies ramp-up. RST_L must be set low for a duration of time afterward and then set high. The following steps describe the proper power-up sequence.

1. Set RST_L and TRST_L low.
2. Power up V_{DD}, V_{DDQ} and start running CLK2X and PHS_L. The order in which these signals (including V_{DD} and V_{DDQ}) are applied is not critical.
3. Hold RST_L low for a minimum of 64 CLK2X cycles. The counting starts on the first rising edge of CLK2X when PHS_L is high, after both V_{DD} and V_{DDQ} have reached their steady state voltages. Set RST_L high afterward to complete the power-up sequence. For JTAG reset, TRST_L can be brought high after both V_{DD} and V_{DDQ} have reached their steady state voltages.

Figure 16-1 illustrates the proper sequences of the power-up operation.

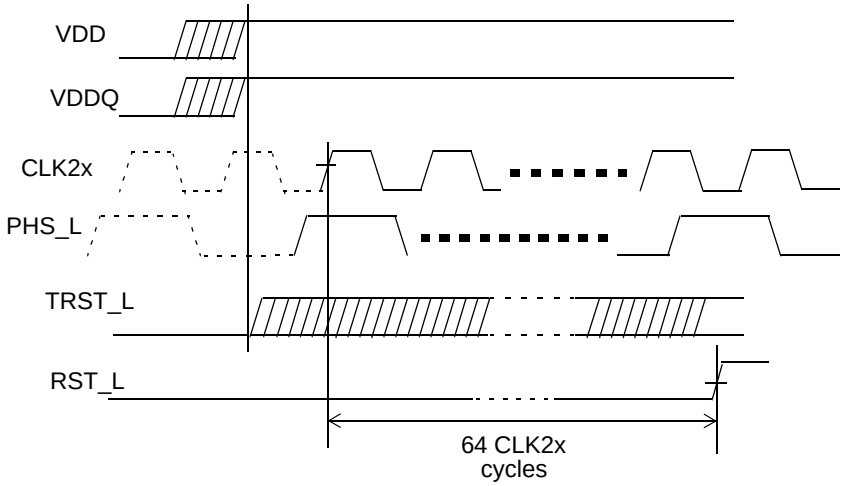


Figure 16-1. Power-up Sequence

17.0 Application

Figure 17-1 shows how a search engine subsystem can be formed using a host ASIC and Cypress's CYNSE70032 bank. It also shows how this search engine subsystem is integrated in a switch or router. The CYNSE70032 can access synchronous as well as asynchronous SRAMs by allowing the host ASIC to set the same HLAT parameter in the all search engines within a bank of search engines.

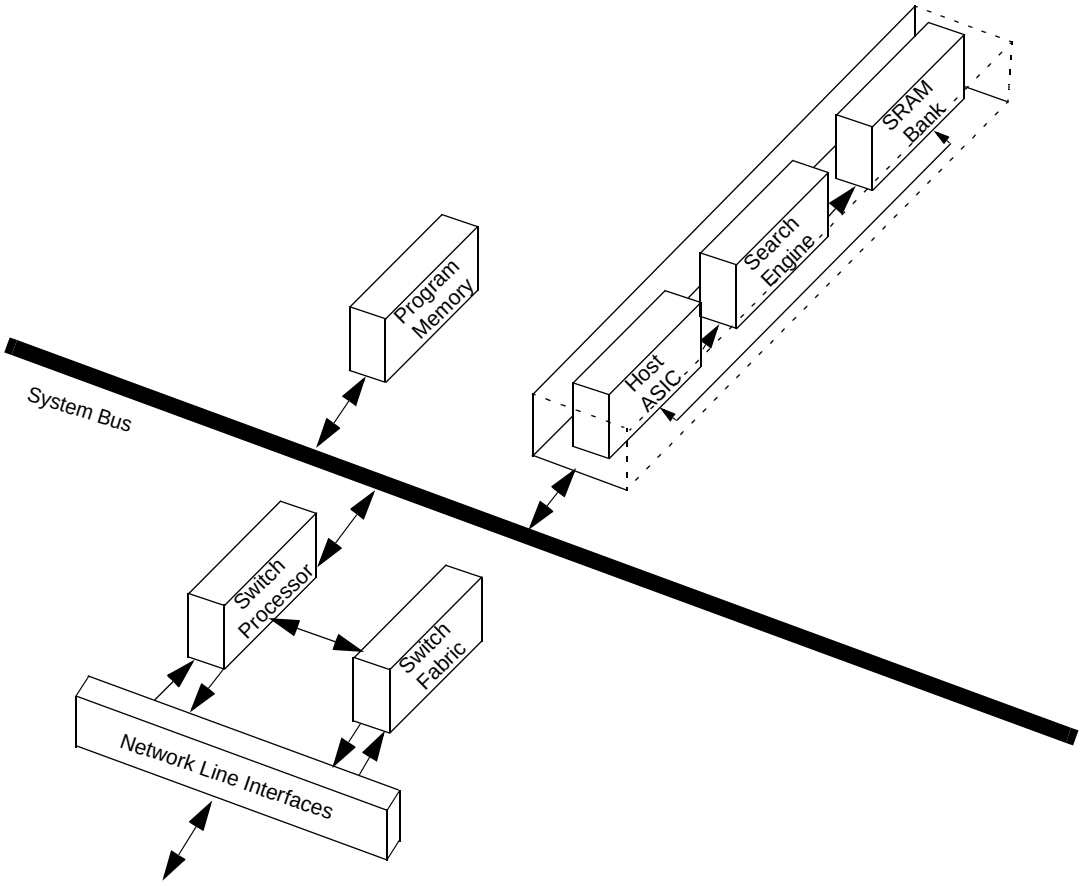


Figure 17-1. Sample Switch/Router Using the CYNSE70032 Device

18.0 JTAG (1149.1) Testing

The CYNSE70032 supports the Test Access Port (TAP) and Boundary Scan Architecture, as specified in the IEEE JTAG standard 1149.1. The pin interface to the chip consists of five signals with the standard definitions: TCK, TMS, TDI, TDO, and TRST_L. *Table 18-1* describes the operations that the test access port controller supports, and *Table 18-2* describes the TAP Device ID Register. ***Note***. To disable JTAG functionality, connect the TCK, TMS and TDI pins to V_{DDQ} through a pull-up, and TRST_L to ground through a pull-down.

Table 18-1. Supported Operations

Instruction	Type	Description
SAMPLE/PRELOAD	Mandatory	**Sample/Preload**. This operation loads the values of signals going to and from I/O pins into the boundary scan shift register to provide a snapshot of the normal functional operation, and to initialize the boundary scan.
EXTEST	Mandatory	**External Test**. This operation uses boundary scan values shifted in from TAP to test connectivity external to the device.
BYPASS	Mandatory	**This operation loads a single bit shift register between TDI and TDO** and provides a minimum-length serial path when no test operation is required.
IDCODE	Optional	**This operation selects the Identification register between TDI and TDO** and allows the “idcode” to be read serially through TDO.
CLAMP	Optional	**This operation drives preset values onto the outputs of devices**.
HIghZ	Optional	**This operation leaves the device output pins in a high impedance state**.

Table 18-2. TAP Device ID Register

Field	Range	Initial Value	Description
Revision	[31:28]	0001	**Revision Number**. This is the current device revision number. Numbers start from 1 and increment by 1 for each revision of the device.
Part Number	[27:12]	0000 0000 0000 0001	**This is the part number of the device**.
MFID	[11:1]	000_1101_1100	**Manufacturer ID**. This field is the same as the manufacturer ID used in the TAP controller.
LSB	[0]	1	**Least significant bit**.

19.0 Electrical Specifications

This section describes the electrical specifications, capacitance, operating conditions, DC characteristics, and AC timing parameters for the CYNSE70032, as shown in *Table 19-1* and *Table 19-2*.

Operating Conditions for CYNSE70032

Table 19-1. DC Electrical Characteristics for CYNSE70032

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{DDQ} = V_{DDQ}$ Max., V_{IN}= 0 to V_{DDQ} Max.	–10	10	µA
I_{LO}	Output leakage current	$V_{DDQ} = V_{DDQ}$ Max., V_{IN}= 0 to V_{DDQ} Max.	–10	10	µA
V_{IL}	Input LOW voltage (V_{DDQ} = 3.3V)		–0.3	0.8	V
V_{IL}	Input LOW voltage (V_{DDQ} = 2.5V)		–0.3	0.8	V
V_{IH}	Input HIGH voltage (V_{DDQ} = 3.3V)		2.0	V_{DDQ} + 0.3	V
V_{IH}	Input HIGH voltage (V_{DDQ} = 2.5V)		2.0	V_{DDQ} + 0.3	V
V_{OL}	Output LOW voltage (V_{DDQ} = 3.3V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OL} = 8 mA		0.4	V
V_{OL}	Output LOW voltage (V_{DDQ} = 2.5V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH voltage (V_{DDQ} = 3.3V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OH} = 8 mA	2.4		V
V_{OH}	Output HIGH voltage (V_{DDQ} = 2.5V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OH} = 8.mA	2.4		V
I_{DD2}	3.3V supply current at V_{DD} Max	83-MHz search rate, I_{OUT} = 0 mA		300	mA
I_{DD2}	3.3V supply current at V_{DD} Max	66-MHz search rate, I_{OUT} = 0 mA		240	mA
I_{DD2}	2.5V supply current at V_{DD} Max	83-MHz search rate, I_{OUT} = 0 mA		180	mA
I_{DD2}	2.5V supply current at V_{DD} Max	66-MHz search rate, I_{OUT} = 0 mA		150	mA
I_{DDI}	1.8V supply current at V_{DD} Max	83-MHz search rate		1250	mA
I_{DDI}	1.8V supply current at V_{DD} Max	66-MHz search rate		1000	mA

Parameter	Description	Max.	Unit
C_{IN}	Input capacitance	6	pF[7]
C_{OUT}	Output capacitance	6	pF[8]

Table 19-2. Operating Conditions for CYNSE70032

Parameter	Description	Min. (3.3V)	Max. (3.3V)	Min. (2.5V)	Max. (2.5V)	Unit
V_{DDQ}	Operating voltage for IO	3.135	3.465	2.4	2.6	V
V_{DD}	Operating supply voltage	1.7	1.9	1.7	1.9	V
V_{IH}	Input HIGH voltage[9]	2.0	V_{DDQ}+ 0.3	1.7	V_{DDQ}+ 0.3	V
V_{IL}	Input LOW voltage[10]	–0.3	0.8	–0.3	0.7	V
	Supply voltage tolerance	–5%	+5%	–5%	+5%	

Notes:
7. f = 1 MHz, V_{IN} = 0V.
8. f = 1 MHz, V_{OUT} = 0V.
9. Maximum allowable applies to overshoot only (V_{DDQ} is 2.5V supply).
10. Minimum allowable applies to undershoot only.

Table 19-3. Operating Range for CYNSE70032

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+2.5V to +3.3V ±5%
Industrial	–40°C to +85°C	+2.5V to +3.3V ±5%

20.0 AC Timing Waveforms

Table 20-1 shows the AC timing parameters for the CYNSE70032 device; *Table 20-2* shows the same parameters but for 2.5V. *Figure 20-1* shows the device's input wave form, and *Figure 20-2* and *Figure 20-3* show the device's output load. *Figure 20-4* shows a timing waveform diagram.

Table 20-1. AC Timing Parameters with CLK2X

Parameter	Description	CYNSE70032-066		CYNSE70032-083		Unit
		Min.	Max.	Min.	Max.	
F_{CLOCK}	CLK2X frequency		133		166	MHz
t_{CLK}	CLK2X period	7.5		6.0		ns
T_{CKHI}	CLK2X high pulse[11]	3.0		2.4		ns
T_{CKLO}	CLK2X low pulse[11]	3.0		2.4		ns
T_{ISCH}	Input set-up time to CLK2X rising edge[11]	2.5		**1.8**		ns
T_{IHCH}	Input hold time to CLK2X rising edge[11]	0.6		**0.6**		ns
T_{ICSCH}	Cascaded input set-up time to CLK2X rising edge[11]	4.2		**3.5**		ns
T_{ICHCH}	Cascaded input hold time to CLK2X rising edge[11]	0.6		**0.6**		ns
T_{CKHOV}	Rising edge of CLK2X to LHO, FULO, BHO, FULL valid[12]		8.5		**7.0**	ns
T_{CKHDV}	Rising edge of CLK2X to DQ valid[12]		9.0		**7.5**	ns
T_{CKHDZ}	Rising edge of CLK2X to DQ High-Z[13]		8.5		**7.0**	ns
T_{CKHSV}	Rising edge of CLK2X to SRAM bus valid[12]		9.0		**7.5**	ns
T_{CKHSHZ}	Rising edge of CLK2X to SRAM bus High-Z[13]		6.5		**6.0**	ns
T_{CKHSLZ}	Rising edge of CLK2X to SRAM bus Low-Z[13]	7.0		**6.5**		ns

Table 20-2. Test Conditions of CYNSE70032

Conditions	Results
Input pulse levels (V_{DDQ} = 3.3V)	GND to 3.0V
Input pulse levels (V_{DDQ} = 2.5V)	GND to 2.5V
Input rise and fall times measured at 0.3V and 2.7V (V_{DDQ} = 3.3V)	≤ 2 ns (see *Figure 20-1*)
Input rise and fall times measured at 0.25V and 2.25V (V_{DDQ} = 2.5V)	≤ 2 ns (see *Figure 20-1*)
Input timing reference levels (V_{DDQ} = 3.3V)	1.5V
Input timing reference levels (V_{DDQ} = 2.5V)	1.25V
Output reference levels (V_{DDQ} = 3.3V)	1.5V
Output reference levels (V_{DDQ} = 2.5V)	1.25V
Output load	See *Figure 20-2* and *Figure 20-3*

Notes:
11. Values are based on 50% signal levels.
12. Based on an AC load of CL = 30 pF (see *Figure 20-1*, *Figure 20-2*, and *Figure 20-3*).
13. These parameters are sampled but not 100% tested, and are based on an AC load of 5 pF.

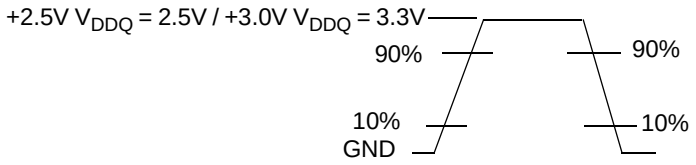


Figure 20-1. Input Waveform for CYNSE70032

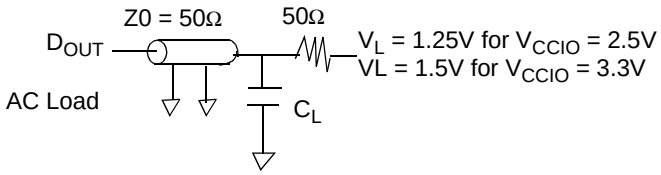


Figure 20-2. Output Load for CYNSE70032

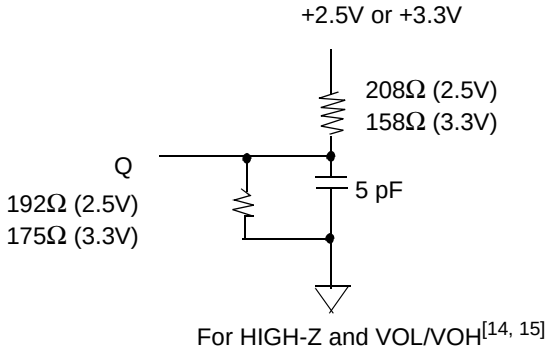
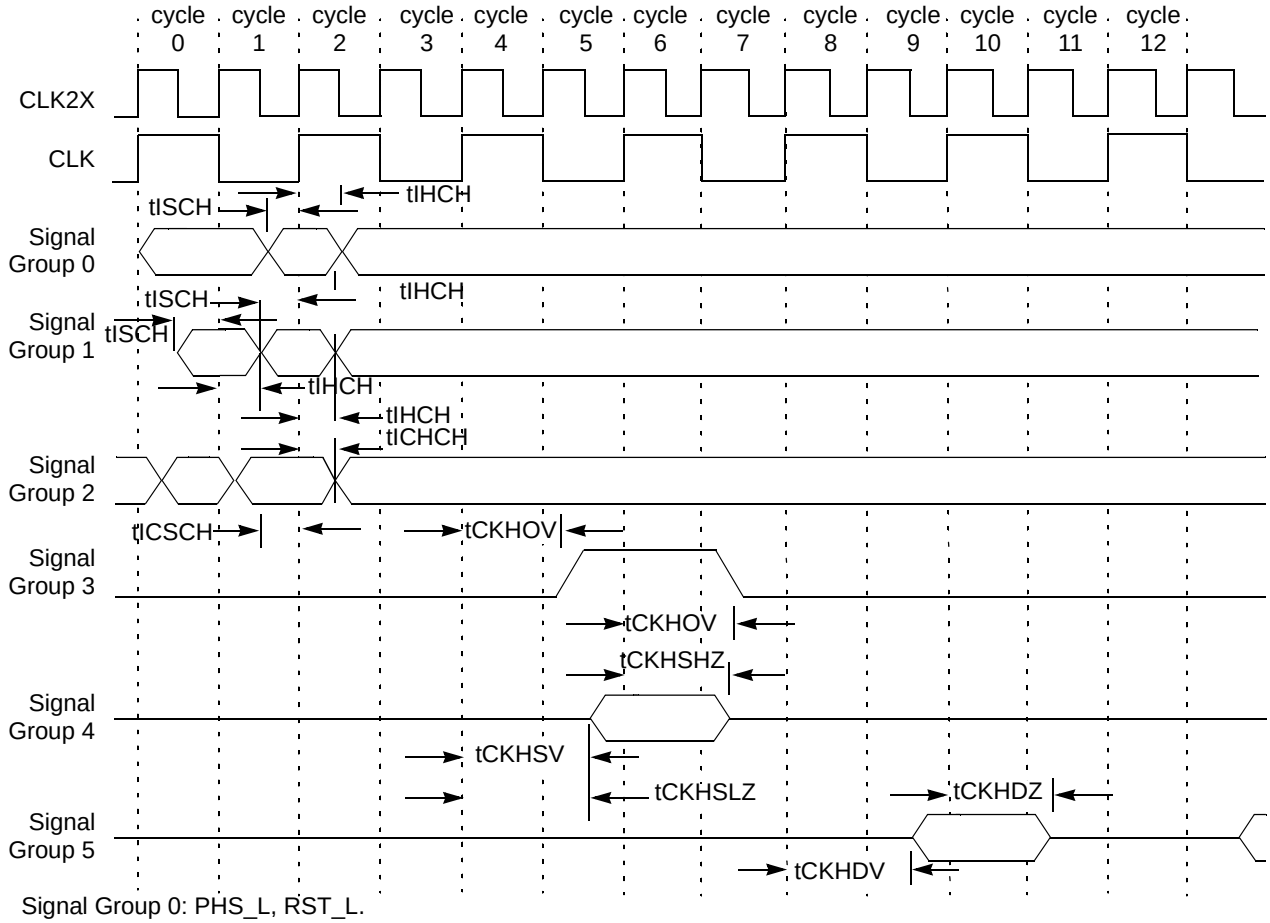


Figure 20-3. 2.5 I/O Output Load Equivalent for CYNSE70032

Notes:
14. Output loading is specified with C_L = 5 pF, as in *Figure 20-3*. Transition is measured at ± 200 mV from steady-state voltage.
15. The load used for V_{OH}, V_{OL} testing is shown in *Figure 20-3*.



Signal Group 0: PHS_L, RST_L.
Signal Group 1: DQ, CMD, CMDV.
Signal Group 2: LHI, BHI, FULI.
Signal Group 3: LHO, BHO, FULO, FULL.
Signal Group 4: SADR, CE_L, OE_L, WE_L, ALE_L, SSF, SSV.
Signal Group 5: DQ, ACK, EOT.

Figure 20-4. AC Timing Waveforms with CLK2X

21.0 Pinout Descriptions and Package Diagrams

In the following figure and table the CYNSE70032 device pinout diagram and pinout descriptions are shown.

	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	NC	GND	EOT	NC	NC	VDD	FULI5	FULI4	FULI1	BHO0	VDD	BHI0	LHI6	NC	VDD	ID2	ID0	TDO	NC	NC	1
2	NC	NC	ACK	FULL	NC	FULO1	NC	FULI6	FULI2	BHO1	BHI2	VDDQ	LHI5	LHI3	LHI2	ID3	TMS	TDI	VDD	NC	2
3	DQ64	NC	NC	VDDQ	VDD	VDDQ	NC	NC	VDDQ	BHO2	VDD	LHO1	LHI4	VDDQ	LHIO	ID1	TCK	NC	NC	DQ65	3
4	DQ62	NC	VDD	GND	RSTL	NC	FULO0	GND	FULI3	FULI0	BHI1	LHO0	GND	LHI1	ID4	TRST_L	GND	DQ63	DQ61	DQ57	4
5	DQ60	VDDQ	NC	DQ66						TOP							DQ67	DQ59	NC	DQ53	5
6	VDD	NC	DQ56	DQ58													VDDQ	DQ55	DQ49	VDD	6
7	DQ50	VDDQ	DQ52	DQ54													DQ47	VDDQ	DQ51	VDDQ	7
8	NC	DQ46	DQ48	GND													GND	NC	DQ45	DQ43	8
9	DQ40	DQ42	VDDQ	DQ44					GND	GND	GND	GND					DQ41	DQ39	VDD	DQ37	9
10	VDD	NC	DQ36	DQ38					GND	GND	GND	GND					VDDQ	DQ35	DQ33	DQ31	10
11	VDDQ	DQ34	DQ32	DQ30	LEFT				GND	GND	GND	GND				RIGHT	VDDQ	NC	DQ29	VDD	11
12	NC	DQ28	VDDQ	DQ26					GND	GND	GND	GND					NC	DQ23	DQ25	DQ27	12
13	DQ24	VDD	DQ20	GND													GND	DQ19	VDDQ	DQ21	13
14	DQ22	DQ16	DQ14	VDDQ													VDDQ	NC	DQ15	DQ17	14
15	VDD	DQ18	VDDQ	DQ6													DQ9	DQ11	DQ13	VDD	15
16	NC	DQ12	DQ8	DQ0						BOTTOM							DQ1	DQ5	DQ7	NC	16
17	DQ10	NC	VDDQ	GND	NC	CMD4	CMD2	GND	WE_L	CLK2X	VDD	SAD15	GND	VDDQ	SAD5	VDDQ	GND	NC	NC	VDDQ	17
18	DQ2	DQ4	VDD	SSF	CMD6	CMD3	CMD0	ALE_L	OE_L	SAD21	SAD18	SAD16	SAD12	SAD9	SAD7	SAD6	NC	SAD0	VDD	DQ3	18
19	NC	NC	NC	SSV	CMD5	CMD1	CMDV	VDDQ	PHS_L	VDDQ	SAD19	VDDQ	NC	SAD10	SAD11	NC	SAD4	SAD3	NC	NC	19
20	NC	NC	CMD8	CMD7	VDDQ	VDD	NC	CE_L	NC	VDD	SAD20	SAD17	SAD14	SAD13	VDD	SAD8	VDDQ	SAD2	SAD1	NC	20
	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 21-1. Pinout Diagram (Top View)

Table 21-1. Pinout Descriptions for Pinout Diagram

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
A1	NC		C4	DQ63	I/O
A2	NC		C5	DQ59	I/O
A3	DQ65	I/O	C6	DQ55	I/O
A4	DQ57	I/O	C7	VDDQ	3.3V/2.5V
A5	DQ53	I/O	C8	NC	
A6	VDD	1.8V	C9	DQ39	I/O
A7	VDDQ	3.3V/2.5V	C10	DQ35	I/O
A8	DQ43	I/O	C11	NC	
A9	DQ37	I/O	C12	DQ23	I/O
A10	DQ31	I/O	C13	DQ19	I/O
A11	VDD	1.8V	C14	NC	
A12	DQ27	I/O	C15	DQ11	I/O
A13	DQ21	I/O	C16	DQ5	I/O
A14	DQ17	I/O	C17	NC	
A15	VDD	1.8V	C18	SAD0	Output-T
A16	NC		C19	SAD3	Output-T
A17	VDDQ	3.3V/2.5V	C20	SAD2	Output-T
A18	DQ3	I/O	D1	ID0	Input
A19	NC		D2	TMS	Input
A20	NC		D3	TCK	Input
B1	NC		D4	GND	Ground
B2	VDD	1.8V	D5	DQ67	I/O
B3	NC		D6	VDDQ	3.3V/2.5V
B4	DQ61	I/O	D7	DQ47	I/O
B5	NC		D8	GND	Ground
B6	DQ49	I/O	D9	DQ41	I/O
B7	DQ51	I/O	D10	VDDQ	3.3V/2.5V
B8	DQ45	I/O	D11	VDDQ	3.3V/2.5V
B9	VDD	1.8V	D12	NC	
B10	DQ33	I/O	D13	GND	Ground
B11	DQ29	I/O	D14	VDDQ	3.3V/2.5V
B12	DQ25	I/O	D15	DQ9	I/O
B13	VDDQ	3.3V/2.5V	D16	DQ1	I/O
B14	DQ15	I/O	D17	GND	Ground
B15	DQ13	I/O	D18	NC	
B16	DQ7	I/O	D19	SAD4	Output-T
B17	NC		D20	VDDQ	3.3V/2.5V
B18	VDD	1.8V	E1	ID2	Input
B19	NC		E2	ID3	Input
B20	SAD1	Output-T	E3	ID1	Input
C1	TDO	Output-T	E4	TRST_L	Input
C2	TDI	Input	E17	VDDQ	3.3V/2.5V
C3	NC		E18	SAD6	Output-T

Table 21-1. Pinout Descriptions for Pinout Diagram (continued)

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
E19	NC		L2	BHO1	Output
E20	SAD8	Output-T	L3	BHO2	Output
F1	VDD	1.8V	L4	FULI0	Input
F2	LHI2	Input	L17	CLK2X	Input
F3	LHI0	Input	L18	SAD21	Output-T
F4	ID4	Input	L19	VDDQ	3.3V/2.5V
F17	SAD5	Output-T	L20	VDD	1.8V
F18	SAD7	Output-T	M1	FULI1	Input
F19	SAD11	Output-T	M2	FULI2	Input
F20	VDD	1.8V	M3	VDDQ	3.3V/2.5V
G1	NC		M4	FULI3	Input
G2	LHI3	Input	M17	WE_L	Output-T
G3	VDDQ	3.3V/2.5V	M18	OE_L	Output-T
G4	LHI1	Input	M19	PHS_L	Input
G17	VDDQ	3.3V/2.5V	M20	NC	
G18	SAD9	Output-T	N1	FULI4	Input
G19	SAD10	Output-T	N2	FULI6	Input
G20	SAD13	Output-T	N3	NC	
H1	LHI6	Input	N4	GND	Ground
H2	LHI5	Input	N17	GND	Ground
H3	LHI4	Input	N18	ALE_L	Output-T
H4	GND	Ground	N19	VDDQ	3.3V/2.5V
H17	GND	Ground	N20	CE_L	Output-T
H18	SAD12	Output-T	P1	FULI5	Input
H19	NC		P2	NC	
H20	SAD14	Output-T	P3	NC	
J1	BHI0	Input	P4	FULO0	Output
J2	VDDQ	3.3V/2.5V	P17	CMD2	Input
J3	LHO1	Output	P18	CMD0	Input
J4	LHO0	Output	P19	CMDV	Input
J17	SAD15	Output-T	P20	NC	
J18	SAD16	Output-T	R1	VDD	1.8V
J19	VDDQ	3.3V/2.5V	R2	FULO1	Output
J20	SAD17	Output-T	R3	VDDQ	3.3V/2.5V
K1	VDD	1.8V	R4	NC	
K2	BHI2	Input	R17	CMD4	Input
K3	VDD	1.8V	R18	CMD3	Input
K4	BHI1	Input	R19	CMD1	Input
K17	VDD	1.8V	R20	VDD	1.8V
K18	SAD18	Output-T	T1	NC	
K19	SAD19	Output-T	T2	NC	
K20	SAD20	Output-T	T3	VDD	1.8V
L1	BHO0	Output	T4	RSTL	Input

Table 21-1. Pinout Descriptions for Pinout Diagram (continued)

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
T17	NC		V20	CMD8	Input
T18	CMD6	Input	W1	GND	Ground
T19	CMD5	Input	W2	NC	
T20	VDDQ	3.3V/2.5V	W3	NC	
U1	NC		W4	NC	
U2	FULL	Output	W5	VDDQ	3.3V/2.5V
U3	VDDQ	3.3V/2.5V	W6	NC	
U4	GND	Ground	W7	VDDQ	3.3V/2.5V
U5	DQ66	I/O	W8	DQ46	I/O
U6	DQ58	I/O	W9	DQ42	I/O
U7	DQ54	I/O	W10	NC	
U8	GND	Ground	W11	DQ34	I/O
U9	DQ44	I/O	W12	DQ28	I/O
U10	DQ38	I/O	W13	VDD	1.8V
U11	DQ30	I/O	W14	DQ16	I/O
U12	DQ26	I/O	W15	DQ18	I/O
U13	GND	Ground	W16	DQ12	I/O
U14	VDDQ	3.3V/2.5V	W17	NC	
U15	DQ6	I/O	W18	DQ4	I/O
U16	DQ0	I/O	W19	NC	
U17	GND	Ground	W20	NC	
U18	SSF	Output-T	Y1	NC	
U19	SSV	Output-T	Y2	NC	
U20	CMD7	Input	Y3	DQ64	I/O
V1	EOT	Output-T	Y4	DQ62	I/O
V2	ACK	Output-T	Y5	DQ60	I/O
V3	NC		Y6	VDD	1.8V
V4	VDD	1.8V	Y7	DQ50	I/O
V5	NC		Y8	NC	
V6	DQ56	I/O	Y9	DQ40	I/O
V7	DQ52	I/O	Y10	VDD	1.8V
V8	DQ48	I/O	Y11	VDDQ	3.3V/2.5V
V9	VDDQ	3.3V/2.5V	Y12	NC	
V10	DQ36	I/O	Y13	DQ24	I/O
V11	DQ32	I/O	Y14	DQ22	I/O
V12	VDDQ	3.3V/2.5V	Y15	VDD	1.8V
V13	DQ20	I/O	Y16	NC	
V14	DQ14	I/O	Y17	DQ10	I/O
V15	VDDQ	3.3V/2.5V	Y18	DQ2	I/O
V16	DQ8	I/O	Y19	NC	
V17	VDDQ	3.3V/2.5V	Y20	NC	
V18	VDD	1.8V	J9	GND	Ground
V19	NC		J10	GND	Ground

Table 21-1. Pinout Descriptions for Pinout Diagram (continued)

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
J11	GND	Ground	L10	GND	Ground
J12	GND	Ground	L11	GND	Ground
K9	GND	Ground	L12	GND	Ground
K10	GND	Ground	M9	GND	Ground
K11	GND	Ground	M10	GND	Ground
K12	GND	Ground	M11	GND	Ground
L9	GND	Ground	M12	GND	Ground

22.0 Ordering Information

Table 22-1 provides ordering information.

Table 22-1. Ordering Information

Part Number	Description	Frequency	Temperature Range
CYNSE70032-66BGC	Search Engine	66 MHz	Commercial
CYNSE70032-66BGI	Search Engine	66 MHz	Industrial
CYNSE70032-83BGC	Search Engine	83 MHz	Commercial

23.0 Package Diagrams

272-Lead Ball Grid Array (27 × 27 × 2.33 mm) BG272

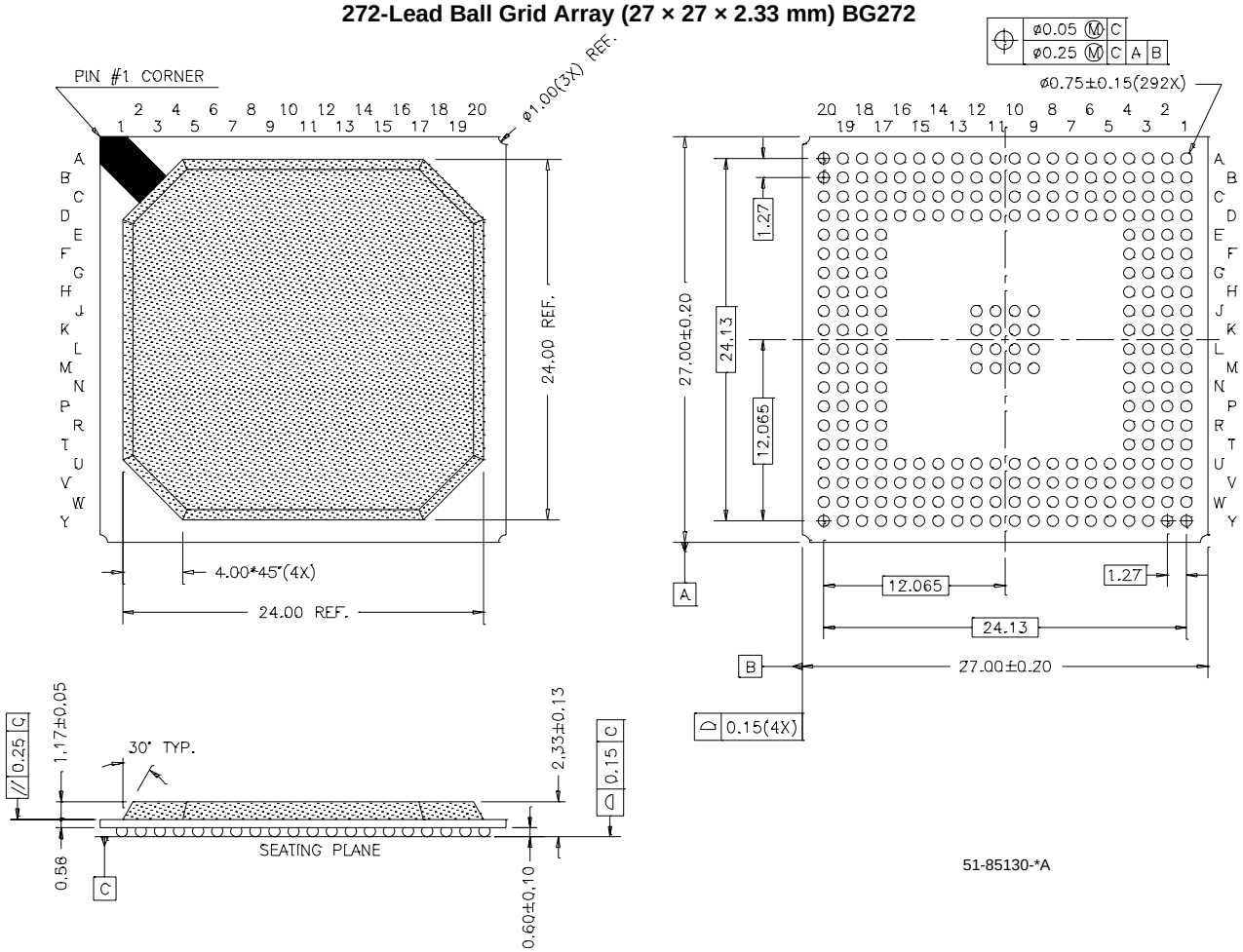


Figure 23-1. Package

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Document History Page

Document Title: CYNSE70032 Network Search Engine Document Number: 38-02042				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111441	02/12/02	AFX	New Data Sheet
*A	116611	07/10/02	OOR	Added industrial temp parts
*B	118152	9/19/02	OOR	Added power section that covers the power-up sequence Updating JTAG section with supported operations table
*C	121027	12/17/02	ED	Added note to power-up sequence instructions Removed CYNSE70128-/256-specific power-up instructions Removed Alternative power-up sequence from TOC Removed references to Alternative power-up sequence instructions including timing *Figure 16-1*
*D	123685	02/20/03	KOS	Removed TEST from Signal Description *Table 5-1* Add Pin A10 to the pinout descriptions *Table 21-1* Add ”Output-T” in the Signal Type field of the Pin E18 *Table 21-1* Change F1 Signal Name and Type from VDDQ to VDD and 3.3V/2.5V to 1.8V *Table 21-1* Add “1.8V” in the Signal Type field of Pin F20 *Table 21-1* Change U6 Package Ball Number from U6I/O to U6 *Table 21-1* Re-order the pinouts list *Table 21-1*
*E	126019	05/07/03	ITL	Updated *Figure 16-1* on page 114 to relect the correct waveforms. Also corrected the power-up sequence description above the figure.