16-Mb Static RAM with ECC and RADSTOP™ technology

2M × 8

Radiation performance

- Radiation data
  - Total dose = 200 **Krad**
  - Embedded error-correcting code (ECC) for single-bit error correction[1, 2]
  - Soft error rate (both heavy ion and proton) Heavy ions ≤ 1×10^{-10} upsets/bit-day
  - **Neutron** = 1.5×10^{11} N/cm^2
  - Dose rate:
    - ≥ 3.0×10^8 (rad(Si)/s) (R/W)
    - ≥ 2.0×10^9 (rad(Si)/s) (Static)
  - Latch up immunity > 60 MeV.cm^2/mg (95°C)
- Processing flows
  - V Grade - Class V flow in compliance with MIL-PRF 38535
- Prototyping options
  - CYPT1069G prototype units with same functional and timing as flight units using non-radiation hardened die in a 36-pin ceramic flat package

Features

- Temperature ranges
  - Military/Space: –55°C to 125°C
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 90 mA at 10 ns (typical)
- Low CMOS standby power
  - I_{SB2} = 20 mA (typical)
- 1.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Gold plated lead 36-pin ceramic flat package

Notes
1. This device does not support automatic write-back on error detection.
2. SER FIT Rate < 0.1 FIT/Mb. Refer **AN88889** or details.

Block diagram

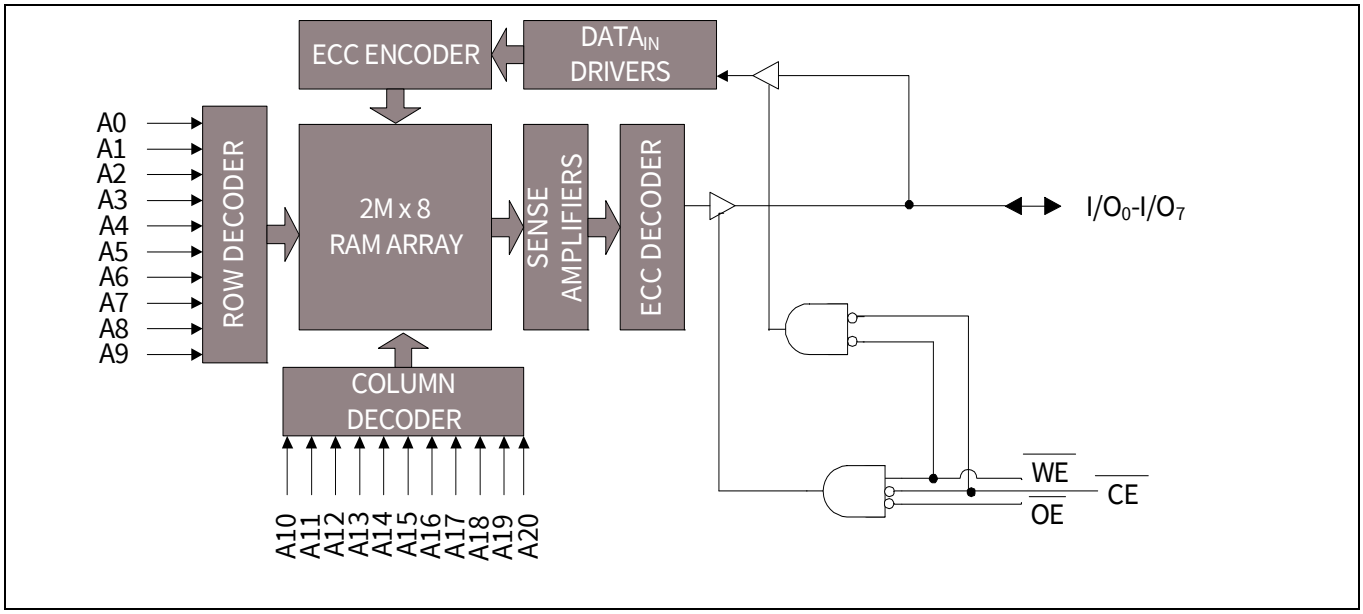


Table of contents

1 Functional description

The CYRS1069G is a high-performance complementary metal oxide semiconductor (CMOS) static RAM organized as 2M words by 8 bits with RADSTOP™ technology. Infineon state-of-the-art RADSTOP™ technology is radiation hardened through proprietary design and process hardening techniques. The 16-Mbit fast asynchronous SRAM with RADSTOP technology is also QML V certified with Defense Logistics Agency Land and Maritime (DLAM).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See the **"Truth table"** on page 18 for a complete description of read and write modes.

The eight input or output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW)

The CYRS1069G is available in a ceramic 36-pin flat package with center power and ground (revolutionary) pinout.

For best practice recommendations, refer to the application note **AN1064, SRAM system guidelines**.

2 Selection guide

Table 1 Selection guide

Description	3.3 V / 5.0 V	Unit
Maximum access time	10	ns
Maximum operating current	160	mA
Maximum CMOS standby current	50	mA

3 Pin configuration

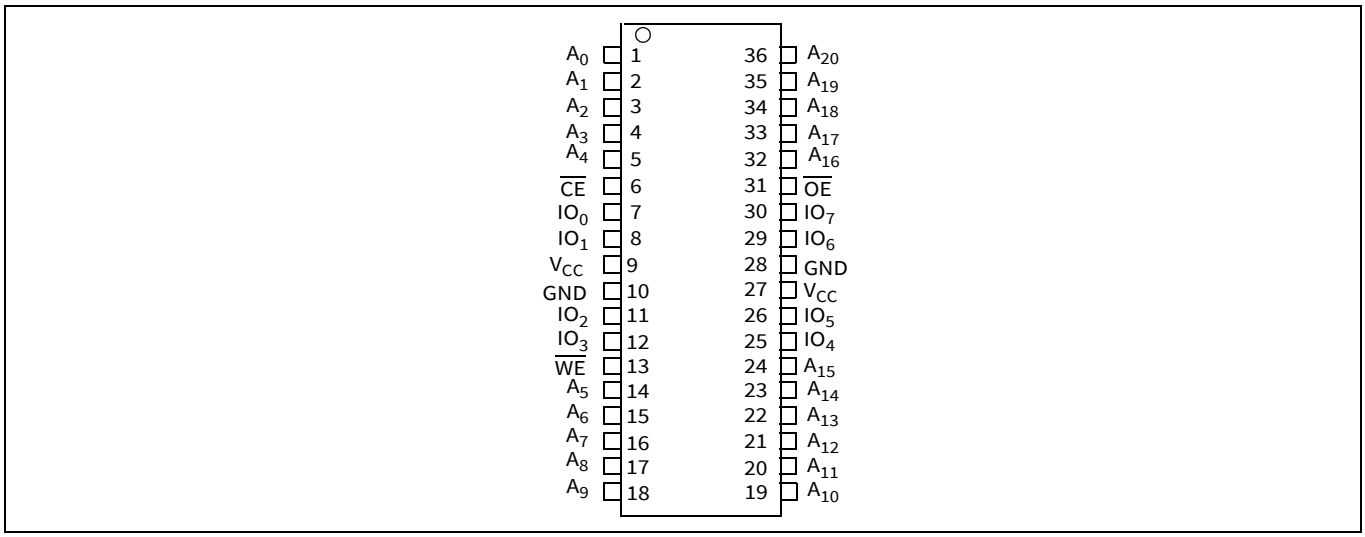


Figure 1 36-pin ceramic flat package pinout (top view) [3]

Note
3. NC pins are not connected on the die.

4 Maximum ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Table 2 Maximum ratings

Parameter	Max ratings
Storage temperature	–65°C to +150°C
Ambient temperature with power applied	–55°C to +125°C
Supply voltage on V_{CC} relative to GND [4]	–0.5 V to +6.0 V
DC voltage applied to outputs in High Z state [4]	–0.5 V to V_{CC} + 0.5 V
DC input voltage [4]	–0.5 V to V_{CC} + 0.5 V
Current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch up current	> 140 mA

Note
4. Tested initially and after any design or process changes that may affect these parameters.

5 Operating range

Table 3 Operating range

Range	Ambient temperature	V_{CC}	Speed
Military/Space	–55°C to +125°C	2.2 V to 3.6 V 4.5 V to 5.5 V	10 ns 10 ns

6 DC electrical characteristics

Table 4 DC electrical characteristics

Over the operating range

Parameter	Voltage description	Test conditions		Military/Space		Unit
				Min	Max	
V_{OH}	Output HIGH	V_{CC} = Min, I_{OH} = –1.0 mA	2.2 V to 2.7 V	2.0	–	V
		V_{CC} = Min, I_{OH} = –4.0 mA	2.7 V to 3.0 V	2.2	–	
		V_{CC} = Min, I_{OH} = –4.0 mA	3.0 V to 3.6 V	2.4	–	
		V_{CC} = Min, I_{OH} = –4.0 mA	4.5 V to 5.5 V	2.4	–	
		V_{CC} = Min, I_{OH} = –0.1 mA	4.5 V to 5.5 V	V_{CC} – 0.4	–	
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 2 mA	2.2 V to 2.7 V	–	0.4	V
		V_{CC} = Min, I_{OL} = 8 mA	2.7 V to 3.6 V	–	0.4	
		V_{CC} = Min, I_{OL} = 8 mA	4.5 V to 5.5 V	–	0.4	
V_{IH}	Input HIGH voltage		2.2 V to 2.7 V	2.0	V_{CC} + 0.3	V
			2.7 V to 3.6 V	2.0	V_{CC} + 0.3	
			4.5 V to 5.5 V	2.0	V_{CC} + 0.5	
V_{IL}	Input LOW voltage		2.2 V to 2.7 V	–0.3	0.6	V
			2.7 V to 3.6 V	–0.3	0.8	
			4.5 V to 5.5 V	–0.5	0.8	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, output disabled		–5	+5	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = 1/t_{RC}	100 MHz	–	160	mA
			83 MHz	–	130	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	60	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V V_{IN} ≥ V_{CC} – 0.2 V, or V_{IN} ≤ 0.2 V, f = 0		–	50	mA

7 Capacitance

Table 5 Capacitance

Parameter [5]	Description	Test conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25°C, f = 1\,MHz, V_{CC} = 3.3\,V$	10	pF
C_{OUT}	I/O capacitance		10	pF

Note
5. Tested initially and after any design or process changes that may affect these parameters.

8 Thermal resistance

Table 6 Thermal resistance

Parameter [6]	Description	Test conditions	Ceramic flat package	Unit
Θ_{JC}	Thermal resistance (junction to case)	Test according to MIL-PRF 38538	1.6	°C/W

Note
6. Tested initially and after any design or process changes that may affect these parameters.

9 AC test loads and waveforms

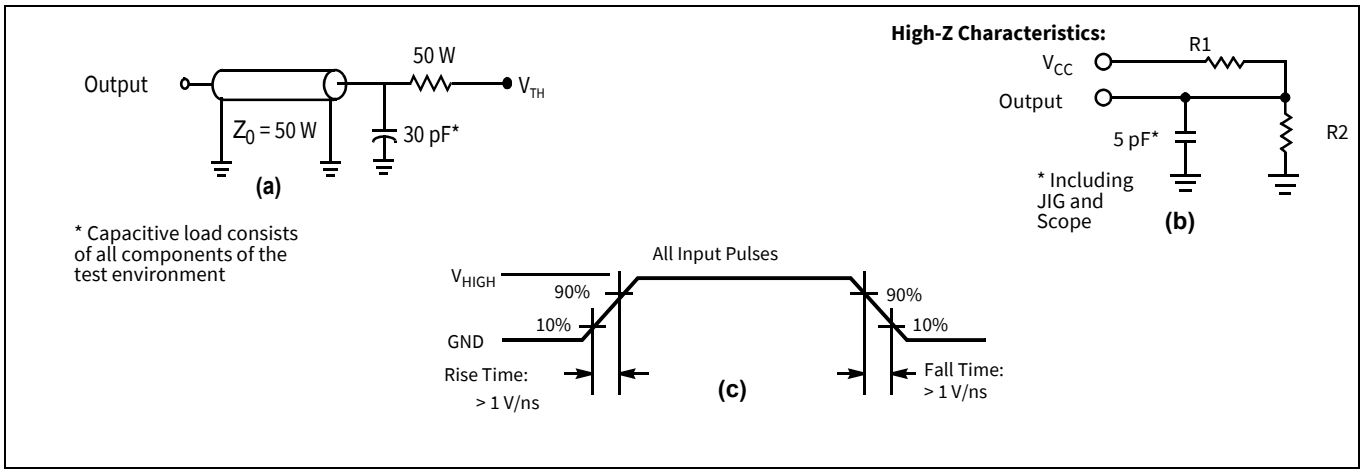


Figure 2 AC test loads and waveforms[7]

Parameters	3.0 V	5.0 V	Unit
R1	317	317	Ω
R2	351	351	Ω
V_{TH}	1.5	1.5	V
V_{HIGH}	3	3	V

Note
7. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC}(min) and 100-µs wait time after V_{CC} stabilization.

10 Data retention

10.1 Data retention characteristics

Table 7 Data retention characteristics

Over the operating range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC}=V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	50.0	mA
t_{CDR}[8]	Chip deselect to data retention time	–	0	–	ns
t_R[8, 9]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	ns
		$V_{CC} < 2.2$ V	12.0	–	ns

10.2 Data retention waveform

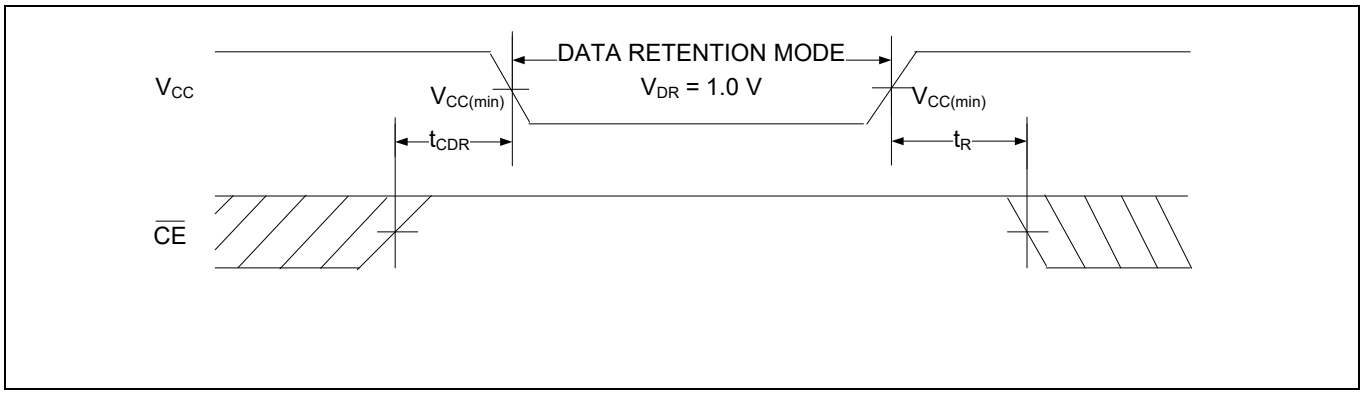


Figure 3 Data retention waveform

Notes

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

11 AC switching characteristics

Table 8 AC switching characteristics

Over the Operating Range

Parameter [10]	Description	10ns		Unit
		Min	Max	
Read cycle				
t_{power}	V_{CC} (typical) to the first access [11, 12]	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	
t_{OHA}	Data hold from address change	3	–	
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	
t_{LZOE}	$\overline{OE}$ LOW to Low Z [13, 14, 15]	0	–	
t_{HZOE}	$\overline{OE}$ HIGH to High Z [13, 14, 15]	–	5	
t_{LZCE}	$\overline{CE}$ LOW to Low Z [13, 14, 15]	3	–	
t_{HZCE}	$\overline{CE}$ HIGH to High Z [13, 14, 15]	–	5	
t_{PU}	$\overline{CE}$ LOW to Power-up [12]	0	–	
t_{PD}	$\overline{CE}$ HIGH to Power-down [12]	–	10	
Write cycle [14, 15]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [12]	7	–	
t_{AW}	Address setup to write end	7	–	
t_{HA}	Address hold from write end	0	–	
t_{SA}	Address setup to write start	0	–	
t_{PWE}	$\overline{WE}$ pulse width	7	–	
t_{SD}	Data setup to write end	5	–	
t_{HD}	Data hold from write end	0	–	
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [13, 14, 15]	3	–	
t_{HZWE}	$\overline{WE}$ LOW to High Z [13, 14, 15]	–	5	

Notes

10. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of **Figure 2**, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
12. These parameters are guaranteed by design and are not tested.
13. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of **Figure 2**. Transition is measured ±200 mV from steady state voltage.
14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
15. Tested initially and after any design or process changes that may affect these parameters.

12 Switching waveforms

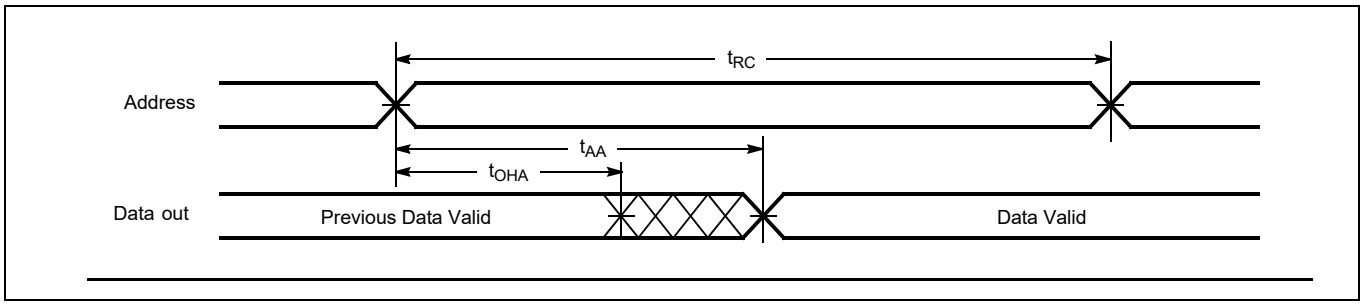


Figure 4 Read cycle No. 1[16, 17]

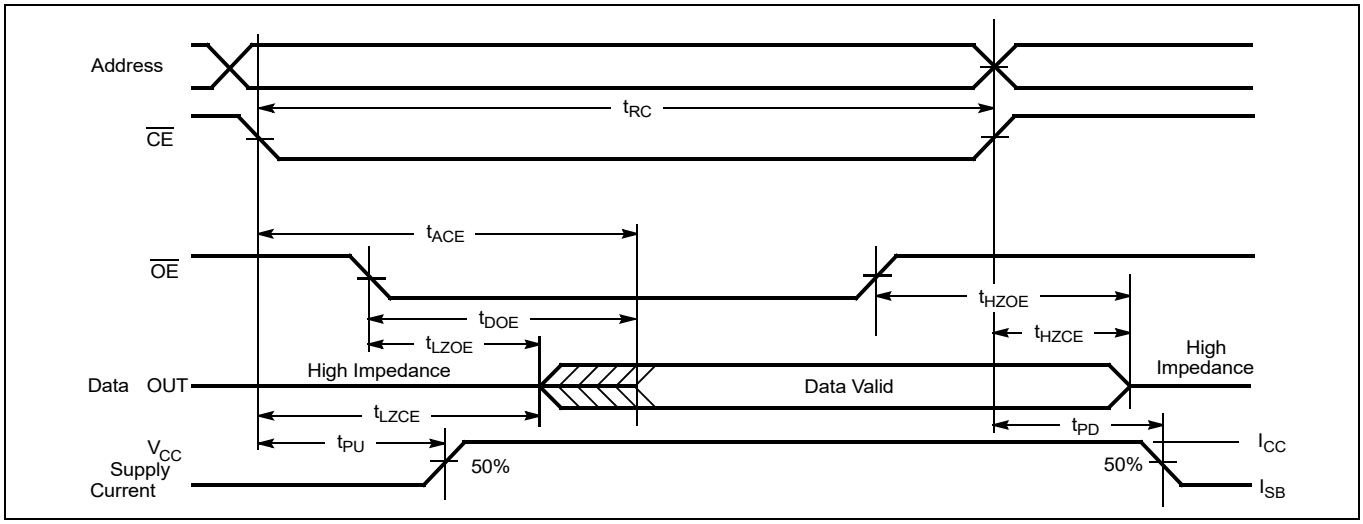


Figure 5 Read cycle No. 2 ($\overline{OE}$ Controlled, $\overline{WE}$ HIGH)[18, 19]

Notes
16. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching waveforms

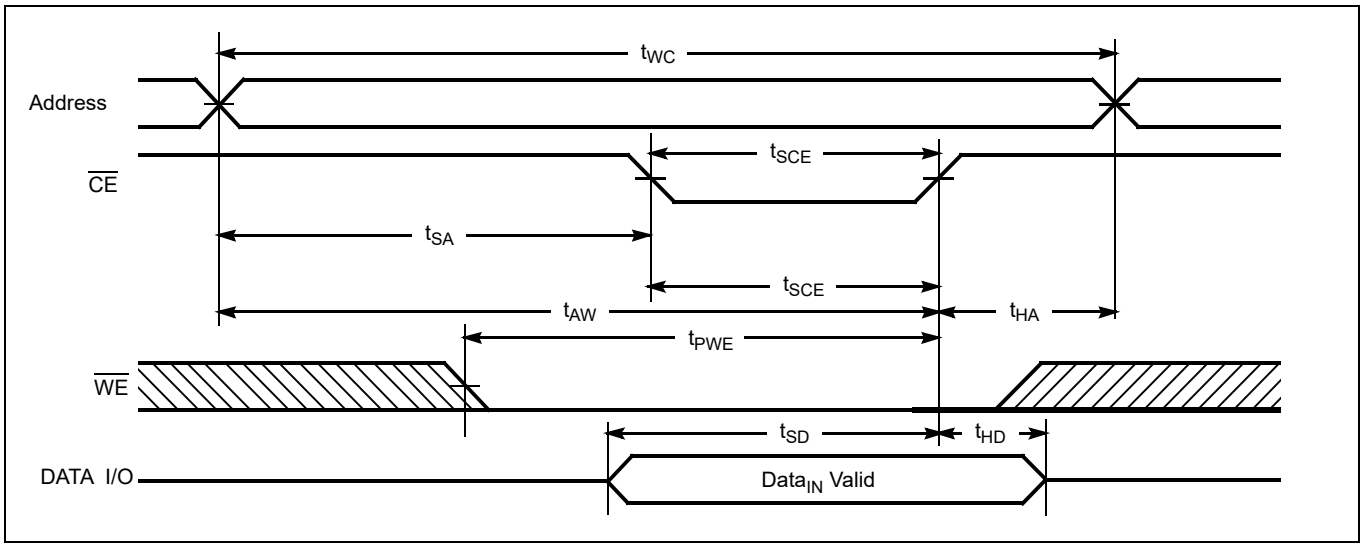


Figure 6 Write cycle No. 1 ($\overline{CE}$ Controlled)[20, 21]

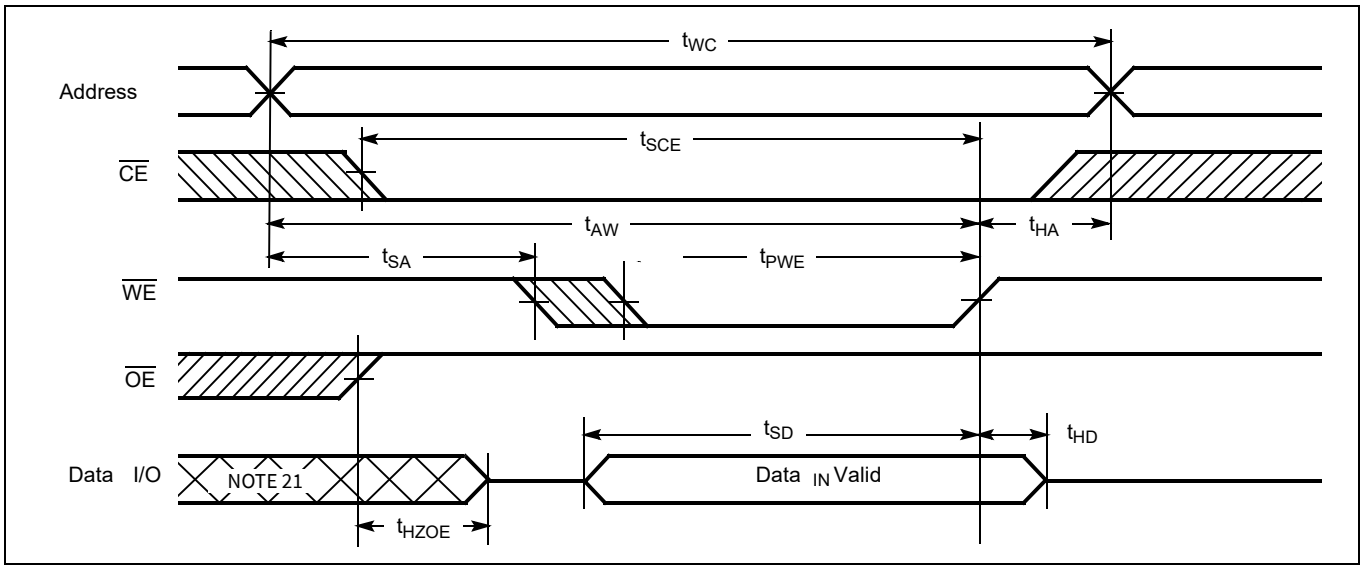


Figure 7 Write cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH)[20, 21, 22]

Notes

20. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
22. The minimum write cycle width should be sum of t_{HZWE} and t_{SD}.

Switching waveforms

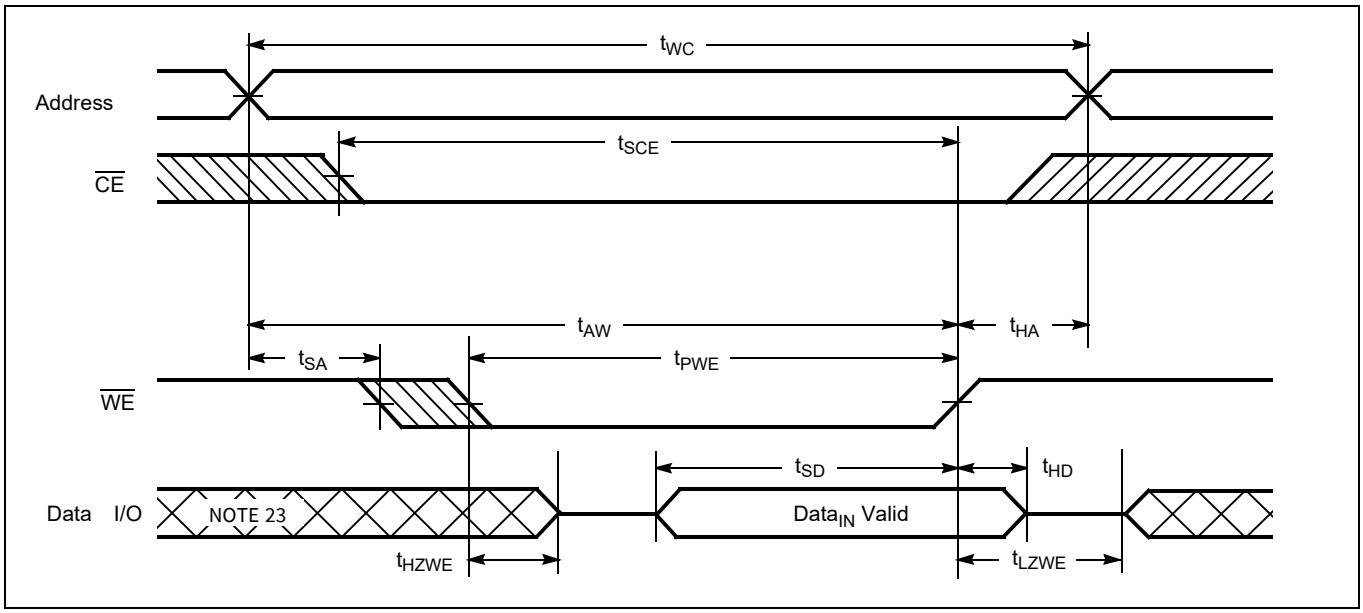


Figure 8 Write cycle No. 3 (WE Controlled, OE LOW)

Note
23.During this period the I/Os are in the output state and input signals should not be applied.

13 Truth table

Table 9 Truth table

CE	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB1} or I_{SB2})
L	L	H	Data out	Read	Active (I_{CC})
L	X	L	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs disabled	Active (I_{CC})

14 Ordering information

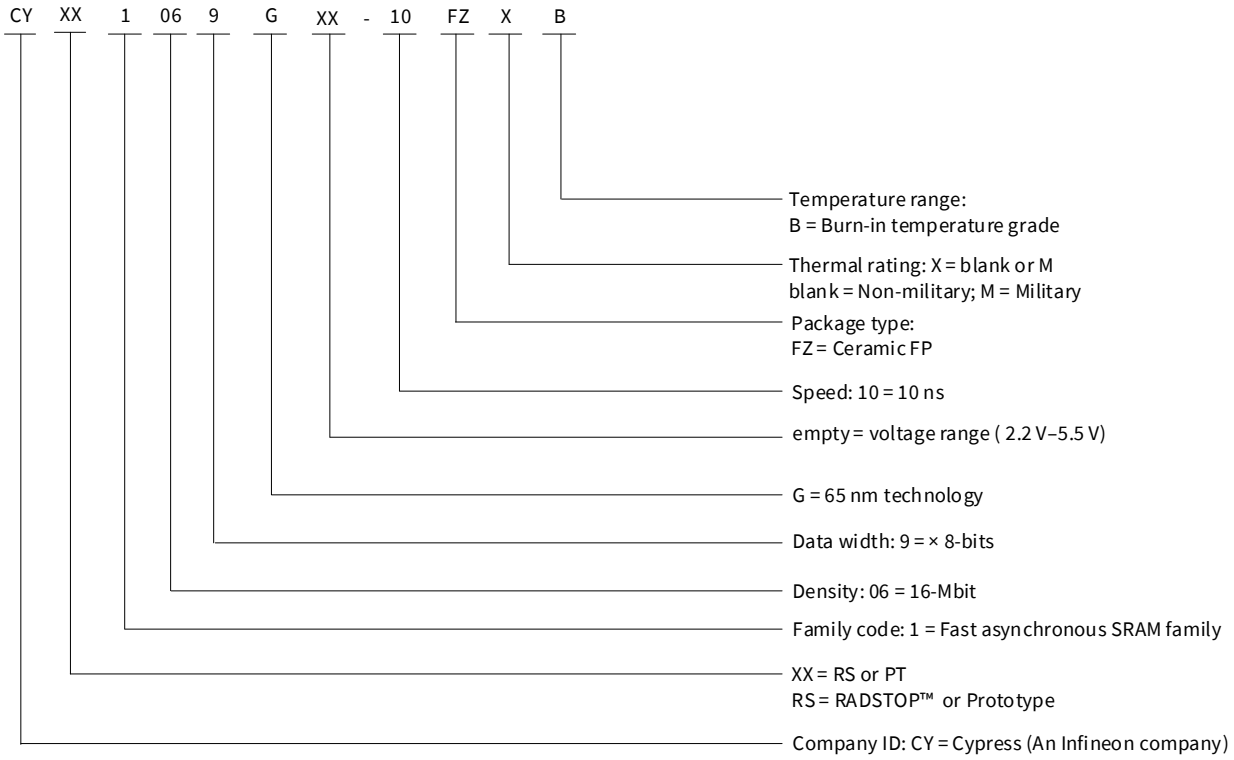
The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Infineon website at **www.infineon.com**. Infineon maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors.

Table 10 Ordering information

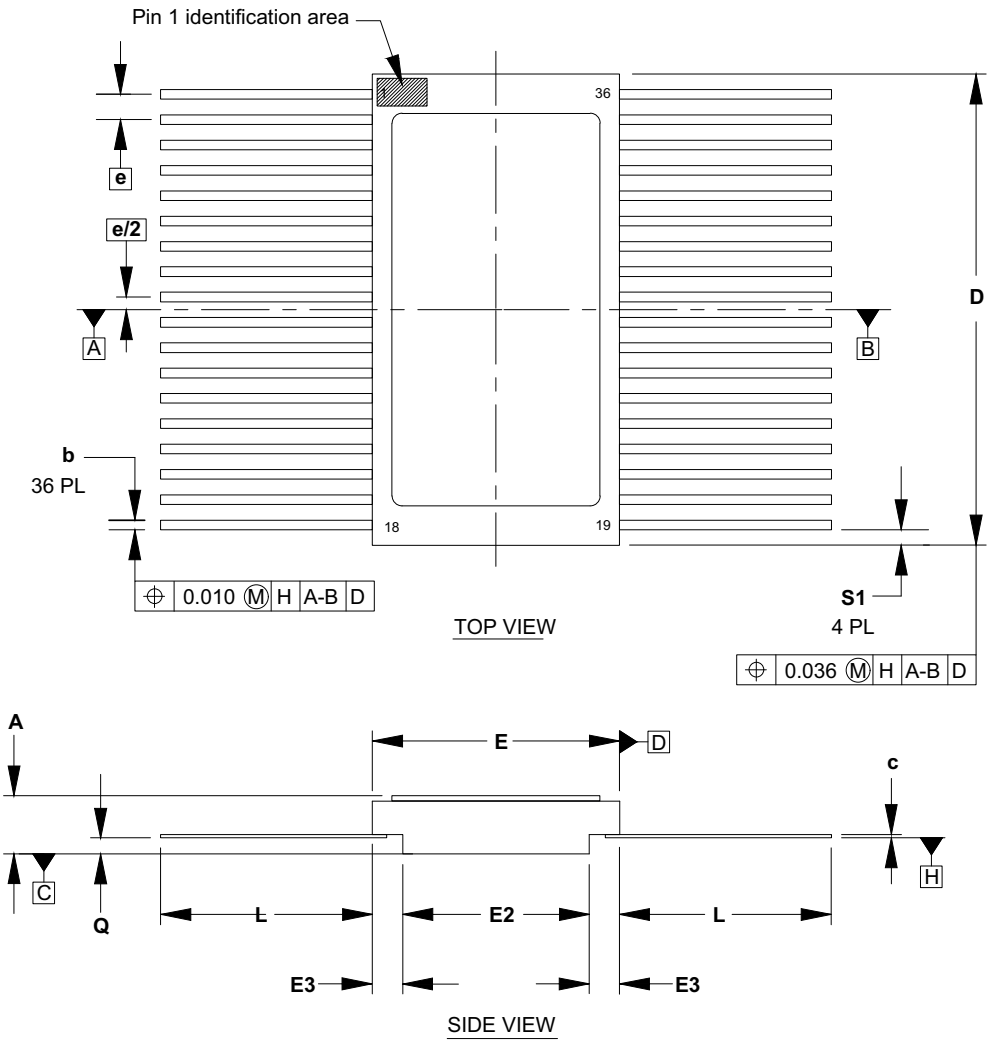
Speed (ns)	Ordering code	Package diagram	Package type	Operating range
10	CYRS1069G30-10FZMB	001-67583	36-pin ceramic flat package	Military
	CYPT1069G30-10FZMB		36-pin ceramic flat package, prototype part	
	5962R2020202VXC		36-pin ceramic flat package, QML-V certified	

Contact your local Infineon sales representative for availability of these parts

14.1 Ordering code definitions



15 Package diagram



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	-	-	2.95
b	0.38	-	0.48
c	0.08	-	0.18
D	23.12	23.37	23.62
E	11.99	12.19	13.08
E2	9.78	-	10.04
E3	1.52 BSC		
e	1.27 BSC		
L	8.89	-	10.64
Q	0.64	-	-
S1	0.68 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL EXPOSED METAL AND METALIZED AREAS SHALL BE GOLD PLATED PER MIL-PRF-38535.
3. LEAD FINISH IS IN ACCORDANCE WITH MIL-PRF-38535.
4. PACKAGE MATERIAL: OPAQUE 90% MINIMUM ALUMINA CERAMIC.

001-67583 *E

Figure 9 36-lead ceramic flat pack (23.37 × 12.19 × 2.95 mm) F36/FZ36 package outline (CG-FP-36), 001-67583

16 Acronyms

Table 11 Acronyms used in this document

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
DLAM	Defense Logistics Agency Land and Maritime
DNU	Do Not Use
EDAC	Error Detection and Correction
I/O	Input/Output
LET	Linear Energy Transfer
OE	Output Enable
QML	Qualified Manufacturers List
SEC-DED	Single Error Correction – Double Error Detection
SEL	Single-Event Latch-up
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
WE	Write Enable

See the **"Glossary"** on page 23 for definitions of terms used in this document.

17 Document conventions

17.1 Units of measure

Table 12 Unit of measure

Symbol	Unit of measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

18 Glossary

Table 13 Glossary

Glossary	Description
Total Dose	Permanent device damage due to ions over device life
Heavy Ion	Instantaneous device latch up due to single ion
LET	Linear energy transfer (measured in MeVcm^2)
Krad	Unit of measurement to determine device life in radiation environments.
Neutron	Permanent device damage due to energetic neutrons or protons
Prompt Dose	Data loss of permanent device damage due to X-rays and gamma rays <20 ns
RADSTOP™ technology	Infineon patented Rad Hard design methodology
QML V	Space level certification from DSCC.
DLAM	Defense Logistics Agency Land and Maritime
LSBU	Logical Single Bit Upset. Single bits in a single correction word are in error.
LMBU	Logical Multi Bit Upset. Multiple bits in a single correction word are in error

Revision history

Document version	Date of release	Description of changes
*B	2023-11-06	Post to external web.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-11-06
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-34202 Rev. *B

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.