TRAVEO™ T2G 32-bit Automotive MCU

Based on Arm® Cortex®-M7 dual

General description

CYT4DN is a family of TRAVEO™ T2G microcontrollers targeted at automotive systems such as instrument clusters and Head-Up Displays (HUD). CYT4DN has a 2D Graphics engine, Sound Processing, two Arm® Cortex®-M7 CPUs for primary processing, and an Arm® Cortex®-M0+ CPU for peripheral and security processing. These devices contain embedded peripherals supporting controller area network with flexible data rate (CAN FD), local interconnect network (LIN), clock extension peripheral interface (CXPI), and Gigabit Ethernet. TRAVEO™ T2G devices are manufactured on an advanced 40-nm process. CYT4DN incorporates a low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

Features

- **Graphics subsystem**
  - Supports 2D and 2.5D (perspective warping, 3D effects) graphics rendering
  - 40-bit for internal processing (RGBA 10-bit per color channel)
  - 24-bit for interfaces (RGB 8-bit per color channel)
  - 4096 KB of embedded video RAM memory (VRAM)
  - Up to two video output interfaces supporting two displays from
    - Parallel RGB (max display size: 1600 × 600 at 80 MHz)
    - FPD-link single (max display size: 1920 × 720 at 110 MHz)
    - FPD-link dual (max display size: 2880 × 1080 at 220 MHz)
  - One Capture engine for video input processing for ITU 656 or parallel RGB/YUV or MIPI CSI-2 input
    - ITU656 (standard camera capture: up to 800 × 480)
    - RGB (max capture size 1600 × 600 at 80 MHz) or
    - Two-/four-lane MIPI CSI-2 interface (max capture size: 1920 × 720 for two lanes at 110 MHz, 2880 × 1080 for four lanes at 220 MHz)
  - Display warping on-the-fly for HUD applications
  - Direct video feed through from capture to display interface with graphics overlay
  - Composition engine for scene composition from display layers
  - Display engine for video timing generation and display functions
  - Drawing engine for acceleration of vector graphics rendering
  - Command sequencer for setup and control of the rendering process
  - Supports graphics rendering without frame buffers (on-the-fly to both displays)
  - Dual-channel FPD-Link interface for up to Wide-HD resolution video output
  - JPEG Decoder
    - Decodes JPEG images of various formats into pixel data with conformance to a subset of standard ISO/IEC10918-1
    - Color spaces supporting RGB/YUV/Grayscale
    - Supports YUV sub-sampling 4:4:4/4:2:2/4:1:1/4:2:0
    - Image size between 1×1 to 16384×16384 pixels
- **Sound subsystem**
  - Four time-division multiplexing (TDM) interfaces
  - Two pulse-code modulation-pulse width modulation (PCM-PWM) interfaces
  - Up to five sound generator (SG) interfaces
  - Two PCM Audio stream mixers with five input streams
  - One audio digital-to-analog converter (DAC)

Errata: For information on silicon errata, see **"Errata"** on page 195. Details include trigger conditions, devices affected, and proposed workaround.

- **CPU subsystem**
  - Two 320-MHz 32-bit Arm® Cortex®-M7 CPUs, each with
    - Single-cycle multiply
    - Single/double-precision floating point unit (FPU)
    - 16-KB data cache, 16-KB instruction cache
    - Memory protection unit (MPU)
    - 64-KB instruction and 64-KB data Tightly-Coupled Memories (TCM)
  - One 100-MHz 32-bit Arm® Cortex®-M0+ CPU with
    - Single-cycle multiply
    - Memory protection unit
  - Inter-processor communication in hardware
  - Three DMA controllers
    - Peripheral DMA controller #0 (P-DMA0) with 76 channels
    - Peripheral DMA controller #1 (P-DMA1) with 84 channels
    - Memory DMA (AHB) controller (M-DMA0) with 8 channels
    - Memory DMA (AXI) controller (M-DMA1) with 4 channels
- **Integrated memories**
  - 6336-KB code-flash with an additional 128-KB of work-flash
    - Read-While-Write (RWW) allows updating the code-flash/work-flash while executing from it
    - Single- and dual-bank modes (specifically for Firmware update Over The Air [FOTA])
    - Flash programming through SWD/JTAG interface
  - 640-KB of SRAM with selectable retention granularity
- **Crypto engine**[1]
  - Supports Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM)
  - Secure boot and authentication
    - Using digital signature verification[1]
    - Using fast secure boot
  - AES: 128-bit blocks, 128-/192-/256-bit keys
  - 3DES[1]: 64-bit blocks, 64-bit key
  - Vector unit[1] supporting asymmetric key cryptography such as Rivest-Shamir-Adleman (RSA) and Elliptic Curve (ECC)
  - SHA-1/2/3[1]: SHA-512, SHA-256, SHA-160 with variable length input data
  - CRC[1]: supports CCITT CRC16 and IEEE-802.3 CRC32
  - True random number generator (TRNG) and pseudo random number generator (PRNG)
  - Galois/Counter Mode (GCM)
- **Functional safety for ASIL-B**
  - Memory protection unit (MPU)
  - Shared memory protection unit (SMPU)
  - Peripheral protection unit (PPU)
  - Watchdog timer (WDT)
  - Multi-counter watchdog timer (MCWDT)
  - Low-voltage detector (LVD)
  - Brown-out detection (BOD)
  - Over-voltage detection (OVD)
  - Overcurrent detection (OCD)
  - Clock supervisor (CSV)
    - Supported in all power modes
  - Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash, TCM)

Note
1. The Crypto engine features are available on select MPNs.

- **Low-power 2.7-V to 5.5-V operation**
  - Low-power Active, Sleep, Low-power Sleep, DeepSleep, and Hibernate modes for fine-grained power management
  - Configurable options for robust BOD
    - Two threshold levels (2.7 V and 3.0 V) for BOD on V_{DDD} and V_{DDA_ADC}
    - One threshold level (1.1 V) for BOD on V_{CCD}
- **Wakeup support**
  - Up to 10 pins to wakeup from Hibernate mode
  - Wakeup recognition bit for each wakeup source
  - Up to 81 GPIO pins to wakeup from DeepSleep mode
  - Event Generator, SCB, Watchdog Timer, RTC alarms to wake from DeepSleep modes
- **Clocks**
  - Internal main oscillator (IMO)
  - Internal low-speed oscillator (ILO)
  - External crystal oscillator (ECO)
  - Watch crystal oscillator (WCO)
  - Phase-locked loop (PLL)
  - Frequency-locked loop (FLL)
  - Low-power external crystal oscillator (LPECO)
- **Communication interfaces**
  - Up to four CAN FD channels
    - Increased data rate (up to 8 Mbps) compared to classic CAN, limited by physical layer topology and transceivers
    - Compliant to ISO 11898-1:2015
    - Supports all the requirements of Bosch CAN FD Specification V1.0 non-ISO CAN FD
    - ISO 16845:2015 certificate available
  - Up to 12 runtime-reconfigurable SCB (serial communication block) channels, each configurable as I^2C, SPI, or UART
  - Up to two independent LIN channels
    - LIN protocol compliant with ISO 17987
  - Up to two CXPI channels with data rate up to 20 kbps
  - 10/100/1000 Mbps Ethernet MAC interface conforming to IEEE-802.3az
    - Supports the following PHY interfaces:
      Media-independent interface (MII)
      Reduced media-independent interface (RMII)
      Reduced gigabit media-independent interface (RGMII)
    - Compliant with IEEE-802.1AS, IEEE-802.1Qav, and IEEE-802.1Qbb for audio video bridging (AVB)
    - Compliant with IEEE-1588 precision time protocol (PTP)
- **Serial memory interface (SMIF)**
  - Two SPIs (single, dual, quad, or octal), xSPI interface
  - On-the-fly encryption and decryption
  - Execute-In-Place (XIP) from external memory
- **Timers**
  - Up to 50 16-bit and 32 32-bit Timer/Counter Pulse-Width modulator (TCPWM) blocks for regular operations
    - Up to 12 16-bit counters optimized for motor-control operations (Equivalent to 6 stepper motor-control [SMC] channels with ZPD and slew rate control capability)
    - Supports timer, capture, quadrature decoding, pulse-width modulation (PWM), PWM with dead time (PW-M_DT), pseudo-random PWM (PWM_PR), and shift-register (SR) modes
  - Up to 16 Event Generation (EVTGEN) timers supporting cyclic wakeup from DeepSleep
    - Events trigger a specific device operation (such as execution of an interrupt handler, a SAR ADC conversion, and so on)

- **Real time clock (RTC)**
  - Year/Month/Date, Day-of-week, Hour:Minute:Second fields
  - 12- and 24-hour formats
  - Automatic leap-year correction
- **I/O**
  - Up to 168 programmable I/Os
  - Six I/O types
    - GPIO Standard (GPIO_STD)
    - GPIO Enhanced (GPIO_ENH)
    - GPIO Stepper Motor Control (GPIO_SMC)
    - High-Speed I/O Standard (HSIO_STD)
    - High-Speed I/O Standard with Low Noise (HSIO_STDLN)
    - High-Speed I/O Enhanced (HSIO_ENH)
    - High-Speed I/O Enhanced Differential (HSIO_ENH_PDIFF)
- **Power**
  - Regulators
    - Generates 1.1-V nominal core supply from a 2.7-V to 5.5-V input supply
    - Two regulators:
      DeepSleep
      Core internal
  - PMIC control module
- **Programmable analog**
  - One SAR A/D converter
    - Each ADC supports 32 logical channels, with 48 external channels. Any external channel can be connected to any logical channel in the SAR.
    - 12-bit resolution and sampling rates up to 1 Msps
  - The ADC also supports six internal analog inputs like
    - Bandgap reference to establish absolute voltage levels
    - Calibrated diode for junction temperature calculations
    - Two AMUXBUS inputs and two direct connections to monitor supply levels
  - ADC supports addressing of external multiplexers
  - ADC has a sequencer supporting autonomous scanning of configured channels
- **Smart I/O**
  - One smart I/O block, which can perform Boolean operations on signals going to and from I/Os
  - Up to eight I/Os (GPIO_STD) supported
- **Debug interface**
  - JTAG controller and interface compliant to IEEE-1149.1-2001
  - Arm® SWD (serial wire debug) port
  - Supports Arm® Embedded Trace Macrocell (ETM) Trace
    - Data trace using SWD
    - Instruction and data trace using JTAG
- **Compatible with industry-standard tools**
  - GHS MULTI or IAR EWARM for code development and debugging
- **Packages**
  - 327-BGA, 17 × 17 × 1.70 mm

Table of contents

1 Features list

Table 1-1 CYT4DN feature list

Features	Packages
	327-BGA
CPU	
Core	Two 32-bit Arm® Cortex®-M7 CPUs and a 32-bit Arm® Cortex®-M0+ CPU
Functional safety	ASIL-B
Operation voltage for GPIO_STD, GPIO_ENH	2.7 V to 5.5 V
Operation voltage for GPIO_SMC	2.7 V to 5.5 V
Operation voltage for HSIO_STD/HSIO_STDLN	3.0 V to 3.6 V
Operation voltage for HSIO_ENH	1.7 V to 2.0 V
Operation Voltage for HSIO_ENH_PDIFF	1.7 V to 2.0 V
Core voltage VCCD	1.09 V to 1.21 V
Operation frequency	Arm® Cortex®-M7 320 MHz (max for each) and Arm® Cortex®-M0+ 100 MHz (max)
MPU, PPU	Supported
FPU	Supports both single (32-bit) and double (64-bit) precision
DSP-MUL/DIV/MAC	Supported by Arm® Cortex®-M7 CPUs
TCM	64-KB instruction and 64-KB data for each Cortex®-M7 CPU
Memory	
Code-flash	6336 KB (6080 KB/Large Sectors + 256 KB/Small Sectors)
Work-flash	128 KB (96 KB/Large Sectors+ 32 KB/Small Sectors)
SRAM (configurable for retention)	640 KB (SRAM0/256 KB + SRAM1/256 KB + SRAM2/128 KB)
ROM	64 KB
Communication Interfaces	
CAN0/1 (CAN-FD: Up to 8 Mbps)	4 ch
CAN RAM	16 KB per instance (2 ch), 32 KB in total
Serial communication block (SCB)	12 ch
LIN0	2 ch
CXPI controller	2 ch
Ethernet MAC	1 ch × 10/100/1000
Memory Interfaces	
SMIF (Single SPI / Dual SPI / Quad SPI / Octal SPI / xSPI)	2 ch (HSIO_ENH + HSIO_ENH_PDIFF at 166 MHz)
Timers	
RTC	1 ch
TCPWM (16-bit)	38 ch
TCPWM (16-bit) Motor Control	12 ch (Equivalent to 6 ch SMC with ZPD and slew rate control)
TCPWM (32-bit)	32 ch
External Interrupts	168
Analog	
12-bit, 1 Msps SAR ADC	1 Unit (SAR0, 32 logical channels)
	48 external channels
	6 ch for Internal sampling
Security	
Flash Security (program/work read protection)	Supported
Flash Chip erase enable	Configurable

Table 1-1 CYT4DN feature list *(continued)*

Features	Packages
	327-BGA
eSHE / HSM	By separate firmware[2]
Sound	
Mixer	2 ch (5 mixer sources)
PCM-PWM	2 ch
TDM	4 TDM structures (each support 32 channels)
TDM/I^2S	4 ch (TDM0/1/2/3: TX and RX)
Audio DAC	1 ch
Sound Generator (SG)	5 ch
Graphics	
2/2.5 D Engine	Supported
Embedded Video RAM	4096 KB (with protection)
Vector Drawing	Supported
Warping	Supported (on the fly)
Scale/Rotate/Blend	Supported (on the fly)
Graphics Engine Clock	250 MHz (max)
Timing Control	One output
Video Capture	One Capture (1 × RGB or 1 × MIPI CSI-2, up to 4 lanes)
Video Capture Formats	**TTL** - ITU656 (8-/10-bit, RGB/YUV interlaced or progressive), Parallel RGB (1 to 24 bpp), YUV444, YUV422 **MIPI CSI-2** - **Table 29-3**
Number of Displays	Maximum two displays simultaneously (2 × LVDS single or 1 × LVDS dual and 1 × RGB)
RGB888/TTL Output	1 ch at 80 MHz (max)
FPD-link/LVDS Output	Dual channel LVDS at 220 MHz pixel clock (max)
	Single channel LVDS at 110 MHz pixel clock (max)
MIPI CSI-2 Input	4 lane MIPI CSI-2 at 220 MHz pixel clock (max)
	2 lane MIPI CSI-2 at 110 MHz pixel clock (max)
JPEG Decoder	Video performance up to 1600 × 800 @ 60 Hz Decompressed data in either packed (YUV444, RGB, Gray - 8/24 bpp) or semi-planar (YUV422, YUV420, YUV411 - 8/16 bpp) buffer formats
System	
DMA Controller	P-DMA0 with 76 channels (32 general purpose), P-DMA1 with 84 channels (16 general purpose), M-DMA0 with 8 channels, and AXI M-DMA1 with 4 channels
Internal Main Oscillator	8 MHz
Internal Low speed Oscillator	32.768 kHz (nominal)
PLL	Input frequency: 3.988 to 33.34 MHz, PLL output frequency: up to 320 MHz
FLL	Input frequency: 0.25 to 100 MHz, FLL output frequency: up to 100 MHz
Watchdog timer and multi-counter watchdog timer	Supported (WDT + 3× MCWDT) MCWDT#0 tied to CM0+, MCWDT#1 to CM7_0, MCWDT#2 to CM7_1
Clock supervisor	Supported
Cyclic wakeup from DeepSleep	Supported
GPIO Standard (GPIO_STD)	49
GPIO Enhanced (GPIO_ENH)	8
GPIO SMC (GPIO_SMC)[3]	24

Notes

[2] Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM) support are enabled by third-party firmware.

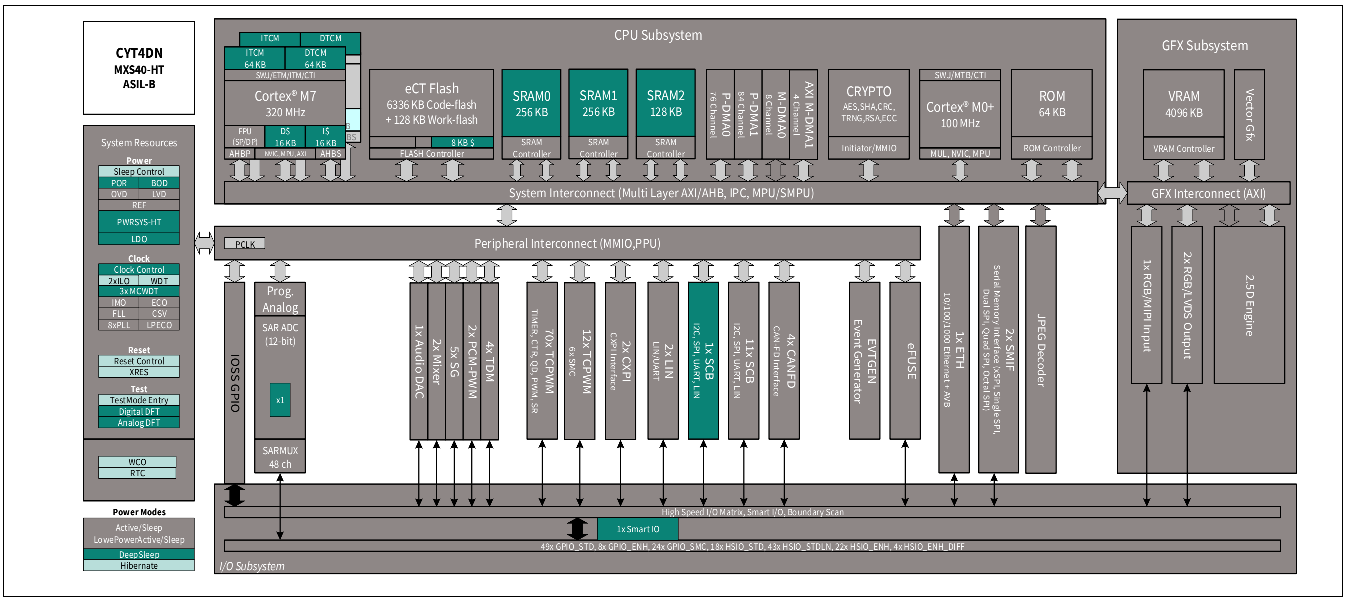
[3] High current SMC I/O for direct connections to stepper motor coils for pointer instruments.

Table 1-1 CYT4DN feature list *(continued)*

Features	Packages
	327-BGA
HSIO Standard (HSIO_STD)	18
HSIO Standard Low Noise (HSIO_STDLN)	43
HSIO Enhanced (HSIO_ENH)	22
HSIO Enhanced Differential (HSIO_ENH_PDIFF)	4
Smart I/O (Blocks)	1 block, mapped through 8 I/Os
Low-voltage detect	Two, 26 selectable levels
Maximum ambient temperature	105 °C for S-grade
Debug interface	SWD/JTAG
Debug Trace	Arm® Cortex®-M7 ETB size of 8 KB, Arm® Cortex®-M0+ MTB size of 4 KB

2 Blocks and functionality

Block diagram



The **Block diagram** shows a simplified view of the interconnection between subsystems and blocks. CYT4DN has five major subsystems: CPU, system resources, peripherals, graphics, and I/O[4,5,6,7,8]. The color-coding shows the lowest power mode where the particular block is still functional.

CYT4DN provides extensive support for programming, testing, debugging, and tracing of both hardware and firmware.

Debug-on-chip functionality enables in-system debugging using the production device. It does not require special interfaces, debugging pods, simulators, or emulators.

The JTAG interface is fully compatible with industry-standard third-party probes such as I-jet, J-Link, and GHS.

The debug circuits are enabled by default.

CYT4DN provides a high level of security with robust flash protection and the ability to disable features such as debug.

Additionally, each device interface can be permanently disabled for applications concerned with phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled.

Notes

4. GPIO_STD supporting 2.7 V to 5.5 V V_{DDIO} range.
5. GPIO_ENH supporting 2.7 V to 5.5 V V_{DDIO} range with higher currents at lower voltages.
6. GPIO_SMC supporting 2.7 V to 5.5 V V_{DDIO} range with currents higher than GPIO_ENH.
7. HSIO_STD/HSIO_STDLN supporting 3.0 V to 3.6 V V_{DDIO} range with high-speed signaling and programmable drive strength.
8. HSIO_ENH and HSIO_ENH_PDIFF supporting 1.7 V to 2.0 V V_{DDIO} range.

3 Functional description

3.1 CPU subsystem

3.1.1 CPU

The CYT4DN CPU subsystem contains a 32-bit Arm® Cortex®-M0+ CPU with MPU, and two 32-bit Arm® Cortex®-M7 CPUs, each with MPU, single/double-precision FPU, and 16-KB data and instruction caches. This subsystem also includes P-/M-DMA controllers, a cryptographic accelerator, 6336 KB of code-flash, 128 KB of work-flash, 640 KB of SRAM, and 64 KB of ROM.

The Cortex®-M0+ CPU provides a secure, un-interruptible boot function. This guarantees that, following completion of the boot function, system integrity is valid and privileges are enforced. Shared resources (flash, SRAM, peripherals, and so on) can be accessed through bus arbitration, and exclusive accesses are supported by an inter-processor communication (IPC) mechanism using hardware semaphores.

Each Cortex®-M7 CPU has 64 KB of instruction and 64 KB of data TCM with programmable read wait states. Each TCM is clocked by the associated Cortex®-M7 CPU clock.

3.1.2 DMA controllers

CYT4DN has three DMA controllers: P-DMA0 with 32 general purpose and 44 dedicated channels, P-DMA1 with 16 general purpose and 68 dedicated channels, M-DMA0 with eight channels, and AXI M-DMA1 with four channels. P-DMA is used for peripheral-to-memory and memory-to-peripheral data transfers and provides low latency for a large number of channels. Each P-DMA controller uses a single data-transfer engine that is shared by the associated channels. General purpose channels have a rich interconnect matrix including P-DMA cross triggering which enables demanding data-transfer scenarios. Dedicated channels have a single triggering input (such as an ADC channel) to handle common transfer needs. M-DMA is used for memory-to-memory data transfers and provides high memory bandwidth for a small number of channels. M-DMA uses a dedicated data-transfer engine for each channel. They support independent accesses to peripherals using the AHB multi-layer bus. AXI M-DMA is used to provide access to AXI slaves like VRAM.

3.1.3 Flash

CYT4DN has 6336 KB (6080 KB with a 32-KB sector size, and 256 KB with an 8-KB sector size) of code-flash with an additional work-flash of 128 KB (96 KB with a 2-KB sector size, and 32 KB with a 128-B sector size). Work-flash is optimized for reprogramming many more times than code-flash. Code-flash supports Read-While-Write (RWW) operation so that flash may be updated while the CPU is active. Both the code-flash and work-flash areas support dual-bank operation for over-the-air (OTA) programming.

3.1.4 SRAM

CYT4DN has 640 KB of SRAM with three independent controllers. SRAM0 provides DeepSleep retention in 32-KB increments while SRAM1/2 are selectable between fully retained and not retained.

3.1.5 ROM

CYT4DN has 64 KB of ROM that contains boot and configuration routines. This ROM enables secure boot and authentication of user flash to guarantee a secure system.

3.1.6 Cryptography accelerator for security

The cryptography accelerator implements (3)DES block cipher, AES block cipher, SHA hash, cyclic redundancy check, pseudo random number generation, true random number generation, Galois/counter mode, and a vector unit to support asymmetric key cryptography such as RSA and ECC.

Depending on the part number, this block is either completely or partially available or not available at all. See **"Ordering information"** on page 187 for more details.

3.2 System resources

3.2.1 Power system

The power system ensures that the supply voltage levels meet the requirements of each power mode, and provides a full-system reset when these levels are not valid. Internal power-on reset (POR) guarantees full-chip reset during the initial power ramp.

Three BOD circuits monitor the external supply voltages (V_{DDD}, V_{DDA_ADC}, V_{CCD}). The BOD on V_{DDD} and V_{CCD} is initially enabled and cannot be disabled. The BOD on V_{DDA_ADC} is initially disabled and can be enabled by the user. For the external supplies V_{DDD} and V_{DDA_ADC}, BOD circuits are software-configurable with two settings; a 2.7-V minimum voltage that is robust for all internal signaling, and a 3.0-V minimum voltage, which is also robust for all I/O specifications (which are guaranteed at 2.7 V). The BOD on V_{CCD} is provided as a safety measure and is not a robust detector.

Three over-voltage detection (OVD) circuits are provided for monitoring external supplies (V_{DDD}, V_{DDA_ADC}, V_{CCD}), and overcurrent detection circuits (OCD) for monitoring internal and external regulators. OVD thresholds on V_{DDD} and V_{DDA_ADC} are configurable with two settings; a 5.0-V and 5.5-V maximum voltage.

Two voltage detection circuits are provided to monitor the external supply voltage (V_{DDD}) for falling and rising levels, each configurable for one of the 26 selectable levels.

All BOD, OVD, and OCD circuits on V_{DDD} and V_{CCD} generate a reset, because these protect the CPUs and fault logic. The BOD and OVD circuits on V_{DDA_ADC} can be configured to generate either a reset, or a fault.

3.2.2 Regulators

CYT4DN contains two regulators that provide power to the low-voltage core transistors: DeepSleep, and core internal. These regulators accept a 2.7-V to 5.5-V V_{DDD} supply and provide a low-noise 1.1-V supply to various parts of the device. These regulators are automatically enabled and disabled by hardware and firmware when switching between power modes. The core internal regulator operates in Active mode, and provide power to the CPU subsystem and associated peripherals.

3.2.2.1 DeepSleep

The DeepSleep regulator is used to maintain power in a small number of blocks when in DeepSleep mode. These blocks include the ILO and WDT timers, BOD detector, SCB0, SRAM memories, Smart I/O, and other configuration memories. The DeepSleep regulator is enabled when in DeepSleep mode, and the core internal regulator is disabled. It is disabled when XRES_L is asserted (LOW) and when the core internal regulator is disabled.

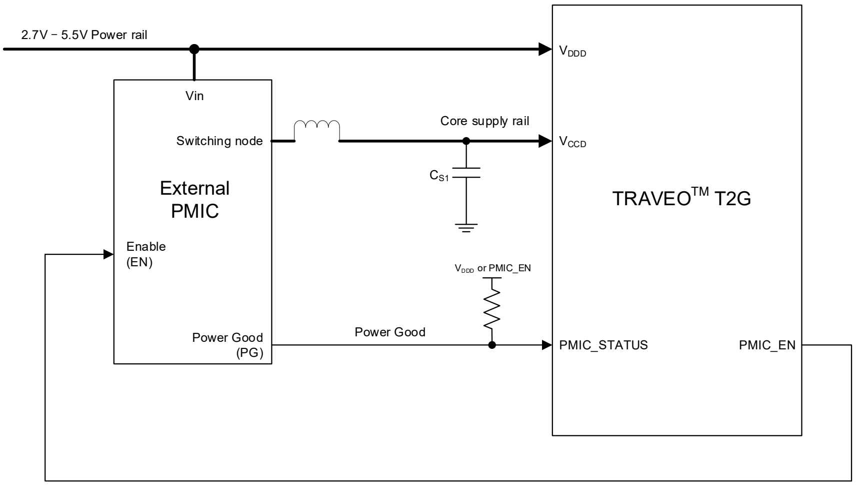
3.2.2.2 Core internal

The core internal regulator supports load currents up to 300 mA, and is operational during device start-up (boot process), and in Active/Sleep modes. (Graphics subsystem is not supported)

3.2.3 PMIC control module[9]

An internal PMIC module is available to control an external PMIC. The PMIC control module manages the handoff between the internal active regulator, used only for boot, and the external PMIC.

Both the core internal and external PMIC require an external bulk storage capacitor connected to the VCCD pin. This capacitor provides charge under the dynamic loads of the low-voltage core transistors.



- PMIC EN pin polarity is HIGH for enable. PMIC PG pin polarity is HIGH for power good.
- If EN pin of PMIC does not have the internal pull-down resistor, an external pull-down resistor must be placed to keep the PMIC disabled during power-on reset.
- See the Electrical Specifications section for more details on C_{S1}.

Figure 3-1 **Sample PMIC control interface**

3.2.4 Clock system

The CYT4DN clock system provides clocks to all subsystems that require them, and glitch-free switching between different clock sources. In addition, the clock system ensures that no metastable conditions occur.

The clock system for CYT4DN consists of the 8-MHz IMO, two ILOs, four watchdog timers, eight PLLs, an FLL, five clock supervisors (CSV), a 7.2- to 33.34-MHz ECO, a 3.99- to 8.01-MHz LPECO, and a 32.768-kHz WCO.

The clock system supports three main clock domains: CLK_HF, CLK_SLOW, and CLK_LF.

- CLK_HFx are the Active mode clocks. Each can use any of the high frequency clock sources including IMO, EXT_CLK, ECO, LPECO, FLL, or PLL
- CLK_SLOW provides a reference clock for the Cortex®-CM0+ CPU, Crypto, P-/M-DMA, and other slow infrastructure blocks of CPU subsystem
- CLK_LF is a DeepSleep domain clock and provides a reference clock for the MCWDT or RTC modules. The reference clock for the CLK_LF domain is either disabled or selectable from ILO0, ILO1, or WCO.

Table 3-1 **CLK_HF destinations**

Name	Description
CLK_HF0	CPUSS (Memories, CLK_SLOW, Peripherals)
CLK_HF1	CPUSS (Cortex®-M7 CPU 0, 1)
CLK_HF2	CAN FD, CXPI, LIN, SCB, SAR
CLK_HF3	Event Generator, Clock output (CLK_EXT)

Note

9. While CYT4DN can control various external PMICs, it is verified to work with both the Cypress S6BP501A and Infineon TLS208D1.

Table 3-1 CLK_HF destinations *(continued)*

Name	Description
CLK_HF4	Ethernet Internal Clock
CLK_HF5	Sound Subsystem #0 (TDM, SG, PWM, MIXER, DAC), Ethernet TSU
CLK_HF6	Sound Subsystem #1 (TDM, SG, PWM, MIXER)
CLK_HF7	Sound Subsystem #2 (TDM, SG, PWM)
CLK_HF8	SMIF #0
CLK_HF9	SMIF #1
CLK_HF10	Video Subsystem
CLK_HF11	Video Display #0
CLK_HF12	Video Display #1
CLK_HF13	CSV

3.2.4.1 IMO clock source

The IMO is the frequency reference in CYT4DN when no external reference is available or enabled. The IMO operates at a frequency of around 8 MHz.

3.2.4.2 ILO clock source

An ILO is a low-power oscillator, nominally 32.768 kHz, which generates clocks for a watchdog timer when in DeepSleep mode. There are two ILOs to ensure clock supervisor (CSV) capability in DeepSleep mode. ILO-driven counters can be calibrated to the IMO, WCO, or ECO to improve their accuracy. ILO1 is also used for clock supervision.

3.2.4.3 PLL and FLL

A PLL (three 200 MHz and five 400 MHz) or FLL may be used to generate high-speed clocks from the IMO, ECO, or an EXT_CLK. The FLL provides a much faster lock than the PLL (5 µs instead of 35 µs) in exchange for a small amount (±2%) of frequency error[10] and a lower max output frequency (100 MHz instead of up to 400 MHz). 400-MHz PLLs supports spread spectrum clock generation (SSCG) with down spreading.

3.2.4.4 Clock supervisor

Each clock supervisor (CSV) allows one clock (reference) to supervise the behavior of another clock (monitored). Each CSV has counters for both the monitored and reference clocks. Parameters for each counter determine the frequency of the reference clock as well as the upper and lower frequency limits of the monitored clock. If the frequency range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled and either a reset or an interrupt is generated.

3.2.4.5 EXT_CLK

One of three GPIO_STD I/Os can be used to provide an external clock input of up to 100 MHz. This clock can be used as the source clock for either the PLL or FLL, or can be used directly by the CLK_HF domain.

3.2.4.6 ECO

The ECO provides high-frequency clocking using an external crystal connected to the ECO_IN and ECO_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 7.2 to 33.34 MHz. When used in conjunction with the PLL, it generates CPU and peripheral clocks up to device’s maximum frequency. ECO accuracy depends on the selected crystal. If the ECO is disabled, the associated pins can be used for any of the available I/O functions.

Note

10.Operation of reference-timed peripherals (such as a UART) with an FLL-based reference is not recommended due to the allowed.

3.2.4.7 LPECO

The LPECO provides high-frequency clocking using an external crystal connected to the LPECO_IN and LPECO_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 3.99 to 8.01 MHz. LPECO can operate during DeepSleep, and Hibernate modes with significant lower current consumptions. It can also be used for real-time-clock applications. When used in conjunction with the PLL, it generates CPU and peripheral clocks up to device's maximum frequency.

3.2.4.8 WCO

The WCO is a low-power, watch-crystal oscillator intended for real-time-clock applications. It requires an external 32.768-kHz crystal connected to the WCO_IN and WCO_OUT pins. The WCO can also be configured as a clock reference for CLK_LF, which is the clock source for the MCWDT and RTC.

3.2.5 Reset

CYT4DN can be reset from a variety of sources, including software. Most reset events are asynchronous and guarantee reversion to a known state. The reset cause (POR, BOD, OVD, overcurrent, XRES_L, WDT, MCWDT, software reset, fault, CSV, Hibernate wakeup, debug) is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES_L pin is available for external reset.

3.2.6 Watchdog timer

CYT4DN has one watchdog timer (WDT) and three multi-counter watchdog timers (MCWDT).

The WDT is a free-running counter clocked only by ILO0, which allows it to be used as a wakeup source from Hibernate. Watchdog operation is possible during all power modes. To prevent a device reset from a WDT timeout, the WDT must be serviced during a configured window. A watchdog reset is recorded in the reset cause register.

An MCWDT is available for each of the CPU cores. These timers provide more capabilities than the WDT, and are only available in Active, Sleep, and DeepSleep modes. These timers have multiple counters that can be used separately or cascaded to trigger interrupts and/or resets. They are clocked from ILO0 or the WCO.

3.2.7 Power modes

CYT4DN has six power modes that apply to the core functions, CM0+ core, and peripherals without power switches. Power modes for the CM7 cores and VIDEOSS are controlled separately.

- Active – all peripherals are available
- Low-Power Active (LPACTIVE) – Low-power profile of Active mode where all peripherals and the CPUs are available, but with limited capability
- Sleep – all peripherals except the CPUs are available
- Low-Power Sleep (LPSLEEP) – Low-power profile of Sleep mode where all peripherals except the CPUs are available, but with limited capability
- DeepSleep – only peripherals which work with CLK_LF are available
- Hibernate – the device and I/O states are frozen, the device resets on wakeup

3.3 Peripherals

3.3.1 Peripheral clock dividers

Integer and fractional clock dividers are provided for peripheral and timing purposes.

Table 3-2 Clock dividers - CPUSS Group (Number 0)

Divider Type	Instances	Description
div_8	9	Integer divider, 8 bits
div_16	16	Integer divider, 16 bits
div_16_5	7	Fractional divider, 16.5 bits (16 integer bits, 5 fractional bits)
div_24_5	3	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

Table 3-3 Clock dividers - CPUSS Group (Number 1)

Divider Type	Instances	Description
div_8	3	Integer divider, 8 bits
div_16	4	Integer divider, 16 bits
div_24_5	7	Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits)

3.3.2 Peripheral protection unit

The peripheral protection unit (PPU) controls and monitors unauthorized access from all masters (CPU, P-/M-DMA, Crypto, and any enabled debug interface) to the peripherals. It allows or restricts data transfers on the bus infrastructure. The access rules are enforced based on specific properties of a transfer, such as an address range for the transfer and access attributes (such as read/write, user/privilege, and secure/non-secure).

3.3.3 12-bit SAR ADC

CYT4DN contains one 1-Msps SAR ADC. This ADC can be clocked at up to 26.67 MHz and provide a 12-bit result in 26 clock cycles.

The references for the SAR ADC comes from a dedicated pair of inputs: VREFH and VREFL[11].

CYT4DN supports 32 logical ADC channels which can select one of 54 input sources. Sources include 48 external inputs from I/Os, and six internal connections for diagnostic and monitoring purposes.

The number of ADC channels (per ADC and package type) are listed in **Table 1-1**.

SAR ADC has a sequencer, which autonomously cycles through the configured channels (sequencer scan) with zero-switching overhead (that is, the aggregate sampling bandwidth, when clocked at 26.67 MHz, is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is controlled through a state machine or firmware. The sequencer prioritizes trigger requests, enables the appropriate analog channel, controls ADC sampling, initiates ADC data conversion, manages results, and initiates subsequent conversions for repetitive or group conversions without CPU intervention.

SAR ADC has two analog multiplexers used to connect the signals to be measured to the ADC. One is SARMUX0 which has 24 GPIO_STD inputs (ADC[0]_0 to ADC[0]_23), and six additional inputs to measure internal signals such as a band-gap reference, a temperature sensor, VCCD, VDDA_ADC power supplies and AMUXBUSA/B signals. The other multiplexer is SARMUX1 which has 24 GPIO_SMC inputs (ADC[1]_0 to ADC[1]_23).

CYT4DN has a temperature sensor. Software post processing is required to convert the temperature sensor reading into kelvin or Celsius values.

To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmed for each channel. ADC also supports range comparison, which allows fast detection of out-of-range values without having to wait for a sequencer scan to complete and for the CPU firmware to evaluate the measurement for out-of-range values.

The ADC is not usable in DeepSleep and Hibernate modes as they require a high-speed clock. The ADC input reference voltage VREFH range is 2.7 V to V_{DDA_ADC} and VREFL is V_{SSA_ADC}.

Note

[11] VREF_L prevents IR drops in the VSSIO and VSSA_ADC paths from impacting the measurements. VREF_L, when properly connected, reduces or removes the impact of IR drops in the VSS and VSSA_ADC paths from measurements.

3.3.4 Timer/counter/PWM block (TCPWM)

The TCPWM block consists of 16-bit (50 channels) and 32-bit (32 channels) counters with user-programmable period.

Each TCPWM counter contains a capture register to record the count at the time of an event, a period register (used to either stop or auto-reload the counter when its count is equal to the period register), and compare registers to generate signals that are used as PWM duty-cycle outputs.

Each counter within the TCPWM block supports several functional modes such as timer, capture, quadrature, PWM, PWM with dead-time insertion (PWM_DT, 8-bit), pseudo-random PWM (PWM_PR), and shift-register.

The TCPWM block also provides true and complement outputs, with programmable offset between them, to allow their use as deadband complementary PWM outputs. The TCPWM block also has a kill input (only for the PWM mode) to force outputs to a predetermined state; for example, this may be used in motor-drive systems when an overcurrent state is detected and the PWMs driving the FETs need to be shut off immediately (no time for software intervention).

Twelve of the 16-bit counters are optimized for DC and stepper motor-control operations, these also have ZPD (Zero Point detection) and slew rate control capabilities. Two of these TCPWM channels constitute one SMC channel.

3.3.5 Serial Communication Blocks (SCB)

CYT4DN contains up to 12 serial communication blocks, each configurable to support I^{2}C, UART, or SPI.

3.3.5.1 I^{2}C interface

An SCB can be configured to implement a full I^{2}C master (capable of multi-master arbitration) or slave interface. Each SCB configured for I^{2}C can operate at speeds of up to 1 Mbps (Fast-mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency of the CPU. In addition, each SCB supports FIFO buffering for receive and transmit data, which, by increasing the time for the CPU to read the data, reduces the need for clock stretching. The I^{2}C interface is compatible with Standard, Fast-mode, and Fast-mode Plus devices as specified in the NXP I^{2}C-bus specification and user manual (UM10204). The I^{2}C-bus I/O is implemented with GPIO in open-drain modes[12, 13].

3.3.5.2 UART interface

When configured as a UART, each SCB provides a full-featured UART with maximum signaling rate determined by the configured peripheral-clock frequency and over-sampling rate. It supports infrared interface (IrDA) and SmartCard (ISO 7816) protocols, which are minor variants of the UART protocol. It also supports the 9-bit multi-processor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity, number of stop bits, break detect, and frame error are supported. FIFO buffering of transmit and receive data allows greater CPU service latencies to be tolerated.

The LIN protocol is supported by the UART. LIN is based on a single-master multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports only LIN slave functionality. Compared to the dedicated LIN blocks, an SCB/UART used for LIN requires a higher level of software interaction and increased CPU load.

Notes

[12] This is not 100% compliant with the I^{2}C-bus specification; I/Os are not over-voltage tolerant, do not support the 20-mA sink requirement of Fast-mode Plus, and violate the leakage specification when no power is applied.

[13] See **Table 26-10** 'Serial Communication Block (SCB) specifications' for supported IO-cells and I^{2}C modes.

3.3.5.3 SPI interface

The SPI configuration supports full Motorola SPI, TI Synchronous Serial Protocol (SSP, essentially adds a start pulse that is used to synchronize SPI-based Codecs), and National Microwire (a half-duplex form of SPI). The SPI interface can use the FIFO. The SPI interface operates with up to a 12.5-MHz SPI Clock. SCB also supports EZSPI[14] mode.

SCB0 supports the following additional features:

- Operable as a slave in DeepSleep mode
- I^{2}C slave EZ (EZI2C[14]) mode with up to 256-B data buffer for multi-byte communication without CPU intervention
- I^{2}C slave externally-clocked operations
- Command/response mode with a 512-B data buffer for multi-byte communication without CPU intervention

3.3.6 Controller area network flexible data-rate (CAN FD)

CYT4DN supports two CAN FD controller blocks, each supporting two CAN FD channel. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware. All functions concerning the handling of messages are implemented by the Rx and Tx handlers. The Rx handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The Tx handler is responsible for the transfer of transmit messages from the message RAM to the CAN core, and provides transmit-message status.

3.3.7 Local interconnect network (LIN)

CYT4DN contains up to two LIN channels. Each channel supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN channel connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each block also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

3.3.8 Clock extension peripheral interface (CXPI)

CYT4DN contains up to four CXPI channels compliant with JASO D015 and ISO standard 20794 including the controller specification.

Each channel supports:

- Master and slave functionality
- Polling and event trigger method for both normal and long frames
- Non-return to zero (NRZ) and PWM signaling modes
- Collision resolution and carries sense multiple access
- Wakeup pulse generation and detection
- CRC8 and CRC16 for both normal and long frames
- Error detection
- Dedicated FIFO (16 B) for transmit and receive

Notes

14. The Easy SPI (EZSPI) protocol is based on the Motorola SPI protocol operating in any mode (0, 1, 2, or 3). It allows communication between master and slave while reducing the need for CPU intervention.
15. The Easy I^{2}C (EZI2C) protocol is a unique communication scheme built on top of the I^{2}C protocol by Infineon. It uses a meta protocol around the standard I^{2}C protocol to communicate to an I^{2}C slave using indexed memory transfers. This reduces the need for CPU intervention.

3.3.9 Ethernet MAC

CYT4DN supports one Ethernet channel with transfer rates of 10, 100, or 1000 (RGMII) Mbps. The input/output frames and flow control are compliant with the Ethernet/IEEE 802.3az standard and also IEEE-1588 precision-time protocol (PTP). CYT4DN supports full-duplex data transport using external PHY devices. The MAC supports glue-free connection to PHYs through IEEE standard MII, RMII, and RGMII interfaces. The device also supports Audio-Video Bridging (AVB). The MAC supports standard 6-byte programmable addresses. Module uses **AXI** interface for DMA access.

3.3.10 Serial memory interface (SMIF)

In addition to the internal flash memory, CYT4DN supports direct connection to two units of 512 MB of external flash or RAM memory. This connection is made through either a xSPI or serial peripheral interface (SPI). xSPI allows connection to HyperFlash and HyperRAM devices, while SPI (single, dual, quad, or octal SPI) can connect with serial flash memory. Code stored in memory connected through this interface allows execute-in-place (XIP) operation, which does not require the instructions to be first copied to internal memory, and on-the-fly encryption and decryption for environments requiring secure external data and code.

3.3.11 Sound subsystem

CYT4DN supports the following:

- Four time-division multiplexing (TDM) interfaces
  - Full-duplex transmitter and receiver operation
  - Independent transmitter or receiver operation, each in master or slave mode
  - Up to 32 channels, each channel can be individually enabled or disabled
- Two pulse code modulation-pulse width modulation (PCM-PWM) interface
  - Conversion of PCM audio streaming to PWM signals
  - Up to 32-bit output sample resolution
  - Supports E- and H-bridge formats
  - Dead time insertion
- Up to five sound generator (SG) interfaces
  - PWM modulated (amplitude, tone) sound generation
  - Separate volume and frequency control (two signals) and combined volume-frequency control (one signal) formats
- Up to five mixers
  - Combines multiple PCM source streams into a single PCM destination stream
  - PCM source stream can be gain/volume controlled
  - Fixed PCM sample formatting (16-bit pairs)
  - LPF support by FIR filter
  - Fade-in and Fade-out control for both source and destination PCM streams
- One audio digital-to-analog converter (DAC)
  - Programmable sampling rate and frequency control
  - Supports stereo (Left and Right)
  - Supports CIC filter, FIR filter, Interpolation filter, and Delta-Sigma modulator
  - Multi-level DAC

3.3.12 One-time-programmable (OTP) eFuse

CYT4DN contains a 1024-bit OTP eFuse memory that can be used to store and access a unique and unalterable identifier or serial number for each device. eFuses are also used to control the device life-cycle (manufacturing, programming, normal operation, end-of-life, and so on) and the security state. Of the 1024 bits, 192 are available for user purposes.

3.3.13 Event generator

The event generator supports generation of interrupts and triggers in Active mode and interrupts in DeepSleep mode. The event generators are used to trigger a specific device operation (execution of an interrupt handler, a SAR ADC conversion, and so on) and to provide a cyclic wakeup mechanism from DeepSleep mode. They provide CPU-free triggers for device functions, and reduce CPU involvement in triggering device functions, thus reducing overall power consumption and processing overhead.

3.3.14 Trigger multiplexer

CYT4DN supports connecting various peripherals using trigger signals. Triggers are used to inform a peripheral of the occurrence of an event or change of state. These triggers are used to affect or initiate some action in other peripherals. The trigger multiplexer is used to route triggers from a source peripheral to a destination. Triggers provide active logic functionality and are typically supported in Active mode.

3.4 Graphics

CYT4DN supports one instance of the graphics subsystem which includes 4096 KB of embedded Video RAM, a 2D graphics core and interfaces for video input and output processing.

CYT4DN supports 4-lane MIPI CSI-2 interface for up to Wide-HD resolution video inputs and dual channel FPD-link interface for up to Wide-HD resolution video output. The 2D graphics core supports a BLock Image Transfer (BLIT) engine for faster graphics rendering to memory or on-the-fly to display, a drawing engine for acceleration of vector graphics rendering and a command sequencer for setup and control of the rendering process. The video I/O supports a composition engine for scene composition from display layers, a display engine for video timing generation, and display functions and a capture engine for video input processing. The device also supports perspective correction for 3D effects ("2.5D"). One layer can be warped on-the-fly, e.g., for head-up displays. It includes a JPEG decoder, which decodes JPEG images of various formats into pixel data with conformance to a subset of ISO/IEC10918-1 (JPEG Part 1). It also supports RGB/YUV/Grayscale color space.

3.5 I/Os

CYT4DN has up to 168 programmable I/Os.

The I/Os are organized as logical entities called ports, which are a maximum of 8 bits wide. During power-on, and reset, the I/Os are forced to the High-Z state. During the Hibernate mode, I/Os are frozen.

Every I/O can generate an interrupt (if enabled) and each port has an interrupt request (IRQ) and interrupt service routine (ISR) associated with it.

I/O port power source mapping is listed in **Table 3-4**. The associated supply determines the V_{OH}, V_{OL}, V_{IH}, and V_{IL} levels when configured for CMOS and Automotive thresholds.

Table 3-4 I/O port power source

Supply pins	Ports
VDDD[16]	P1
VDDIO_GPIO_0[16]	P0, P2, P3
VDDIO_GPIO_1[16]	P4, P5, P6
VDDIO_GPIO_2[16]	P7, P8, P29
VDDIO_SMC[16]	P9, P11, P12
VDDIO_HSIO	P13, P14, P15, P16, P17, P18, P19, P20, P21, P30
VDDIO_SMIF	P23, P24, P25, P26, P27, P28

Notes

16. Ensure that $V_{DDD} \geq V_{DDIO\_GPIO\_2} \geq V_{DDIO\_GPIO\_1}$. Ensure that V_{DDD} is turned on before $V_{DDIO\_GPIO\_1}$, and $V_{DDIO\_GPIO\_1}$ is turned on before $V_{DDIO\_GPIO\_2}$, or all at the same time. Also ensure $V_{DDIO\_GPIO\_2} \geq V_{DDA\_ADC}$ and $V_{DDIO\_SMC} \geq V_{DDA\_ADC}$ to avoid increased leakage. Operating the mentioned supplies within the same voltage range (i.e. within 2.7 V-3.6 V, respectively within 4.5 V-5.5 V) fulfills being "equal".
17. Refer to the device Architecture TRM for more details on the I/O configuration.

All I/Os support the following programmable drive modes:

- High impedance
- Resistive pull-up
- Resistive pull-down
- Open drain with strong pull-down
- Open drain with strong pull-up
- Strong pull-up or pull-down
- Weak pull-up or pull-down

CYT4DN has six types of programmable GPIOs: GPIO Standard, GPIO Enhanced, GPIO SMC, HSIO Standard, HSIO Standard with low-noise, HSIO Enhanced, HSIO Enhanced Differential. Only GPIO_STD, GPIO_ENH, and GPIO_SMC have the capability to wakeup the device from DeepSleep mode. All these I/Os have GPIO input/output functionality, HSIO_ENH_PDIFF I/Os (P24, P27) have limitations in single ended mode[18].

3.5.1 GPIOs

Three types of GPIOs are supported:

- GPIO_STD, GPIO_ENH, and GPIO_SMC

These implement the following:

- Configurable input threshold (CMOS, TTL, or Automotive)
- Hold mode for latching previous state (used for retaining the I/O state in DeepSleep mode)
- Analog input mode (input and output buffers disabled)
- Edge-triggered interrupts on rising edge, falling edge, or on both the edges, on pin basis

3.5.1.1 GPIO Standard (GPIO_STD)

Supports standard automotive signaling across the 2.7-V to 5.5-V V_{DDIO} range. GPIO Standard I/Os have multiple configurable drive levels, drive modes, and selectable input levels.

3.5.1.2 GPIO Enhanced (GPIO_ENH)

Supports extended functionality automotive signaling across the 2.7-V to 5.5-V V_{DDIO} range with higher currents at lower voltages (full I^2C timing support, slew-rate control).

3.5.1.3 GPIO SMC (GPIO_SMC)

Provides significant drive strength compared to GPIO_STD and GPIO_ENH (supports 30-mA drive).

3.5.2 HSIO

These I/Os are optimized exclusively for high-speed signaling and do not support slew-rate control, DeepSleep operation, POR mode control, analog connections, or non-CMOS signaling levels. HSIO support programmable drive strength. They are available only in Active mode.

3.5.2.1 HSIO Standard (HSIO_STD)

Supports clocking and signaling up to 125 MHz. Supports high-speed peripherals such as Graphics input/output. Also supports holding state during DeepSleep mode.

3.5.2.2 HSIO Standard Low Noise (HSIO_STDLN)

This I/O supports clocking and signaling up to 133 MHz. Supports high-speed peripherals such as Graphics input/output, and Ethernet. Also supports holding state during DeepSleep mode. Low noise version optimizes the noise generated by having specific modes for each interface support.

3.5.2.3 HSIO Enhanced (HSIO_ENH)[18]

Supports clocking and signaling up to 166 MHz. Supports high-speed peripherals such as QSPI and xSPI.

Note

[18] VDDIO_SMIF_HV provides the supply for the HSIO_ENH and HSIO_ENH_PDIFF pre-drivers.

3.5.2.4 HSIO Enhanced Differential (HSIO_ENH_PDIFF)[18]

Supports clocking and signaling up to 200 MHz, to output SMIF clocks (normal and inverted).

3.5.3 Port nomenclature

Px.y describes a particular bit “y” available within an I/O port “x.”

For example, P4.2 reads “port 4, bit 2”.

3.5.4 Smart I/O

Smart I/O allows Boolean operations on signals going to the I/O from the subsystems of the chip or on signals coming into the chip. CYT4DN has one Smart I/O block. Operation can be synchronous or asynchronous and the blocks operate in all device power modes except for the Hibernate mode.

4 CYT4DN address map

The CYT4DN microcontroller supports the memory spaces shown in **Figure 4-1**.

- 6336 KB (6080 KB + 256 KB) of code-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register4
  - Single-bank mode: 6336 KB
  - Dual-bank mode: 3168 KB per bank
- 128 KB (92 KB + 32 KB) of work-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
  - Single-bank mode: 128 KB
  - Dual-bank mode: 64 KB per bank
- 64 KB of secure ROM
- 640 KB of SRAM (First 2 KB is reserved for internal usage)
- 64 KB of Instruction TCM for each Cortex®-M7 CPU
- 64 KB of Data TCM for each Cortex®-M7 CPU
- 512 MB SMIF XIP1
- 512 MB SMIF XIP2
- 4096 KB of VRAM

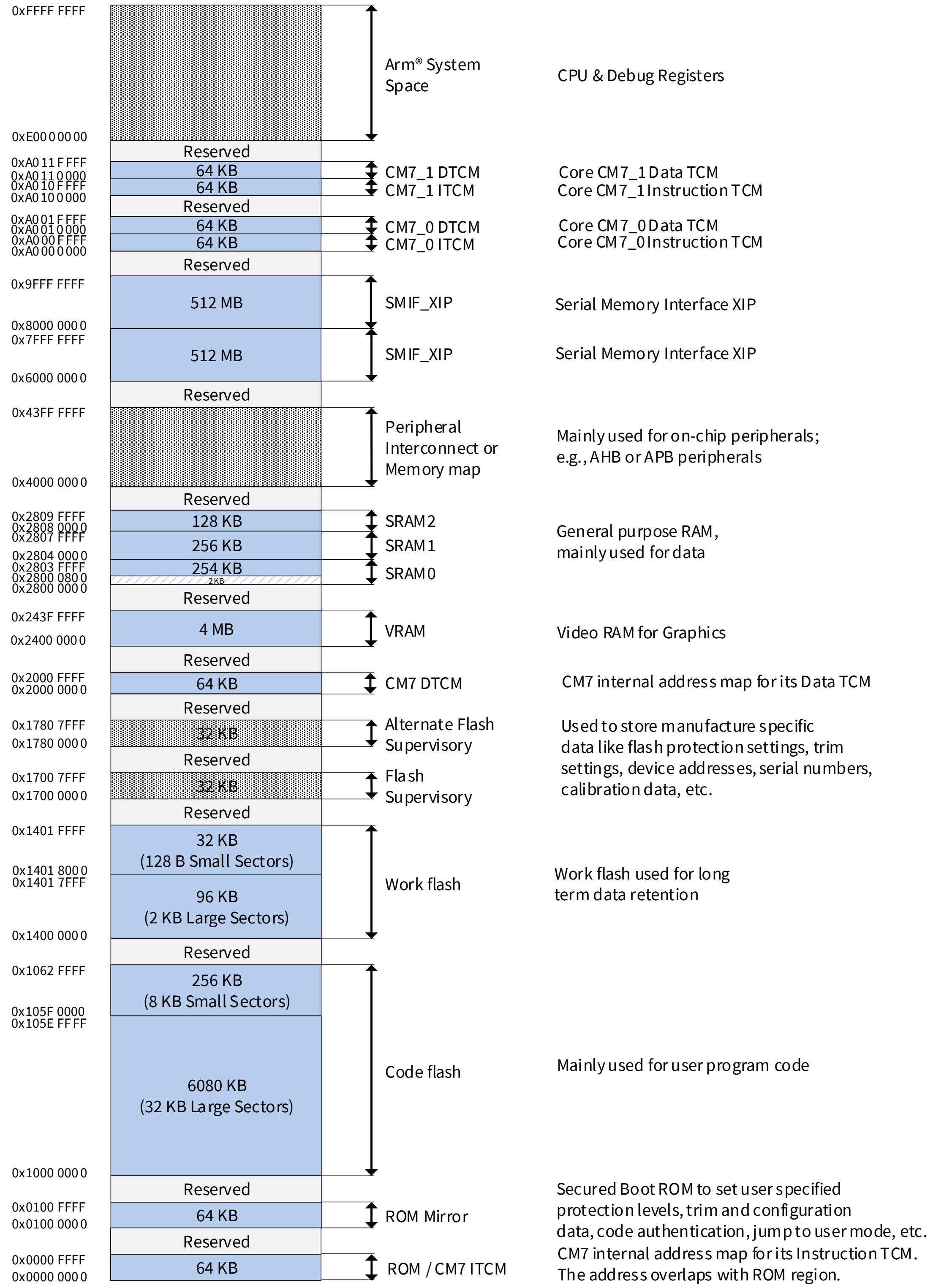


Figure 4-1 **CYT4DN address map**[19, 20]

Notes
[19] The size representation is not up to scale.
[20] First 2KB of SRAM is reserved, not available for users. User must keep the power of first 32KB block of SRAM0 in enabled or retained in all Active, LP Active, Sleep, LP Sleep, DeepSleep modes.

5 Flash base address map

Table 5-1 through **Table 5-6** give information about the sector mapping of the code- and work-flash regions along with their respective base addresses.

Table 5-1 Code-flash address mapping in single bank mode

Code-flash Size (KB)	Large Sectors (LS)	Small Sectors (SS)	Large Sector Base Address	Small Sector Base Address
6336	32 KB × 190	8 KB × 32	0x1000 0000	0x105F 0000

Table 5-2 Work-flash address mapping in single bank mode

Work-flash Size (KB)	Large Sectors	Small Sectors	Large Sector Base Address	Small Sector Base Address
128	2 KB × 48	128 B × 256	0x1400 0000	0x1401 8000

Table 5-3 Code-flash address mapping in dual bank mode (Mapping A)

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
6336	32 KB × 95	8 KB × 16	32 KB × 95	8 KB × 16	0x1000 0000	0x102F 8000	0x1200 0000	0x122F 8000

Table 5-4 Code-flash address mapping in dual bank mode (Mapping B)

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
6336	32 KB × 95	8 KB × 16	32 KB × 95	8 KB × 16	0x1200 0000	0x122F 8000	0x1000 0000	0x102F 8000

Table 5-5 Work-flash address mapping in dual bank mode (Mapping A)

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1400 0000	0x1400 C000	0x1500 0000	0x1500 C000

Table 5-6 Work-flash address mapping in dual bank mode (Mapping B)

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address
128	2 KB × 24	128 B × 128	2 KB × 24	128 B × 128	0x1500 0000	0x1500 C000	0x1400 0000	0x1401 8000

6 Peripheral I/O map

Table 6-1 CYT4DN peripheral I/O map

Section	Description	Base address	Instances	Instance size	Group	Slave
PERI	Peripheral interconnect	0x4000 0000			0	0
	Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9, 10)	0x4000 4000	10	0x40		
	Peripheral trigger group	0x4000 8000	13	0x400		
	Peripheral 1:1 trigger group	0x4000 C000	8	0x400		
PERI_MS	Peripheral interconnect, master interface	0x4002 0000			0	1
	PERI Programmable PPU	0x4002 0000	10[21]	0x40		
	PERI Fixed PPU	0x4002 0800	582	0x40		
PERI_PCLK	Peripheral Clock Groups	0x4004 0000	2	0x2000	0	2
Crypto	Cryptography component	0x4010 0000			1	0
CPUSS	CPU subsystem (CPUSS)	0x4020 0000			2	0
FAULT	Fault structure subsystem	0x4021 0000			2	1
	Fault structures	0x4021 0000	4	0x100		
IPC	Inter process communication	0x4022 0000			2	2
	IPC structures	0x4022 0000	8	0x20		
	IPC interrupt structures	0x4022 1000	8	0x20		
PROT	Protection	0x4023 0000			2	3
	Shared memory protection unit structures	0x4023 2000	16	0x40		
	Memory protection unit structures	0x4023 4000	16	0x400		
FLASHC	Flash controller	0x4024 0000			2	4
SRSS	System Resources Subsystem Core Registers	0x4026 0000			2	5
	Clock Supervision High Frequency	0x4026 1400	14	0x10		
	Clock Supervision Reference Frequency	0x4026 1710	1			
	Clock Supervision Low Frequency	0x4026 1720	1			
	Clock Supervision Internal Low Frequency	0x4026 1730	1			
	Clock PLL 400 MHz	0x4026 1900	5	0x10		
	Multi Counter WDT	0x4026 8000	3	0x100		
	Free Running WDT	0x4026 C000	1			
BACKUP	SRSS Backup Domain/RTC	0x4027 0000			2	6
	Backup Register	0x4027 1000	4	0x04		

Note

[21] These programmable PPUs are configured by the Boot ROM and are available for the user based on the access rights. Refer to the device specific TRM to know more about the configuration of these programmable PPUs.

Table 6-1 CYT4DN peripheral I/O map *(continued)*

Section	Description	Base address	Instances	Instance size	Group	Slave
P-DMA	P-DMA 0 Controller	0x4028 0000			2	7
	P-DMA 0 channel structures	0x4028 8000	76	0x40		
	P-DMA 1 Controller	0x4029 0000			2	8
	P-DMA 1 channel structures	0x4029 8000	84	0x40		
M-DMA	M-DMA0 Controller (AHB Bus)	0x402A 0000			2	9
	M-DMA0 channels	0x402A 1000	8	0x100		
	M-DMA1 Controller (AXI Bus)	0x402B 0000			2	10
	M-DMA1 channels	0x402B 1000	8	0x100		
eFUSE	eFUSE Customer Data (192 bits)	0x402C 0868	6	0x04	2	11
HSIOM	High-Speed I/O Matrix (HSIOM)	0x4030 0000	31	0x10	3	0
GPIO	GPIO port control/configuration	0x4031 0000	31	0x80	3	1
SMARTIO	Programmable I/O configuration	0x4032 0000			3	2
	SMARTIO port configuration	0x4032 0C00	1	0x100		
TCPWM	Timer/Counter/PWM 0 (TCPWM0)	0x4038 0000			3	3
	TCPWM0 Group #0 (16-bit)	0x4038 0000	38	0x80		
	TCPWM0 Group #1 (16-bit, Motor control)	0x4038 8000	12	0x80		
	TCPWM0 Group #2 (32-bit)	0x4039 0000	32	0x80		
EVTGEN	Event generator 0 (EVTGEN0)	0x403F 0000			3	4
	Event generator 0 comparator structures	0x403F 0800	16	0x20		
SMIF	Serial Memory Interface 0 (SMIF0) Bridge	0x4040 0000			4	0
	SMIF0 CORE0	0x4042 0000				
	SMIF0 CORE0 Devices	0x4042 0800	2	0x80		
	SMIF0 CORE1	0x4043 0000				
	SMIF0 CORE1 Devices	0x4043 0800	2	0x80		
ETH	Ethernet 0 (ETH0)	0x4048 0000	1		4	1
LIN	Local Interconnect Network 0 (LIN0)	0x4050 0000			5	0
	LIN0 Channels	0x4050 8000	2	0x100		
CXPI	Clock Extension Peripheral Interface 0 (CXPI0)	0x4051 0000			5	1
	CXPI0 Channels	0x4051 8000	2	0x100		
CAN	CAN0 controller	0x4052 0000	2	0x200	5	2
	Message RAM CAN0	0x4053 0000		0x4000		
	CAN1 controller	0x4054 0000	2	0x200	5	3
	Message RAM CAN1	0x4055 0000		0x4000		
SCB	Serial Communications Block (SPI/UART/I^{2}C)	0x4060 0000	12	0x10000	6	0-11

Table 6-1 **CYT4DN peripheral I/O map** *(continued)*

Section	Description	Base address	Instances	Instance size	Group	Slave
Sound	Time Division Multiplexer 0 (TDM0)	0x4081 0000			8	0
	TDM0 Structures	0x4081 8000	4	0x200		
	Sound Generator 0 (SG0)	0x4082 0000			8	1
	SG0 Structures	0x4082 8000	5	0x100		
	Pulse Width Modulation 0 (PWM0)	0x4083 0000			8	2
	PWM0 Structures	0x4083 8000	2	0x100		
	Audio DAC0	0x4084 0000	1		8	3
	Mixer0	0x4088 0000			8	4
	Mixer0 Source Structures	0x4088 8000	5	0x100		
	Mixer0 Destination Structures	0x4088 C000	1			
	Mixer1	0x4089 0000			8	5
	Mixer1 Source Structures	0x4089 8000	5	0x100		
	Mixer1 Destination Structures	0x4089 C000	1			
SAR PASS	Programmable Analog Subsystem (PASS0)	0x4090 0000			9	0
	SAR0 channel controller	0x4090 0000				
	SAR0 channel structures	0x4090 0800	24[22]	0x40		
	SAR1 channel structures	0x4090 1800	24	0x40		
Graphics	Video Subsystem (VIDEOSS0)	0x40A0 0000			10	0
	Subsystem Interface	0x40A0 0000	1	0x80000		
	Video IO	0x40A8 0000	1	0x40000		
	Display Engine	0x40AA 0000	2	0x4000		
	FPD-Link	0x40AC 0000	2	0x400		
	MIPI CSI0	0x40AD 0000	1	0x400		
	VIDEOSS0 Power Domain Control	0x40B0 0000	1	0x400	10	1
	JPEGDEC Decoder	0x40B1 0000	1	0x2000	10	2

Note

22.Remaining 24 external channels are accessed from SAR1 Multiplexer. (SAR0 uses SARMUX1).

7 CYT4DN clock diagram

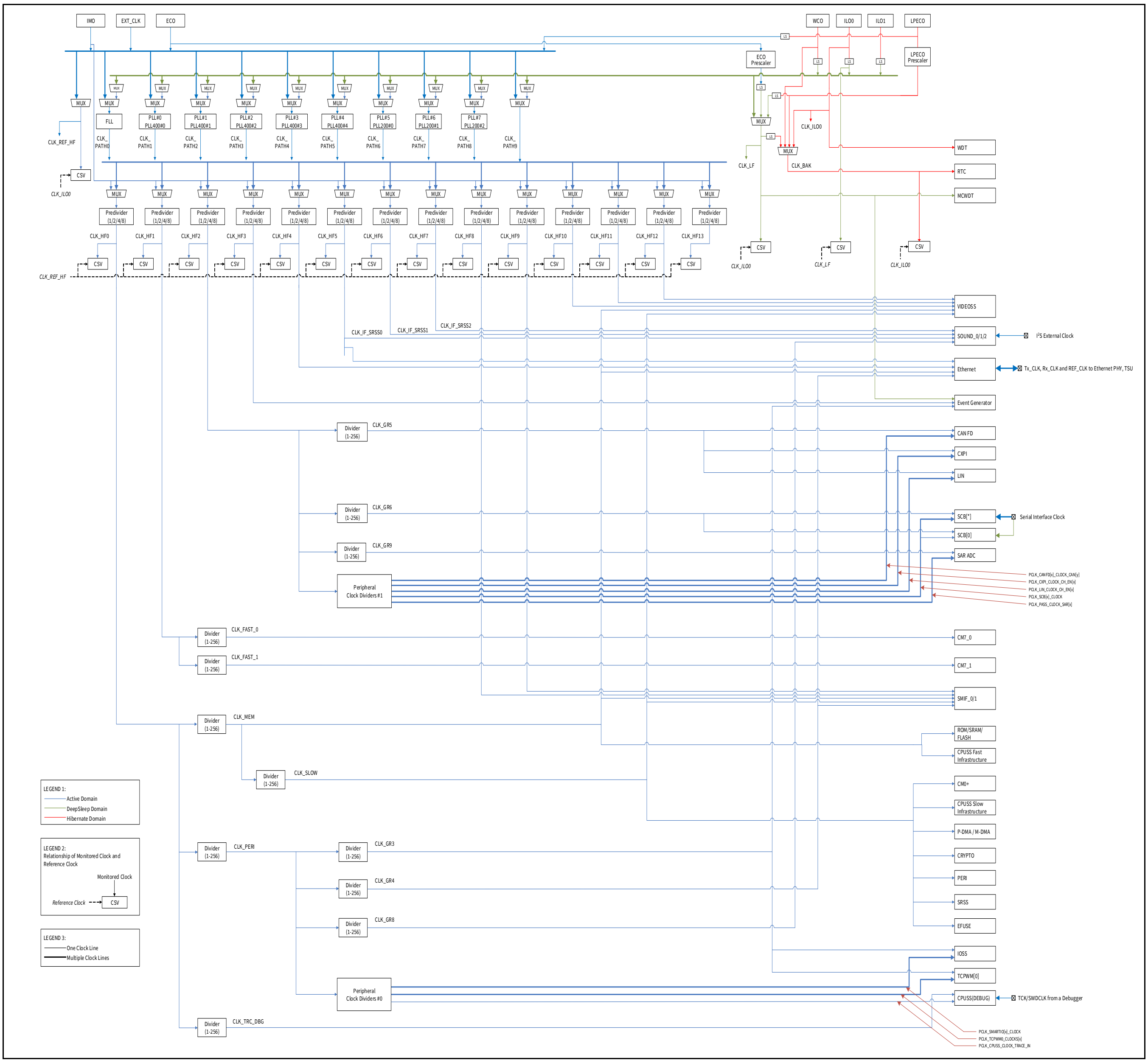


Figure 7-1 CYT4DN clock diagram

8 CYT4DN CPU start-up sequence

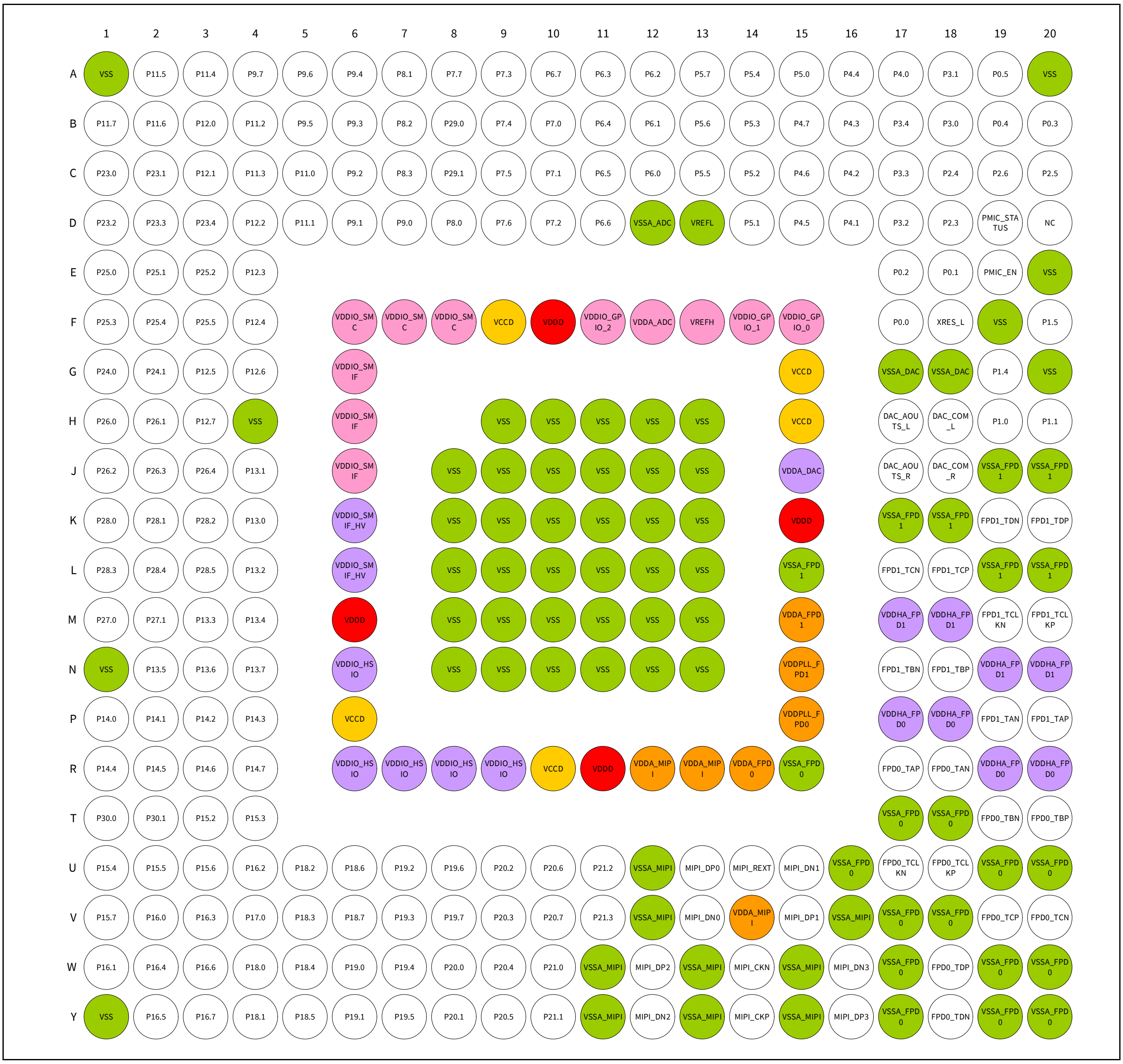
The start-up sequence is described in the following steps:

1. System Reset (@0x0000 0000)
2. CM0+ executes ROM boot (@0x0000 0004)
    i. Applies trims
    ii. Applies Debug Access port (DAP) access restrictions and system protection from eFuse and supervisory flash
    iii. Authenticates flash boot (only in SECURE life-cycle stage) and transfers control to it
3. CM0+ executes flash boot (from Supervisory flash @0x1700 2000)
    i. Debug pins are configured as per the SWD/JTAG spec[23]
    ii. Sets CM0+ vector offset register (CM0_VTOR part of the Arm® system space) to the beginning of flash (@0x1000 0000)
    iii. CM0+ branches to its Reset handler
4. CM0+ starts execution
    i. Moves CM0+ vector table to SRAM (updates CM0+ vector table base)
    i. Sets up wait states for different memory subsystems
    i. Sets up root clocks, enable core external supply (PMIC), graphics subsystem etc.
    i. Sets clocks for CM7_0 (CLK_HF1) and CM7_1 (CLK_HF1)
    ii. Sets CM7_0 (CM7_0_VECTOR_TABLE_BASE @0x4020 0200) and CM7_1 (CM7_1_VECTOR_TABLE_BASE @0x4020 0600) vector tables to the respective locations, also and mentioned in flash (specified in the linker definition file)
    iii. Enables the power for both the CPU cores CM7_0 and CM7_1
    iv. Disables CPU_WAIT so as to be able to be accessed by the debugger
    v. Releases CM7_0 and/or CM7_1 from reset
    vi. Continues execution of CM0+ user application
5. CM7_0 and/or CM7_1 executes directly from either code-flash or SRAM
    i. CM7_0/CM7_1 branches to its Reset handler
    ii. Continues execution of the user application

Note

[23] Port configuration of SWD/JTAG pins will be changed from the default GPIO mode to support debugging after the boot process, refer to **Table 11-1** for pin assignments.

9 Pin assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	P11.5	P11.4	P9.7	P9.6	P9.4	P8.1	P7.7	P7.3	P6.7	P6.3	P6.2	P5.7	P5.4	P5.0	P4.4	P4.0	P3.1	P0.5	VSS
B	P11.7	P11.6	P12.0	P11.2	P9.5	P9.3	P8.2	P29.0	P7.4	P7.0	P6.4	P6.1	P5.6	P5.3	P4.7	P4.3	P3.4	P3.0	P0.4	P0.3
C	P23.0	P23.1	P12.1	P11.3	P11.0	P9.2	P8.3	P29.1	P7.5	P7.1	P6.5	P6.0	P5.5	P5.2	P4.6	P4.2	P3.3	P2.4	P2.6	P2.5
D	P23.2	P23.3	P23.4	P12.2	P11.1	P9.1	P9.0	P8.0	P7.6	P7.2	P6.6	VSSA_ADC	VREFL	P5.1	P4.5	P4.1	P3.2	P2.3	PMIC_STATUS	NC
E	P25.0	P25.1	P25.2	P12.3													P0.2	P0.1	PMIC_EN	VSS
F	P25.3	P25.4	P25.5	P12.4		VDDIO_SMC	VDDIO_SMC	VDDIO_SMC	VCCD	VDDD	VDDIO_GPIO_2	VDDA_ADC	VREFH	VDDIO_GPIO_1	VDDIO_GPIO_0		P0.0	XRES_L	VSS	P1.5
G	P24.0	P24.1	P12.5	P12.6		VDDIO_SMIF									VCCD		VSSA_DAC	VSSA_DAC	P1.4	VSS
H	P26.0	P26.1	P12.7	VSS		VDDIO_SMIF			VSS	VSS	VSS	VSS	VSS		VCCD		DAC_AOUTS_L	DAC_COM_L	P1.0	P1.1
J	P26.2	P26.3	P26.4	P13.1		VDDIO_SMIF		VSS	VSS	VSS	VSS	VSS	VSS		VDDA_DAC		DAC_AOUTS_R	DAC_COM_R	VSSA_FPD1	VSSA_FPD1
K	P28.0	P28.1	P28.2	P13.0		VDDIO_SMIF_HV		VSS	VSS	VSS	VSS	VSS	VSS		VDDD		VSSA_FPD1	VSSA_FPD1	FPD1_TDN	FPD1_TDP
L	P28.3	P28.4	P28.5	P13.2		VDDIO_SMIF_HV		VSS	VSS	VSS	VSS	VSS	VSS		VSSA_FPD1		FPD1_TCN	FPD1_TCP	VSSA_FPD1	VSSA_FPD1
M	P27.0	P27.1	P13.3	P13.4		VDDD		VSS	VSS	VSS	VSS	VSS	VSS		VDDA_FPD1		VDDHA_FPD1	VDDHA_FPD1	FPD1_TCLKN	FPD1_TCLKP
N	VSS	P13.5	P13.6	P13.7		VDDIO_HSIO		VSS	VSS	VSS	VSS	VSS	VSS		VDDPLL_FPD1		FPD1_TBN	FPD1_TBP	VDDHA_FPD1	VDDHA_FPD1
P	P14.0	P14.1	P14.2	P14.3		VCCD									VDDPLL_FPD0		VDDHA_FPD0	VDDHA_FPD0	FPD1_TAN	FPD1_TAP
R	P14.4	P14.5	P14.6	P14.7		VDDIO_HSIO	VDDIO_HSIO	VDDIO_HSIO	VDDIO_HSIO	VCCD	VDDD	VDDA_MIPI	VDDA_MIPI	VDDA_FPD0	VSSA_FPD0		FPD0_TAP	FPD0_TAN	VDDHA_FPD0	VDDHA_FPD0
T	P30.0	P30.1	P15.2	P15.3													VSSA_FPD0	VSSA_FPD0	FPD0_TBN	FPD0_TBP
U	P15.4	P15.5	P15.6	P16.2	P18.2	P18.6	P19.2	P19.6	P20.2	P20.6	P21.2	VSSA_MIPI	MIPI_DP0	MIPI_REXT	MIPI_DN1	VSSA_FPD0	FPD0_TCLKN	FPD0_TCLKP	VSSA_FPD0	VSSA_FPD0
V	P15.7	P16.0	P16.3	P17.0	P18.3	P18.7	P19.3	P19.7	P20.3	P20.7	P21.3	VSSA_MIPI	MIPI_DN0	VDDA_MIPI	MIPI_DP1	VSSA_MIPI	VSSA_FPD0	VSSA_FPD0	FPD0_TCP	FPD0_TCN
W	P16.1	P16.4	P16.6	P18.0	P18.4	P19.0	P19.4	P20.0	P20.4	P21.0	VSSA_MIPI	MIPI_DP2	VSSA_MIPI	MIPI_CKN	VSSA_MIPI	MIPI_DN3	VSSA_FPD0	FPD0_TDP	VSSA_FPD0	VSSA_FPD0
Y	VSS	P16.5	P16.7	P18.1	P18.5	P19.1	P19.5	P20.1	P20.5	P21.1	VSSA_MIPI	MIPI_DN2	VSSA_MIPI	MIPI_CKP	VSSA_MIPI	MIPI_DP3	VSSA_FPD0	FPD0_TDN	VSSA_FPD0	VSSA_FPD0

Figure 9-1 327-BGA ball map

10 High-speed I/O matrix connections

Table 10-1 HSIOM connections reference

Name	Number	Description
HSIOM_SEL_GPIO	0	GPIO controls 'out'
HSIOM_SEL_GPIO_DSI	1	Reserved
HSIOM_SEL_DSI_DSI	2	
HSIOM_SEL_DSI_GPIO	3	
HSIOM_SEL_AMUXA	4	
HSIOM_SEL_AMUXB	5	
HSIOM_SEL_AMUXA_DSI	6	
HSIOM_SEL_AMUXB_DSI	7	
HSIOM_SEL_ACT_0	8	Active functionality 0
HSIOM_SEL_ACT_1	9	Active functionality 1
HSIOM_SEL_ACT_2	10	Active functionality 2
HSIOM_SEL_ACT_3	11	Active functionality 3
HSIOM_SEL_DS_0	12	DeepSleep functionality 0
HSIOM_SEL_DS_1	13	DeepSleep functionality 1
HSIOM_SEL_DS_2	14	DeepSleep functionality 2
HSIOM_SEL_DS_3	15	DeepSleep functionality 3
HSIOM_SEL_ACT_4	16	Active functionality 4
HSIOM_SEL_ACT_5	17	Active functionality 5
HSIOM_SEL_ACT_6	18	Active functionality 6
HSIOM_SEL_ACT_7	19	Active functionality 7
HSIOM_SEL_ACT_8	20	Active functionality 8
HSIOM_SEL_ACT_9	21	Active functionality 9
HSIOM_SEL_ACT_10	22	Active functionality 10
HSIOM_SEL_ACT_11	23	Active functionality 11
HSIOM_SEL_ACT_12	24	Active functionality 12
HSIOM_SEL_ACT_13	25	Active functionality 13
HSIOM_SEL_ACT_14	26	Active functionality 14
HSIOM_SEL_ACT_15	27	Active functionality 15
HSIOM_SEL_DS_4	28	DeepSleep functionality 4
HSIOM_SEL_DS_5	29	DeepSleep functionality 5
HSIOM_SEL_DS_6	30	DeepSleep functionality 6
HSIOM_SEL_DS_7	31	DeepSleep functionality 7

11 Package pin list and alternate functions

Most pins have alternate functionality, as specified in **Table 11-1**.

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[36]

Name	Package	I/O Type	DeepSleep Mapping		Analog/HV	Smart I/O
	327-BGA	HCon#0	HCon#29[31]	HCon#30		
	Pin		DS#5[32, 33]	DS#6		
P0.0	F17	GPIO_ENH				
P0.1	E18	GPIO_ENH			HIBERNATE_WAKEUP[4]	
P0.2	E17	GPIO_ENH		SCB0_SDA		
P0.3	B20	GPIO_ENH		SCB0_SCL	HIBERNATE_WAKEUP[5]	
P0.4	B19	GPIO_ENH				
P0.5	A19	GPIO_ENH				
P1.0	H19	GPIO_STD			ECO_IN[34]	
P1.1	H20	GPIO_STD			ECO_OUT[34]	
P1.4	G19	GPIO_STD			WCO_IN, LPECO_IN[34]	
P1.5	F20	GPIO_STD			WCO_OUT, LPECO_OUT[34]	
P2.3	D18	GPIO_STD	RTC_CAL			
P2.4	C18	GPIO_STD	SWJ_TRSTN		HIBERNATE_WAKEUP[2]	
P2.5	C20	GPIO_STD	RTC_CAL		HIBERNATE_WAKEUP[9]	
P2.6	C19	GPIO_STD	SWJ_SWO_TDO			
P3.0	B18	GPIO_STD	SWJ_SWCLK_TCLK			
P3.1[35]	A18	GPIO_STD			HIBERNATE_WAKEUP[0]	
P3.2	D17	GPIO_STD	SWJ_SWDIO_TMS			
P3.3	C17	GPIO_STD	SWJ_SWDOE_TDI		HIBERNATE_WAKEUP[1]	
P3.4	B17	GPIO_STD				
P4.0	A17	GPIO_STD				
P4.1	D16	GPIO_STD				
P4.2	C16	GPIO_STD				
P4.3	B16	GPIO_STD				
P4.4	A16	GPIO_STD				
P4.5	D15	GPIO_STD			HIBERNATE_WAKEUP[6]	
P4.6	C15	GPIO_STD				
P4.7	B15	GPIO_STD				
P5.0	A15	GPIO_STD				
P5.1	D14	GPIO_STD			HIBERNATE_WAKEUP[7]	
P5.2	C14	GPIO_STD				
P5.3	B14	GPIO_STD			HIBERNATE_WAKEUP[8]	
P5.4	A14	GPIO_STD				
P5.5	C13	GPIO_STD			HIBERNATE_WAKEUP[3]	
P5.6	B13	GPIO_STD			ADC[0]_0	

Notes

[31] HCON (High Speed I/O matrix connection) reference as per **Table 10-1**.

[32] DeepSleep ordering (DS#0, DS#1, DS#2) does not have any impact on choosing any alternate functions; the HSIOM module handles the individual alternate function assignment.

[33] All port pin functions available in DeepSleep mode are also available in Active mode.

[34] I/O pins that support an oscillator function (WCO or ECO) must be configured for high-impedance if the oscillator is enabled.

[35] This I/O will have increased leakage to ground when V_{DDD} is below the POR threshold.

[36] The output pins of FPD and DAC (FPDx_y/DAC_x) peripherals during the reset will be in high impedance state.

[37] See **Table 26-10** 'Serial Communication Block (SCB) specifications' for supported IO-cells and I^2C modes.

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[36] *(continued)*

Name	Package	I/O Type	DeepSleep Mapping		Analog/HV	Smart I/O
	327-BGA	HCon#0	HCon#29[31]	HCon#30		
	Pin		DS#5[32, 33]	DS#6		
P5.7	A13	GPIO_STD			ADC[0]_1	
P6.0	C12	GPIO_STD			ADC[0]_2	
P6.1	B12	GPIO_STD			ADC[0]_3	
P6.2	A12	GPIO_STD			ADC[0]_4	
P6.3	A11	GPIO_STD			ADC[0]_5	
P6.4	B11	GPIO_STD			ADC[0]_6	
P6.5	C11	GPIO_STD			ADC[0]_7	
P6.6	D11	GPIO_STD			ADC[0]_8	
P6.7	A10	GPIO_STD			ADC[0]_9	
P7.0	B10	GPIO_STD			ADC[0]_10	SMARTIO7_0
P7.1	C10	GPIO_STD			ADC[0]_11	SMARTIO7_1
P7.2	D10	GPIO_STD			ADC[0]_12	SMARTIO7_2
P7.3	A9	GPIO_STD			ADC[0]_13	SMARTIO7_3
P7.4	B9	GPIO_STD			ADC[0]_14	SMARTIO7_4
P7.5	C9	GPIO_STD			ADC[0]_15	SMARTIO7_5
P7.6	D9	GPIO_STD			ADC[0]_16	SMARTIO7_6
P7.7	A8	GPIO_STD			ADC[0]_17	SMARTIO7_7
P8.0	D8	GPIO_STD			ADC[0]_20	
P8.1	A7	GPIO_STD			ADC[0]_21	
P8.2	B7	GPIO_STD			ADC[0]_22	
P8.3	C7	GPIO_STD			ADC[0]_23	
P9.0	D7	GPIO_SMC			ADC[1]_0	
P9.1	D6	GPIO_SMC			ADC[1]_1	
P9.2	C6	GPIO_SMC			ADC[1]_2	
P9.3	B6	GPIO_SMC			ADC[1]_3	
P9.4	A6	GPIO_SMC		SCB0_SDA[37]	ADC[1]_4	
P9.5	B5	GPIO_SMC		SCB0_SCL[37]	ADC[1]_5	
P9.6	A5	GPIO_SMC			ADC[1]_6	
P9.7	A4	GPIO_SMC			ADC[1]_7	
P11.0	C5	GPIO_SMC		SCB0_MISO	ADC[1]_8	
P11.1	D5	GPIO_SMC		SCB0_SEL0	ADC[1]_9	
P11.2	B4	GPIO_SMC		SCB0_CLK	ADC[1]_10	
P11.3	C4	GPIO_SMC		SCB0_MOSI	ADC[1]_11	
P11.4	A3	GPIO_SMC		SCB0_MISO	ADC[1]_12	
P11.5	A2	GPIO_SMC		SCB0_SEL0	ADC[1]_13	
P11.6	B2	GPIO_SMC		SCB0_SEL1	ADC[1]_14	
P11.7	B1	GPIO_SMC		SCB0_SEL2	ADC[1]_15	
P12.0	B3	GPIO_SMC		SCB0_SEL3	ADC[1]_16	
P12.1	C3	GPIO_SMC			ADC[1]_17	
P12.2	D4	GPIO_SMC			ADC[1]_18	
P12.3	E4	GPIO_SMC			ADC[1]_19	
P12.4	F4	GPIO_SMC			ADC[1]_20	
P12.5	G3	GPIO_SMC			ADC[1]_21	

Table 11-1 **Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O**[36] *(continued)*

Name	Package	I/O Type	DeepSleep Mapping		Analog/HV	Smart I/O
	327-BGA	HCon#0	HCon#29[31]	HCon#30		
	Pin		DS#5[32, 33]	DS#6		
P12.6	G4	GPIO_SMC			ADC[1]_22	
P12.7	H3	GPIO_SMC			ADC[1]_23	
P13.0	K4	HSIO_STD				
P13.1	J4	HSIO_STD				
P13.2	L4	HSIO_STD				
P13.3	M3	HSIO_STD				
P13.4	M4	HSIO_STD				
P13.5	N2	HSIO_STD				
P13.6	N3	HSIO_STD				
P13.7	N4	HSIO_STD				
P14.0	P1	HSIO_STD				
P14.1	P2	HSIO_STD				
P14.2	P3	HSIO_STD				
P14.3	P4	HSIO_STD				
P14.4	R1	HSIO_STD				
P14.5	R2	HSIO_STD				
P14.6	R3	HSIO_STD				
P14.7	R4	HSIO_STD				
P15.2	T3	HSIO_STDLN				
P15.3	T4	HSIO_STDLN				
P15.4	U1	HSIO_STDLN				
P15.5	U2	HSIO_STDLN				
P15.6	U3	HSIO_STDLN				
P15.7	V1	HSIO_STDLN				
P16.0	V2	HSIO_STDLN				
P16.1	W1	HSIO_STDLN				
P16.2	U4	HSIO_STDLN				
P16.3	V3	HSIO_STDLN				
P16.4	W2	HSIO_STDLN				
P16.5	Y2	HSIO_STDLN				
P16.6	W3	HSIO_STDLN				
P16.7	Y3	HSIO_STDLN				
P17.0	V4	HSIO_STDLN				
P18.0	W4	HSIO_STDLN				
P18.1	Y4	HSIO_STDLN				
P18.2	U5	HSIO_STDLN				
P18.3	V5	HSIO_STDLN				
P18.4	W5	HSIO_STDLN				
P18.5	Y5	HSIO_STDLN				
P18.6	U6	HSIO_STDLN				
P18.7	V6	HSIO_STDLN				
P19.0	W6	HSIO_STDLN				
P19.1	Y6	HSIO_STDLN				

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[36] *(continued)*

Name	Package	I/O Type	DeepSleep Mapping		Analog/HV	Smart I/O
	327-BGA	HCon#0	HCon#29[31]	HCon#30		
	Pin		DS#5[32, 33]	DS#6		
P19.2	U7	HSIO_STDLN				
P19.3	V7	HSIO_STDLN				
P19.4	W7	HSIO_STDLN				
P19.5	Y7	HSIO_STDLN				
P19.6	U8	HSIO_STDLN				
P19.7	V8	HSIO_STDLN				
P20.0	W8	HSIO_STDLN				
P20.1	Y8	HSIO_STDLN				
P20.2	U9	HSIO_STDLN				
P20.3	V9	HSIO_STDLN				
P20.4	W9	HSIO_STDLN				
P20.5	Y9	HSIO_STDLN				
P20.6	U10	HSIO_STDLN				
P20.7	V10	HSIO_STDLN				
P21.0	W10	HSIO_STDLN				
P21.1	Y10	HSIO_STDLN				
P21.2	U11	HSIO_STDLN				
P21.3	V11	HSIO_STDLN				
P23.0	C1	HSIO_ENH				
P23.1	C2	HSIO_ENH				
P23.2	D1	HSIO_ENH				
P23.3	D2	HSIO_ENH				
P23.4	D3	HSIO_ENH				
P24.0	G1	HSIO_ENH_PDIFF[30]				
P24.1	G2	HSIO_ENH_PDIFF[30]				
P25.0	E1	HSIO_ENH				
P25.1	E2	HSIO_ENH				
P25.2	E3	HSIO_ENH				
P25.3	F1	HSIO_ENH				
P25.4	F2	HSIO_ENH				
P25.5	F3	HSIO_ENH				
P26.0	H1	HSIO_ENH				
P26.1	H2	HSIO_ENH				
P26.2	J1	HSIO_ENH				
P26.3	J2	HSIO_ENH				
P26.4	J3	HSIO_ENH				
P27.0	M1	HSIO_ENH_PDIFF[30]				
P27.1	M2	HSIO_ENH_PDIFF[30]				
P28.0	K1	HSIO_ENH				
P28.1	K2	HSIO_ENH				

Note

30.To use SMIF differential clock pin as GPIO output, it is recommended to disable the other associated I/O pin. Refer to the device Architecture TRM for more information.

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[36] *(continued)*

Name	Package	I/O Type	DeepSleep Mapping		Analog/HV	Smart I/O
	327-BGA	HCon#0	HCon#29[31]	HCon#30		
	Pin		DS#5[32, 33]	DS#6		
P28.2	K3	HSIO_ENH				
P28.3	L1	HSIO_ENH				
P28.4	L2	HSIO_ENH				
P28.5	L3	HSIO_ENH				
P29.0	B8	GPIO_ENH			ADC[0]_18	
P29.1	C8	GPIO_ENH			ADC[0]_19	
P30.0	T1	HSIO_STD				
P30.1	T2	HSIO_STD				
MIPI_DP2	W12					
MIPI_DN2	Y12					
MIPI_DN0	V13					
MIPI_DP0	U13					
MIPI_CKP	Y14					
MIPI_CKN	W14					
MIPI_REXT	U14					
MIPI_DP1	V15					
MIPI_DN1	U15					
MIPI_DN3	W16					
MIPI_DP3	Y16					
FPD0_TDN	Y18					
FPD0_TDP	W18					
FPD0_TCN	V20					
FPD0_TCP	V19					
FPD0_TCLKN	U17					
FPD0_TCLKP	U18					
FPD0_TBN	T19					
FPD0_TBP	T20					
FPD0_TAN	R18					
FPD0_TAP	R17					
FPD1_TAP	P20					
FPD1_TAN	P19					
FPD1_TBP	N18					
FPD1_TBN	N17					
FPD1_TCLKP	M20					
FPD1_TCLKN	M19					
FPD1_TCP	L18					
FPD1_TCN	L17					
FPD1_TDP	K20					
FPD1_TDN	K19					
DAC_AOUTS_R	J17					
DAC_COM_R	J18					
DAC_COM_L	H18					
DAC_AOUTS_L	H17					
PMIC_EN	E19					
PMIC_STATUS	D19					
XRES_L	F18					

12 Power pin assignments

Table 12-1 Power pin assignments

Name	Package	Description
	327-BGA	
VDDD	F10, K15, R11, M6	Main supply for SRSS
VDDIO_GPIO_0	F15	Supply for GPIO0 (2.7 V - 5.5 V)
VDDIO_GPIO_1	F14	Supply for GPIO1 (2.7 V - 5.5 V)
VDDIO_GPIO_2	F11	Supply for GPIO2 (2.7 V - 5.5 V)
VDDIO_HSIO	N6, R7, R8, R9, R6	Supply for HSIO domain (3.0 V - 3.6 V)
VDDIO_SMC	F7, F8, F6	Supply for GPIO_SMC (2.7 V - 5.5 V)
VDDIO_SMIF	J6, G6, H6	1.8V supply for 200 MHz HSIO
VDDIO_SMIF_HV	K6, L6	3.3V supply for 200 MHz HSIO
VCCD[31]	F9, G15, H15, R10, P6	Main regulated supply. Driven by LDO regulator
VDDPLL_FPD0	P15	Dedicated supplies for FPD0 (1.09 V - 1.21 V)
VDDPLL_FPD1	N15	Dedicated supplies for FPD1 (1.09 V - 1.21 V)
VDDA_ADC	F12	Main analog supply (for PASS/SAR, 2.7 V - 5.5 V)
VDDA_DAC	J15	Supply for DAC (3.0 V - 3.6 V)
VDDA_FPD0	R14	Dedicated supplies for FPD0 (1.09 V - 1.21 V)
VDDA_FPD1	M15	Dedicated supplies for FPD1 (1.09 V - 1.21 V)
VDDA_MIPI	R13, V14, R12	Dedicated supplies for MIPI (1.09 V - 1.21 V)
VDDHA_FPD0	R19, R20, P17, P18	Dedicated supplies for FPD0 (3.0 V - 3.6 V)
VDDHA_FPD1	M17, M18, N19, N20	Dedicated supplies for FPD1 (3.0 V - 3.6 V)
VREFH	F13	High reference voltage for SAR
VREFL	D13	Low reference voltage for SAR
VSS	A1, A20, H13, E20, F19, G20, H9, H10, H11, H12, J8, J9, J10, J11, J12, J13, K8, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L13, N1, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13, Y1, H4	Main digital ground
VSSA_ADC	D12	Main analog ground
VSSA_DAC	G17, G18	Ground for DAC
VSSA_FPD0	U16, V17, V18, W17, W19, W20, Y17, Y19, Y20, R15, T17, T18, U19, U20	Dedicated ground for FPD0
VSSA_FPD1	J19, J20, K17, K18, L19, L20, L15	Dedicated ground for FPD1
VSSA_MIPI	U12, V12, V16, W11, W13, W15, Y11, Y13, Y15	Dedicated ground for MIPI

Note

31.The V_{CCD} pins must be connected together to ensure a low-impedance connection (see the requirement in **Figure 26-2**).

13 Alternate function pin assignments

Table 13-1 Alternate pin functions in active power mode [33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P0.0		PWM0_20_N			TDM_TX_MCK[2](0)	TDM_RX_MCK[2](0)						LIN1_TX		SCB10_CLK	SCB10_RX	SCB10_SDA
P0.1	PWM0_20		TC0_20_TR		TDM_TX_SCK[2](0)	TDM_RX_SCK[2](0)						LIN1_RX		SCB10_MOSI	SCB10_TX	SCB10_SCL
P0.2		PWM0_21_N			TDM_TX_FSYNC[2](0)	TDM_RX_FSYNC[2](0)							CXPI1_TX	SCB10_MISO	SCB10_RTS	
P0.3	PWM0_21		TC0_21_TR		TDM_TX_SD[2](0)	TDM_RX_SD[2](0)							CXPI1_RX	SCB10_SEL0	SCB10_CTS	
P0.4		PWM0_22_N												SCB11_CLK	SCB11_RX	SCB11_SDA
P0.5	PWM0_22		TC0_22_TR											SCB11_MOSI	SCB11_TX	SCB11_SCL
P1.0											EXT_CLK					
P1.1																
P1.4																
P1.5																
P2.3	PWM0_24		TC0_24_TR							CXPI0_EN		LIN0_EN		CAN1_0_TX		CAL_SUP_NZ
P2.4		PWM0_25_N								CXPI0_RX		LIN0_RX		CAN1_0_RX		
P2.5													DAC_MCK			TRIG_IN[0]
P2.6																
P3.0	PWM0_25		TC0_25_TR							CXPI0_TX		LIN0_TX		CAN0_0_TX		
P3.1		PWM0_26_N												CAN0_0_RX		
P3.2	PWM0_26		TC0_26_TR											CAN0_1_TX		
P3.3		PWM0_27_N									EXT_CLK			CAN0_1_RX		
P3.4	PWM0_27		TC0_27_TR									LIN1_EN	CXPI1_EN	SCB10_SEL1		FAULT_OUT_0
P4.0		PWM0_28_N									SG_AMPL[0](1)		PWM_LINE1_P[0](0)			FAULT_OUT_1
P4.1	PWM0_28		TC0_28_TR								SG_TONE[0](1)		PWM_LINE1_N[0](0)			FAULT_OUT_2
P4.2		PWM0_29_N									SG_AMPL[1](1)		PWM_LINE2_P[0](0)			FAULT_OUT_3
P4.3	PWM0_29		TC0_29_TR								SG_TONE[1](1)		PWM_LINE2_N[0](0)			
P4.4		PWM0_30_N			TDM_TX_MCK[3](0)	TDM_RX_MCK[3](0)				CXPI0_EN	SG_AMPL[2](1)	LIN0_EN	PWM_LINE1_P[1](0)			

Notes

32. High-Speed I/O matrix connection (HCON) reference as per **Table 10-1**.
33. Active Mode ordering (ACT#0, ACT#1, and so on) does not have any impact on configuring alternate functions; the HSIOM module handles the alternate function assignments.
34. Refer to **Table 13-2** for more information on pin multiplexer abbreviations used.
35. For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group “n”.
36. See **Table 26-10** 'Serial Communication Block (SCB) specifications' for supported IO-cells and I^{2}C modes.

Table 13-1 Alternate pin functions in active power mode *(continued)*[33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P4.5	PWM0_30		TC0_30_TR		TDM_TX_SCK[3](0)	TDM_RX_SCK[3](0)				CXPI0_RX	SG_TONE[2](1)	LIN0_RX	PWM_LINE1_N[1](0)			
P4.6		PWM0_31_N			TDM_TX_FSYNC[3](0)	TDM_RX_FSYNC[3](0)				CXPI0_TX	SG_AMPL[3](1)	LIN0_TX	PWM_LINE2_P[1](0)			
P4.7	PWM0_31		TC0_31_TR		TDM_TX_SD[3](0)	TDM_RX_SD[3](0)					SG_TONE[3](1)		PWM_LINE2_N[1](0)			
P5.0	PWM0_H_12	PWM0_H_17_N	TC0_H_16_TR		TDM_TX_MCK[2](1)	TDM_RX_MCK[2](1)								CAN0_0_TX		
P5.1	PWM0_H_13	PWM0_H_12_N	TC0_H_17_TR		TDM_TX_SCK[2](1)	TDM_RX_SCK[2](1)								CAN0_0_RX		
P5.2	PWM0_H_14	PWM0_H_13_N	TC0_H_12_TR		TDM_TX_FSYNC[2](1)	TDM_RX_FSYNC[2](1)					SG_AMPL[0](0)			CAN0_1_TX		
P5.3	PWM0_H_15	PWM0_H_14_N	TC0_H_13_TR		TDM_TX_SD[2](1)	TDM_RX_SD[2](1)					SG_TONE[0](0)			CAN0_1_RX		
P5.4	PWM0_H_16	PWM0_H_15_N	TC0_H_14_TR											CAN1_1_TX		
P5.5	PWM0_H_17	PWM0_H_16_N	TC0_H_15_TR											CAN1_1_RX		
P5.6	PWM0_20	PWM0_29_N	TC0_28_TR		TDM_TX_MCK[3](1)	TDM_RX_MCK[3](1)								SCB8_CLK	SCB8_RX	SCB8_SDA[36]
P5.7	PWM0_21	PWM0_20_N	TC0_29_TR		TDM_TX_SCK[3](1)	TDM_RX_SCK[3](1)								SCB8_MOSI	SCB8_TX	SCB8_SCL[36]
P6.0	PWM0_22	PWM0_21_N	TC0_20_TR		TDM_TX_FSYNC[3](1)	TDM_RX_FSYNC[3](1)								SCB8_MISO	SCB8_RTS	
P6.1	PWM0_23	PWM0_22_N	TC0_21_TR		TDM_TX_SD[3](1)	TDM_RX_SD[3](1)								SCB8_SEL0	SCB8_CTS	
P6.2	PWM0_24	PWM0_23_N	TC0_22_TR											SCB8_SEL1		TRIG_IN[0]
P6.3	PWM0_25	PWM0_24_N	TC0_23_TR													TRIG_IN[29]
P6.4	PWM0_26	PWM0_25_N	TC0_24_TR													TRIG_IN[30]
P6.5	PWM0_27	PWM0_26_N	TC0_25_TR													TRIG_IN[31]
P6.6	PWM0_28	PWM0_27_N	TC0_26_TR													TRIG_IN[32]
P6.7	PWM0_29	PWM0_28_N	TC0_27_TR													TRIG_IN[33]
P7.0	PWM0_20	PWM0_33_N	TC0_32_TR													TRIG_IN[10]
P7.1	PWM0_21	PWM0_20_N	TC0_33_TR										PWM_LINE1_P[0](1)			TRIG_IN[11]
P7.2	PWM0_22	PWM0_21_N	TC0_20_TR										PWM_LINE1_N[0](1)			TRIG_IN[12]
P7.3	PWM0_23	PWM0_22_N	TC0_21_TR										PWM_LINE2_P[0](1)			TRIG_IN[13]
P7.4	PWM0_24	PWM0_23_N	TC0_22_TR										PWM_LINE2_N[0](1)			TRIG_IN[14]
P7.5	PWM0_25	PWM0_24_N	TC0_23_TR										PWM_LINE1_P[1](1)			TRIG_IN[15]
P7.6	PWM0_26	PWM0_25_N	TC0_24_TR		EXT_MUX[0]_0								PWM_LINE1_N[1](1)			TRIG_IN[16]
P7.7	PWM0_27	PWM0_26_N	TC0_25_TR		EXT_MUX[0]_1								PWM_LINE2_P[1](1)			TRIG_IN[17]
P8.0	PWM0_30	PWM0_29_N	TC0_28_TR		EXT_MUX[1]_0									SCB9_MISO	SCB9_RTS	
P8.1	PWM0_31	PWM0_30_N	TC0_29_TR		EXT_MUX[1]_1									SCB9_SEL0	SCB9_CTS	
P8.2	PWM0_32	PWM0_31_N	TC0_30_TR		EXT_MUX[1]_2									SCB9_SEL1		

Table 13-1 Alternate pin functions in active power mode *(continued)*[33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P8.3	PWM0_33	PWM0_32_N	TC0_31_TR		EXT_MUX[1]_EN											
P9.0	PWM0_M_0		TC0_H_18_TR		TDM_TX_MCK[2](2)	TDM_RX_MCK[2](2)					SG_AMPL[1](0)			SCB7_CLK	SCB7_RX	SCB7_SDA[36]
P9.1	PWM0_35	PWM0_M_0_N	TC0_35_TR		TDM_TX_SCK[2](2)	TDM_RX_SCK[2](2)					SG_TONE[1](0)			SCB7_MOSI	SCB7_TX	SCB7_SCL[36]
P9.2	PWM0_M_1	PWM0_35_N	TC0_H_19_TR		TDM_TX_FSYNC[2](2)	TDM_RX_FSYNC[2](2)					SG_AMPL[2](0)			SCB7_MISO	SCB7_RTS	
P9.3	PWM0_36	PWM0_M_1_N	TC0_36_TR		TDM_TX_SD[2](2)	TDM_RX_SD[2](2)					SG_TONE[2](0)			SCB7_SEL0	SCB7_CTS	
P9.4	PWM0_M_2	PWM0_36_N	TC0_H_20_TR			TDM_RX_MCK[3](2)					SG_AMPL[3](0)			SCB7_SEL1	SCB0_RX	
P9.5	PWM0_37	PWM0_M_2_N	TC0_37_TR			TDM_RX_SCK[3](2)					SG_TONE[3](0)				SCB0_TX	
P9.6	PWM0_M_3	PWM0_37_N	TC0_H_21_TR			TDM_RX_FSYNC[3](2)					SG_AMPL[4](0)					FAULT_OUT_0
P9.7		PWM0_M_3_N	TC0_H_22_TR			TDM_RX_SD[3](2)					SG_TONE[4](0)					FAULT_OUT_1
P11.0	PWM0_M_4		TC0_H_2_TR												SCB0_RTS	TRIG_IN[34]
P11.1		PWM0_M_4_N	TC0_H_23_TR												SCB0_CTS	TRIG_IN[35]
P11.2	PWM0_M_5		TC0_H_3_TR													TRIG_IN[36]
P11.3		PWM0_M_5_N	TC0_H_24_TR													TRIG_IN[37]
P11.4	PWM0_M_6		TC0_H_4_TR		TDM_TX_MCK[3](2)	TDM_RX_MCK[3](3)										TRIG_IN[38]
P11.5		PWM0_M_6_N	TC0_H_25_TR		TDM_TX_SCK[3](2)	TDM_RX_SCK[3](3)										TRIG_IN[39]
P11.6	PWM0_M_7		TC0_H_5_TR		TDM_TX_FSYNC[3](2)	TDM_RX_FSYNC[3](3)										TRIG_IN[40]
P11.7		PWM0_M_7_N	TC0_H_26_TR		TDM_TX_SD[3](2)	TDM_RX_SD[3](3)										TRIG_IN[41]
P12.0	PWM0_M_8		TC0_H_6_TR													TRIG_IN[42]
P12.1		PWM0_M_8_N	TC0_H_27_TR													TRIG_IN[43]
P12.2	PWM0_M_9		TC0_H_7_TR													TRIG_IN[44]
P12.3		PWM0_M_9_N	TC0_H_28_TR													TRIG_IN[45]
P12.4	PWM0_M_10		TC0_H_8_TR								SG_AMPL[4](1)					TRIG_IN[46]
P12.5		PWM0_M_10_N	TC0_H_29_TR								SG_TONE[4](1)					TRIG_IN[47]
P12.6	PWM0_M_11		TC0_H_30_TR													
P12.7		PWM0_M_11_N	TC0_H_31_TR													
P13.0	PWM0_32	PWM0_34_N	TC0_33_TR										ETH_MDC			
P13.1	PWM0_33	PWM0_32_N	TC0_34_TR										ETH_MDIO			
P13.2													ETH_TXD_0			
P13.3							TTL_DSP1_CONTROL[3]	TTL_DSP0_CONTROL[3]					ETH_TXD_1			

Table 13-1 Alternate pin functions in active power mode *(continued)*[33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P13.4							TTL_DSP1_CONTROL[4]	TTL_DSP0_CONTROL[4]					ETH_TX_CLK			
P13.5													ETH_REF_CLK			
P13.6													ETH_TXD_2			
P13.7													ETH_TXD_3			
P14.0							TTL_DSP1_CONTROL[5]	TTL_DSP0_CONTROL[5]					ETH_TX_CTL			
P14.1							TTL_DSP1_CONTROL[6]	TTL_DSP0_CONTROL[6]					ETH_TX_ER			
P14.2													ETH_RX_CLK			
P14.3													ETH_RXD_0			
P14.4													ETH_RXD_1			
P14.5							TTL_DSP1_CONTROL[7]	TTL_DSP0_CONTROL[7]					ETH_RXD_2			
P14.6							TTL_DSP1_CONTROL[8]	TTL_DSP0_CONTROL[8]	TRIG_IN[18]				ETH_RXD_3			
P14.7							TTL_DSP1_CONTROL[9]	TTL_DSP0_CONTROL[9]	TRIG_IN[19]				ETH_RX_CTL			
P15.2	PWM0_34	PWM0_33_N	TC0_32_TR				TTL_DSP1_CONTROL[11]	TTL_DSP0_CONTROL[11]			EXT_CLK			SCB1_CLK(1)	SCB1_RX	SCB1_SDA[36]
P15.3	PWM0_H_9	PWM0_H_11_N	TC0_H_10_TR							TTL_CAP0_DATA[26]				SCB1_MOSI(1)	SCB1_TX	SCB1_SCL[36]
P15.4	PWM0_H_10	PWM0_H_9_N	TC0_H_11_TR								EXT_CLK	TTL_CAP0_DATA[25]		SCB1_MISO(1)	SCB1_RTS	CAL_SUP_NZ
P15.5	PWM0_H_11	PWM0_H_10_N	TC0_H_9_TR	TRACE_CLOCK(0)						TTL_CAP0_DATA[24]			PWM_LINE1_P[0](3)	SCB1_SEL0(1)	SCB1_CTS	
P15.6	PWM0_20	PWM0_31_N	TC0_30_TR		TDM_TX_MCK[0](1)	TDM_RX_MCK[0](2)	TDM_RX_MCK[1](2)				SG_MCK[0]	TTL_CAP0_CLK	PWM_LINE1_N[0](3)	SCB1_SEL1(1)		TRIG_IN[22]
P15.7	PWM0_21	PWM0_20_N	TC0_31_TR	TRACE_DATA_0(0)	TDM_TX_SCK[0](1)	TDM_RX_SCK[0](2)	TDM_RX_SCK[1](2)		TTL_DSP1_DATA_A0[0]	TTL_CAP0_DATA[0]	SG_MCK[1]	TTL_CAP0_DATA[23]	PWM_LINE2_P[0](3)			TRIG_IN[23]
P16.0	PWM0_22	PWM0_21_N	TC0_20_TR	TRACE_DATA_1(0)	TDM_TX_FSYNC[0](1)	TDM_RX_FSYNC[0](2)	TDM_RX_FSYNC[1](2)		TTL_DSP1_DATA_A1[0]	TTL_CAP0_DATA[22]	SG_MCK[2]	TTL_CAP0_DATA[1]	PWM_LINE2_N[0](3)			TRIG_IN[24]
P16.1	PWM0_23	PWM0_22_N	TC0_21_TR	TRACE_DATA_2(0)	TDM_TX_SD[0](1)	TDM_RX_SD[0](2)	TDM_RX_SD[1](2)			TTL_CAP0_DATA[2]	SG_MCK[3]	TTL_CAP0_DATA[21]	PWM_LINE1_P[1](3)			TRIG_IN[25]
P16.2	PWM0_24	PWM0_23_N	TC0_22_TR	TRACE_DATA_3(0)	TDM_TX_MCK[1](1)	TDM_RX_MCK[0](3)	TDM_RX_MCK[1](3)			TTL_CAP0_DATA[20]	SG_MCK[4]	TTL_CAP0_DATA[3]	PWM_LINE1_N[1](3)			TRIG_IN[26]
P16.3	PWM0_25	PWM0_24_N	TC0_23_TR	TRACE_DATA_4(0)	TDM_TX_SCK[1](1)	TDM_RX_SCK[0](3)	TDM_RX_SCK[1](3)			TTL_CAP0_DATA[4]	PWM_MCK[0]	TTL_CAP0_DATA[19]				TRIG_IN[27]
P16.4	PWM0_26	PWM0_25_N	TC0_24_TR	TRACE_DATA_5(0)	TDM_TX_FSYNC[1](1)	TDM_RX_FSYNC[0](3)	TDM_RX_FSYNC[1](3)			TTL_CAP0_DATA[18]	PWM_MCK[1]	TTL_CAP0_DATA[5]				
P16.5	PWM0_27	PWM0_26_N	TC0_25_TR	TRACE_DATA_6(0)	TDM_TX_SD[1](1)	TDM_RX_SD[0](3)	TDM_RX_SD[1](3)			TTL_CAP0_DATA[6]		TTL_CAP0_DATA[17]	PWM_LINE2_P[1](3)	SCB1_SEL1(0)		
P16.6	PWM0_28	PWM0_27_N	TC0_26_TR	TRACE_DATA_7(0)						TTL_CAP0_DATA[16]		TTL_CAP0_DATA[7]	PWM_LINE2_N[1](3)	SCB1_SEL0(0)	SCB1_CTS	
P16.7	PWM0_29	PWM0_28_N	TC0_27_TR						TTL_DSP1_DATA_A0[0]	TTL_CAP0_DATA[8]		TTL_CAP0_DATA[15]		SCB1_CLK(0)	SCB1_RX	TRIG_DBG[0]
P17.0	PWM0_30	PWM0_29_N	TC0_28_TR						TTL_DSP1_DATA_A1[0]	TTL_CAP0_DATA[14]		TTL_CAP0_DATA[9]		SCB1_MOSI(0)	SCB1_TX	TRIG_DBG[1]
P18.0	PWM0_32	PWM0_31_N	TC0_30_TR	TRACE_CLOCK(1)						TTL_CAP0_DATA[10]		TTL_CAP0_DATA[13]	TTL_DSP1_DATA_A0[1]	SCB3_CLK	SCB3_RX	SCB3_SDA[36]

Table 13-1 Alternate pin functions in active power mode *(continued)*[33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P18.1	PWM0_33	PWM0_32_N	TC0_31_TR	TRACE_DATA_0(1)						TTL_CAP0_DATA[12]		TTL_CAP0_DATA[11]	TTL_DSP1_DATA_A1[1]	SCB3_MOSI	SCB3_TX	SCB3_SCL[36]
P18.2	PWM0_34	PWM0_33_N	TC0_32_TR	TRACE_DATA_1(1)						TTL_CAP0_DATA[12]		TTL_CAP0_DATA[11]	TTL_DSP1_DATA_A0[2]	SCB3_MISO	SCB3_RTS	
P18.3	PWM0_35	PWM0_34_N	TC0_33_TR	TRACE_DATA_2(1)						TTL_CAP0_DATA[10]		TTL_CAP0_DATA[13]	TTL_DSP1_DATA_A1[2]	SCB3_SEL0	SCB3_CTS	
P18.4	PWM0_36	PWM0_35_N	TC0_34_TR	TRACE_DATA_3(1)						TTL_CAP0_DATA[14]		TTL_CAP0_DATA[9]	TTL_DSP1_DATA_A0[3]	SCB4_CLK	SCB4_RX	SCB4_SDA[36]
P18.5	PWM0_37	PWM0_36_N	TC0_35_TR							TTL_CAP0_DATA[8]		TTL_CAP0_DATA[15]	TTL_DSP1_DATA_A1[3]	SCB4_MOSI	SCB4_TX	SCB4_SCL[36]
P18.6	PWM0_20	PWM0_37_N	TC0_36_TR							TTL_CAP0_DATA[16]		TTL_CAP0_DATA[7]	TTL_DSP1_DATA_A0[4]	SCB4_MISO	SCB4_RTS	
P18.7	PWM0_21	PWM0_20_N	TC0_37_TR							TTL_CAP0_DATA[6]		TTL_CAP0_DATA[17]	TTL_DSP1_DATA_A1[4]	SCB4_SEL0	SCB4_CTS	
P19.0	PWM0_22	PWM0_21_N	TC0_20_TR							TTL_CAP0_DATA[18]		TTL_CAP0_DATA[5]	TTL_DSP1_DATA_A0[5]	SCB3_SEL1		
P19.1	PWM0_23	PWM0_22_N	TC0_21_TR							TTL_CAP0_DATA[4]		TTL_CAP0_DATA[19]	TTL_DSP1_DATA_A1[5]	SCB4_SEL1		
P19.2	PWM0_24	PWM0_23_N	TC0_22_TR							TTL_CAP0_DATA[20]		TTL_CAP0_DATA[3]	TTL_DSP1_DATA_A0[6]	SCB5_CLK	SCB5_RX	SCB5_SDA[36]
P19.3	PWM0_25	PWM0_24_N	TC0_23_TR							TTL_CAP0_DATA[2]		TTL_CAP0_DATA[21]	TTL_DSP1_DATA_A1[6]	SCB5_MOSI	SCB5_TX	SCB5_SCL[36]
P19.4	PWM0_26	PWM0_25_N	TC0_24_TR							TTL_CAP0_DATA[22]		TTL_CAP0_DATA[1]	TTL_DSP1_DATA_A0[7]	SCB5_MISO	SCB5_RTS	
P19.5	PWM0_27	PWM0_26_N	TC0_25_TR							TTL_CAP0_DATA[0]		TTL_CAP0_DATA[23]	TTL_DSP1_DATA_A1[7]	SCB5_SEL0	SCB5_CTS	
P19.6	PWM0_28	PWM0_27_N	TC0_26_TR							TTL_CAP0_DATA[24]			TTL_DSP1_DATA_A0[8]	SCB5_SEL1		
P19.7	PWM0_29	PWM0_28_N	TC0_27_TR									TTL_CAP0_DATA[25]	TTL_DSP1_DATA_A1[8]			TRIG_IN[1]
P20.0	PWM0_30	PWM0_29_N	TC0_28_TR							TTL_CAP0_DATA[26]			TTL_DSP1_DATA_A0[9]			TRIG_IN[2]
P20.1	PWM0_31	PWM0_30_N	TC0_29_TR									TTL_CAP0_CLK	TTL_DSP1_DATA_A1[9]			TRIG_IN[3]
P20.2	PWM0_32	PWM0_31_N	TC0_30_TR		TDM_TX_MCK[0](0)	TDM_RX_MCK[0](0)	TDM_RX_MCK[1](0)						TTL_DSP1_DATA_A0[10]			TRIG_IN[4]
P20.3	PWM0_33	PWM0_32_N	TC0_31_TR		TDM_TX_SCK[0](0)	TDM_RX_SCK[0](0)	TDM_RX_SCK[1](0)						TTL_DSP1_DATA_A1[10]			TRIG_IN[5]
P20.4	PWM0_34	PWM0_33_N	TC0_32_TR		TDM_TX_FSYNC[0](0)	TDM_RX_FSYNC[0](0)	TDM_RX_FSYNC[1](0)						TTL_DSP1_DATA_A0[11]			TRIG_IN[6]
P20.5	PWM0_35	PWM0_34_N	TC0_33_TR		TDM_TX_SD[0](0)	TDM_RX_SD[0](0)	TDM_RX_SD[1](0)						TTL_DSP1_DATA_A1[11]	SCB2_SEL1		TRIG_IN[7]
P20.6	PWM0_36	PWM0_35_N	TC0_34_TR		TDM_TX_MCK[1](0)	TDM_RX_MCK[0](1)	TDM_RX_MCK[1](1)						TTL_DSP1_CONTROL[0]	SCB2_SEL0	SCB2_CTS	TRIG_IN[8]
P20.7	PWM0_37	PWM0_36_N	TC0_35_TR		TDM_TX_SCK[1](0)	TDM_RX_SCK[0](1)	TDM_RX_SCK[1](1)						TTL_DSP1_CONTROL[1]	SCB2_MISO	SCB2_RTS	TRIG_IN[9]
P21.0	PWM0_20	PWM0_37_N	TC0_36_TR		TDM_TX_FSYNC[1](0)	TDM_RX_FSYNC[0](1)	TDM_RX_FSYNC[1](1)						TTL_DSP1_CONTROL[2]	SCB2_CLK	SCB2_RX	SCB2_SDA[36]
P21.1	PWM0_21	PWM0_20_N	TC0_37_TR		TDM_TX_SD[1](0)	TDM_RX_SD[0](1)	TDM_RX_SD[1](1)						TTL_DSP1_CLOCK	SCB2_MOSI	SCB2_TX	SCB2_SCL[36]
P21.2	PWM0_22	PWM0_21_N	TC0_20_TR										PWM_LINE1_P[0](2)	CAN1_0_TX		
P21.3	PWM0_23	PWM0_22_N	TC0_21_TR										PWM_LINE1_N[0](2)	CAN1_0_RX		
P23.0																SPIHB[0]_DATA4[0]

Table 13-1 Alternate pin functions in active power mode *(continued)*[33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P23.1																SPIHB[0]_DATA2[0]
P23.2																SPIHB[0]_DATA3[0]
P23.3																SPIHB[0]_DATA5[0]
P23.4																SPIHB[0]_RWDS[0]
P24.0																SPIHB[0]_CLK_INV[0][38]
P24.1																SPIHB[0]_CLK[0][37]
P25.0																SPIHB[0]_DATA0[0]
P25.1																SPIHB[0]_DATA6[0]
P25.2																SPIHB[0]_SELECT0[0]
P25.3																SPIHB[0]_DATA1[0]
P25.4																SPIHB[0]_DATA7[0]
P25.5																SPIHB[0]_SELECT1[0]
P26.0																SPIHB[0]_DATA4[1]
P26.1																SPIHB[0]_DATA2[1]
P26.2																SPIHB[0]_DATA3[1]
P26.3																SPIHB[0]_DATA5[1]
P26.4																SPIHB[0]_RWDS[1]
P27.0																SPIHB[0]_CLK_INV[1][38]
P27.1																SPIHB[0]_CLK[1][37]
P28.0																SPIHB[0]_DATA0[1]
P28.1																SPIHB[0]_DATA6[1]
P28.2																SPIHB[0]_SELECT0[1]
P28.3																SPIHB[0]_DATA1[1]
P28.4																SPIHB[0]_DATA7[1]
P28.5																SPIHB[0]_SELECT1[1]
P29.0	PWM0_28	PWM0_27_N	TC0_26_TR		EXT_MUX[0]_2						CLK_FM_PUMP		PWM_LINE2_N[1](1)	SCB9_CLK	SCB9_RX	SCB9_SDA
P29.1	PWM0_29	PWM0_28_N	TC0_27_TR		EXT_MUX[0]_EN									SCB9_MOSI	SCB9_TX	SCB9_SCL
P30.0									TRIG_IN[20]				ETH_RX_ER			

Table 13-1 Alternate pin functions in active power mode *(continued)*[33, 34, 35]

Name	Active Mapping															
	HCon#8[32]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#22	HCon#23	HCon#24	HCon#25	HCon#26	HCon#27
	ACT#0[33]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#10	ACT#11	ACT#12	ACT#13	ACT#14	ACT#15
P30.1							TTL_DSP1_CONTROL[10]	TTL_DSP0_CONTROL[10]	TRIG_IN[21]		IO_CLK_HF[5]		ETH_TSU_TIMER_CMP_VAL			

Notes
37.This clock is used as a feedback clock in SPI mode.
38.This clock must not be selected when using feedback clock in SPI mode.

13.1 Pin function description

Table 13-2 Pin function description

Sl. No.	Pin	Module	Description
1	PWMx_y	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
2	PWMx_y_N	TCPWM	TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
3	PWMx_M_y[39]	TCPWM	TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number
4	PWMx_M_y_N[39]	TCPWM	TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number
5	PWMx_H_y	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number
6	PWMx_H_y_N	TCPWM	TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number
7	TCx_y_TRz	TCPWM	TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
8	TCx_H_y_TRz	TCPWM	TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number
9	SCBx_RX	SCB	UART Receive, x-SCB block
10	SCBx_TX	SCB	UART Transmit, x-SCB block
11	SCBx_RTS	SCB	UART Request to Send (Handshake), x-SCB block
12	SCBx_CTS	SCB	UART Clear to Send (Handshake), x-SCB block
13	SCBx_SDA	SCB	I^2C Data line, x-SCB block
14	SCBx_SCL	SCB	I^2C Clock line, x-SCB block
15	SCBx_MISO	SCB	SPI Master Input Slave Output, x-SCB block
16	SCBx_MOSI	SCB	SPI Master Output Slave Input, x-SCB block
17	SCBx_CLK	SCB	SPI Serial Clock, x-SCB block
18	SCBx_SELy	SCB	SPI Slave Select, x-SCB block, y-select line
19	LINx_RX	LIN	LIN Receive line, x-LIN block
20	LINx_TX	LIN	LIN Transmit line, x-LIN block
21	LINx_EN	LIN	LIN Enable line, x-LIN block
22	CXPIx_RX	CXPI	CXPI Receive line, x-CXPI block
23	CXPIx_TX	CXPI	CXPI Transmit line, x-CXPI block
24	CXPIx_EN	CXPI	CXPI Enable line, x-CXPI block
25	CANx_y_TX	CANFD	CAN Transmit line, x-CAN block, y-channel number
26	CANx_y_RX	CANFD	CAN Receive line, x-CAN block, y-channel number
27	SPIHB[x]_CLK[y]/CLK_INV[y]	SMIF	SMIF interface clock/inverted clock, x-SMIF block number, y-device number
28	SPIHB[x]_RWDS[y]	SMIF	SMIF (SPI/xSPI) read-write-data-strobe line, x-SMIF block number, y-device number
29	SPIHB[x]_SELECTy[z]	SMIF	SMIF (SPI/xSPI) memory select line, x-SMIF block number, y-select line number, z-device number
30	SPIHB[x]_DATAy[z]	SMIF	SMIF (SPI/xSPI) memory data read and write line, x-SMIF block number, y-0 to 7 data lines, z-device number
31	ETHx_RX_ER	Ethernet	Ethernet receive error indication line, x-ETH module number
32	ETHx_ETH_TSU_TIMER_C-MP_VAL	Ethernet	Ethernet time stamp unit timer compare indication line, x-ETH module number
33	ETHx_MDIO	Ethernet	Ethernet management data input/output (MDIO) interface to PHY, x-ETH module number
34	ETHx_MDC	Ethernet	Ethernet management data clock (MDC) line, x-ETH module number
35	ETHx_REF_CLK	Ethernet	Ethernet reference clock line, x-ETH module number
36	ETHx_TX_CTL	Ethernet	Ethernet transmit control line, x-ETH module number
37	ETHx_TX_ER	Ethernet	Ethernet transmit error indication line, x-ETH module number
38	ETHx_TX_CLK	Ethernet	Ethernet transmit clock line, x-ETH module number

Note
39.This pin/line is intended for a direct connection to the coil of stepper motor for pointer instruments.

Table 13-2 Pin function description *(continued)*

Sl. No.	Pin	Module	Description
39	ETHx_TXD_y	Ethernet	Ethernet transmit data line, x-ETH module number, y-transmit channel number
40	ETHx_RXD_y	Ethernet	Ethernet receive data line, x-ETH module number, y-receive channel number
41	ETHx_RX_CTL	Ethernet	Ethernet receive control line, x-ETH module number
42	ETHx_RX_CLK	Ethernet	Ethernet receive clock line, x-ETH module number
43	CAL_SUP_NZ	System	ETAS Calibration support line
44	FAULT_OUT_x	SRSS	Fault output line x-0 to 3
45	TRACE_DATA_x	SRSS	Trace data-out line x-0 to 3
46	TRACE_CLOCK	SRSS	Trace clock line
47	RTC_CAL	SRSS RTC	RTC calibration clock input
48	SWJ_TRSTN	SRSS	JTAG Test reset line (Active low)
49	SWJ_SWO_TDO	SRSS	JTAG Test data output/SWO (Serial Wire Output)
50	SWJ_SWCLK_TCLK	SRSS	JTAG Test clock/SWD clock (Serial Wire Clock)
51	SWJ_SWDIO_TMS	SRSS	JTAG Test mode select/SWD data (Serial Wire Data Input/Output)
52	SWJ_SWDOE_TDI	SRSS	JTAG Test data input
53	HIBERNATE_WAKEUP[x]	SRSS	Hibernate wakeup line x-0 to N (Check **Table 11-1**)
54	EXT_CLK	SRSS	External clock input
55	IO_CLK_HF[5]	SRSS	CLK_HF5 clock output
56	PMIC_EN	SRSS PMIC	PMIC control line, Enable output for PMIC
57	PMIC_STATUS	SRSS PMIC	PMIC status line, Power good input from PMIC
58	ADC[x]_y	PASS SAR	SAR, channel, x-SAR number, y-channel number
59	ADC[x]_M	PASS SAR	SAR motor control input, x-SAR number
60	EXT_MUX[x]_y	PASS SAR	External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2
61	EXT_MUX[x]_EN	PASS SAR	External SAR MUX enable line
62	PWM_LINEx_N[y]	PCMPWM	Audio PWM complementary output line, x-PWM module instance
63	PWM_LINEx_P[y]	PCMPWM	Audio PWM output line, x-PWM module instance
64	PWM_MCK[x]	PCMPWM	Audio PWM master clock input, x-PWM module instance
65	SG_AMPL[x]	SG	Sound generator (SG) amplitude output, x-SG module number
66	SG_MCK[x]	SG	Sound generator (SG) master clock input, x-SG module number
67	SG_TONE[x]	SG	Sound generator (SG) tone output, x-SG module number
68	TDM_RX_FSYNC[x]	TDM	TDM receive frame sync, x-TDM module number
69	TDM_RX_MCK[x]	TDM	TDM receive master clock input, x-TDM module number
70	TDM_RX_SCK[x]	TDM	TDM receive bit clock, x-TDM module number
71	TDM_RX_SD[x]	TDM	TDM receive serial data, x-TDM module number
72	TDM_TX_FSYNC[x]	TDM	TDM transmit frame sync, x-TDM module number
73	TDM_TX_MCK[x]	TDM	TDM transmit master clock input, x-TDM module number
74	TDM_TX_SCK[x]	TDM	TDM transmit bit clock, x-TDM module number
75	TDM_TX_SD[x]	TDM	TDM transmit serial data, x-TDM module number
76	TTL_CAPx_CLK	VIDEOSS	Capture clock, x-capture module number
77	TTL_CAPx_DATA[y]	VIDEOSS	Capture data lines, x-capture module number, y- (0-26) data line
78	TTL_DSPx_CONTROL[y]	VIDEOSS	Display control line, x-display number, y-0/lvalid, 1/vertical sync signal, 2/display enable (DE)
79	TTL_DSPx_CLOCK	VIDEOSS	Display clock line (PCLK), x-display number
80	TTL_DSPx_DATA_A0[y]	VIDEOSS	Display data (A0/1 used in pairs), x-display number, y- (0-11) color data
81	TTL_DSPx_DATA_A1[y]	VIDEOSS	Display data (A0/1 used in pairs), x-display number, y- (0-11) color data
82	DAC_MCK	AUDIODAC	DAC external master clock input
83	DAC_AOUTS_x	AUDIODAC	DAC output signal, x-left (L) or right (R) signal

Table 13-2 Pin function description *(continued)*

Sl. No.	Pin	Module	Description
84	DAC_COM_x	AUDIODAC	DAC common signal, x-left (L) or right (R) signal
85	MIPI_DPx	VIDEOSS	MIPI CSI-2 positive Data-Y input signal
86	MIPI_DNx	VIDEOSS	MIPI CSI-2 negative Data-Y input signal
87	MIPI_CKP	VIDEOSS	MIPI CSI-2 positive clock input signal
88	MIPI_CKN	VIDEOSS	MIPI CSI-2 negative clock input signal
89	MIPI_REXT	VIDEOSS	MIPI CSI-2 external reference resistor pin for auto-calibration
90	FPDx_TyP	VIDEOSS	FPD-link positive transmit signal, x-FPD instance, y-(0-3/A-C) output signal
91	FPDx_TyN	VIDEOSS	FPD-link negative transmit signal, x-FPD instance, y-(0-3/A-C) output signal
92	FPDx_TCLKP	VIDEOSS	FPD-link positive clock signal, x-FPD instance
93	FPDx_TCLKN	VIDEOSS	FPD-link negative clock signal, x-FPD instance

14 Interrupts and wake-up assignments

Table 14-1 Peripheral interrupt assignments and wake-up sources

Interrupt	Source	Power mode	Description
0	cpuss_interrupts_ipc_0_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #0
1	cpuss_interrupts_ipc_1_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #1
2	cpuss_interrupts_ipc_2_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #2
3	cpuss_interrupts_ipc_3_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #3
4	cpuss_interrupts_ipc_4_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #4
5	cpuss_interrupts_ipc_5_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #5
6	cpuss_interrupts_ipc_6_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #6
7	cpuss_interrupts_ipc_7_IRQn	DeepSleep	CPUSS Inter Process Communication Interrupt #7
8	cpuss_interrupts_fault_0_IRQn	DeepSleep	CPUSS Fault Structure #0 Interrupt
9	cpuss_interrupts_fault_1_IRQn	DeepSleep	CPUSS Fault Structure #1 Interrupt
10	cpuss_interrupts_fault_2_IRQn	DeepSleep	CPUSS Fault Structure #2 Interrupt
11	cpuss_interrupts_fault_3_IRQn	DeepSleep	CPUSS Fault Structure #3 Interrupt
12	srss_interrupt_backup_IRQn	DeepSleep	BACKUP domain Interrupt
13	srss_interrupt_mcwdt_0_IRQn	DeepSleep	Multi Counter Watchdog Timer#0 interrupt
14	srss_interrupt_mcwdt_1_IRQn	DeepSleep	Multi Counter Watchdog Timer#1 interrupt
15	srss_interrupt_mcwdt_2_IRQn	DeepSleep	Multi Counter Watchdog Timer#2 interrupt
17	srss_interrupt_wdt_IRQn	DeepSleep	Hardware Watchdog Timer interrupt
18	srss_interrupt_IRQn	DeepSleep	Other combined Interrupts for SRSS (LVD, CLKCAL)
19	evtgen_0_interrupt_dpslp_IRQn	DeepSleep	Event gen DeepSleep domain interrupt
20	scb_0_interrupt_IRQn	DeepSleep	SCB0 interrupt (DeepSleep capable)
22	ioss_interrupt_vdd_IRQn	DeepSleep	I/O Supply (VDDIO, VDDA_ADC, VDDD) state change Interrupt
23	ioss_interrupt_gpio_dpslp_IRQn	DeepSleep	Consolidated Interrupt for GPIO*, All Ports
24	ioss_interrupts_gpio_dpslp_0_IRQn	DeepSleep	GPIO_ENH Port #0 Interrupt
25	ioss_interrupts_gpio_dpslp_1_IRQn	DeepSleep	GPIO_STD Port #1 Interrupt
26	ioss_interrupts_gpio_dpslp_2_IRQn	DeepSleep	GPIO_STD Port #2 Interrupt
27	ioss_interrupts_gpio_dpslp_3_IRQn	DeepSleep	GPIO_STD Port #3 Interrupt
28	ioss_interrupts_gpio_dpslp_4_IRQn	DeepSleep	GPIO_STD Port #4 Interrupt
29	ioss_interrupts_gpio_dpslp_5_IRQn	DeepSleep	GPIO_STD Port #5 Interrupt
30	ioss_interrupts_gpio_dpslp_6_IRQn	DeepSleep	GPIO_STD Port #6 Interrupt
31	ioss_interrupts_gpio_dpslp_7_IRQn	DeepSleep	GPIO_STD Port #7 Interrupt
32	ioss_interrupts_gpio_dpslp_8_IRQn	DeepSleep	GPIO_STD Port #8 Interrupt
33	ioss_interrupts_gpio_dpslp_9_IRQn	DeepSleep	GPIO_SMC Port #9 Interrupt
35	ioss_interrupts_gpio_dpslp_11_IRQn	DeepSleep	GPIO_SMC Port #11 Interrupt
36	ioss_interrupts_gpio_dpslp_12_IRQn	DeepSleep	GPIO_SMC Port #12 Interrupt
37	ioss_interrupts_gpio_dpslp_29_IRQn	DeepSleep	GPIO_ENH Port #29 Interrupt
50	ioss_interrupt_gpio_act_IRQn	Active	Consolidated Interrupt for HSIO*, All Ports
53	ioss_interrupts_gpio_act_13_IRQn	Active	HSIO_STD Port Interrupt #13 Interrupt
54	ioss_interrupts_gpio_act_14_IRQn	Active	HSIO_STD Port Interrupt #14 Interrupt
55	ioss_interrupts_gpio_act_15_IRQn	Active	HSIO_STD_LN Port Interrupt #15 Interrupt
56	ioss_interrupts_gpio_act_16_IRQn	Active	HSIO_STD_LN Port Interrupt #16 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
57	ioss_interrupts_gpio_act_17_IRQn	Active	HSIO_STD_LN Port Interrupt #17 Interrupt
58	ioss_interrupts_gpio_act_18_IRQn	Active	HSIO_STD_LN Port Interrupt #18 Interrupt
59	ioss_interrupts_gpio_act_19_IRQn	Active	HSIO_STD_LN Port Interrupt #19 Interrupt
60	ioss_interrupts_gpio_act_20_IRQn	Active	HSIO_STD_LN Port Interrupt #20 Interrupt
61	ioss_interrupts_gpio_act_21_IRQn	Active	HSIO_STD_LN Port Interrupt #21 Interrupt
63	ioss_interrupts_gpio_act_23_IRQn	Active	HSIO_ENH Port Interrupt #23 Interrupt
64	ioss_interrupts_gpio_act_24_IRQn	Active	HSIO_ENH_PDIFF Port Interrupt #24 Interrupt
65	ioss_interrupts_gpio_act_25_IRQn	Active	HSIO_ENH Port Interrupt #25 Interrupt
66	ioss_interrupts_gpio_act_26_IRQn	Active	HSIO_ENH Port Interrupt #26 Interrupt
67	ioss_interrupts_gpio_act_27_IRQn	Active	HSIO_ENH_PDIFF Port Interrupt #27 Interrupt
68	ioss_interrupts_gpio_act_28_IRQn	Active	HSIO_ENH Port Interrupt #28 Interrupt
69	ioss_interrupts_gpio_act_30_IRQn	Active	HSIO_STD Port Interrupt #30 Interrupt
70	cpuss_interrupt_crypto_IRQn	Active	Crypto Accelerator Interrupt
71	cpuss_interrupt_fm_IRQn	Active	FLASH Macro Interrupt
72	cpuss_interrupts_cm7_0_fp_IRQn	Active	CM7_0 Floating Point operation fault
73	cpuss_interrupts_cm7_1_fp_IRQn	Active	CM7_1 Floating Point operation fault
74	cpuss_interrupts_cm0_cti_0_IRQn	Active	CM0+ CTI (Cross Trigger Interface) #0
75	cpuss_interrupts_cm0_cti_1_IRQn	Active	CM0+ CTI #1
76	cpuss_interrupts_cm7_0_cti_0_IRQn	Active	CM7_0 CTI #0
77	cpuss_interrupts_cm7_0_cti_1_IRQn	Active	CM7_0 CTI #1
78	cpuss_interrupts_cm7_1_cti_0_IRQn	Active	CM7_1 CTI #0
79	cpuss_interrupts_cm7_1_cti_1_IRQn	Active	CM7_1 CTI #1
80	evtgen_0_interrupt_IRQn	Active	Event gen Active domain interrupt
81	smif_0_interrupt_IRQn	Active	SMIF #0 (QSPI) interrupt
82	smif_1_interrupt_IRQn	Active	SMIF #1 (QSPI) interrupt
83	eth_0_interrupt_eth_0_IRQn	Active	Ethernet #0 priority queue[0]
84	eth_0_interrupt_eth_1_IRQn	Active	Ethernet #0 priority queue[1]
85	eth_0_interrupt_eth_2_IRQn	Active	Ethernet #0 priority queue[2]
86	canfd_0_interrupt0_IRQn	Active	CAN0, Consolidated interrupt #0 for all channels
87	canfd_0_interrupt1_IRQn	Active	CAN0, Consolidated interrupt #1 for all channels
88	canfd_1_interrupt0_IRQn	Active	CAN1, Consolidated interrupt #0 for all channels
89	canfd_1_interrupt1_IRQn	Active	CAN1, Consolidated interrupt #1 for all channels
90	canfd_0_interrupts0_0_IRQn	Active	CAN0, Interrupt #0, Channel #0
91	canfd_0_interrupts0_1_IRQn	Active	CAN0, Interrupt #0, Channel #1
96	canfd_0_interrupts1_0_IRQn	Active	CAN0, Interrupt #1, Channel #0
97	canfd_0_interrupts1_1_IRQn	Active	CAN0, Interrupt #1, Channel #1
102	canfd_1_interrupts0_0_IRQn	Active	CAN1, Interrupt #0, Channel #0
103	canfd_1_interrupts0_1_IRQn	Active	CAN1, Interrupt #0, Channel #1
108	canfd_1_interrupts1_0_IRQn	Active	CAN1, Interrupt #1, Channel #0
109	canfd_1_interrupts1_1_IRQn	Active	CAN1, Interrupt #1, Channel #1
114	lin_0_interrupts_0_IRQn	Active	LIN0 Channel #0 Interrupt
115	lin_0_interrupts_1_IRQn	Active	LIN0 Channel #1 Interrupt
130	cxpi_0_interrupts_0_IRQn	Active	CXPI0 Channel #0 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
131	cxpi_0_interrupts_1_IRQn	Active	CXPI0 Channel #1 Interrupt
135	scb_1_interrupt_IRQn	Active	SCB1 Interrupt
136	scb_2_interrupt_IRQn	Active	SCB2 Interrupt
137	scb_3_interrupt_IRQn	Active	SCB3 Interrupt
138	scb_4_interrupt_IRQn	Active	SCB4 Interrupt
139	scb_5_interrupt_IRQn	Active	SCB5 Interrupt
140	scb_6_interrupt_IRQn	Active	SCB6 Interrupt
141	scb_7_interrupt_IRQn	Active	SCB7 Interrupt
142	scb_8_interrupt_IRQn	Active	SCB8 Interrupt
143	scb_9_interrupt_IRQn	Active	SCB9 Interrupt
144	scb_10_interrupt_IRQn	Active	SCB10 Interrupt
145	scb_11_interrupt_IRQn	Active	SCB11 Interrupt
150	videoss_0_interrupt_gfx2d_IRQn	Active	GFX2D Interrupt
151	videoss_0_interrupt_mipicsi_IRQn	Active	MIPICSI Interrupt
152	videoss_0_interrupt_videoio0_IRQn	Active	VIDEOSS I/O Interrupt #0
153	videoss_0_interrupt_videoio1_IRQn	Active	VIDEOSS I/O Interrupt #1
154	videoss_0_interrupt_videoio0_safety_IRQn	Active	VIDEOSS I/O Safety Interrupt #0
155	videoss_0_interrupt_videoio1_safety_IRQn	Active	VIDEOSS I/O Safety Interrupt #1
156	jpegdec.interrupt_jpeg	Active	JPEG Decoder Interrupt
160	pass_0_interrupts_sar_0_IRQn	Active	SAR0, Logical Channel #0 Interrupt
161	pass_0_interrupts_sar_1_IRQn	Active	SAR0, Logical Channel #1 Interrupt
162	pass_0_interrupts_sar_2_IRQn	Active	SAR0, Logical Channel #2 Interrupt
163	pass_0_interrupts_sar_3_IRQn	Active	SAR0, Logical Channel #3 Interrupt
164	pass_0_interrupts_sar_4_IRQn	Active	SAR0, Logical Channel #4 Interrupt
165	pass_0_interrupts_sar_5_IRQn	Active	SAR0, Logical Channel #5 Interrupt
166	pass_0_interrupts_sar_6_IRQn	Active	SAR0, Logical Channel #6 Interrupt
167	pass_0_interrupts_sar_7_IRQn	Active	SAR0, Logical Channel #7 Interrupt
168	pass_0_interrupts_sar_8_IRQn	Active	SAR0, Logical Channel #8 Interrupt
169	pass_0_interrupts_sar_9_IRQn	Active	SAR0, Logical Channel #9 Interrupt
170	pass_0_interrupts_sar_10_IRQn	Active	SAR0, Logical Channel #10 Interrupt
171	pass_0_interrupts_sar_11_IRQn	Active	SAR0, Logical Channel #11 Interrupt
172	pass_0_interrupts_sar_12_IRQn	Active	SAR0, Logical Channel #12 Interrupt
173	pass_0_interrupts_sar_13_IRQn	Active	SAR0, Logical Channel #13 Interrupt
174	pass_0_interrupts_sar_14_IRQn	Active	SAR0, Logical Channel #14 Interrupt
175	pass_0_interrupts_sar_15_IRQn	Active	SAR0, Logical Channel #15 Interrupt
176	pass_0_interrupts_sar_16_IRQn	Active	SAR0, Logical Channel #16 Interrupt
177	pass_0_interrupts_sar_17_IRQn	Active	SAR0, Logical Channel #17 Interrupt
178	pass_0_interrupts_sar_18_IRQn	Active	SAR0, Logical Channel #18 Interrupt
179	pass_0_interrupts_sar_19_IRQn	Active	SAR0, Logical Channel #19 Interrupt
180	pass_0_interrupts_sar_20_IRQn	Active	SAR0, Logical Channel #20 Interrupt
181	pass_0_interrupts_sar_21_IRQn	Active	SAR0, Logical Channel #21 Interrupt
182	pass_0_interrupts_sar_22_IRQn	Active	SAR0, Logical Channel #22 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
183	pass_0_interrupts_sar_23_IRQn	Active	SAR0, Logical Channel #23 Interrupt
184	pass_0_interrupts_sar_24_IRQn	Active	SAR0, Logical Channel #24 Interrupt
185	pass_0_interrupts_sar_25_IRQn	Active	SAR0, Logical Channel #25 Interrupt
186	pass_0_interrupts_sar_26_IRQn	Active	SAR0, Logical Channel #26 Interrupt
187	pass_0_interrupts_sar_27_IRQn	Active	SAR0, Logical Channel #27 Interrupt
188	pass_0_interrupts_sar_28_IRQn	Active	SAR0, Logical Channel #28 Interrupt
189	pass_0_interrupts_sar_29_IRQn	Active	SAR0, Logical Channel #29 Interrupt
190	pass_0_interrupts_sar_30_IRQn	Active	SAR0, Logical Channel #30 Interrupt
191	pass_0_interrupts_sar_31_IRQn	Active	SAR0, Logical Channel #31 Interrupt
280	axi_dmac_0_interrupts_0_IRQn	Active	CPUSS AXI M-DMA1, Channel #0 Interrupt
281	axi_dmac_0_interrupts_1_IRQn	Active	CPUSS AXI M-DMA1, Channel #1 Interrupt
282	axi_dmac_0_interrupts_2_IRQn	Active	CPUSS AXI M-DMA1, Channel #2 Interrupt
283	axi_dmac_0_interrupts_3_IRQn	Active	CPUSS AXI M-DMA1, Channel #3 Interrupt
288	cpuss_interrupts_dmac_0_IRQn	Active	CPUSS M-DMA0, Channel #0 Interrupt
289	cpuss_interrupts_dmac_1_IRQn	Active	CPUSS M-DMA0, Channel #1 Interrupt
290	cpuss_interrupts_dmac_2_IRQn	Active	CPUSS M-DMA0, Channel #2 Interrupt
291	cpuss_interrupts_dmac_3_IRQn	Active	CPUSS M-DMA0, Channel #3 Interrupt
292	cpuss_interrupts_dmac_4_IRQn	Active	CPUSS M-DMA0, Channel #4 Interrupt
293	cpuss_interrupts_dmac_5_IRQn	Active	CPUSS M-DMA0, Channel #5 Interrupt
294	cpuss_interrupts_dmac_6_IRQn	Active	CPUSS M-DMA0, Channel #6 Interrupt
295	cpuss_interrupts_dmac_7_IRQn	Active	CPUSS M-DMA0, Channel #7 Interrupt
296	cpuss_interrupts_dw0_0_IRQn	Active	CPUSS P-DMA0, Channel #0 Interrupt
297	cpuss_interrupts_dw0_1_IRQn	Active	CPUSS P-DMA0, Channel #1 Interrupt
298	cpuss_interrupts_dw0_2_IRQn	Active	CPUSS P-DMA0, Channel #2 Interrupt
299	cpuss_interrupts_dw0_3_IRQn	Active	CPUSS P-DMA0, Channel #3 Interrupt
300	cpuss_interrupts_dw0_4_IRQn	Active	CPUSS P-DMA0, Channel #4 Interrupt
301	cpuss_interrupts_dw0_5_IRQn	Active	CPUSS P-DMA0, Channel #5 Interrupt
302	cpuss_interrupts_dw0_6_IRQn	Active	CPUSS P-DMA0, Channel #6 Interrupt
303	cpuss_interrupts_dw0_7_IRQn	Active	CPUSS P-DMA0, Channel #7 Interrupt
304	cpuss_interrupts_dw0_8_IRQn	Active	CPUSS P-DMA0, Channel #8 Interrupt
305	cpuss_interrupts_dw0_9_IRQn	Active	CPUSS P-DMA0, Channel #9 Interrupt
306	cpuss_interrupts_dw0_10_IRQn	Active	CPUSS P-DMA0, Channel #10 Interrupt
307	cpuss_interrupts_dw0_11_IRQn	Active	CPUSS P-DMA0, Channel #11 Interrupt
308	cpuss_interrupts_dw0_12_IRQn	Active	CPUSS P-DMA0, Channel #12 Interrupt
309	cpuss_interrupts_dw0_13_IRQn	Active	CPUSS P-DMA0, Channel #13 Interrupt
310	cpuss_interrupts_dw0_14_IRQn	Active	CPUSS P-DMA0, Channel #14 Interrupt
311	cpuss_interrupts_dw0_15_IRQn	Active	CPUSS P-DMA0, Channel #15 Interrupt
312	cpuss_interrupts_dw0_16_IRQn	Active	CPUSS P-DMA0, Channel #16 Interrupt
313	cpuss_interrupts_dw0_17_IRQn	Active	CPUSS P-DMA0, Channel #17 Interrupt
314	cpuss_interrupts_dw0_18_IRQn	Active	CPUSS P-DMA0, Channel #18 Interrupt
315	cpuss_interrupts_dw0_19_IRQn	Active	CPUSS P-DMA0, Channel #19 Interrupt
316	cpuss_interrupts_dw0_20_IRQn	Active	CPUSS P-DMA0, Channel #20 Interrupt
317	cpuss_interrupts_dw0_21_IRQn	Active	CPUSS P-DMA0, Channel #21 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
318	cpuss_interrupts_dw0_22_IRQn	Active	CPUSS P-DMA0, Channel #22 Interrupt
319	cpuss_interrupts_dw0_23_IRQn	Active	CPUSS P-DMA0, Channel #23 Interrupt
320	cpuss_interrupts_dw0_24_IRQn	Active	CPUSS P-DMA0, Channel #24 Interrupt
321	cpuss_interrupts_dw0_25_IRQn	Active	CPUSS P-DMA0, Channel #25 Interrupt
322	cpuss_interrupts_dw0_26_IRQn	Active	CPUSS P-DMA0, Channel #26 Interrupt
323	cpuss_interrupts_dw0_27_IRQn	Active	CPUSS P-DMA0, Channel #27 Interrupt
324	cpuss_interrupts_dw0_28_IRQn	Active	CPUSS P-DMA0, Channel #28 Interrupt
325	cpuss_interrupts_dw0_29_IRQn	Active	CPUSS P-DMA0, Channel #29 Interrupt
326	cpuss_interrupts_dw0_30_IRQn	Active	CPUSS P-DMA0, Channel #30 Interrupt
327	cpuss_interrupts_dw0_31_IRQn	Active	CPUSS P-DMA0, Channel #31 Interrupt
328	cpuss_interrupts_dw0_32_IRQn	Active	CPUSS P-DMA0, Channel #32 Interrupt
329	cpuss_interrupts_dw0_33_IRQn	Active	CPUSS P-DMA0, Channel #33 Interrupt
330	cpuss_interrupts_dw0_34_IRQn	Active	CPUSS P-DMA0, Channel #34 Interrupt
331	cpuss_interrupts_dw0_35_IRQn	Active	CPUSS P-DMA0, Channel #35 Interrupt
332	cpuss_interrupts_dw0_36_IRQn	Active	CPUSS P-DMA0, Channel #36 Interrupt
333	cpuss_interrupts_dw0_37_IRQn	Active	CPUSS P-DMA0, Channel #37 Interrupt
334	cpuss_interrupts_dw0_38_IRQn	Active	CPUSS P-DMA0, Channel #38 Interrupt
335	cpuss_interrupts_dw0_39_IRQn	Active	CPUSS P-DMA0, Channel #39 Interrupt
336	cpuss_interrupts_dw0_40_IRQn	Active	CPUSS P-DMA0, Channel #40 Interrupt
337	cpuss_interrupts_dw0_41_IRQn	Active	CPUSS P-DMA0, Channel #41 Interrupt
338	cpuss_interrupts_dw0_42_IRQn	Active	CPUSS P-DMA0, Channel #42 Interrupt
339	cpuss_interrupts_dw0_43_IRQn	Active	CPUSS P-DMA0, Channel #43 Interrupt
340	cpuss_interrupts_dw0_44_IRQn	Active	CPUSS P-DMA0, Channel #44 Interrupt
341	cpuss_interrupts_dw0_45_IRQn	Active	CPUSS P-DMA0, Channel #45 Interrupt
342	cpuss_interrupts_dw0_46_IRQn	Active	CPUSS P-DMA0, Channel #46 Interrupt
343	cpuss_interrupts_dw0_47_IRQn	Active	CPUSS P-DMA0, Channel #47 Interrupt
344	cpuss_interrupts_dw0_48_IRQn	Active	CPUSS P-DMA0, Channel #48 Interrupt
345	cpuss_interrupts_dw0_49_IRQn	Active	CPUSS P-DMA0, Channel #49 Interrupt
346	cpuss_interrupts_dw0_50_IRQn	Active	CPUSS P-DMA0, Channel #50 Interrupt
347	cpuss_interrupts_dw0_51_IRQn	Active	CPUSS P-DMA0, Channel #51 Interrupt
348	cpuss_interrupts_dw0_52_IRQn	Active	CPUSS P-DMA0, Channel #52 Interrupt
349	cpuss_interrupts_dw0_53_IRQn	Active	CPUSS P-DMA0, Channel #53 Interrupt
350	cpuss_interrupts_dw0_54_IRQn	Active	CPUSS P-DMA0, Channel #54 Interrupt
351	cpuss_interrupts_dw0_55_IRQn	Active	CPUSS P-DMA0, Channel #55 Interrupt
352	cpuss_interrupts_dw0_56_IRQn	Active	CPUSS P-DMA0, Channel #56 Interrupt
353	cpuss_interrupts_dw0_57_IRQn	Active	CPUSS P-DMA0, Channel #57 Interrupt
354	cpuss_interrupts_dw0_58_IRQn	Active	CPUSS P-DMA0, Channel #58 Interrupt
355	cpuss_interrupts_dw0_59_IRQn	Active	CPUSS P-DMA0, Channel #59 Interrupt
356	cpuss_interrupts_dw0_60_IRQn	Active	CPUSS P-DMA0, Channel #60 Interrupt
357	cpuss_interrupts_dw0_61_IRQn	Active	CPUSS P-DMA0, Channel #61 Interrupt
358	cpuss_interrupts_dw0_62_IRQn	Active	CPUSS P-DMA0, Channel #62 Interrupt
359	cpuss_interrupts_dw0_63_IRQn	Active	CPUSS P-DMA0, Channel #63 Interrupt
360	cpuss_interrupts_dw0_64_IRQn	Active	CPUSS P-DMA0, Channel #64 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
361	cpuss_interrupts_dw0_65_IRQn	Active	CPUSS P-DMA0, Channel #65 Interrupt
362	cpuss_interrupts_dw0_66_IRQn	Active	CPUSS P-DMA0, Channel #66 Interrupt
363	cpuss_interrupts_dw0_67_IRQn	Active	CPUSS P-DMA0, Channel #67 Interrupt
364	cpuss_interrupts_dw0_68_IRQn	Active	CPUSS P-DMA0, Channel #68 Interrupt
365	cpuss_interrupts_dw0_69_IRQn	Active	CPUSS P-DMA0, Channel #69 Interrupt
366	cpuss_interrupts_dw0_70_IRQn	Active	CPUSS P-DMA0, Channel #70 Interrupt
367	cpuss_interrupts_dw0_71_IRQn	Active	CPUSS P-DMA0, Channel #71 Interrupt
368	cpuss_interrupts_dw0_72_IRQn	Active	CPUSS P-DMA0, Channel #72 Interrupt
369	cpuss_interrupts_dw0_73_IRQn	Active	CPUSS P-DMA0, Channel #73 Interrupt
370	cpuss_interrupts_dw0_74_IRQn	Active	CPUSS P-DMA0, Channel #74 Interrupt
371	cpuss_interrupts_dw0_75_IRQn	Active	CPUSS P-DMA0, Channel #75 Interrupt
424	cpuss_interrupts_dw1_0_IRQn	Active	CPUSS P-DMA1, Channel #0 Interrupt
425	cpuss_interrupts_dw1_1_IRQn	Active	CPUSS P-DMA1, Channel #1 Interrupt
426	cpuss_interrupts_dw1_2_IRQn	Active	CPUSS P-DMA1, Channel #2 Interrupt
427	cpuss_interrupts_dw1_3_IRQn	Active	CPUSS P-DMA1, Channel #3 Interrupt
428	cpuss_interrupts_dw1_4_IRQn	Active	CPUSS P-DMA1, Channel #4 Interrupt
429	cpuss_interrupts_dw1_5_IRQn	Active	CPUSS P-DMA1, Channel #5 Interrupt
430	cpuss_interrupts_dw1_6_IRQn	Active	CPUSS P-DMA1, Channel #6 Interrupt
431	cpuss_interrupts_dw1_7_IRQn	Active	CPUSS P-DMA1, Channel #7 Interrupt
432	cpuss_interrupts_dw1_8_IRQn	Active	CPUSS P-DMA1, Channel #8 Interrupt
433	cpuss_interrupts_dw1_9_IRQn	Active	CPUSS P-DMA1, Channel #9 Interrupt
434	cpuss_interrupts_dw1_10_IRQn	Active	CPUSS P-DMA1, Channel #10 Interrupt
435	cpuss_interrupts_dw1_11_IRQn	Active	CPUSS P-DMA1, Channel #11 Interrupt
436	cpuss_interrupts_dw1_12_IRQn	Active	CPUSS P-DMA1, Channel #12 Interrupt
437	cpuss_interrupts_dw1_13_IRQn	Active	CPUSS P-DMA1, Channel #13 Interrupt
438	cpuss_interrupts_dw1_14_IRQn	Active	CPUSS P-DMA1, Channel #14 Interrupt
439	cpuss_interrupts_dw1_15_IRQn	Active	CPUSS P-DMA1, Channel #15 Interrupt
440	cpuss_interrupts_dw1_16_IRQn	Active	CPUSS P-DMA1, Channel #16 Interrupt
441	cpuss_interrupts_dw1_17_IRQn	Active	CPUSS P-DMA1, Channel #17 Interrupt
442	cpuss_interrupts_dw1_18_IRQn	Active	CPUSS P-DMA1, Channel #18 Interrupt
443	cpuss_interrupts_dw1_19_IRQn	Active	CPUSS P-DMA1, Channel #19 Interrupt
444	cpuss_interrupts_dw1_20_IRQn	Active	CPUSS P-DMA1, Channel #20 Interrupt
445	cpuss_interrupts_dw1_21_IRQn	Active	CPUSS P-DMA1, Channel #21 Interrupt
446	cpuss_interrupts_dw1_22_IRQn	Active	CPUSS P-DMA1, Channel #22 Interrupt
447	cpuss_interrupts_dw1_23_IRQn	Active	CPUSS P-DMA1, Channel #23 Interrupt
448	cpuss_interrupts_dw1_24_IRQn	Active	CPUSS P-DMA1, Channel #24 Interrupt
449	cpuss_interrupts_dw1_25_IRQn	Active	CPUSS P-DMA1, Channel #25 Interrupt
450	cpuss_interrupts_dw1_26_IRQn	Active	CPUSS P-DMA1, Channel #26 Interrupt
451	cpuss_interrupts_dw1_27_IRQn	Active	CPUSS P-DMA1, Channel #27 Interrupt
452	cpuss_interrupts_dw1_28_IRQn	Active	CPUSS P-DMA1, Channel #28 Interrupt
453	cpuss_interrupts_dw1_29_IRQn	Active	CPUSS P-DMA1, Channel #29 Interrupt
454	cpuss_interrupts_dw1_30_IRQn	Active	CPUSS P-DMA1, Channel #30 Interrupt
455	cpuss_interrupts_dw1_31_IRQn	Active	CPUSS P-DMA1, Channel #31 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
456	cpuss_interrupts_dw1_32_IRQn	Active	CPUSS P-DMA1, Channel #32 Interrupt
457	cpuss_interrupts_dw1_33_IRQn	Active	CPUSS P-DMA1, Channel #33 Interrupt
458	cpuss_interrupts_dw1_34_IRQn	Active	CPUSS P-DMA1, Channel #34 Interrupt
459	cpuss_interrupts_dw1_35_IRQn	Active	CPUSS P-DMA1, Channel #35 Interrupt
460	cpuss_interrupts_dw1_36_IRQn	Active	CPUSS P-DMA1, Channel #36 Interrupt
461	cpuss_interrupts_dw1_37_IRQn	Active	CPUSS P-DMA1, Channel #37 Interrupt
462	cpuss_interrupts_dw1_38_IRQn	Active	CPUSS P-DMA1, Channel #38 Interrupt
463	cpuss_interrupts_dw1_39_IRQn	Active	CPUSS P-DMA1, Channel #39 Interrupt
464	cpuss_interrupts_dw1_40_IRQn	Active	CPUSS P-DMA1, Channel #40 Interrupt
465	cpuss_interrupts_dw1_41_IRQn	Active	CPUSS P-DMA1, Channel #41 Interrupt
466	cpuss_interrupts_dw1_42_IRQn	Active	CPUSS P-DMA1, Channel #42 Interrupt
467	cpuss_interrupts_dw1_43_IRQn	Active	CPUSS P-DMA1, Channel #43 Interrupt
468	cpuss_interrupts_dw1_44_IRQn	Active	CPUSS P-DMA1, Channel #44 Interrupt
469	cpuss_interrupts_dw1_45_IRQn	Active	CPUSS P-DMA1, Channel #45 Interrupt
470	cpuss_interrupts_dw1_46_IRQn	Active	CPUSS P-DMA1, Channel #46 Interrupt
471	cpuss_interrupts_dw1_47_IRQn	Active	CPUSS P-DMA1, Channel #47 Interrupt
472	cpuss_interrupts_dw1_48_IRQn	Active	CPUSS P-DMA1, Channel #48 Interrupt
473	cpuss_interrupts_dw1_49_IRQn	Active	CPUSS P-DMA1, Channel #49 Interrupt
474	cpuss_interrupts_dw1_50_IRQn	Active	CPUSS P-DMA1, Channel #50 Interrupt
475	cpuss_interrupts_dw1_51_IRQn	Active	CPUSS P-DMA1, Channel #51 Interrupt
476	cpuss_interrupts_dw1_52_IRQn	Active	CPUSS P-DMA1, Channel #52 Interrupt
477	cpuss_interrupts_dw1_53_IRQn	Active	CPUSS P-DMA1, Channel #53 Interrupt
478	cpuss_interrupts_dw1_54_IRQn	Active	CPUSS P-DMA1, Channel #54 Interrupt
479	cpuss_interrupts_dw1_55_IRQn	Active	CPUSS P-DMA1, Channel #55 Interrupt
480	cpuss_interrupts_dw1_56_IRQn	Active	CPUSS P-DMA1, Channel #56 Interrupt
481	cpuss_interrupts_dw1_57_IRQn	Active	CPUSS P-DMA1, Channel #57 Interrupt
482	cpuss_interrupts_dw1_58_IRQn	Active	CPUSS P-DMA1, Channel #58 Interrupt
483	cpuss_interrupts_dw1_59_IRQn	Active	CPUSS P-DMA1, Channel #59 Interrupt
484	cpuss_interrupts_dw1_60_IRQn	Active	CPUSS P-DMA1, Channel #60 Interrupt
485	cpuss_interrupts_dw1_61_IRQn	Active	CPUSS P-DMA1, Channel #61 Interrupt
486	cpuss_interrupts_dw1_62_IRQn	Active	CPUSS P-DMA1, Channel #62 Interrupt
487	cpuss_interrupts_dw1_63_IRQn	Active	CPUSS P-DMA1, Channel #63 Interrupt
488	cpuss_interrupts_dw1_64_IRQn	Active	CPUSS P-DMA1, Channel #64 Interrupt
489	cpuss_interrupts_dw1_65_IRQn	Active	CPUSS P-DMA1, Channel #65 Interrupt
490	cpuss_interrupts_dw1_66_IRQn	Active	CPUSS P-DMA1, Channel #66 Interrupt
491	cpuss_interrupts_dw1_67_IRQn	Active	CPUSS P-DMA1, Channel #67 Interrupt
492	cpuss_interrupts_dw1_68_IRQn	Active	CPUSS P-DMA1, Channel #68 Interrupt
493	cpuss_interrupts_dw1_69_IRQn	Active	CPUSS P-DMA1, Channel #69 Interrupt
494	cpuss_interrupts_dw1_70_IRQn	Active	CPUSS P-DMA1, Channel #70 Interrupt
495	cpuss_interrupts_dw1_71_IRQn	Active	CPUSS P-DMA1, Channel #71 Interrupt
496	cpuss_interrupts_dw1_72_IRQn	Active	CPUSS P-DMA1, Channel #72 Interrupt
497	cpuss_interrupts_dw1_73_IRQn	Active	CPUSS P-DMA1, Channel #73 Interrupt
498	cpuss_interrupts_dw1_74_IRQn	Active	CPUSS P-DMA1, Channel #74 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
499	cpuss_interrupts_dw1_75_IRQn	Active	CPUSS P-DMA1, Channel #75 Interrupt
500	cpuss_interrupts_dw1_76_IRQn	Active	CPUSS P-DMA1, Channel #76 Interrupt
501	cpuss_interrupts_dw1_77_IRQn	Active	CPUSS P-DMA1, Channel #77 Interrupt
502	cpuss_interrupts_dw1_78_IRQn	Active	CPUSS P-DMA1, Channel #78 Interrupt
503	cpuss_interrupts_dw1_79_IRQn	Active	CPUSS P-DMA1, Channel #79 Interrupt
504	cpuss_interrupts_dw1_80_IRQn	Active	CPUSS P-DMA1, Channel #80 Interrupt
505	cpuss_interrupts_dw1_81_IRQn	Active	CPUSS P-DMA1, Channel #81 Interrupt
506	cpuss_interrupts_dw1_82_IRQn	Active	CPUSS P-DMA1, Channel #82 Interrupt
507	cpuss_interrupts_dw1_83_IRQn	Active	CPUSS P-DMA1, Channel #83 Interrupt
552	tcpwm_0_interrupts_0_IRQn	Active	TCPWM0 Group #0, Counter #0 Interrupt
553	tcpwm_0_interrupts_1_IRQn	Active	TCPWM0 Group #0, Counter #1 Interrupt
554	tcpwm_0_interrupts_2_IRQn	Active	TCPWM0 Group #0, Counter #2 Interrupt
555	tcpwm_0_interrupts_3_IRQn	Active	TCPWM0 Group #0, Counter #3 Interrupt
556	tcpwm_0_interrupts_4_IRQn	Active	TCPWM0 Group #0, Counter #4 Interrupt
557	tcpwm_0_interrupts_5_IRQn	Active	TCPWM0 Group #0, Counter #5 Interrupt
558	tcpwm_0_interrupts_6_IRQn	Active	TCPWM0 Group #0, Counter #6 Interrupt
559	tcpwm_0_interrupts_7_IRQn	Active	TCPWM0 Group #0, Counter #7 Interrupt
560	tcpwm_0_interrupts_8_IRQn	Active	TCPWM0 Group #0, Counter #8 Interrupt
561	tcpwm_0_interrupts_9_IRQn	Active	TCPWM0 Group #0, Counter #9 Interrupt
562	tcpwm_0_interrupts_10_IRQn	Active	TCPWM0 Group #0, Counter #10 Interrupt
563	tcpwm_0_interrupts_11_IRQn	Active	TCPWM0 Group #0, Counter #11 Interrupt
564	tcpwm_0_interrupts_12_IRQn	Active	TCPWM0 Group #0, Counter #12 Interrupt
565	tcpwm_0_interrupts_13_IRQn	Active	TCPWM0 Group #0, Counter #13 Interrupt
566	tcpwm_0_interrupts_14_IRQn	Active	TCPWM0 Group #0, Counter #14 Interrupt
567	tcpwm_0_interrupts_15_IRQn	Active	TCPWM0 Group #0, Counter #15 Interrupt
568	tcpwm_0_interrupts_16_IRQn	Active	TCPWM0 Group #0, Counter #16 Interrupt
569	tcpwm_0_interrupts_17_IRQn	Active	TCPWM0 Group #0, Counter #17 Interrupt
570	tcpwm_0_interrupts_18_IRQn	Active	TCPWM0 Group #0, Counter #18 Interrupt
571	tcpwm_0_interrupts_19_IRQn	Active	TCPWM0 Group #0, Counter #19 Interrupt
572	tcpwm_0_interrupts_20_IRQn	Active	TCPWM0 Group #0, Counter #20 Interrupt
573	tcpwm_0_interrupts_21_IRQn	Active	TCPWM0 Group #0, Counter #21 Interrupt
574	tcpwm_0_interrupts_22_IRQn	Active	TCPWM0 Group #0, Counter #22 Interrupt
575	tcpwm_0_interrupts_23_IRQn	Active	TCPWM0 Group #0, Counter #23 Interrupt
576	tcpwm_0_interrupts_24_IRQn	Active	TCPWM0 Group #0, Counter #24 Interrupt
577	tcpwm_0_interrupts_25_IRQn	Active	TCPWM0 Group #0, Counter #25 Interrupt
578	tcpwm_0_interrupts_26_IRQn	Active	TCPWM0 Group #0, Counter #26 Interrupt
579	tcpwm_0_interrupts_27_IRQn	Active	TCPWM0 Group #0, Counter #27 Interrupt
580	tcpwm_0_interrupts_28_IRQn	Active	TCPWM0 Group #0, Counter #28 Interrupt
581	tcpwm_0_interrupts_29_IRQn	Active	TCPWM0 Group #0, Counter #29 Interrupt
582	tcpwm_0_interrupts_30_IRQn	Active	TCPWM0 Group #0, Counter #30 Interrupt
583	tcpwm_0_interrupts_31_IRQn	Active	TCPWM0 Group #0, Counter #31 Interrupt
584	tcpwm_0_interrupts_32_IRQn	Active	TCPWM0 Group #0, Counter #32 Interrupt
585	tcpwm_0_interrupts_33_IRQn	Active	TCPWM0 Group #0, Counter #33 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
586	tcpwm_0_interrupts_34_IRQn	Active	TCPWM0 Group #0, Counter #34 Interrupt
587	tcpwm_0_interrupts_35_IRQn	Active	TCPWM0 Group #0, Counter #35 Interrupt
588	tcpwm_0_interrupts_36_IRQn	Active	TCPWM0 Group #0, Counter #36 Interrupt
589	tcpwm_0_interrupts_37_IRQn	Active	TCPWM0 Group #0, Counter #37 Interrupt
616	tcpwm_0_interrupts_256_IRQn	Active	TCPWM0 Group #1, Counter #0 Interrupt
617	tcpwm_0_interrupts_257_IRQn	Active	TCPWM0 Group #1, Counter #1 Interrupt
618	tcpwm_0_interrupts_258_IRQn	Active	TCPWM0 Group #1, Counter #2 Interrupt
619	tcpwm_0_interrupts_259_IRQn	Active	TCPWM0 Group #1, Counter #3 Interrupt
620	tcpwm_0_interrupts_260_IRQn	Active	TCPWM0 Group #1, Counter #4 Interrupt
621	tcpwm_0_interrupts_261_IRQn	Active	TCPWM0 Group #1, Counter #5 Interrupt
622	tcpwm_0_interrupts_262_IRQn	Active	TCPWM0 Group #1, Counter #6 Interrupt
623	tcpwm_0_interrupts_263_IRQn	Active	TCPWM0 Group #1, Counter #7 Interrupt
624	tcpwm_0_interrupts_264_IRQn	Active	TCPWM0 Group #1, Counter #8 Interrupt
625	tcpwm_0_interrupts_265_IRQn	Active	TCPWM0 Group #1, Counter #9 Interrupt
626	tcpwm_0_interrupts_266_IRQn	Active	TCPWM0 Group #1, Counter #10 Interrupt
627	tcpwm_0_interrupts_267_IRQn	Active	TCPWM0 Group #1, Counter #11 Interrupt
680	tcpwm_0_interrupts_512_IRQn	Active	TCPWM0 Group #2, Counter #0 Interrupt
681	tcpwm_0_interrupts_513_IRQn	Active	TCPWM0 Group #2, Counter #1 Interrupt
682	tcpwm_0_interrupts_514_IRQn	Active	TCPWM0 Group #2, Counter #2 Interrupt
683	tcpwm_0_interrupts_515_IRQn	Active	TCPWM0 Group #2, Counter #3 Interrupt
684	tcpwm_0_interrupts_516_IRQn	Active	TCPWM0 Group #2, Counter #4 Interrupt
685	tcpwm_0_interrupts_517_IRQn	Active	TCPWM0 Group #2, Counter #5 Interrupt
686	tcpwm_0_interrupts_518_IRQn	Active	TCPWM0 Group #2, Counter #6 Interrupt
687	tcpwm_0_interrupts_519_IRQn	Active	TCPWM0 Group #2, Counter #7 Interrupt
688	tcpwm_0_interrupts_520_IRQn	Active	TCPWM0 Group #2, Counter #8 Interrupt
689	tcpwm_0_interrupts_521_IRQn	Active	TCPWM0 Group #2, Counter #9 Interrupt
690	tcpwm_0_interrupts_522_IRQn	Active	TCPWM0 Group #2, Counter #10 Interrupt
691	tcpwm_0_interrupts_523_IRQn	Active	TCPWM0 Group #2, Counter #11 Interrupt
692	tcpwm_0_interrupts_524_IRQn	Active	TCPWM0 Group #2, Counter #12 Interrupt
693	tcpwm_0_interrupts_525_IRQn	Active	TCPWM0 Group #2, Counter #13 Interrupt
694	tcpwm_0_interrupts_526_IRQn	Active	TCPWM0 Group #2, Counter #14 Interrupt
695	tcpwm_0_interrupts_527_IRQn	Active	TCPWM0 Group #2, Counter #15 Interrupt
696	tcpwm_0_interrupts_528_IRQn	Active	TCPWM0 Group #2, Counter #16 Interrupt
697	tcpwm_0_interrupts_529_IRQn	Active	TCPWM0 Group #2, Counter #17 Interrupt
698	tcpwm_0_interrupts_530_IRQn	Active	TCPWM0 Group #2, Counter #18 Interrupt
699	tcpwm_0_interrupts_531_IRQn	Active	TCPWM0 Group #2, Counter #19 Interrupt
700	tcpwm_0_interrupts_532_IRQn	Active	TCPWM0 Group #2, Counter #20 Interrupt
701	tcpwm_0_interrupts_533_IRQn	Active	TCPWM0 Group #2, Counter #21 Interrupt
702	tcpwm_0_interrupts_534_IRQn	Active	TCPWM0 Group #2, Counter #22 Interrupt
703	tcpwm_0_interrupts_535_IRQn	Active	TCPWM0 Group #2, Counter #23 Interrupt
704	tcpwm_0_interrupts_536_IRQn	Active	TCPWM0 Group #2, Counter #24 Interrupt
705	tcpwm_0_interrupts_537_IRQn	Active	TCPWM0 Group #2, Counter #25 Interrupt
706	tcpwm_0_interrupts_538_IRQn	Active	TCPWM0 Group #2, Counter #26 Interrupt

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power mode	Description
707	tcpwm_0_interrupts_539_IRQn	Active	TCPWM0 Group #2, Counter #27 Interrupt
708	tcpwm_0_interrupts_540_IRQn	Active	TCPWM0 Group #2, Counter #28 Interrupt
709	tcpwm_0_interrupts_541_IRQn	Active	TCPWM0 Group #2, Counter #29 Interrupt
710	tcpwm_0_interrupts_542_IRQn	Active	TCPWM0 Group #2, Counter #30 Interrupt
711	tcpwm_0_interrupts_543_IRQn	Active	TCPWM0 Group #2, Counter #31 Interrupt
752	tdm_0_interrupts_tx_0_IRQn	Active	TDM0 TX #0 Interrupt
753	tdm_0_interrupts_rx_0_IRQn	Active	TDM0 RX #0 Interrupt
754	tdm_0_interrupts_tx_1_IRQn	Active	TDM0 TX #1 Interrupt
755	tdm_0_interrupts_rx_1_IRQn	Active	TDM0 RX #1 Interrupt
756	tdm_0_interrupts_tx_2_IRQn	Active	TDM0 TX #2 Interrupt
757	tdm_0_interrupts_rx_2_IRQn	Active	TDM0 RX #2 Interrupt
758	tdm_0_interrupts_tx_3_IRQn	Active	TDM0 TX #3 Interrupt
759	tdm_0_interrupts_rx_3_IRQn	Active	TDM0 RX #3 Interrupt
760	sg_0_interrupts_0_IRQn	Active	SG0 #0 Interrupt
761	sg_0_interrupts_1_IRQn	Active	SG0 #1 Interrupt
762	sg_0_interrupts_2_IRQn	Active	SG0 #2 Interrupt
763	sg_0_interrupts_3_IRQn	Active	SG0 #3 Interrupt
764	sg_0_interrupts_4_IRQn	Active	SG0 #4 Interrupt
768	pwm_0_interrupts_0_IRQn	Active	PCM-PWM0 #0 Interrupt
769	pwm_0_interrupts_1_IRQn	Active	PCM-PWM0 #1 Interrupt
776	dac_0_interrupt_IRQn	Active	Audio DAC interrupt
780	mixer_0_interrupt_dst_IRQn	Active	MIXER0 Destination interrupt
781	mixer_0_interrupts_src_0_IRQn	Active	MIXER0 Source #0 Interrupt
782	mixer_0_interrupts_src_1_IRQn	Active	MIXER0 Source #1 Interrupt
783	mixer_0_interrupts_src_2_IRQn	Active	MIXER0 Source #2 Interrupt
784	mixer_0_interrupts_src_3_IRQn	Active	MIXER0 Source #3 Interrupt
785	mixer_0_interrupts_src_4_IRQn	Active	MIXER0 Source #4 Interrupt
789	mixer_1_interrupt_dst_IRQn	Active	MIXER1 Destination interrupt
790	mixer_1_interrupts_src_0_IRQn	Active	MIXER1 Source #0 Interrupt
791	mixer_1_interrupts_src_1_IRQn	Active	MIXER1 Source #1 Interrupt
792	mixer_1_interrupts_src_2_IRQn	Active	MIXER1 Source #2 Interrupt
793	mixer_1_interrupts_src_3_IRQn	Active	MIXER1 Source #3 Interrupt
794	mixer_1_interrupts_src_4_IRQn	Active	MIXER1 Source #4 Interrupt

15 Core interrupt types

Table 15-1 Core interrupt types

Interrupt	Source	Power mode	Description
0	CPUIntIdx0_IRQn[40]	DeepSleep	CPU User Interrupt #0
1	CPUIntIdx1_IRQn[40]	DeepSleep	CPU User Interrupt #1
2	CPUIntIdx2_IRQn	DeepSleep	CPU User Interrupt #2
3	CPUIntIdx3_IRQn	DeepSleep	CPU User Interrupt #3
4	CPUIntIdx4_IRQn	DeepSleep	CPU User Interrupt #4
5	CPUIntIdx5_IRQn	DeepSleep	CPU User Interrupt #5
6	CPUIntIdx6_IRQn	DeepSleep	CPU User Interrupt #6
7	CPUIntIdx7_IRQn	DeepSleep	CPU User Interrupt #7
8	Internal0_IRQn	Active	Internal Software Interrupt #0
9	Internal1_IRQn	Active	Internal Software Interrupt #1
10	Internal2_IRQn	Active	Internal Software Interrupt #2
11	Internal3_IRQn	Active	Internal Software Interrupt #3
12	Internal4_IRQn	Active	Internal Software Interrupt #4
13	Internal5_IRQn	Active	Internal Software Interrupt #5
14	Internal6_IRQn	Active	Internal Software Interrupt #6
15	Internal7_IRQn	Active	Internal Software Interrupt #7

Note

[40] User interrupt cannot be used for CM0+ application, as it is used internally by system calls. Note, this does not impact CM7 application.

16 Trigger multiplexer

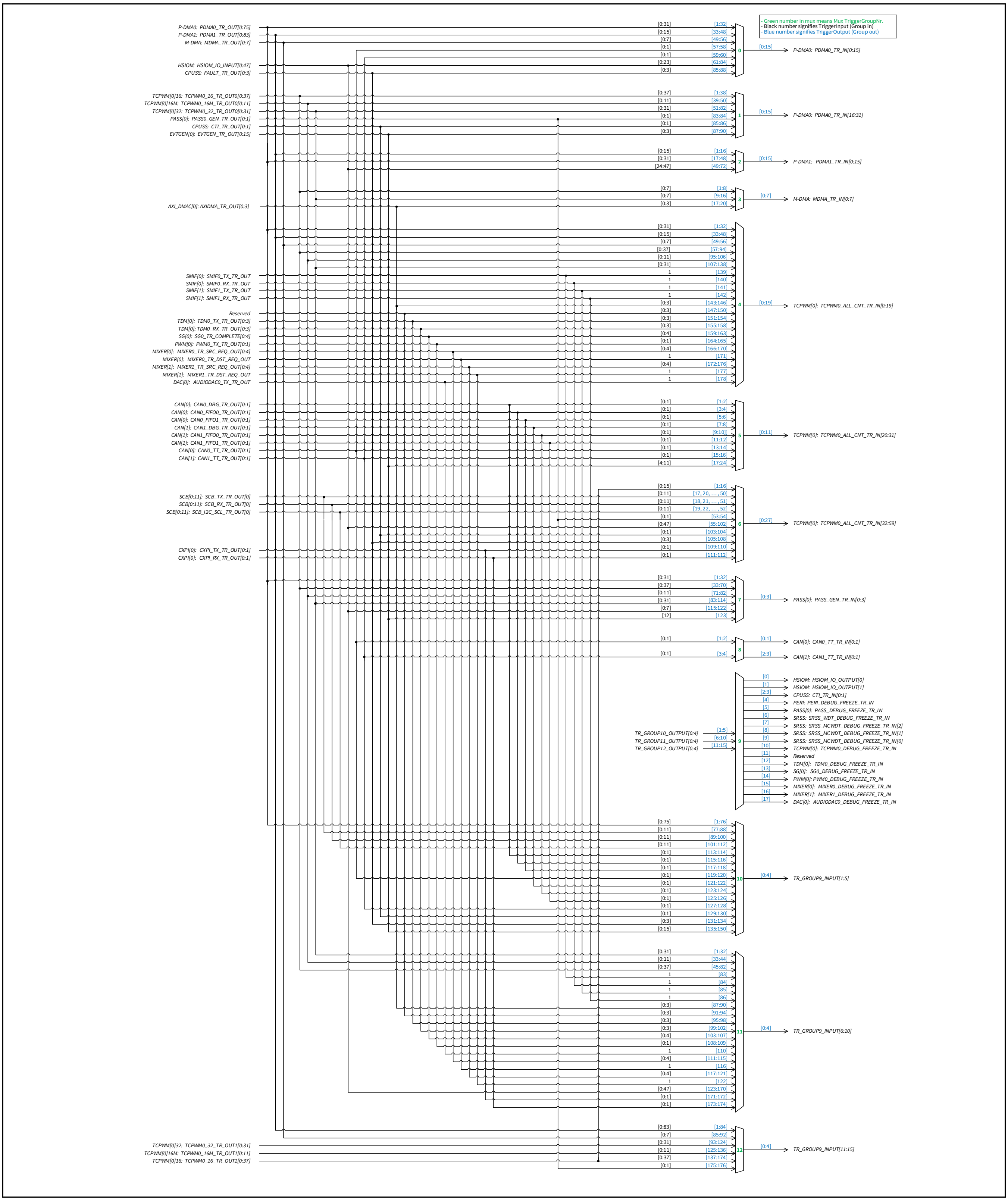


Figure 16-1 Trigger multiplexer[41]

Note

41.The diagram shows only the TRIG_LABEL; the final trigger formation is based on the formula TRIG_{PREFIX(IN/OUT)}_{MUX-_x}_{TRIG_LABEL} and the information provided in **Table 17-1**, and **Table 18-1**.

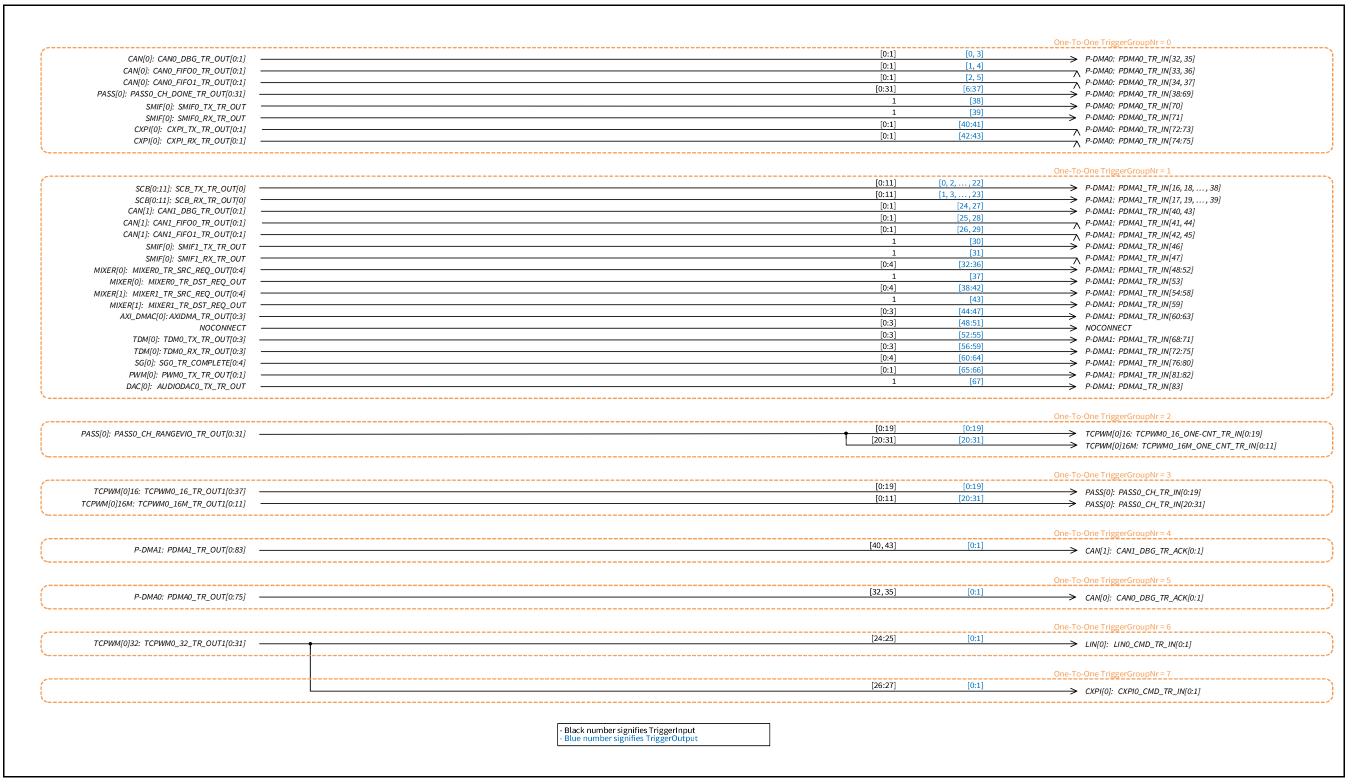


Figure 16-2 Triggers one-to-one[42]

Note

[42] The diagram shows only the TRIG_LABEL; the final trigger formation is based on the formula TRIG_{PREFIX(IN_1TO1/OUT_1-TO1)}_{x}_{TRIG_LABEL} and the information provided in **Table 19-1**.

17 Triggers group inputs

Table 17-1 Trigger inputs

Input	Trigger Label (TRIG_LABEL)	Description
MUX Group 0: P-DMA0_0_15 trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	Allow P-DMA0 to chain to itself. Channels 0 - 32 are general purpose channels available for chaining
33:48	PDMA1_TR_OUT[0:15]	Cross connections from P-DMA1 to P-DMA0, Channels 0-15 are used
49:56	MDMA_TR_OUT[0:7]	Cross connections from M-DMA0 to P-DMA0
57:58	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
59:60	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
61:84	HSIOM_IO_INPUT[0:23]	I/O Inputs
85:88	FAULT_TR_OUT[0:3]	Fault events
MUX Group 1: P-DMA0_16_31 trigger multiplexer		
1:38	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
39:50	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
51:82	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
83:84	PASS_GEN_TR_OUT[0:1]	PASS0 SAR events
85:86	CTI_TR_OUT[0:1]	Trace events
87:90	EVTGEN_TR_OUT[0:3]	Event generator triggers
MUX Group 2: P-DMA1_0_15 trigger multiplexer		
1:16	PDMA1_TR_OUT[0:15]	Allow P-DMA1 to chain to itself. Channels 0 - 15 are dedicated for chaining
17:48	PDMA0_TR_OUT[0:31]	Cross connections from P-DMA0 to P-DMA1, channels 0-31 are used.
49:72	HSIOM_IO_INPUT[24:47]	I/O Inputs
MUX Group 3: M-DMA0 trigger multiplexer		
1:8	TCPWM0_16_TR_OUT0[0:7]	16-bit TCPWM0 counters
9:16	TCPWM0_32_TR_OUT0[0:7]	32-bit TCPWM0 counters
17:20	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers
MUX Group 4: TCPWM0 Trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA0 triggers
33:48	PDMA1_TR_OUT[0:15]	General purpose P-DMA1 triggers
49:56	MDMA_TR_OUT[0:7]	AHB M-DMA0 triggers
57:94	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
95:106	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
107:138	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
139	SMIF0_TX_TR_OUT	SMIF0 TX trigger
140	SMIF0_RX_TR_OUT	SMIF0 RX trigger
141	SMIF1_TX_TR_OUT	SMIF1 TX trigger
142	SMIF1_RX_TR_OUT	SMIF1 RX trigger
143:146	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers
151:154	TDM0_TX_TR_OUT[0:3]	TDM0 TX trigger
155:158	TDM0_RX_TR_OUT[0:3]	TDM0 RX trigger
159:163	SG0_TX_TR_OUT[0:4]	SG0 TX trigger
164:165	PWM0_TX_TR_OUT[0:1]	PWM0 TX trigger
166:170	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER0 SRC trigger
171	MIXER0_TR_DST_REQ_OUT	MIXER0 DST trigger
172:176	MIXER1_TR_SRC_REQ_OUT[0:4]	MIXER1 SRC trigger
177	MIXER1_TR_DST_REQ_OUT	MIXER1 DST trigger

Table 17-1 Trigger inputs *(continued)*

Input	Trigger Label (TRIG_LABEL)	Description
178	AUDIODAC0_TX_TR_OUT	AUDIO DAC0 TX trigger
MUX Group 5: TCPWM0_20_31 Trigger multiplexer		
1:2	CAN0_DBG_TR_OUT[0:1]	CAN0 DMA events
3:4	CAN0_FIFO0_TR_OUT[0:1]	CAN0 FIFO0 events
5:6	CAN0_FIFO1_TR_OUT[0:1]	CAN0 FIFO1 events
7:8	CAN1_DBG_TR_OUT[0:1]	CAN1 DMA events
9:10	CAN1_FIFO0_TR_OUT[0:1]	CAN1 FIFO0 events
11:12	CAN1_FIFO1_TR_OUT[0:1]	CAN1 FIFO1 events
13:14	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
15:16	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
17:24	EVTGEN_TR_OUT[4:11]	Event generator triggers
MUX Group 6: TCPWM0_32_59 Trigger Multiplexer		
1:16	TCPWM0_16_TR_OUT1[0:15]	16-bit TCPWM0 counters
17	SCB_TX_TR_OUT[0]	SCB0 TX trigger
18	SCB_RX_TR_OUT[0]	SCB0 RX trigger
19	SCB_I2C_SCL_TR_OUT[0]	SCB0 I^2C trigger
20	SCB_TX_TR_OUT[1]	SCB1 TX trigger
21	SCB_RX_TR_OUT[1]	SCB1 RX trigger
22	SCB_I2C_SCL_TR_OUT[1]	SCB1 I^2C trigger
23	SCB_TX_TR_OUT[2]	SCB2 TX trigger
24	SCB_RX_TR_OUT[2]	SCB2 RX trigger
25	SCB_I2C_SCL_TR_OUT[2]	SCB2 I^2C trigger
26	SCB_TX_TR_OUT[3]	SCB3 TX trigger
27	SCB_RX_TR_OUT[3]	SCB3 RX trigger
28	SCB_I2C_SCL_TR_OUT[3]	SCB3 I^2C trigger
29	SCB_TX_TR_OUT[4]	SCB4 TX trigger
30	SCB_RX_TR_OUT[4]	SCB4 RX trigger
31	SCB_I2C_SCL_TR_OUT[4]	SCB4 I^2C trigger
32	SCB_TX_TR_OUT[5]	SCB5 TX trigger
33	SCB_RX_TR_OUT[5]	SCB5 RX trigger
34	SCB_I2C_SCL_TR_OUT[5]	SCB5 I^2C trigger
35	SCB_TX_TR_OUT[6]	SCB6 TX trigger
36	SCB_RX_TR_OUT[6]	SCB6 RX trigger
37	SCB_I2C_SCL_TR_OUT[6]	SCB6 I^2C trigger
38	SCB_TX_TR_OUT[7]	SCB7 TX trigger
39	SCB_RX_TR_OUT[7]	SCB7 RX trigger
40	SCB_I2C_SCL_TR_OUT[7]	SCB7 I^2C trigger
41	SCB_TX_TR_OUT[8]	SCB8 TX trigger
42	SCB_RX_TR_OUT[8]	SCB8 RX trigger
43	SCB_I2C_SCL_TR_OUT[8]	SCB8 I^2C trigger
44	SCB_TX_TR_OUT[9]	SCB9 TX trigger
45	CB_RX_TR_OUT[9]	SCB9 RX trigger
46	SCB_I2C_SCL_TR_OUT[9]	SCB9 I^2C trigger
47	SCB_TX_TR_OUT[10]	SCB10 TX trigger
48	SCB_RX_TR_OUT[10]	SCB10 RX trigger

Table 17-1 Trigger inputs *(continued)*

Input	Trigger Label (TRIG_LABEL)	Description
49	SCB_I2C_SCL_TR_OUT[10]	SCB10 I^2C trigger
50	SCB_TX_TR_OUT[11]	SCB11 TX trigger
51	SCB_RX_TR_OUT[11]	SCB11 RX trigger
52	SCB_I2C_SCL_TR_OUT[11]	SCB11 I^2C trigger
53:54	PASS_GEN_TR_OUT[0:1]	PASS0 SAR events
55:102	HSIOM_IO_INPUT[0:47]	I/O Inputs
103:104	CTI_TR_IN[0:1]	Trace events
105:108	FAULT_TR_OUT[0:3]	Fault events
109:110	CXPI_TX_TR_OUT[0:1]	CXPI0 transmit events
111:112	CXPI_RX_TR_OUT[0:1]	CXPI0 receive events
MUX Group 7: PASS0 SAR trigger multiplexer		
1:32	PDMA0_TR_OUT[0:31]	General purpose P-DMA0 triggers
33:70	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
71:82	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
83:114	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
115:122	HSIOM_IO_INPUT[0:7]	I/O Inputs
123	EVTGEN_TR_OUT[12]	Event generator triggers
MUX Group 8: CAN TT Sync		
1:2	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
3:4	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
MUX Group 9: Debug MUX		
1:5	TR_GROUP10_OUTPUT[0:4]	Output from debug reduction multiplexer #1
6:10	TR_GROUP11_OUTPUT[0:4]	Output from debug reduction multiplexer #2
11:15	TR_GROUP12_OUTPUT[0:4]	Output from debug reduction multiplexer #3
MUX Group 10: Debug Reduction #1		
1:76	PDMA0_TR_OUT[0:75]	General purpose P-DMA0 triggers
77:88	SCB_TX_TR_OUT[0:11]	SCB TX triggers
89:100	SCB_RX_TR_OUT[0:11]	SCB RX triggers
101:112	SCB_I2C_SCL_TR_OUT[0:11]	SCB I^2C triggers
113:114	CAN0_DBG_TR_OUT[0:1]	CAN0 DMA
115:116	CAN0_FIFO0_TR_OUT[0:1]	CAN0 FIFO0
117:118	CAN0_FIFO1_TR_OUT[0:1]	CAN0 FIFO1
119:120	CAN0_TT_TR_OUT[0:1]	CAN0 TT Sync Outputs
121:122	CAN1_DBG_TR_OUT[0:1]	CAN1 DMA
123:124	CAN1_FIFO0_TR_OUT[0:1]	CAN1 FIFO0
125:126	CAN1_FIFO1_TR_OUT[0:1]	CAN1 FIFO1
127:128	CAN1_TT_TR_OUT[0:1]	CAN1 TT Sync Outputs
129:130	CTI_TR_OUT[0:1]	Trace events
131:134	FAULT_TR_OU[0:3]	Fault events
135:150	EVTGEN_TR_OUT[0:15]	EVTGEN Triggers
MUX Group 11: Debug Reduction #2		
1:32	TCPWM0_32_TR_OUT0[0:31]	32-bit TCPWM0 counters
33:44	TCPWM0_16M_TR_OUT0[0:11]	16-bit Motor enhanced TCPWM0 counters
45:82	TCPWM0_16_TR_OUT0[0:37]	16-bit TCPWM0 counters
83	SMIF0_TX_TR_OUT	SMIF0 TX trigger

Table 17-1 Trigger inputs *(continued)*

Input	Trigger Label (TRIG_LABEL)	Description
84	SMIF0_RX_TR_OUT	SMIF0 RX trigger
85	SMIF1_TX_TR_OUT	SMIF1 TX trigger
86	SMIF1_RX_TR_OUT	SMIF1 RX trigger
87:90	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers
95:98	TDM0_TX_TR_OUT[0:3]	TDM0 TX trigger
99:102	TDM0_RX_TR_OUT[0:3]	TDM0 RX trigger
103:107	SG0_TX_TR_OUT[0:4]	SG0 TX trigger
108:109	PWM0_TX_TR_OUT[0:1]	PWM0 TX trigger
110	AUDIODAC0_TX_TR_OUT	AUDIO DAC0 TX trigger
111:115	MIXER0_TR_SRC_REQ_OUT[0:4]	MIXER0 SRC trigger
116	MIXER0_TR_DST_REQ_OUT	MIXER0 DST trigger
117:121	MIXER1_TR_SRC_REQ_OUT[0:4]	MIXER1 SRC trigger
122	MIXER1_TR_DST_REQ_OUT	MIXER1 DST trigger
123:170	HSIOM_IO_INPUT[0:47]	I/O inputs
171:172	CXPI_TX_TR_OUT[0:1]	CXPI0 TX trigger
173:174	CXPI_RX_TR_OUT[0:1]	CXPI0 RX trigger
MUX Group 12: Debug Reduction #3		
1:84	PDMA1_TR_OUT[0:83]	General purpose P-DMA1 triggers
85:92	MDMA_TR_OUT[0:7]	M-DMA0 triggers
93:124	TCPWM0_32_TR_OUT1[0:31]	32-bit TCPWM0 counters
125:136	TCPWM0_16M_TR_OUT1[0:11]	16-bit Motor enhanced TCPWM0 counters
137:174	TCPWM0_16_TR_OUT1[0:37]	16-bit TCPWM0 counters
175:176	PASS_GEN_TR_OUT[0:1]	PASS0 SAR events
MUX Group 13: AXI M-DMA trigger multiplexer		
1:4	TCPWM0_16_TR_OUT0[0:3]	16-bit TCPWM0 counters
5:8	TCPWM0_32_TR_OUT0[0:3]	32-bit TCPWM0 counters
9:12	AXIDMA_TR_OUT[0:3]	AXI M-DMA1 triggers

18 Triggers group outputs

Table 18-1 Trigger outputs

Output	Trigger	Description
MUX Group 0: P-DMA0_0_15 trigger multiplexer		
0:15	PDMA0_TR_IN[0:15]	Triggers to P-DMA0[0:15]
MUX Group 1: P-DMA0_16_31 trigger multiplexer		
0:15	PDMA0_TR_IN[16:31]	Triggers to P-DMA0[16:31]
MUX Group 2: P-DMA1_0_15 trigger multiplexer		
0:15	PDMA1_TR_IN[0:15]	Triggers to P-DMA1
MUX Group 3: M-DMA0 trigger multiplexer		
0:7	MDMA_TR_IN[0:7]	Triggers to M-DMA0
MUX Group 4: TCPWM0 Trigger multiplexer		
0:19	TCPWM0_ALL_CNT_TR_IN[0:19]	Triggers to TCPWM0
MUX Group 5: TCPWM0_20_31 Trigger multiplexer		
0:11	TCPWM0_ALL_CNT_TR_IN[20:31]	Triggers to TCPWM0
MUX Group 6: TCPWM0_32_59 Trigger Multiplexer		
0:27	TCPWM0_ALL_CNT_TR_IN[32:59]	Triggers to TCPWM0
MUX Group 7: PASS0 SAR trigger multiplexer		
0:3	PASS_GEN_TR_IN[0:3]	Triggers to PASS0 SAR
MUX Group 8: CAN TT Sync		
0:1	CAN0_TT_TR_IN[0:1]	CAN0 TT Sync Inputs
2:3	CAN1_TT_TR_IN[0:1]	CAN1 TT Sync Inputs
MUX Group 9: Debug MUX		
0	HSIOM_IO_OUTPUT[0]	To HSIOM as an output
1	HSIOM_IO_OUTPUT[1]	To HSIOM as an output
2:3	CTI_TR_IN[0:1]	To the Cross Trigger system
4	PERI_DEBUG_FREEZE_TR_IN	Signal to Freeze PERI operation
5	PASS_DEBUG_FREEZE_TR_IN	Signal to Freeze PASS0 SAR operation
6	SRSS_WDT_DEBUG_FREEZE_TR_IN	Signal to Freeze WDT operation
7	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[2]	Signal to Freeze MCWDT2 operation
8	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1]	Signal to Freeze MCWDT1 operation
9	SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0]	Signal to Freeze MCWDT0 operation
10	TCPWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TCPWM0 operation
12	TDM0_DEBUG_FREEZE_TR_IN	Signal to Freeze TDM0 operation
13	SG0_DEBUG_FREEZE_TR_IN	Signal to Freeze SG0 operation
14	PWM0_DEBUG_FREEZE_TR_IN	Signal to Freeze PWM0 operation
15	MIXER0_DEBUG_FREEZE_TR_IN	Signal to Freeze MIXER0 operation
16	MIXER1_DEBUG_FREEZE_TR_IN	Signal to Freeze MIXER1 operation
17	AUDIODAC0_DEBUG_FREEZE_TR_IN	Signal to Freeze AUDIO DAC0 operation
MUX Group 10: Debug Reduction #1		
0:4	TR_GROUP9_INPUT[1:5]	To main debug multiplexer
MUX Group 11: Debug Reduction #2		
0:4	TR_GROUP9_INPUT[6:10]	To main debug multiplexer
MUX Group 12: Debug Reduction #3		
0:4	TR_GROUP9_INPUT[11:15]	To main debug multiplexer
MUX Group 13: AXI-DMA trigger multiplexer		
0:3	AXIDMA_TR_IN[0:3]	Triggers to AXI M-DMA1

19 Triggers one-to-one

Table 19-1 Triggers 1:1

Input	Trigger In	Trigger Out	Description
MUX Group 0: CAN0 to P-DMA0 Triggers			
0	CAN0_DBG_TR_OUT[0]	PDMA0_TR_IN[32]	CAN0, Channel #0 P-DMA0 trigger
1	CAN0_FIFO0_TR_OUT[0]	PDMA0_TR_IN[33]	CAN0, Channel #0 FIFO0 trigger
2	CAN0_FIFO1_TR_OUT[0]	PDMA0_TR_IN[34]	CAN0, Channel #0 FIFO1 trigger
3	CAN0_DBG_TR_OUT[1]	PDMA0_TR_IN[35]	CAN0, Channel #1 P-DMA0 trigger
4	CAN0_FIFO0_TR_OUT[1]	PDMA0_TR_IN[36]	CAN0, Channel #1 FIFO0 trigger
5	CAN0_FIFO1_TR_OUT[1]	PDMA0_TR_IN[37]	CAN0, Channel #1 FIFO1 trigger
6:37	PASS0_CH_DONE_TR_OUT[0:31]	PDMA0_TR_IN[38:69]	PASS0 SAR0 to P-DMA0 direct connect
38	SMIF0_TX_TR_OUT	PDMA0_TR_IN[70]	SMIF TX to P-DMA0 Trigger
39	SMIF0_RX_TR_OUT	PDMA0_TR_IN[71]	SMIF RX to P-DMA0 Trigger
40:41	CXPI0_TX_TR_OUT[0:1]	PDMA0_TR_IN[72:73]	CXPI 0 TX P-DMA0 Triggers
42:43	CXPI0_RX_TR_OUT[0:1]	PDMA0_TR_IN[74:75]	CXPI 0 RX P-DMA0 Triggers
MUX Group 1: SCBx to P-DMA1 Triggers			
0	SCB0_TX_TR_OUT	PDMA1_TR_IN[16]	SCB0 to P-DMA1 Trigger
1	SCB0_RX_TR_OUT	PDMA1_TR_IN[17]	SCB0 to P-DMA1 Trigger
2	SCB1_TX_TR_OUT	PDMA1_TR_IN[18]	SCB1 to P-DMA1 Trigger
3	SCB1_RX_TR_OUT	PDMA1_TR_IN[19]	SCB1 to P-DMA1 Trigger
4	SCB2_TX_TR_OUT	PDMA1_TR_IN[20]	SCB2 to P-DMA1 Trigger
5	SCB2_RX_TR_OUT	PDMA1_TR_IN[21]	SCB2 to P-DMA1 Trigger
6	SCB3_TX_TR_OUT	PDMA1_TR_IN[22]	SCB3 to P-DMA1 Trigger
7	SCB3_RX_TR_OUT	PDMA1_TR_IN[23]	SCB3 to P-DMA1 Trigger
8	SCB4_TX_TR_OUT	PDMA1_TR_IN[24]	SCB4 to P-DMA1 Trigger
9	SCB4_RX_TR_OUT	PDMA1_TR_IN[25]	SCB4 to P-DMA1 Trigger
10	SCB5_TX_TR_OUT	PDMA1_TR_IN[26]	SCB5 to P-DMA1 Trigger
11	SCB5_RX_TR_OUT	PDMA1_TR_IN[27]	SCB5 to P-DMA1 Trigger
12	SCB6_TX_TR_OUT	PDMA1_TR_IN[28]	SCB6 to P-DMA1 Trigger
13	SCB6_RX_TR_OUT	PDMA1_TR_IN[29]	SCB6 to P-DMA1 Trigger
14	SCB7_TX_TR_OUT	PDMA1_TR_IN[30]	SCB7 to P-DMA1 Trigger
15	SCB7_RX_TR_OUT	PDMA1_TR_IN[31]	SCB7 to P-DMA1 Trigger
16	SCB8_TX_TR_OUT	PDMA1_TR_IN[32]	SCB8 to P-DMA1 Trigger
17	SCB8_RX_TR_OUT	PDMA1_TR_IN[33]	SCB8 to P-DMA1 Trigger
18	SCB9_TX_TR_OUT	PDMA1_TR_IN[34]	SCB9 to P-DMA1 Trigger
19	SCB9_RX_TR_OUT	PDMA1_TR_IN[35]	SCB9 to P-DMA1 Trigger
20	SCB10_TX_TR_OUT	PDMA1_TR_IN[36]	SCB10 to P-DMA1 Trigger
21	SCB10_RX_TR_OUT	PDMA1_TR_IN[37]	SCB10 to P-DMA1 Trigger
22	SCB11_TX_TR_OUT	PDMA1_TR_IN[38]	SCB11 to P-DMA1 Trigger
23	SCB11_RX_TR_OUT	PDMA1_TR_IN[39]	SCB11 to P-DMA1 Trigger
24	CAN1_DBG_TR_OUT[0]	PDMA1_TR_IN[40]	CAN1 Channel #0 P-DMA1 trigger
25	CAN1_FIFO0_TR_OUT[0]	PDMA1_TR_IN[41]	CAN1 Channel #0 FIFO0 trigger
26	CAN1_FIFO1_TR_OUT[0]	PDMA1_TR_IN[42]	CAN1 Channel #0 FIFO1 trigger
27	CAN1_DBG_TR_OUT[1]	PDMA1_TR_IN[43]	CAN1 Channel #1 P-DMA1 trigger
28	CAN1_FIFO0_TR_OUT[1]	PDMA1_TR_IN[44]	CAN1 Channel #1 FIFO0 trigger
29	CAN1_FIFO1_TR_OUT[1]	PDMA1_TR_IN[45]	CAN1 Channel #1 FIFO1 trigger

Table 19-1 Triggers 1:1 *(continued)*

Input	Trigger In	Trigger Out	Description
30	SMIF1_TX_TR_OUT	PDMA1_TR_IN[46]	SMIF1 TX to P-DMA1 Trigger
31	SMIF1_RX_TR_OUT	PDMA1_TR_IN[47]	SMIF1 RX to P-DMA1 Trigger
32:36	MIXER0_TR_SRC_REQ_OUT[0:4]	PDMA1_TR_IN[48:52]	MIXER0 to P-DMA1 trigger
37	MIXER0_TR_DST_REQ_OUT	PDMA1_TR_IN[53]	MIXER0 to P-DMA1 trigger
38:42	MIXER1_TR_SRC_REQ_OUT[0:4]	PDMA1_TR_IN[54:58]	MIXER1 to P-DMA1 trigger
43	MIXER1_TR_DST_REQ_OUT	PDMA1_TR_IN[59]	MIXER1 to P-DMA1 trigger
44:47	AXIDMA_TR_OUT[0:3]	PDMA1_TR_IN[60:63]	AXI M-DMA1 to P-DMA1 trigger
52:55	TDM0_TX_TR_OUT[0:3]	PDMA1_TR_IN[68:71]	TDM0 TX to P-DMA1 trigger
56:59	TDM0_RX_TR_OUT[0:3]	PDMA1_TR_IN[72:75]	TDM0 RX to P-DMA1 trigger
60:64	SG0_TX_TR_OUT[0:4]	PDMA1_TR_IN[76:80]	SG0 TX to P-DMA1 trigger
65:66	PWM0_TX_TR_OUT[0:1]	PDMA1_TR_IN[81:82]	PWM0 TX to P-DMA1 trigger
67	AUDIODAC0_TX_TR_OUT	PDMA1_TR_IN[83]	AUDIODAC0 to P-DMA1 trigger
MUX Group 2: PASS SARx to TCPWM1 direct connect			
0	PASS0_CH_RANGEVIO_TR_OUT[0]	TCPWM0_16_ONE_CNT_TR_IN[0]	SAR0 ch#0[43], range violation to TCPWM0 Group#0 Counter#00 trig=2
1	PASS0_CH_RANGEVIO_TR_OUT[1]	TCPWM0_16_ONE_CNT_TR_IN[1]	SAR0 ch#1, range violation to TCPWM0 Group#0 Counter#01 trig=2
2	PASS0_CH_RANGEVIO_TR_OUT[2]	TCPWM0_16_ONE_CNT_TR_IN[2]	SAR0 ch#2, range violation to TCPWM0 Group#0 Counter#02 trig=2
3	PASS0_CH_RANGEVIO_TR_OUT[3]	TCPWM0_16_ONE_CNT_TR_IN[3]	SAR0 ch#3, range violation to TCPWM0 Group#0 Counter#03 trig=2
4	PASS0_CH_RANGEVIO_TR_OUT[4]	TCPWM0_16_ONE_CNT_TR_IN[4]	SAR0 ch#4, range violation to TCPWM0 Group#0 Counter#04 trig=2
5	PASS0_CH_RANGEVIO_TR_OUT[5]	TCPWM0_16_ONE_CNT_TR_IN[5]	SAR0 ch#5, range violation to TCPWM0 Group#0 Counter#05 trig=2
6	PASS0_CH_RANGEVIO_TR_OUT[6]	TCPWM0_16_ONE_CNT_TR_IN[6]	SAR0 ch#6, range violation to TCPWM0 Group#0 Counter#06 trig=2
7	PASS0_CH_RANGEVIO_TR_OUT[7]	TCPWM0_16_ONE_CNT_TR_IN[7]	SAR0 ch#7, range violation to TCPWM0 Group#0 Counter#07 trig=2
8	PASS0_CH_RANGEVIO_TR_OUT[8]	TCPWM0_16_ONE_CNT_TR_IN[8]	SAR0 ch#8, range violation to TCPWM0 Group#0 Counter#08 trig=2
9	PASS0_CH_RANGEVIO_TR_OUT[9]	TCPWM0_16_ONE_CNT_TR_IN[9]	SAR0 ch#9, range violation to TCPWM0 Group#0 Counter#09 trig=2
10	PASS0_CH_RANGEVIO_TR_OUT[10]	TCPWM0_16_ONE_CNT_TR_IN[10]	SAR0 ch#10, range violation to TCPWM0 Group#0 Counter#10 trig=2
11	PASS0_CH_RANGEVIO_TR_OUT[11]	TCPWM0_16_ONE_CNT_TR_IN[11]	SAR0 ch#11, range violation to TCPWM0 Group#0 Counter#11 trig=2
12	PASS0_CH_RANGEVIO_TR_OUT[12]	TCPWM0_16_ONE_CNT_TR_IN[12]	SAR0 ch#12, range violation to TCPWM0 Group#0 Counter#12 trig=2
13	PASS0_CH_RANGEVIO_TR_OUT[13]	TCPWM0_16_ONE_CNT_TR_IN[13]	SAR0 ch#13, range violation to TCPWM0 Group#0 Counter#13 trig=2
14	PASS0_CH_RANGEVIO_TR_OUT[14]	TCPWM0_16_ONE_CNT_TR_IN[14]	SAR0 ch#14, range violation to TCPWM0 Group#0 Counter#14 trig=2
15	PASS0_CH_RANGEVIO_TR_OUT[15]	TCPWM0_16_ONE_CNT_TR_IN[15]	SAR0 ch#15, range violation to TCPWM0 Group#0 Counter#15 trig=2
16	PASS0_CH_RANGEVIO_TR_OUT[16]	TCPWM0_16_ONE_CNT_TR_IN[16]	SAR0 ch#16, range violation to TCPWM0 Group#0 Counter#16 trig=2
17	PASS0_CH_RANGEVIO_TR_OUT[17]	TCPWM0_16_ONE_CNT_TR_IN[17]	SAR0 ch#17, range violation to TCPWM0 Group#0 Counter#17 trig=2
18	PASS0_CH_RANGEVIO_TR_OUT[18]	TCPWM0_16_ONE_CNT_TR_IN[18]	SAR0 ch#18, range violation to TCPWM0 Group#0 Counter#18 trig=2
19	PASS0_CH_RANGEVIO_TR_OUT[19]	TCPWM0_16_ONE_CNT_TR_IN[19]	SAR0 ch#19, range violation to TCPWM0 Group#0 Counter#19 trig=2
20	PASS0_CH_RANGEVIO_TR_OUT[20]	TCPWM0_16M_ONE_CNT_TR_IN[0]	SAR0 ch#20, range violation to TCPWM0 Group#1 Counter#00 trig=2
21	PASS0_CH_RANGEVIO_TR_OUT[21]	TCPWM0_16M_ONE_CNT_TR_IN[1]	SAR0 ch#21, range violation to TCPWM0 Group#1 Counter#01 trig=2

Note

43.Each logical channel of SAR ADC[x] can be connected to any of the SAR ADC[x]_y external pin. (x = 0, or 1, or, 2 and y=0 to max 31)

Table 19-1 Triggers 1:1 *(continued)*

Input	Trigger In	Trigger Out	Description
22	PASS0_CH_RANGEVIO_TR_OUT[22]	TCPWM0_16M_ONE_CNT_TR_IN[2]	SAR0 ch#22, range violation to TCPWM0 Group#1 Counter#02 trig=2
23	PASS0_CH_RANGEVIO_TR_OUT[23]	TCPWM0_16M_ONE_CNT_TR_IN[3]	SAR0 ch#23, range violation to TCPWM0 Group#1 Counter#03 trig=2
24	PASS0_CH_RANGEVIO_TR_OUT[24]	TCPWM0_16M_ONE_CNT_TR_IN[4]	SAR0 ch#24, range violation to TCPWM0 Group#1 Counter#04 trig=2
25	PASS0_CH_RANGEVIO_TR_OUT[25]	TCPWM0_16M_ONE_CNT_TR_IN[5]	SAR0 ch#25, range violation to TCPWM0 Group#1 Counter#05 trig=2
26	PASS0_CH_RANGEVIO_TR_OUT[26]	TCPWM0_16M_ONE_CNT_TR_IN[6]	SAR0 ch#26, range violation to TCPWM0 Group#1 Counter#06 trig=2
27	PASS0_CH_RANGEVIO_TR_OUT[27]	TCPWM0_16M_ONE_CNT_TR_IN[7]	SAR0 ch#27, range violation to TCPWM0 Group#1 Counter#07 trig=2
28	PASS0_CH_RANGEVIO_TR_OUT[28]	TCPWM0_16M_ONE_CNT_TR_IN[8]	SAR0 ch#28, range violation to TCPWM0 Group#1 Counter#08 trig=2
29	PASS0_CH_RANGEVIO_TR_OUT[29]	TCPWM0_16M_ONE_CNT_TR_IN[9]	SAR0 ch#29, range violation to TCPWM0 Group#1 Counter#09 trig=2
30	PASS0_CH_RANGEVIO_TR_OUT[30]	TCPWM0_16M_ONE_CNT_TR_IN[10]	SAR0 ch#30, range violation to TCPWM0 Group#1 Counter#10 trig=2
31	PASS0_CH_RANGEVIO_TR_OUT[31]	TCPWM0_16M_ONE_CNT_TR_IN[11]	SAR0 ch#31, range violation to TCPWM0 Group#1 Counter#11 trig=2
MUX Group 3: TCPWM0 to PASS SARx			
0:19	TCPWM0_16_TR_OUT1[0:19]	PASS0_CH_TR_IN[0:19]	TCPWM0 Group #0 Counter #00 through 19 (PWM0_0 to PWM0_19) to SAR0 ch#0 through SAR0 ch#19
20:31	TCPWM0_16M_TR_OUT1[0:11]	PASS0_CH_TR_IN[20:31]	TCPWM0 Group #1 Counter #00 through 11 (PWM0_M_0 to PWM0_M_11) to SAR0 ch#20 through SAR0 ch#31
MUX Group 4: Acknowledge triggers from P-DMA1 to CAN1			
0	PDMA1_TR_OUT[40]	CAN1_DBG_TR_ACK[0]	CAN1 Channel#0 P-DMA1 acknowledge
1	PDMA1_TR_OUT[43]	CAN1_DBG_TR_ACK[1]	CAN1 Channel#1 P-DMA1 acknowledge
MUX Group 5: Acknowledge triggers from P-DMA0 to CAN0			
0	PDMA0_TR_OUT[32]	CAN0_DBG_TR_ACK[0]	CAN0 Channel#0 P-DMA0 acknowledge
1	PDMA0_TR_OUT[35]	CAN0_DBG_TR_ACK[1]	CAN0 Channel#1 P-DMA0 acknowledge
MUX Group 6: TCPWM0 to LIN0 triggers			
0:1	TCPWM0_16_TR_OUT1[24:25]	LIN0_CMD_TR_IN[0:1]	TCPWM0 (Group #0 Counter #24 to #25) to LIN0
MUX Group 7: TCPWM0_TO_CXPI (TCPWM0 to CXPI)			
0:1	TCPWM0_16_TR_OUT1[26:27]	CXPI0_CMD_TR_IN[0:1]	TCPWM0 (Group #0 Counter #24 to #25) to CXPI0

20 Peripheral clocks

Table 20-1 Peripheral clock assignments

Output	Destination	Description
CPUSS Root Clocks (Group 0)		
0	PCLK_CPUSS_CLOCK_TRACE_IN	Trace clock
1	PCLK_SMARTIO7_CLOCK	Smart I/O #7
2	PCLK_TCPWM0_CLOCKS0	TCPWM0 Group #0, Counter #0
3	PCLK_TCPWM0_CLOCKS1	TCPWM0 Group #0, Counter #1
4	PCLK_TCPWM0_CLOCKS2	TCPWM0 Group #0, Counter #2
5	PCLK_TCPWM0_CLOCKS3	TCPWM0 Group #0, Counter #3
6	PCLK_TCPWM0_CLOCKS4	TCPWM0 Group #0, Counter #4
7	PCLK_TCPWM0_CLOCKS5	TCPWM0 Group #0, Counter #5
8	PCLK_TCPWM0_CLOCKS6	TCPWM0 Group #0, Counter #6
9	PCLK_TCPWM0_CLOCKS7	TCPWM0 Group #0, Counter #7
10	PCLK_TCPWM0_CLOCKS8	TCPWM0 Group #0, Counter #8
11	PCLK_TCPWM0_CLOCKS9	TCPWM0 Group #0, Counter #9
12	PCLK_TCPWM0_CLOCKS10	TCPWM0 Group #0, Counter #10
13	PCLK_TCPWM0_CLOCKS11	TCPWM0 Group #0, Counter #11
14	PCLK_TCPWM0_CLOCKS12	TCPWM0 Group #0, Counter #12
15	PCLK_TCPWM0_CLOCKS13	TCPWM0 Group #0, Counter #13
16	PCLK_TCPWM0_CLOCKS14	TCPWM0 Group #0, Counter #14
17	PCLK_TCPWM0_CLOCKS15	TCPWM0 Group #0, Counter #15
18	PCLK_TCPWM0_CLOCKS16	TCPWM0 Group #0, Counter #16
19	PCLK_TCPWM0_CLOCKS17	TCPWM0 Group #0, Counter #17
20	PCLK_TCPWM0_CLOCKS18	TCPWM0 Group #0, Counter #18
21	PCLK_TCPWM0_CLOCKS19	TCPWM0 Group #0, Counter #19
22	PCLK_TCPWM0_CLOCKS20	TCPWM0 Group #0, Counter #20
23	PCLK_TCPWM0_CLOCKS21	TCPWM0 Group #0, Counter #21
24	PCLK_TCPWM0_CLOCKS22	TCPWM0 Group #0, Counter #22
25	PCLK_TCPWM0_CLOCKS23	TCPWM0 Group #0, Counter #23
26	PCLK_TCPWM0_CLOCKS24	TCPWM0 Group #0, Counter #24
27	PCLK_TCPWM0_CLOCKS25	TCPWM0 Group #0, Counter #25
28	PCLK_TCPWM0_CLOCKS26	TCPWM0 Group #0, Counter #26
29	PCLK_TCPWM0_CLOCKS27	TCPWM0 Group #0, Counter #27
30	PCLK_TCPWM0_CLOCKS28	TCPWM0 Group #0, Counter #28
31	PCLK_TCPWM0_CLOCKS29	TCPWM0 Group #0, Counter #29
32	PCLK_TCPWM0_CLOCKS30	TCPWM0 Group #0, Counter #30
33	PCLK_TCPWM0_CLOCKS31	TCPWM0 Group #0, Counter #31
34	PCLK_TCPWM0_CLOCKS32	TCPWM0 Group #0, Counter #32
35	PCLK_TCPWM0_CLOCKS33	TCPWM0 Group #0, Counter #33
36	PCLK_TCPWM0_CLOCKS34	TCPWM0 Group #0, Counter #34
37	PCLK_TCPWM0_CLOCKS35	TCPWM0 Group #0, Counter #35

Table 20-1 Peripheral clock assignments *(continued)*

Output	Destination	Description
38	PCLK_TCPWM0_CLOCKS36	TCPWM0 Group #0, Counter #36
39	PCLK_TCPWM0_CLOCKS37	TCPWM0 Group #0, Counter #37
40	PCLK_TCPWM0_CLOCKS256	TCPWM0 Group #1, Counter #0
41	PCLK_TCPWM0_CLOCKS257	TCPWM0 Group #1, Counter #1
42	PCLK_TCPWM0_CLOCKS258	TCPWM0 Group #1, Counter #2
43	PCLK_TCPWM0_CLOCKS259	TCPWM0 Group #1, Counter #3
44	PCLK_TCPWM0_CLOCKS260	TCPWM0 Group #1, Counter #4
45	PCLK_TCPWM0_CLOCKS261	TCPWM0 Group #1, Counter #5
46	PCLK_TCPWM0_CLOCKS262	TCPWM0 Group #1, Counter #6
47	PCLK_TCPWM0_CLOCKS263	TCPWM0 Group #1, Counter #7
48	PCLK_TCPWM0_CLOCKS264	TCPWM0 Group #1, Counter #8
49	PCLK_TCPWM0_CLOCKS265	TCPWM0 Group #1, Counter #9
50	PCLK_TCPWM0_CLOCKS266	TCPWM0 Group #1, Counter #10
51	PCLK_TCPWM0_CLOCKS267	TCPWM0 Group #1, Counter #11
52	PCLK_TCPWM0_CLOCKS512	TCPWM0 Group #2, Counter #0
53	PCLK_TCPWM0_CLOCKS513	TCPWM0 Group #2, Counter #1
54	PCLK_TCPWM0_CLOCKS514	TCPWM0 Group #2, Counter #2
55	PCLK_TCPWM0_CLOCKS515	TCPWM0 Group #2, Counter #3
56	PCLK_TCPWM0_CLOCKS516	TCPWM0 Group #2, Counter #4
57	PCLK_TCPWM0_CLOCKS517	TCPWM0 Group #2, Counter #5
58	PCLK_TCPWM0_CLOCKS518	TCPWM0 Group #2, Counter #6
59	PCLK_TCPWM0_CLOCKS519	TCPWM0 Group #2, Counter #7
60	PCLK_TCPWM0_CLOCKS520	TCPWM0 Group #2, Counter #8
61	PCLK_TCPWM0_CLOCKS521	TCPWM0 Group #2, Counter #9
62	PCLK_TCPWM0_CLOCKS522	TCPWM0 Group #2, Counter #10
63	PCLK_TCPWM0_CLOCKS523	TCPWM0 Group #2, Counter #11
64	PCLK_TCPWM0_CLOCKS524	TCPWM0 Group #2, Counter #12
65	PCLK_TCPWM0_CLOCKS525	TCPWM0 Group #2, Counter #13
66	PCLK_TCPWM0_CLOCKS526	TCPWM0 Group #2, Counter #14
67	PCLK_TCPWM0_CLOCKS527	TCPWM0 Group #2, Counter #15
68	PCLK_TCPWM0_CLOCKS528	TCPWM0 Group #2, Counter #16
69	PCLK_TCPWM0_CLOCKS529	TCPWM0 Group #2, Counter #17
70	PCLK_TCPWM0_CLOCKS530	TCPWM0 Group #2, Counter #18
71	PCLK_TCPWM0_CLOCKS531	TCPWM0 Group #2, Counter #19
72	PCLK_TCPWM0_CLOCKS532	TCPWM0 Group #2, Counter #20
73	PCLK_TCPWM0_CLOCKS533	TCPWM0 Group #2, Counter #21
74	PCLK_TCPWM0_CLOCKS534	TCPWM0 Group #2, Counter #22
75	PCLK_TCPWM0_CLOCKS535	TCPWM0 Group #2, Counter #23
76	PCLK_TCPWM0_CLOCKS536	TCPWM0 Group #2, Counter #24
77	PCLK_TCPWM0_CLOCKS537	TCPWM0 Group #2, Counter #25
78	PCLK_TCPWM0_CLOCKS538	TCPWM0 Group #2, Counter #26

Table 20-1 **Peripheral clock assignments** *(continued)*

Output	Destination	Description
79	PCLK_TCPWM0_CLOCKS539	TCPWM0 Group #2, Counter #27
80	PCLK_TCPWM0_CLOCKS540	TCPWM0 Group #2, Counter #28
81	PCLK_TCPWM0_CLOCKS541	TCPWM0 Group #2, Counter #29
82	PCLK_TCPWM0_CLOCKS542	TCPWM0 Group #2, Counter #30
83	PCLK_TCPWM0_CLOCKS543	TCPWM0 Group #2, Counter #31
COMM Root Clocks (Group 1)		
0	PCLK_CANFD0_CLOCK_CAN0	CAN0, Channel #0
1	PCLK_CANFD0_CLOCK_CAN1	CAN0, Channel #1
2	PCLK_CANFD1_CLOCK_CAN0	CAN1, Channel #0
3	PCLK_CANFD1_CLOCK_CAN1	CAN1, Channel #1
4	PCLK_LIN0_CLOCK_CH_EN0	LIN0, Channel #0
5	PCLK_LIN0_CLOCK_CH_EN1	LIN0, Channel #1
6	PCLK_CXPI0_CLOCK_CH_EN0	CXPI0, Channel #0
7	PCLK_CXPI0_CLOCK_CH_EN1	CXPI0, Channel #1
8	PCLK_SCB0_CLOCK	SCB0
9	PCLK_SCB1_CLOCK	SCB1
10	PCLK_SCB2_CLOCK	SCB2
11	PCLK_SCB3_CLOCK	SCB3
12	PCLK_SCB4_CLOCK	SCB4
13	PCLK_SCB5_CLOCK	SCB5
14	PCLK_SCB6_CLOCK	SCB6
15	PCLK_SCB7_CLOCK	SCB7
16	PCLK_SCB8_CLOCK	SCB8
17	PCLK_SCB9_CLOCK	SCB9
18	PCLK_SCB10_CLOCK	SCB10
19	PCLK_SCB11_CLOCK	SCB11
20	PCLK_PASS0_CLOCK_SAR0	SAR0

21 Faults

Table 21-1 Fault assignments

Fault	Source	Description
0	CPUSS_MPU_VIO_0	CM0+ SMPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation.
1	CPUSS_MPU_VIO_1	Crypto SMPU violation. See CPUSS_MPU_VIO_0 description.
2	CPUSS_MPU_VIO_2	P-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
3	CPUSS_MPU_VIO_3	P-DMA1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
4	CPUSS_MPU_VIO_4	M-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
9	CPUSS_MPU_VIO_9	ETH0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
11	CPUSS_MPU_VIO_11	AXI M-DMA1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
12	CPUSS_MPU_VIO_12	VIDEOSS0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
13	CPUSS_MPU_VIO_13	CM7_1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
14	CPUSS_MPU_VIO_14	CM7_0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
15	CPUSS_MPU_VIO_15	Test Controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.
16	CPUSS_CM7_0_CACHE_C_ECC	Correctable ECC error in CM7_0 Cache memories DATA0[16:2]: location information: Tag/Data SRAM, Way, Index and line Offset, see CM7 UGRM IEBR0/DEBR0 description for details. DATA0[31]: 0=Instruction cache, 1= Data cache
17	CPUSS_CM7_0_CACHE_NC_ECC	Non Correctable ECC error in CM7_0 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description
18	CPUSS_CM7_0_TCM_C_ECC	Correctable ECC error in CM7_0 TCM memory DATA0[23:2]: Violating address. DATA1[7:0]: Syndrome of code word (at address offset 0x0). DATA1[31:30]: 0= ITCM, 2=D0TCM, 3=D1TCM
19	CPUSS_CM7_0_TCM_NC_ECC	Non Correctable ECC error in CM7_0 TCM memory. See CPUSS_CM7_0_TCM_C_ECC description.
20	CPUSS_CM7_1_CACHE_C_ECC	Correctable ECC error in CM7_1 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description
21	CPUSS_CM7_1_CACHE_NC_ECC	Non Correctable ECC error in CM7_1 Cache memories. See CPUSS_CM7_0_CACHE_C_ECC description
22	CPUSS_CM7_1_TCM_C_ECC	CPU CM7_1 TCM memory correctable ECC violation. See CPUSS_CM7_0_TCM_C_ECC description.
23	CPUSS_CM7_1_TCM_NC_ECC	CPU CM7_1 TCM memory non-correctable ECC violation. See CPUSS_CM7_0_TCM_C_ECC description.
24	PERI_PERI_C_ECC	Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word.
25	PERI_PERI_NC_ECC	Peripheral protection SRAM non-correctable ECC violation
26	PERI_MS_VIO_0	CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: master interface, PPU violation, “1': timeout detected, “2”: bus error, other: undefined.
27	PERI_MS_VIO_1	CM7_0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.

Table 21-1 Fault assignments *(continued)*

Fault	Source	Description
28	PERI_MS_VIO_2	CM7_1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
29	PERI_MS_VIO_3	P-DMA0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
30	PERI_MS_VIO_4	P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description.
32	PERI_GROUP_VIO_0	Peripheral Group #0 violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: “0”: decoder or peripheral bus error, other: undefined.
33	PERI_GROUP_VIO_1	Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description.
34	PERI_GROUP_VIO_2	Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description.
35	PERI_GROUP_VIO_3	Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description.
36	PERI_GROUP_VIO_4	Peripheral Group #4 violation. See PERI_GROUP_VIO_0 description.
37	PERI_GROUP_VIO_5	Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description.
38	PERI_GROUP_VIO_6	Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description.
40	PERI_GROUP_VIO_8	Peripheral Group #8 violation. See PERI_GROUP_VIO_0 description.
41	PERI_GROUP_VIO_9	Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description.
42	PERI_GROUP_VIO_10	Peripheral Group #10 violation. See PERI_GROUP_VIO_0 description.
48	CPUSS_FLASHC_MAIN_BUS_ERR	Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
49	CPUSS_FLASHC_MAIN_C_ECC	Flash controller main flash correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).
50	CPUSS_FLASHC_MAIN_NC_ECC	Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description.
51	CPUSS_FLASHC_WORK_BUS_ERR	Flash controller work-flash bus error. See CPUSS_FLASHC_MAIN_BUS_ERR description.
52	CPUSS_FLASHC_WORK_C_ECC	Flash controller work flash correctable ECC violation. DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word.
53	CPUSS_FLASHC_WORK_NC_ECC	Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description.
54	CPUSS_FLASHC_CM0_CA_C_ECC	Flash controller CM0+ cache correctable ECC violation. DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).
55	CPUSS_FLASHC_CM0_CA_NC_ECC	Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description.
56	CPUSS_FM_SRAMC_C_ECC	Flash code storage SRAM memory correctable ECC violation: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word.
57	CPUSS_FM_SRAMC_NC_ECC	Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description.
58	CPUSS_RAMC0_C_ECC	System memory controller 0 correctable ECC violation: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word.

Table 21-1 Fault assignments *(continued)*

Fault	Source	Description
59	CPUSS_RAMC0_NC_ECC	System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
60	CPUSS_RAMC1_C_ECC	System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
61	CPUSS_RAMC1_NC_ECC	System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
62	CPUSS_RAMC2_C_ECC	System memory controller 2 correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
63	CPUSS_RAMC2_NC_ECC	System memory controller 2 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description.
64	CPUSS_CRYPTO_C_ECC	Crypto memory correctable ECC violation. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.
65	CPUSS_CRYPTO_NC_ECC	Crypto memory non-correctable ECC violation. See CPUSS_CRYPTO_C_ECC description.
66	CPUSS_DW0_C_ECC	P-DMA0 memory correctable ECC violation: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word.
67	CPUSS_DW0_NC_ECC	P-DMA0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
68	CPUSS_DW1_C_ECC	P-DMA1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description.
69	CPUSS_DW1_NC_ECC	P-DMA1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description.
70	CANFD_0_CAN_C_ECC	CAN0 message buffer correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.
71	CANFD_0_CAN_NC_ECC	CAN0 message buffer non-correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).
72	CANFD_1_CAN_C_ECC	CAN1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description.
73	CANFD_1_CAN_NC_ECC	CAN1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description.
82	VIDEOSS_0_VRPU_RD_0	VIDEOSS Fault Reporting VRPU read 0: DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier of the master within mxvideoss. DATA1[15:12]: Protection context identifier. DATA1[31]: '1': VRPU violation, '0': undefined. other bits: undefined.
83	VIDEOSS_0_VRPU_RD_1	VIDEOSS Fault Reporting VRPU read 1. See VIDEOSS_VRPU0 description.
84	VIDEOSS_0_VRPU_RD_2	VIDEOSS Fault Reporting VRPU read 2. See VIDEOSS_VRPU0 description.
85	VIDEOSS_0_VRPU_RD_3	VIDEOSS Fault Reporting VRPU read 3. See VIDEOSS_VRPU0 description.
86	VIDEOSS_0_VRPU_RD_4	VIDEOSS Fault Reporting VRPU read 4. See VIDEOSS_VRPU0 description.
87	VIDEOSS_0_VRPU_WR_0	VIDEOSS Fault Reporting VRPU write 0. See VIDEOSS_VRPU0 description.
88	VIDEOSS_0_VRPU_WR_1	VIDEOSS Fault Reporting VRPU write 1. See VIDEOSS_VRPU0 description.
90	SRSS_FAULT_CSV	Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CLK_HF* root CSV violation flags. DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs) DATA0[25]: CLK_LF CSV violation flag DATA0[26]: CLK_HVILO CSV violation flag

Table 21-1 Fault assignments *(continued)*

Fault	Source	Description
91	SRSS_FAULT_SSV	Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time. DATA0[0]: BOD on VDDA_ADC DATA[1]: OVD on VDDA_ADC DATA[16]: LVD/HVD #1 DATA0[17]: LVD/HVD #2
92	SRSS_FAULT_MCWDT0	Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT
93	SRSS_FAULT_MCWDT1	Fault output for MCWDT1 (all sub-counters). See SRSS_FAULT_MCWDT0 description.
94	SRSS_FAULT_MCWDT2	Fault output for MCWDT2 (all sub-counters). See SRSS_FAULT_MCWDT0 description.

22 Peripheral protection unit fixed structure pairs

Protection pair is a pair PPU structures, a master, and a slave structure. The master structure protects the slave structure, and the slave structure protects resources such as peripheral registers, or the peripheral itself.

Refer to **Table 6-1** for the FX PPU Base address.

Table 22-1 PPU fixed structure pairs

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
0	PERI_MAIN	0x40000200	0x00000040	Peripheral Interconnect main
1	PERI_SECURE	0x40002000	0x00000004	Peripheral interconnect secure
2	PERI_GR0_GROUP	0x40004010	0x00000004	Peripheral Group #0 main
3	PERI_GR1_GROUP	0x40004050	0x00000004	Peripheral Group #1 main
4	PERI_GR2_GROUP	0x40004090	0x00000004	Peripheral Group #2 main
5	PERI_GR3_GROUP	0x400040C0	0x00000020	Peripheral Group #3 main
6	PERI_GR4_GROUP	0x40004100	0x00000020	Peripheral Group #4 main
7	PERI_GR5_GROUP	0x40004140	0x00000020	Peripheral Group #5 main
8	PERI_GR6_GROUP	0x40004180	0x00000020	Peripheral Group #6 main
9	PERI_GR8_GROUP	0x40004200	0x00000020	Peripheral Group #8 main
10	PERI_GR9_GROUP	0x40004240	0x00000020	Peripheral Group #9 main
11	PERI_GR10_GROUP	0x40004280	0x00000020	Peripheral Group #10 main
12	PERI_GR0_BOOT	0x40004020	0x00000004	Peripheral Group #0 boot
13	PERI_GR1_BOOT	0x40004060	0x00000004	Peripheral Group #1 boot
14	PERI_GR2_BOOT	0x400040A0	0x00000004	Peripheral Group #2 boot
15	PERI_GR3_BOOT	0x400040E0	0x00000004	Peripheral Group #3 boot
16	PERI_GR4_BOOT	0x40004120	0x00000004	Peripheral Group #4 boot
17	PERI_GR5_BOOT	0x40004160	0x00000004	Peripheral Group #5 boot
18	PERI_GR6_BOOT	0x400041A0	0x00000004	Peripheral Group #6 boot
19	PERI_GR8_BOOT	0x40004220	0x00000004	Peripheral Group #8 boot
20	PERI_GR9_BOOT	0x40004260	0x00000004	Peripheral Group #9 boot
21	PERI_GR10_BOOT	0x400042A0	0x00000004	Peripheral Group #10 boot
22	PERI_TR	0x40008000	0x00008000	Peripheral trigger multiplexer
23	PERI_MS_BOOT	0x40030000	0x00001000	Peripheral master slave boot
24	PERI_PCLK_MAIN	0x40040000	0x00004000	Peripheral clock main
25	CRYPTO_MAIN	0x40100000	0x00000400	Crypto main
26	CRYPTO_CRYPTO	0x40101000	0x00000800	Crypto MMIO (Memory Mapped I/O)
27	CRYPTO_BOOT	0x40102000	0x00000100	Crypto boot
28	CRYPTO_KEY0	0x40102100	0x00000004	Crypto Key #0
29	CRYPTO_KEY1	0x40102120	0x00000004	Crypto Key #1
30	CRYPTO_BUF	0x40108000	0x00002000	Crypto buffer
31	CPUSS_CM7_0	0x40200000	0x00000400	CM7_0 CPU core
32	CPUSS_CM7_1	0x40200400	0x00000400	CM7_1 CPU core
33	CPUSS_CM0	0x40201000	0x00001000	CM0+ CPU core
34	CPUSS_BOOT[44]	0x40202000	0x00000200	CPUSS boot
35	CPUSS_CM0_INT	0x40208000	0x00001000	CPUSS CM0+ interrupts
36	CPUSS_CM7_0_INT	0x4020A000	0x00001000	CPUSS CM7_0 interrupts
37	CPUSS_CM7_1_INT	0x4020C000	0x00001000	CPUSS CM7_1 interrupts

Note

44.Fixed PPU is configured inside the Boot and user is not allowed to change the attributes of this PPU.

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
38	FAULT_STRUCT0_MAIN	0x40210000	0x00000100	CPUSS Fault Structure #0 main
39	FAULT_STRUCT1_MAIN	0x40210100	0x00000100	CPUSS Fault Structure #1 main
40	FAULT_STRUCT2_MAIN	0x40210200	0x00000100	CPUSS Fault Structure #2 main
41	FAULT_STRUCT3_MAIN	0x40210300	0x00000100	CPUSS Fault Structure #3 main
42	IPC_STRUCT0_IPC	0x40220000	0x00000020	CPUSS IPC Structure #0
43	IPC_STRUCT1_IPC	0x40220020	0x00000020	CPUSS IPC Structure #1
44	IPC_STRUCT2_IPC	0x40220040	0x00000020	CPUSS IPC Structure #2
45	IPC_STRUCT3_IPC	0x40220060	0x00000020	CPUSS IPC Structure #3
46	IPC_STRUCT4_IPC	0x40220080	0x00000020	CPUSS IPC Structure #4
47	IPC_STRUCT5_IPC	0x402200A0	0x00000020	CPUSS IPC Structure #5
48	IPC_STRUCT6_IPC	0x402200C0	0x00000020	CPUSS IPC Structure #6
49	IPC_STRUCT7_IPC	0x402200E0	0x00000020	CPUSS IPC Structure #7
50	IPC_INTR_STRUCT0_INTR	0x40221000	0x00000010	CPUSS IPC Interrupt Structure #0
51	IPC_INTR_STRUCT1_INTR	0x40221020	0x00000010	CPUSS IPC Interrupt Structure #1
52	IPC_INTR_STRUCT2_INTR	0x40221040	0x00000010	CPUSS IPC Interrupt Structure #2
53	IPC_INTR_STRUCT3_INTR	0x40221060	0x00000010	CPUSS IPC Interrupt Structure #3
54	IPC_INTR_STRUCT4_INTR	0x40221080	0x00000010	CPUSS IPC Interrupt Structure #4
55	IPC_INTR_STRUCT5_INTR	0x402210A0	0x00000010	CPUSS IPC Interrupt Structure #5
56	IPC_INTR_STRUCT6_INTR	0x402210C0	0x00000010	CPUSS IPC Interrupt Structure #6
57	IPC_INTR_STRUCT7_INTR	0x402210E0	0x00000010	CPUSS IPC Interrupt Structure #7
58	PROT_SMPU_MAIN	0x40230000	0x00000040	Peripheral protection SMPU main
59	PROT_MPU0_MAIN	0x40234000	0x00000004	Peripheral protection MPU #0 main
60	PROT_MPU9_MAIN	0x40236400	0x00000400	Peripheral protection MPU #9 main
61	PROT_MPU10_MAIN	0x40236800	0x00000400	Peripheral protection MPU #10 main
62	PROT_MPU11_MAIN	0x40236C00	0x00000004	Peripheral protection MPU #11 main
63	PROT_MPU12_MAIN	0x40237000	0x00000400	Peripheral protection MPU #12 main
64	PROT_MPU13_MAIN	0x40237400	0x00000004	Peripheral protection MPU #13 main
65	PROT_MPU14_MAIN	0x40237800	0x00000004	Peripheral protection MPU #14 main
66	PROT_MPU15_MAIN	0x40237C00	0x00000400	Peripheral protection MPU #15 main
67	FLASHC_MAIN	0x40240000	0x00000008	Flash controller main
68	FLASHC_CMD	0x40240008	0x00000004	Flash controller command
69	FLASHC_DFT	0x40240200	0x00000100	Flash controller tests
70	FLASHC_CM0	0x40240400	0x00000080	Flash controller CM0+
71	FLASHC_CM7_0	0x402404E0	0x00000004	Flash controller CM7_0
72	FLASHC_CM7_1	0x40240560	0x00000004	Flash controller CM7_1
73	FLASHC_CRYPTO	0x40240580	0x00000004	Flash controller Crypto
74	FLASHC_DW0	0x40240600	0x00000004	Flash controller P-DMA#0
75	FLASHC_DW1	0x40240680	0x00000004	Flash controller P-DMA#1
76	FLASHC_DMAC	0x40240700	0x00000004	Flash controller M-DMA#0
77	FLASHC_FlashMgmt[44]	0x4024F000	0x00000080	Flash management
78	FLASHC_MainSafety	0x4024F400	0x00000008	Flash controller main safety
79	FLASHC_WorkSafety	0x4024F500	0x00000004	Flash controller work safety
80	SRSS_GENERAL	0x40260000	0x00000400	SRSS General
81	SRSS_MAIN	0x40261000	0x00001000	SRSS main
82	SRSS_SECURE	0x40262000	0x00002000	SRSS secure

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
83	MCWDT0_CONFIG	0x40268000	0x00000080	MCWDT #0 configuration
84	MCWDT1_CONFIG	0x40268100	0x00000080	MCWDT #1 configuration
85	MCWDT2_CONFIG	0x40268200	0x00000080	MCWDT #2 configuration
86	MCWDT0_MAIN	0x40268080	0x00000040	MCWDT #0 main
87	MCWDT1_MAIN	0x40268180	0x00000040	MCWDT #1 main
88	MCWDT2_MAIN	0x40268280	0x00000040	MCWDT #2 main
89	WDT_CONFIG	0x4026C000	0x00000020	System WDT configuration
90	WDT_MAIN	0x4026C040	0x00000020	System WDT main
91	BACKUP_BACKUP	0x40270000	0x00010000	SRSS backup
92	DW0_DW	0x40280000	0x00000100	P-DMA#0 main
93	DW1_DW	0x40290000	0x00000100	P-DMA#1 main
94	DW0_DW_CRC	0x40280100	0x00000080	P-DMA#0 CRC
95	DW1_DW_CRC	0x40290100	0x00000080	P-DMA#1 CRC
96	DW0_CH_STRUCT0_CH	0x40288000	0x00000040	P-DMA#0 Channel #0
97	DW0_CH_STRUCT1_CH	0x40288040	0x00000040	P-DMA#0 Channel #1
98	DW0_CH_STRUCT2_CH	0x40288080	0x00000040	P-DMA#0 Channel #2
99	DW0_CH_STRUCT3_CH	0x402880C0	0x00000040	P-DMA#0 Channel #3
100	DW0_CH_STRUCT4_CH	0x40288100	0x00000040	P-DMA#0 Channel #4
101	DW0_CH_STRUCT5_CH	0x40288140	0x00000040	P-DMA#0 Channel #5
102	DW0_CH_STRUCT6_CH	0x40288180	0x00000040	P-DMA#0 Channel #6
103	DW0_CH_STRUCT7_CH	0x402881C0	0x00000040	P-DMA#0 Channel #7
104	DW0_CH_STRUCT8_CH	0x40288200	0x00000040	P-DMA#0 Channel #8
105	DW0_CH_STRUCT9_CH	0x40288240	0x00000040	P-DMA#0 Channel #9
106	DW0_CH_STRUCT10_CH	0x40288280	0x00000040	P-DMA#0 Channel #10
107	DW0_CH_STRUCT11_CH	0x402882C0	0x00000040	P-DMA#0 Channel #11
108	DW0_CH_STRUCT12_CH	0x40288300	0x00000040	P-DMA#0 Channel #12
109	DW0_CH_STRUCT13_CH	0x40288340	0x00000040	P-DMA#0 Channel #13
110	DW0_CH_STRUCT14_CH	0x40288380	0x00000040	P-DMA#0 Channel #14
111	DW0_CH_STRUCT15_CH	0x402883C0	0x00000040	P-DMA#0 Channel #15
112	DW0_CH_STRUCT16_CH	0x40288400	0x00000040	P-DMA#0 Channel #16
113	DW0_CH_STRUCT17_CH	0x40288440	0x00000040	P-DMA#0 Channel #17
114	DW0_CH_STRUCT18_CH	0x40288480	0x00000040	P-DMA#0 Channel #18
115	DW0_CH_STRUCT19_CH	0x402884C0	0x00000040	P-DMA#0 Channel #19
116	DW0_CH_STRUCT20_CH	0x40288500	0x00000040	P-DMA#0 Channel #20
117	DW0_CH_STRUCT21_CH	0x40288540	0x00000040	P-DMA#0 Channel #21
118	DW0_CH_STRUCT22_CH	0x40288580	0x00000040	P-DMA#0 Channel #22
119	DW0_CH_STRUCT23_CH	0x402885C0	0x00000040	P-DMA#0 Channel #23
120	DW0_CH_STRUCT24_CH	0x40288600	0x00000040	P-DMA#0 Channel #24
121	DW0_CH_STRUCT25_CH	0x40288640	0x00000040	P-DMA#0 Channel #25
122	DW0_CH_STRUCT26_CH	0x40288680	0x00000040	P-DMA#0 Channel #26
123	DW0_CH_STRUCT27_CH	0x402886C0	0x00000040	P-DMA#0 Channel #27
124	DW0_CH_STRUCT28_CH	0x40288700	0x00000040	P-DMA#0 Channel #28
125	DW0_CH_STRUCT29_CH	0x40288740	0x00000040	P-DMA#0 Channel #29
126	DW0_CH_STRUCT30_CH	0x40288780	0x00000040	P-DMA#0 Channel #30
127	DW0_CH_STRUCT31_CH	0x402887C0	0x00000040	P-DMA#0 Channel #31

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
128	DW0_CH_STRUCT32_CH	0x40288800	0x00000040	P-DMA#0 Channel #32
129	DW0_CH_STRUCT33_CH	0x40288840	0x00000040	P-DMA#0 Channel #33
130	DW0_CH_STRUCT34_CH	0x40288880	0x00000040	P-DMA#0 Channel #34
131	DW0_CH_STRUCT35_CH	0x402888C0	0x00000040	P-DMA#0 Channel #35
132	DW0_CH_STRUCT36_CH	0x40288900	0x00000040	P-DMA#0 Channel #36
133	DW0_CH_STRUCT37_CH	0x40288940	0x00000040	P-DMA#0 Channel #37
134	DW0_CH_STRUCT38_CH	0x40288980	0x00000040	P-DMA#0 Channel #38
135	DW0_CH_STRUCT39_CH	0x402889C0	0x00000040	P-DMA#0 Channel #39
136	DW0_CH_STRUCT40_CH	0x40288A00	0x00000040	P-DMA#0 Channel #40
137	DW0_CH_STRUCT41_CH	0x40288A40	0x00000040	P-DMA#0 Channel #41
138	DW0_CH_STRUCT42_CH	0x40288A80	0x00000040	P-DMA#0 Channel #42
139	DW0_CH_STRUCT43_CH	0x40288AC0	0x00000040	P-DMA#0 Channel #43
140	DW0_CH_STRUCT44_CH	0x40288B00	0x00000040	P-DMA#0 Channel #44
141	DW0_CH_STRUCT45_CH	0x40288B40	0x00000040	P-DMA#0 Channel #45
142	DW0_CH_STRUCT46_CH	0x40288B80	0x00000040	P-DMA#0 Channel #46
143	DW0_CH_STRUCT47_CH	0x40288BC0	0x00000040	P-DMA#0 Channel #47
144	DW0_CH_STRUCT48_CH	0x40288C00	0x00000040	P-DMA#0 Channel #48
145	DW0_CH_STRUCT49_CH	0x40288C40	0x00000040	P-DMA#0 Channel #49
146	DW0_CH_STRUCT50_CH	0x40288C80	0x00000040	P-DMA#0 Channel #50
147	DW0_CH_STRUCT51_CH	0x40288CC0	0x00000040	P-DMA#0 Channel #51
148	DW0_CH_STRUCT52_CH	0x40288D00	0x00000040	P-DMA#0 Channel #52
149	DW0_CH_STRUCT53_CH	0x40288D40	0x00000040	P-DMA#0 Channel #53
150	DW0_CH_STRUCT54_CH	0x40288D80	0x00000040	P-DMA#0 Channel #54
151	DW0_CH_STRUCT55_CH	0x40288DC0	0x00000040	P-DMA#0 Channel #55
152	DW0_CH_STRUCT56_CH	0x40288E00	0x00000040	P-DMA#0 Channel #56
153	DW0_CH_STRUCT57_CH	0x40288E40	0x00000040	P-DMA#0 Channel #57
154	DW0_CH_STRUCT58_CH	0x40288E80	0x00000040	P-DMA#0 Channel #58
155	DW0_CH_STRUCT59_CH	0x40288EC0	0x00000040	P-DMA#0 Channel #59
156	DW0_CH_STRUCT60_CH	0x40288F00	0x00000040	P-DMA#0 Channel #60
157	DW0_CH_STRUCT61_CH	0x40288F40	0x00000040	P-DMA#0 Channel #61
158	DW0_CH_STRUCT62_CH	0x40288F80	0x00000040	P-DMA#0 Channel #62
159	DW0_CH_STRUCT63_CH	0x40288FC0	0x00000040	P-DMA#0 Channel #63
160	DW0_CH_STRUCT64_CH	0x40289000	0x00000040	P-DMA#0 Channel #64
161	DW0_CH_STRUCT65_CH	0x40289040	0x00000040	P-DMA#0 Channel #65
162	DW0_CH_STRUCT66_CH	0x40289080	0x00000040	P-DMA#0 Channel #66
163	DW0_CH_STRUCT67_CH	0x402890C0	0x00000040	P-DMA#0 Channel #67
164	DW0_CH_STRUCT68_CH	0x40289100	0x00000040	P-DMA#0 Channel #68
165	DW0_CH_STRUCT69_CH	0x40289140	0x00000040	P-DMA#0 Channel #69
166	DW0_CH_STRUCT70_CH	0x40289180	0x00000040	P-DMA#0 Channel #70
167	DW0_CH_STRUCT71_CH	0x402891C0	0x00000040	P-DMA#0 Channel #71
168	DW0_CH_STRUCT72_CH	0x40289200	0x00000040	P-DMA#0 Channel #72
169	DW0_CH_STRUCT73_CH	0x40289240	0x00000040	P-DMA#0 Channel #73
170	DW0_CH_STRUCT74_CH	0x40289280	0x00000040	P-DMA#0 Channel #74
171	DW0_CH_STRUCT75_CH	0x402892C0	0x00000040	P-DMA#0 Channel #75
172	DW1_CH_STRUCT0_CH	0x40298000	0x00000040	P-DMA#1 Channel #0

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
173	DW1_CH_STRUCT1_CH	0x40298040	0x00000040	P-DMA#1 Channel #1
174	DW1_CH_STRUCT2_CH	0x40298080	0x00000040	P-DMA#1 Channel #2
175	DW1_CH_STRUCT3_CH	0x402980C0	0x00000040	P-DMA#1 Channel #3
176	DW1_CH_STRUCT4_CH	0x40298100	0x00000040	P-DMA#1 Channel #4
177	DW1_CH_STRUCT5_CH	0x40298140	0x00000040	P-DMA#1 Channel #5
178	DW1_CH_STRUCT6_CH	0x40298180	0x00000040	P-DMA#1 Channel #6
179	DW1_CH_STRUCT7_CH	0x402981C0	0x00000040	P-DMA#1 Channel #7
180	DW1_CH_STRUCT8_CH	0x40298200	0x00000040	P-DMA#1 Channel #8
181	DW1_CH_STRUCT9_CH	0x40298240	0x00000040	P-DMA#1 Channel #9
182	DW1_CH_STRUCT10_CH	0x40298280	0x00000040	P-DMA#1 Channel #10
183	DW1_CH_STRUCT11_CH	0x402982C0	0x00000040	P-DMA#1 Channel #11
184	DW1_CH_STRUCT12_CH	0x40298300	0x00000040	P-DMA#1 Channel #12
185	DW1_CH_STRUCT13_CH	0x40298340	0x00000040	P-DMA#1 Channel #13
186	DW1_CH_STRUCT14_CH	0x40298380	0x00000040	P-DMA#1 Channel #14
187	DW1_CH_STRUCT15_CH	0x402983C0	0x00000040	P-DMA#1 Channel #15
188	DW1_CH_STRUCT16_CH	0x40298400	0x00000040	P-DMA#1 Channel #16
189	DW1_CH_STRUCT17_CH	0x40298440	0x00000040	P-DMA#1 Channel #17
190	DW1_CH_STRUCT18_CH	0x40298480	0x00000040	P-DMA#1 Channel #18
191	DW1_CH_STRUCT19_CH	0x402984C0	0x00000040	P-DMA#1 Channel #19
192	DW1_CH_STRUCT20_CH	0x40298500	0x00000040	P-DMA#1 Channel #20
193	DW1_CH_STRUCT21_CH	0x40298540	0x00000040	P-DMA#1 Channel #21
194	DW1_CH_STRUCT22_CH	0x40298580	0x00000040	P-DMA#1 Channel #22
195	DW1_CH_STRUCT23_CH	0x402985C0	0x00000040	P-DMA#1 Channel #23
196	DW1_CH_STRUCT24_CH	0x40298600	0x00000040	P-DMA#1 Channel #24
197	DW1_CH_STRUCT25_CH	0x40298640	0x00000040	P-DMA#1 Channel #25
198	DW1_CH_STRUCT26_CH	0x40298680	0x00000040	P-DMA#1 Channel #26
199	DW1_CH_STRUCT27_CH	0x402986C0	0x00000040	P-DMA#1 Channel #27
200	DW1_CH_STRUCT28_CH	0x40298700	0x00000040	P-DMA#1 Channel #28
201	DW1_CH_STRUCT29_CH	0x40298740	0x00000040	P-DMA#1 Channel #29
202	DW1_CH_STRUCT30_CH	0x40298780	0x00000040	P-DMA#1 Channel #30
203	DW1_CH_STRUCT31_CH	0x402987C0	0x00000040	P-DMA#1 Channel #31
204	DW1_CH_STRUCT32_CH	0x40298800	0x00000040	P-DMA#1 Channel #32
205	DW1_CH_STRUCT33_CH	0x40298840	0x00000040	P-DMA#1 Channel #33
206	DW1_CH_STRUCT34_CH	0x40298880	0x00000040	P-DMA#1 Channel #34
207	DW1_CH_STRUCT35_CH	0x402988C0	0x00000040	P-DMA#1 Channel #35
208	DW1_CH_STRUCT36_CH	0x40298900	0x00000040	P-DMA#1 Channel #36
209	DW1_CH_STRUCT37_CH	0x40298940	0x00000040	P-DMA#1 Channel #37
210	DW1_CH_STRUCT38_CH	0x40298980	0x00000040	P-DMA#1 Channel #38
211	DW1_CH_STRUCT39_CH	0x402989C0	0x00000040	P-DMA#1 Channel #39
212	DW1_CH_STRUCT40_CH	0x40298A00	0x00000040	P-DMA#1 Channel #40
213	DW1_CH_STRUCT41_CH	0x40298A40	0x00000040	P-DMA#1 Channel #41
214	DW1_CH_STRUCT42_CH	0x40298A80	0x00000040	P-DMA#1 Channel #42
215	DW1_CH_STRUCT43_CH	0x40298AC0	0x00000040	P-DMA#1 Channel #43
216	DW1_CH_STRUCT44_CH	0x40298B00	0x00000040	P-DMA#1 Channel #44
217	DW1_CH_STRUCT45_CH	0x40298B40	0x00000040	P-DMA#1 Channel #45

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
218	DW1_CH_STRUCT46_CH	0x40298B80	0x00000040	P-DMA#1 Channel #46
219	DW1_CH_STRUCT47_CH	0x40298BC0	0x00000040	P-DMA#1 Channel #47
220	DW1_CH_STRUCT48_CH	0x40298C00	0x00000040	P-DMA#1 Channel #48
221	DW1_CH_STRUCT49_CH	0x40298C40	0x00000040	P-DMA#1 Channel #49
222	DW1_CH_STRUCT50_CH	0x40298C80	0x00000040	P-DMA#1 Channel #50
223	DW1_CH_STRUCT51_CH	0x40298CC0	0x00000040	P-DMA#1 Channel #51
224	DW1_CH_STRUCT52_CH	0x40298D00	0x00000040	P-DMA#1 Channel #52
225	DW1_CH_STRUCT53_CH	0x40298D40	0x00000040	P-DMA#1 Channel #53
226	DW1_CH_STRUCT54_CH	0x40298D80	0x00000040	P-DMA#1 Channel #54
227	DW1_CH_STRUCT55_CH	0x40298DC0	0x00000040	P-DMA#1 Channel #55
228	DW1_CH_STRUCT56_CH	0x40298E00	0x00000040	P-DMA#1 Channel #56
229	DW1_CH_STRUCT57_CH	0x40298E40	0x00000040	P-DMA#1 Channel #57
230	DW1_CH_STRUCT58_CH	0x40298E80	0x00000040	P-DMA#1 Channel #58
231	DW1_CH_STRUCT59_CH	0x40298EC0	0x00000040	P-DMA#1 Channel #59
232	DW1_CH_STRUCT60_CH	0x40298F00	0x00000040	P-DMA#1 Channel #60
233	DW1_CH_STRUCT61_CH	0x40298F40	0x00000040	P-DMA#1 Channel #61
234	DW1_CH_STRUCT62_CH	0x40298F80	0x00000040	P-DMA#1 Channel #62
235	DW1_CH_STRUCT63_CH	0x40298FC0	0x00000040	P-DMA#1 Channel #63
236	DW1_CH_STRUCT64_CH	0x40299000	0x00000040	P-DMA#1 Channel #64
237	DW1_CH_STRUCT65_CH	0x40299040	0x00000040	P-DMA#1 Channel #65
238	DW1_CH_STRUCT66_CH	0x40299080	0x00000040	P-DMA#1 Channel #66
239	DW1_CH_STRUCT67_CH	0x402990C0	0x00000040	P-DMA#1 Channel #67
240	DW1_CH_STRUCT68_CH	0x40299100	0x00000040	P-DMA#1 Channel #68
241	DW1_CH_STRUCT69_CH	0x40299140	0x00000040	P-DMA#1 Channel #69
242	DW1_CH_STRUCT70_CH	0x40299180	0x00000040	P-DMA#1 Channel #70
243	DW1_CH_STRUCT71_CH	0x402991C0	0x00000040	P-DMA#1 Channel #71
244	DW1_CH_STRUCT72_CH	0x40299200	0x00000040	P-DMA#1 Channel #72
245	DW1_CH_STRUCT73_CH	0x40299240	0x00000040	P-DMA#1 Channel #73
246	DW1_CH_STRUCT74_CH	0x40299280	0x00000040	P-DMA#1 Channel #74
247	DW1_CH_STRUCT75_CH	0x402992C0	0x00000040	P-DMA#1 Channel #75
248	DW1_CH_STRUCT76_CH	0x40299300	0x00000040	P-DMA#1 Channel #76
249	DW1_CH_STRUCT77_CH	0x40299340	0x00000040	P-DMA#1 Channel #77
250	DW1_CH_STRUCT78_CH	0x40299380	0x00000040	P-DMA#1 Channel #78
251	DW1_CH_STRUCT79_CH	0x402993C0	0x00000040	P-DMA#1 Channel #79
252	DW1_CH_STRUCT80_CH	0x40299400	0x00000040	P-DMA#1 Channel #80
253	DW1_CH_STRUCT81_CH	0x40299440	0x00000040	P-DMA#1 Channel #81
254	DW1_CH_STRUCT82_CH	0x40299480	0x00000040	P-DMA#1 Channel #82
255	DW1_CH_STRUCT83_CH	0x402994C0	0x00000040	P-DMA#1 Channel #83
256	DMAC_TOP	0x402A0000	0x00000010	M-DMA#0 main
257	DMAC_CH0_CH	0x402A1000	0x00000100	M-DMA#0 Channel #0
258	DMAC_CH1_CH	0x402A1100	0x00000100	M-DMA#0 Channel #1
259	DMAC_CH2_CH	0x402A1200	0x00000100	M-DMA#0 Channel #2
260	DMAC_CH3_CH	0x402A1300	0x00000100	M-DMA#0 Channel #3
261	DMAC_CH4_CH	0x402A1400	0x00000100	M-DMA#0 Channel #4
262	DMAC_CH5_CH	0x402A1500	0x00000100	M-DMA#0 Channel #5

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
263	DMAC_CH6_CH	0x402A1600	0x00000100	M-DMA#0 Channel #6
264	DMAC_CH7_CH	0x402A1700	0x00000100	M-DMA#0 Channel #7
265	AXI_DMAC_TOP	0x402B0000	0x00000008	AXI M-DMA#1 main
266	AXI_DMAC_SEC	0x402B0008	0x00000004	AXI M-DMA#1 active secure channels
267	AXI_DMAC_NONSEC	0x402B000C	0x00000004	AXI M-DMA#1 active non-secure channels
268	AXI_DMAC_CH0_CH	0x402B1000	0x00000100	AXI M-DMA#1 Channel #0
269	AXI_DMAC_CH1_CH	0x402B1100	0x00000100	AXI M-DMA#1 Channel #1
270	AXI_DMAC_CH2_CH	0x402B1200	0x00000100	AXI M-DMA#1 Channel #2
271	AXI_DMAC_CH3_CH	0x402B1300	0x00000100	AXI M-DMA#1 Channel #3
272	EFUSE_CTL	0x402C0000	0x00000200	EFUSE control
273	EFUSE_DATA	0x402C0800	0x00000200	EFUSE data
274	DFT	0x402F0000	0x00001000	Built-in self test
275	HSIOM_PRT0_PRT	0x40300000	0x00000008	HSIOm Port #0
276	HSIOM_PRT1_PRT	0x40300010	0x00000008	HSIOm Port #1
277	HSIOM_PRT2_PRT	0x40300020	0x00000008	HSIOm Port #2
278	HSIOM_PRT3_PRT	0x40300030	0x00000008	HSIOm Port #3
279	HSIOM_PRT4_PRT	0x40300040	0x00000008	HSIOm Port #4
280	HSIOM_PRT5_PRT	0x40300050	0x00000008	HSIOm Port #5
281	HSIOM_PRT6_PRT	0x40300060	0x00000008	HSIOm Port #6
282	HSIOM_PRT7_PRT	0x40300070	0x00000008	HSIOm Port #7
283	HSIOM_PRT8_PRT	0x40300080	0x00000008	HSIOm Port #8
284	HSIOM_PRT9_PRT	0x40300090	0x00000008	HSIOm Port #9
286	HSIOM_PRT11_PRT	0x403000B0	0x00000008	HSIOm Port #11
287	HSIOM_PRT12_PRT	0x403000C0	0x00000008	HSIOm Port #12
288	HSIOM_PRT13_PRT	0x403000D0	0x00000008	HSIOm Port #13
289	HSIOM_PRT14_PRT	0x403000E0	0x00000008	HSIOm Port #14
290	HSIOM_PRT15_PRT	0x403000F0	0x00000008	HSIOm Port #15
291	HSIOM_PRT16_PRT	0x40300100	0x00000008	HSIOm Port #16
292	HSIOM_PRT17_PRT	0x40300110	0x00000008	HSIOm Port #17
293	HSIOM_PRT18_PRT	0x40300120	0x00000008	HSIOm Port #18
294	HSIOM_PRT19_PRT	0x40300130	0x00000008	HSIOm Port #19
295	HSIOM_PRT20_PRT	0x40300140	0x00000008	HSIOm Port #20
296	HSIOM_PRT21_PRT	0x40300150	0x00000008	HSIOm Port #21
298	HSIOM_PRT23_PRT	0x40300170	0x00000008	HSIOm Port #23
299	HSIOM_PRT24_PRT	0x40300180	0x00000008	HSIOm Port #24
300	HSIOM_PRT25_PRT	0x40300190	0x00000008	HSIOm Port #25
301	HSIOM_PRT26_PRT	0x403001A0	0x00000008	HSIOm Port #26
302	HSIOM_PRT27_PRT	0x403001B0	0x00000008	HSIOm Port #27
303	HSIOM_PRT28_PRT	0x403001C0	0x00000008	HSIOm Port #28
304	HSIOM_PRT29_PRT	0x403001D0	0x00000008	HSIOm Port #29
305	HSIOM_PRT30_PRT	0x403001E0	0x00000008	HSIOm Port #30
306	HSIOM_AMUX	0x40302000	0x00000020	HSIOm Analog multiplexer
307	HSIOM_MON	0x40302200	0x00000010	HSIOm monitor
308	GPIO_PRT0_PRT	0x40310000	0x00000040	GPIO_ENH Port #0
309	GPIO_PRT1_PRT	0x40310080	0x00000040	GPIO_STD Port #1

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
310	GPIO_PRT2_PRT	0x40310100	0x00000040	GPIO_STD Port #2
311	GPIO_PRT3_PRT	0x40310180	0x00000040	GPIO_STD Port #3
312	GPIO_PRT4_PRT	0x40310200	0x00000040	GPIO_STD Port #4
313	GPIO_PRT5_PRT	0x40310280	0x00000040	GPIO_STD Port #5
314	GPIO_PRT6_PRT	0x40310300	0x00000040	GPIO_STD Port #6
315	GPIO_PRT7_PRT	0x40310380	0x00000040	GPIO_STD Port #7
316	GPIO_PRT8_PRT	0x40310400	0x00000040	GPIO_STD Port #8
317	GPIO_PRT9_PRT	0x40310480	0x00000040	GPIO_SMC Port #9
319	GPIO_PRT11_PRT	0x40310580	0x00000040	GPIO_SMC Port #11
320	GPIO_PRT12_PRT	0x40310600	0x00000040	GPIO_SMC Port #12
321	GPIO_PRT13_PRT	0x40310680	0x00000040	HSIO_STD Port #13
322	GPIO_PRT14_PRT	0x40310700	0x00000040	HSIO_STD Port #14
323	GPIO_PRT15_PRT	0x40310780	0x00000040	HSIO_STD Port #15
324	GPIO_PRT16_PRT	0x40310800	0x00000040	HSIO_STD Port #16
325	GPIO_PRT17_PRT	0x40310880	0x00000040	HSIO_STD Port #17
326	GPIO_PRT18_PRT	0x40310900	0x00000040	HSIO_STD Port #18
327	GPIO_PRT19_PRT	0x40310980	0x00000040	HSIO_STD Port #19
328	GPIO_PRT20_PRT	0x40310A00	0x00000040	HSIO_STD Port #20
329	GPIO_PRT21_PRT	0x40310A80	0x00000040	HSIO_STD Port #21
331	GPIO_PRT23_PRT	0x40310B80	0x00000040	HSIO_ENH Port #23
332	GPIO_PRT24_PRT	0x40310C00	0x00000040	HSIO_ENH_PDIFF Port #24
333	GPIO_PRT25_PRT	0x40310C80	0x00000040	HSIO_ENH Port #25
334	GPIO_PRT26_PRT	0x40310D00	0x00000040	HSIO_ENH Port #26
335	GPIO_PRT27_PRT	0x40310D80	0x00000040	HSIO_ENH_PDIFF Port #27
336	GPIO_PRT28_PRT	0x40310E00	0x00000040	HSIO_ENH Port #28
337	GPIO_PRT29_PRT	0x40310E80	0x00000040	GPIO_ENH Port #29
338	GPIO_PRT30_PRT	0x40310F00	0x00000040	GPIO_ENH Port #30
339	GPIO_PRT0_CFG	0x40310040	0x00000020	GPIO_ENH Port #0 Configuration
340	GPIO_PRT1_CFG	0x403100C0	0x00000020	GPIO_STD Port #1 Configuration
341	GPIO_PRT2_CFG	0x40310140	0x00000020	GPIO_STD Port #2 Configuration
342	GPIO_PRT3_CFG	0x403101C0	0x00000020	GPIO_STD Port #3 Configuration
343	GPIO_PRT4_CFG	0x40310240	0x00000020	GPIO_STD Port #4 Configuration
344	GPIO_PRT5_CFG	0x403102C0	0x00000020	GPIO_STD Port #5 Configuration
345	GPIO_PRT6_CFG	0x40310340	0x00000020	GPIO_STD Port #6 Configuration
346	GPIO_PRT7_CFG	0x403103C0	0x00000020	GPIO_STD Port #7 Configuration
347	GPIO_PRT8_CFG	0x40310440	0x00000020	GPIO_STD Port #8 Configuration
348	GPIO_PRT9_CFG	0x403104C0	0x00000020	GPIO_SMC Port #9 Configuration
350	GPIO_PRT11_CFG	0x403105C0	0x00000020	GPIO_SMC Port #11 Configuration
351	GPIO_PRT12_CFG	0x40310640	0x00000020	GPIO_SMC Port #12 Configuration
352	GPIO_PRT13_CFG	0x403106C0	0x00000020	HSIO_STD Port #13 Configuration
353	GPIO_PRT14_CFG	0x40310740	0x00000020	HSIO_STD Port #14 Configuration
354	GPIO_PRT15_CFG	0x403107C0	0x00000040	HSIO_STD Port #15 Configuration
355	GPIO_PRT16_CFG	0x40310840	0x00000040	HSIO_STD Port #16 Configuration
356	GPIO_PRT17_CFG	0x403108C0	0x00000040	HSIO_STD Port #17 Configuration
357	GPIO_PRT18_CFG	0x40310940	0x00000040	HSIO_STD Port #18 Configuration

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
358	GPIO_PRT19_CFG	0x403109C0	0x00000040	HSIO_STD Port #19 Configuration
359	GPIO_PRT20_CFG	0x40310A40	0x00000040	HSIO_STD Port #20 Configuration
360	GPIO_PRT21_CFG	0x40310AC0	0x00000040	HSIO_STD Port #21 Configuration
362	GPIO_PRT23_CFG	0x40310BC0	0x00000040	HSIO_ENH Port #23 Configuration
363	GPIO_PRT24_CFG	0x40310C40	0x00000040	HSIO_ENH_PDIFF Port #24 Configuration
364	GPIO_PRT25_CFG	0x40310CC0	0x00000040	HSIO_ENH Port #25 Configuration
365	GPIO_PRT26_CFG	0x40310D40	0x00000040	HSIO_ENH Port #26 Configuration
366	GPIO_PRT27_CFG	0x40310DC0	0x00000040	HSIO_ENH_PDIFF Port #27 Configuration
367	GPIO_PRT28_CFG	0x40310E40	0x00000040	HSIO_ENH Port #28 Configuration
368	GPIO_PRT29_CFG	0x40310EC0	0x00000020	GPIO_ENH Port #29 Configuration
369	GPIO_PRT30_CFG	0x40310F40	0x00000020	GPIO_ENH Port #30 Configuration
370	GPIO_GPIO	0x40314000	0x00000040	GPIO main
371	GPIO_TEST	0x40315000	0x00000008	GPIO test
372	SMARTIO_PRT7_PRT	0x40320700	0x00000100	SMART I/O #7
373	TCPWM0_GRP0_CNT0_CNT	0x40380000	0x00000080	TCPWM#0 Group #0, Counter #0
374	TCPWM0_GRP0_CNT1_CNT	0x40380080	0x00000080	TCPWM#0 Group #0, Counter #1
375	TCPWM0_GRP0_CNT2_CNT	0x40380100	0x00000080	TCPWM#0 Group #0, Counter #2
376	TCPWM0_GRP0_CNT3_CNT	0x40380180	0x00000080	TCPWM#0 Group #0, Counter #3
377	TCPWM0_GRP0_CNT4_CNT	0x40380200	0x00000080	TCPWM#0 Group #0, Counter #4
378	TCPWM0_GRP0_CNT5_CNT	0x40380280	0x00000080	TCPWM#0 Group #0, Counter #5
379	TCPWM0_GRP0_CNT6_CNT	0x40380300	0x00000080	TCPWM#0 Group #0, Counter #6
380	TCPWM0_GRP0_CNT7_CNT	0x40380380	0x00000080	TCPWM#0 Group #0, Counter #7
381	TCPWM0_GRP0_CNT8_CNT	0x40380400	0x00000080	TCPWM#0 Group #0, Counter #8
382	TCPWM0_GRP0_CNT9_CNT	0x40380480	0x00000080	TCPWM#0 Group #0, Counter #9
383	TCPWM0_GRP0_CNT10_CNT	0x40380500	0x00000080	TCPWM#0 Group #0, Counter #10
384	TCPWM0_GRP0_CNT11_CNT	0x40380580	0x00000080	TCPWM#0 Group #0, Counter #11
385	TCPWM0_GRP0_CNT12_CNT	0x40380600	0x00000080	TCPWM#0 Group #0, Counter #12
386	TCPWM0_GRP0_CNT13_CNT	0x40380680	0x00000080	TCPWM#0 Group #0, Counter #13
387	TCPWM0_GRP0_CNT14_CNT	0x40380700	0x00000080	TCPWM#0 Group #0, Counter #14
388	TCPWM0_GRP0_CNT15_CNT	0x40380780	0x00000080	TCPWM#0 Group #0, Counter #15
389	TCPWM0_GRP0_CNT16_CNT	0x40380800	0x00000080	TCPWM#0 Group #0, Counter #16
390	TCPWM0_GRP0_CNT17_CNT	0x40380880	0x00000080	TCPWM#0 Group #0, Counter #17
391	TCPWM0_GRP0_CNT18_CNT	0x40380900	0x00000080	TCPWM#0 Group #0, Counter #18
392	TCPWM0_GRP0_CNT19_CNT	0x40380980	0x00000080	TCPWM#0 Group #0, Counter #19
393	TCPWM0_GRP0_CNT20_CNT	0x40380A00	0x00000080	TCPWM#0 Group #0, Counter #20
394	TCPWM0_GRP0_CNT21_CNT	0x40380A80	0x00000080	TCPWM#0 Group #0, Counter #21
395	TCPWM0_GRP0_CNT22_CNT	0x40380B00	0x00000080	TCPWM#0 Group #0, Counter #22
396	TCPWM0_GRP0_CNT23_CNT	0x40380B80	0x00000080	TCPWM#0 Group #0, Counter #23
397	TCPWM0_GRP0_CNT24_CNT	0x40380C00	0x00000080	TCPWM#0 Group #0, Counter #24
398	TCPWM0_GRP0_CNT25_CNT	0x40380C80	0x00000080	TCPWM#0 Group #0, Counter #25
399	TCPWM0_GRP0_CNT26_CNT	0x40380D00	0x00000080	TCPWM#0 Group #0, Counter #26
400	TCPWM0_GRP0_CNT27_CNT	0x40380D80	0x00000080	TCPWM#0 Group #0, Counter #27
401	TCPWM0_GRP0_CNT28_CNT	0x40380E00	0x00000080	TCPWM#0 Group #0, Counter #28
402	TCPWM0_GRP0_CNT29_CNT	0x40380E80	0x00000080	TCPWM#0 Group #0, Counter #29
403	TCPWM0_GRP0_CNT30_CNT	0x40380F00	0x00000080	TCPWM#0 Group #0, Counter #30

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
404	TCPWM0_GRP0_CNT31_CNT	0x40380F80	0x00000080	TCPWM#0 Group #0, Counter #31
405	TCPWM0_GRP0_CNT32_CNT	0x40381000	0x00000080	TCPWM#0 Group #0, Counter #32
406	TCPWM0_GRP0_CNT33_CNT	0x40381080	0x00000080	TCPWM#0 Group #0, Counter #33
407	TCPWM0_GRP0_CNT34_CNT	0x40381100	0x00000080	TCPWM#0 Group #0, Counter #34
408	TCPWM0_GRP0_CNT35_CNT	0x40381180	0x00000080	TCPWM#0 Group #0, Counter #35
409	TCPWM0_GRP0_CNT36_CNT	0x40381200	0x00000080	TCPWM#0 Group #0, Counter #36
410	TCPWM0_GRP0_CNT37_CNT	0x40381280	0x00000080	TCPWM#0 Group #0, Counter #37
411	TCPWM0_GRP1_CNT0_CNT	0x40388000	0x00000080	TCPWM#0 Group #1, Counter #0
412	TCPWM0_GRP1_CNT1_CNT	0x40388080	0x00000080	TCPWM#0 Group #1, Counter #1
413	TCPWM0_GRP1_CNT2_CNT	0x40388100	0x00000080	TCPWM#0 Group #1, Counter #2
414	TCPWM0_GRP1_CNT3_CNT	0x40388180	0x00000080	TCPWM#0 Group #1, Counter #3
415	TCPWM0_GRP1_CNT4_CNT	0x40388200	0x00000080	TCPWM#0 Group #1, Counter #4
416	TCPWM0_GRP1_CNT5_CNT	0x40388280	0x00000080	TCPWM#0 Group #1, Counter #5
417	TCPWM0_GRP1_CNT6_CNT	0x40388300	0x00000080	TCPWM#0 Group #1, Counter #6
418	TCPWM0_GRP1_CNT7_CNT	0x40388380	0x00000080	TCPWM#0 Group #1, Counter #7
419	TCPWM0_GRP1_CNT8_CNT	0x40388400	0x00000080	TCPWM#0 Group #1, Counter #8
420	TCPWM0_GRP1_CNT9_CNT	0x40388480	0x00000080	TCPWM#0 Group #1, Counter #9
421	TCPWM0_GRP1_CNT10_CNT	0x40388500	0x00000080	TCPWM#0 Group #1, Counter #10
422	TCPWM0_GRP1_CNT11_CNT	0x40388580	0x00000080	TCPWM#0 Group #1, Counter #11
423	TCPWM0_GRP2_CNT0_CNT	0x40390000	0x00000080	TCPWM#0 Group #2, Counter #0
424	TCPWM0_GRP2_CNT1_CNT	0x40390080	0x00000080	TCPWM#0 Group #2, Counter #1
425	TCPWM0_GRP2_CNT2_CNT	0x40390100	0x00000080	TCPWM#0 Group #2, Counter #2
426	TCPWM0_GRP2_CNT3_CNT	0x40390180	0x00000080	TCPWM#0 Group #2, Counter #3
427	TCPWM0_GRP2_CNT4_CNT	0x40390200	0x00000080	TCPWM#0 Group #2, Counter #4
428	TCPWM0_GRP2_CNT5_CNT	0x40390280	0x00000080	TCPWM#0 Group #2, Counter #5
429	TCPWM0_GRP2_CNT6_CNT	0x40390300	0x00000080	TCPWM#0 Group #2, Counter #6
430	TCPWM0_GRP2_CNT7_CNT	0x40390380	0x00000080	TCPWM#0 Group #2, Counter #7
431	TCPWM0_GRP2_CNT8_CNT	0x40390400	0x00000080	TCPWM#0 Group #2, Counter #8
432	TCPWM0_GRP2_CNT9_CNT	0x40390480	0x00000080	TCPWM#0 Group #2, Counter #9
433	TCPWM0_GRP2_CNT10_CNT	0x40390500	0x00000080	TCPWM#0 Group #2, Counter #10
434	TCPWM0_GRP2_CNT11_CNT	0x40390580	0x00000080	TCPWM#0 Group #2, Counter #11
435	TCPWM0_GRP2_CNT12_CNT	0x40390600	0x00000080	TCPWM#0 Group #2, Counter #12
436	TCPWM0_GRP2_CNT13_CNT	0x40390680	0x00000080	TCPWM#0 Group #2, Counter #13
437	TCPWM0_GRP2_CNT14_CNT	0x40390700	0x00000080	TCPWM#0 Group #2, Counter #14
438	TCPWM0_GRP2_CNT15_CNT	0x40390780	0x00000080	TCPWM#0 Group #2, Counter #15
439	TCPWM0_GRP2_CNT16_CNT	0x40390800	0x00000080	TCPWM#0 Group #2, Counter #16
440	TCPWM0_GRP2_CNT17_CNT	0x40390880	0x00000080	TCPWM#0 Group #2, Counter #17
441	TCPWM0_GRP2_CNT18_CNT	0x40390900	0x00000080	TCPWM#0 Group #2, Counter #18
442	TCPWM0_GRP2_CNT19_CNT	0x40390980	0x00000080	TCPWM#0 Group #2, Counter #19
443	TCPWM0_GRP2_CNT20_CNT	0x40390A00	0x00000080	TCPWM#0 Group #2, Counter #20
444	TCPWM0_GRP2_CNT21_CNT	0x40390A80	0x00000080	TCPWM#0 Group #2, Counter #21
445	TCPWM0_GRP2_CNT22_CNT	0x40390B00	0x00000080	TCPWM#0 Group #2, Counter #22
446	TCPWM0_GRP2_CNT23_CNT	0x40390B80	0x00000080	TCPWM#0 Group #2, Counter #23
447	TCPWM0_GRP2_CNT24_CNT	0x40390C00	0x00000080	TCPWM#0 Group #2, Counter #24
448	TCPWM0_GRP2_CNT25_CNT	0x40390C80	0x00000080	TCPWM#0 Group #2, Counter #25

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
449	TCPWM0_GRP2_CNT26_CNT	0x40390D00	0x00000080	TCPWM#0 Group #2, Counter #26
450	TCPWM0_GRP2_CNT27_CNT	0x40390D80	0x00000080	TCPWM#0 Group #2, Counter #27
451	TCPWM0_GRP2_CNT28_CNT	0x40390E00	0x00000080	TCPWM#0 Group #2, Counter #28
452	TCPWM0_GRP2_CNT29_CNT	0x40390E80	0x00000080	TCPWM#0 Group #2, Counter #29
453	TCPWM0_GRP2_CNT30_CNT	0x40390F00	0x00000080	TCPWM#0 Group #2, Counter #30
454	TCPWM0_GRP2_CNT31_CNT	0x40390F80	0x00000080	TCPWM#0 Group #2, Counter #31
455	EVTGEN0	0x403F0000	0x00001000	Event generator #0
456	SMIF0_MAIN	0x40400000	0x00040000	Serial Memory Interface #0
457	ETH0	0x40480000	0x00010000	Ethernet#0
458	LIN0_MAIN	0x40500000	0x00000008	LIN#0, main
459	LIN0_CH0_CH	0x40508000	0x00000100	LIN#0, Channel #0
460	LIN0_CH1_CH	0x40508100	0x00000100	LIN#0, Channel #1
461	CXPI0_MAIN	0x40510000	0x00000008	CXPI#0, main
462	CXPI0_CH0_CH	0x40518000	0x00000100	CXPI#0, Channel #0
463	CXPI0_CH1_CH	0x40518100	0x00000100	CXPI#0, Channel #1
464	CANFD0_CH0_CH	0x40520000	0x00000200	CAN#0, Channel #0
465	CANFD0_CH1_CH	0x40520200	0x00000200	CAN#0, Channel #1
466	CANFD1_CH0_CH	0x40540000	0x00000200	CAN#1, Channel #0
467	CANFD1_CH1_CH	0x40540200	0x00000200	CAN#1, Channel #1
468	CANFD0_MAIN	0x40521000	0x00000100	CAN#0 main
469	CANFD1_MAIN	0x40541000	0x00000100	CAN#1 main
470	CANFD0_BUF	0x40530000	0x00010000	CAN#0 buffer
471	CANFD1_BUF	0x40550000	0x00010000	CAN#1 buffer
472	SCB0	0x40600000	0x00010000	Serial Communication Block#0
473	SCB1	0x40610000	0x00010000	Serial Communication Block#1
474	SCB2	0x40620000	0x00010000	Serial Communication Block#2
475	SCB3	0x40630000	0x00010000	Serial Communication Block#3
476	SCB4	0x40640000	0x00010000	Serial Communication Block#4
477	SCB5	0x40650000	0x00010000	Serial Communication Block#5
478	SCB6	0x40660000	0x00010000	Serial Communication Block#6
479	SCB7	0x40670000	0x00010000	Serial Communication Block#7
480	SCB8	0x40680000	0x00010000	Serial Communication Block#8
481	SCB9	0x40690000	0x00010000	Serial Communication Block#9
482	SCB10	0x406A0000	0x00010000	Serial Communication Block#10
483	SCB11	0x406B0000	0x00010000	Serial Communication Block#11
484	TDM0_TDM_STRUCT0_TDM_TX_STRUCT_TX	0x40818000	0x00000100	TDM#0 TX Structure #0
485	TDM0_TDM_STRUCT1_TDM_TX_STRUCT_TX	0x40818200	0x00000100	TDM#0 TX Structure #1
486	TDM0_TDM_STRUCT2_TDM_TX_STRUCT_TX	0x40818400	0x00000100	TDM#0 TX Structure #2
487	TDM0_TDM_STRUCT3_TDM_TX_STRUCT_TX	0x40818600	0x00000100	TDM#0 TX Structure #3
488	TDM0_TDM_STRUCT0_TDM_RX_STRUCT_RX	0x40818100	0x00000100	TDM#0 RX Structure #0
489	TDM0_TDM_STRUCT1_TDM_RX_STRUCT_RX	0x40818300	0x00000100	TDM#0 RX Structure #1
490	TDM0_TDM_STRUCT2_TDM_RX_STRUCT_RX	0x40818500	0x00000100	TDM#0 RX Structure #2
491	TDM0_TDM_STRUCT3_TDM_RX_STRUCT_RX	0x40818700	0x00000100	TDM#0 RX Structure #3
492	SG0_SG_STRUCT0_TX	0x40828000	0x00000100	SG#0 TX Structure #0
493	SG0_SG_STRUCT1_TX	0x40828100	0x00000100	SG#0 TX Structure #1

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
494	SG0_SG_STRUCT2_TX	0x40828200	0x00000100	SG#0 TX Structure #2
495	SG0_SG_STRUCT3_TX	0x40828300	0x00000100	SG#0 TX Structure #3
496	SG0_SG_STRUCT4_TX	0x40828400	0x00000100	SG#0 TX Structure #4
497	PWM0_MAIN	0x40830000	0x00000010	PWM#0 Main
498	PWM0_TX0_TX	0x40838000	0x00000100	PWM#0 TX0
499	PWM0_TX1_TX	0x40838100	0x00000100	PWM#0 TX1
500	DAC0_MAIN	0x40840000	0x00000100	DAC#0 Main
501	MIXER0_MIXER_SRC_STRUCT0_SRC	0x40888000	0x00000100	MIXER#0 Source Structure #0
502	MIXER0_MIXER_SRC_STRUCT1_SRC	0x40888100	0x00000100	MIXER#0 Source Structure #1
503	MIXER0_MIXER_SRC_STRUCT2_SRC	0x40888200	0x00000100	MIXER#0 Source Structure #2
504	MIXER0_MIXER_SRC_STRUCT3_SRC	0x40888300	0x00000100	MIXER#0 Source Structure #3
505	MIXER0_MIXER_SRC_STRUCT4_SRC	0x40888400	0x00000100	MIXER#0 Source Structure #4
506	MIXER1_MIXER_SRC_STRUCT0_SRC	0x40898000	0x00000100	MIXER#1 Source Structure #0
507	MIXER1_MIXER_SRC_STRUCT1_SRC	0x40898100	0x00000100	MIXER#1 Source Structure #1
508	MIXER1_MIXER_SRC_STRUCT2_SRC	0x40898200	0x00000100	MIXER#1 Source Structure #2
509	MIXER1_MIXER_SRC_STRUCT3_SRC	0x40898300	0x00000100	MIXER#1 Source Structure #3
510	MIXER1_MIXER_SRC_STRUCT4_SRC	0x40898400	0x00000100	MIXER#1 Source Structure #4
511	MIXER0_MIXER_DST_STRUCT_DST	0x4088C000	0x00000100	MIXER#0 Destination Structure
512	MIXER1_MIXER_DST_STRUCT_DST	0x4089C000	0x00000100	MIXER#1 Destination Structure
513	PASS0_SAR0_SAR	0x40900000	0x00000400	PASS SAR#0
514	PASS0_SAR1_SAR	0x40901000	0x00000008	PASS SAR#1
515	PASS0_SAR0_CH0_CH	0x40900800	0x00000040	SAR#0, Channel #0
516	PASS0_SAR0_CH1_CH	0x40900840	0x00000040	SAR#0, Channel #1
517	PASS0_SAR0_CH2_CH	0x40900880	0x00000040	SAR#0, Channel #2
518	PASS0_SAR0_CH3_CH	0x409008C0	0x00000040	SAR#0, Channel #3
519	PASS0_SAR0_CH4_CH	0x40900900	0x00000040	SAR#0, Channel #4
520	PASS0_SAR0_CH5_CH	0x40900940	0x00000040	SAR#0, Channel #5
521	PASS0_SAR0_CH6_CH	0x40900980	0x00000040	SAR#0, Channel #6
522	PASS0_SAR0_CH7_CH	0x409009C0	0x00000040	SAR#0, Channel #7
523	PASS0_SAR0_CH8_CH	0x40900A00	0x00000040	SAR#0, Channel #8
524	PASS0_SAR0_CH9_CH	0x40900A40	0x00000040	SAR#0, Channel #9
525	PASS0_SAR0_CH10_CH	0x40900A80	0x00000040	SAR#0, Channel #10
526	PASS0_SAR0_CH11_CH	0x40900AC0	0x00000040	SAR#0, Channel #11
527	PASS0_SAR0_CH12_CH	0x40900B00	0x00000040	SAR#0, Channel #12
528	PASS0_SAR0_CH13_CH	0x40900B40	0x00000040	SAR#0, Channel #13
529	PASS0_SAR0_CH14_CH	0x40900B80	0x00000040	SAR#0, Channel #14
530	PASS0_SAR0_CH15_CH	0x40900BC0	0x00000040	SAR#0, Channel #15
531	PASS0_SAR0_CH16_CH	0x40900C00	0x00000040	SAR#0, Channel #16
532	PASS0_SAR0_CH17_CH	0x40900C40	0x00000040	SAR#0, Channel #17
533	PASS0_SAR0_CH18_CH	0x40900C80	0x00000040	SAR#0, Channel #18
534	PASS0_SAR0_CH19_CH	0x40900CC0	0x00000040	SAR#0, Channel #19
535	PASS0_SAR0_CH20_CH	0x40900D00	0x00000040	SAR#0, Channel #20
536	PASS0_SAR0_CH21_CH	0x40900D40	0x00000040	SAR#0, Channel #21
537	PASS0_SAR0_CH22_CH	0x40900D80	0x00000040	SAR#0, Channel #22
538	PASS0_SAR0_CH23_CH	0x40900DC0	0x00000040	SAR#0, Channel #23

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
539	PASS0_SAR0_CH24_CH	0x40900E00	0x00000040	SAR#0, Channel #24
540	PASS0_SAR0_CH25_CH	0x40900E40	0x00000040	SAR#0, Channel #25
541	PASS0_SAR0_CH26_CH	0x40900E80	0x00000040	SAR#0, Channel #26
542	PASS0_SAR0_CH27_CH	0x40900EC0	0x00000040	SAR#0, Channel #27
543	PASS0_SAR0_CH28_CH	0x40900F00	0x00000040	SAR#0, Channel #28
544	PASS0_SAR0_CH29_CH	0x40900F40	0x00000040	SAR#0, Channel #29
545	PASS0_SAR0_CH30_CH	0x40900F80	0x00000040	SAR#0, Channel #30
546	PASS0_SAR0_CH31_CH	0x40900FC0	0x00000040	SAR#0, Channel #31
547	PASS0_TOP	0x409F0000	0x00001000	PASS0 SAR main
548	VIDEOSS0_VCFG_VIDEOSSCFG	0x40A00000	0x00000400	VIDEOSS#0 Configuration
549	VIDEOSS0_VCFG_VRAM	0x40A00400	0x00000400	VIDEOSS#0 VRAM Configuration
550	VIDEOSS0_GPU_GFX2D	0x40A40000	0x00040000	VIDEOSS#0 Graphics 2D Core
551	VIDEOSS0_VIDEOIOCFG_VIRQ_VIDEOIOCFG	0x40A80020	0x00000020	VIDEOSS#0 I/O Configuration
552	VIDEOSS0_CAPIFC0_FRAMEDUMP	0x40A80400	0x00000400	VIDEOSS#0 Frame Dump Unit
553	VIDEOSS0_CAPIFC0_CAPENG0	0x40A81000	0x00001000	VIDEOSS#0 Capture Engine#0
554	VIDEOSS0_DSPCFG_COMPENGCFG	0x40A90000	0x00002000	VIDEOSS#0 Composition Engine Configuration
555	VIDEOSS0_DSPSEC0_CONSTFRAME0	0x40A92000	0x00000400	VIDEOSS#0 Constant Frame#0 (Content)
556	VIDEOSS0_DSPSEC0_EXTDST0	0x40A92400	0x00000400	VIDEOSS#0 ExtDst#0 (Content)
557	VIDEOSS0_DSPPRIM0_CONSTFRAME4	0x40A92800	0x00000400	VIDEOSS#0 Constant Frame#4 (Content)
558	VIDEOSS0_DSPPRIM0_EXTDST4	0x40A92C00	0x00000400	VIDEOSS#0 ExtDst#4 (Safety)
559	VIDEOSS0_DSPSEC1_CONSTFRAME1	0x40A93000	0x00000400	VIDEOSS#0 Constant Frame#1 (Content)
560	VIDEOSS0_DSPSEC1_EXTDST1	0x40A93400	0x00000400	VIDEOSS#0 ExtDst#1 (Safety)
561	VIDEOSS0_DSPPRIM1_CONSTFRAME5	0x40A93800	0x00000400	VIDEOSS#0 Constant Frame#5 (Safety)
562	VIDEOSS0_DSPPRIM1_EXTDST5	0x40A93C00	0x00000400	VIDEOSS#0 ExtDst#5 (Safety)
563	VIDEOSS0_CAPIFC0_EXTSRC4	0x40A94000	0x00000400	VIDEOSS#0 ExtSrc#4 (Capture)
564	VIDEOSS0_CAPIFC0_STORE4	0x40A94400	0x00000400	VIDEOSS#0 Store#4 (Capture)
565	VIDEOSS0_DSPLAYER1_FETCHLAYER0	0x40A94800	0x00000400	VIDEOSS#0 Fetch Layer#0 (Display)
566	VIDEOSS0_DSPLAYER2_FETCHDECODE4	0x40A94C00	0x00000400	VIDEOSS#0 Fetch Decode#4 (Capture)
567	VIDEOSS0_DSPLAYER2_FETCHECO4	0x40A95000	0x00000400	VIDEOSS#0 Fetch Eco#4 (Capture)
568	VIDEOSS0_DSPLAYER3_FETCHWARP1	0x40A95800	0x00000400	VIDEOSS#0 Fetch Warp#1 (Display)
569	VIDEOSS0_DSPLAYER3_FETCHECO1	0x40A95C00	0x00000400	VIDEOSS#0 Fetch Eco#1 (Display)
570	VIDEOSS0_DSPLAYER4_FETCHLAYER1	0x40A96000	0x00000400	VIDEOSS#0 Fetch Layer#1 (Display)
571	VIDEOSS0_DSPLAYER5_FETCHDECODE0	0x40A96400	0x00000400	VIDEOSS#0 Fetch Decode#0 (Display)
572	VIDEOSS0_DSPVPB_GAMMACOR4	0x40A96800	0x00000400	Video Processing Block #0 GammaCor (Capture)
573	VIDEOSS0_DSPVPB_MATRIX4	0x40A96C00	0x00000400	Video Processing Block #0 Matrix (Capture)
574	VIDEOSS0_DSPVPB_GPSCALER4	0x40A97000	0x00000400	GPscaler #4 (Capture)
575	VIDEOSS0_DSPVPB_HISTOGRAM4	0x40A97400	0x00000400	Video Processing Block #0 Histogram (Capture)
576	VIDEOSS0_DSPBLEND1_LAYERBLEND1	0x40A97800	0x00000400	LayerBlend #1 (Display, Alpha Plane 1)
577	VIDEOSS0_DSPBLEND2_LAYERBLEND2	0x40A97C00	0x00000400	LayerBlend #2 (Display, Alpha Plane 2)
578	VIDEOSS0_DSPBLEND3_LAYERBLEND3	0x40A98000	0x00000400	LayerBlend #3 (Display, Alpha Plane 3)
579	VIDEOSS0_DSPBLEND4_LAYERBLEND4	0x40A98400	0x00000400	LayerBlend #4 (Display, Alpha Plane 4)
580	VIDEOSS0_DSPBLEND5_LAYERBLEND5	0x40A98800	0x00000400	LayerBlend #5 (Display, Alpha Plane 5)
581	VIDEOSS0_CAPIFC0_EXTSRC8	0x40A98C00	0x00000400	ExtSrc #8 (Display)
582	VIDEOSS0_DSPCFG0_DISENGCFG0	0x40AA0000	0x00000400	VIDEOSS#0 Display Engine#0 Configuration
583	VIDEOSS0_DSPMON0_SIG0	0x40AA1000	0x00000400	VIDEOSS#0 Display Engine#0 Signature Unit#0

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
584	VIDEOSS0_DSPCFG0_FRAMEGEN0	0x40AA2000	0x00000400	VIDEOSS#0 Display Engine#0 Frame Generator#0
585	VIDEOSS0_DSPCOL0_GAMMACOR0	0x40AA2400	0x00000400	VIDEOSS#0 Display Engine#0 Gamma Correction Unit#0
586	VIDEOSS0_DSPCOL0_DITHER0	0x40AA2800	0x00000400	VIDEOSS#0 Display Engine#0 Dither Unit#0
587	VIDEOSS0_DSPIFC0_TCON0	0x40AA3000	0x00000800	VIDEOSS#0 Display Engine#0 Timing Controller#0
588	VIDEOSS0_DSPCFG1_DISENGCFG1	0x40AA4000	0x00000400	VIDEOSS#0 Display Engine#1 Configuration
589	VIDEOSS0_DSPMON1_SIG1	0x40AA5000	0x00000400	VIDEOSS#0 Display Engine#1 Signature Unit#1
590	VIDEOSS0_DSPCFG1_FRAMEGEN1	0x40AA6000	0x00000400	VIDEOSS#0 Display Engine#1 Frame Generator
591	VIDEOSS0_DSPCOL1_GAMMACOR1	0x40AA6400	0x00000400	VIDEOSS#0 Display Engine#1 Gamma Correction Unit#1
592	VIDEOSS0_DSPCOL1_DITHER1	0x40AA6800	0x00000400	VIDEOSS#0 Display Engine#1 Dither Unit#1
593	VIDEOSS0_DSPIFC1_TCON1	0x40AA7000	0x00000800	VIDEOSS#0 Display Engine#1 Timing Controller#1
594	VIDEOSS0_DSPIFC0_FPDLINK0	0x40AC0000	0x00000400	VIDEOSS#0 Display interface0 FPD-Link#0
595	VIDEOSS0_DSPIFC1_FPDLINK1	0x40AC8000	0x00000400	VIDEOSS#0 Display interface0 FPD-Link#1
596	VIDEOSS0_MIPICSI0_MIPICSI_STRUCT_MIPICSI_WRAP_MAIN	0x40AD0000	0x00000100	VIDEOSS#0 MIPICSI#0 D-PHY wrapper configuration and status
597	VIDEOSS0_MIPICSI0_MIPICSI_STRUCT_MIPICSI_CORE_3PIP	0x40AD0200	0x00000080	VIDEOSS#0 MIPICSI#0 RX Core through APB interface
598	VIDEOSS0_VRPU_MAIN	0x40AF0000	0x00000080	VIDEOSS#0 VRPU Configuration
599	VIDEOSS0_GFX_MPU_RD0_MAIN	0x40AF4000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
600	VIDEOSS0_GFX_MPU_RD1_MAIN	0x40AF4400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
601	VIDEOSS0_GFX_MPU_RD2_MAIN	0x40AF4800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
602	VIDEOSS0_GFX_MPU_RD3_MAIN	0x40AF4C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
603	VIDEOSS0_GFX_MPU_RD4_MAIN	0x40AF5000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
604	VIDEOSS0_GFX_MPU_RD5_MAIN	0x40AF5400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
605	VIDEOSS0_GFX_MPU_RD6_MAIN	0x40AF5800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
606	VIDEOSS0_GFX_MPU_RD7_MAIN	0x40AF5C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
607	VIDEOSS0_GFX_MPU_RD8_MAIN	0x40AF6000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
608	VIDEOSS0_GFX_MPU_RD9_MAIN	0x40AF6400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
609	VIDEOSS0_GFX_MPU_RD10_MAIN	0x40AF6800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
610	VIDEOSS0_GFX_MPU_RD11_MAIN	0x40AF6C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
611	VIDEOSS0_GFX_MPU_RD12_MAIN	0x40AF7000	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
612	VIDEOSS0_GFX_MPU_RD13_MAIN	0x40AF7400	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
613	VIDEOSS0_GFX_MPU_RD14_MAIN	0x40AF7800	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
614	VIDEOSS0_GFX_MPU_RD15_MAIN	0x40AF7C00	0x00000004	VIDEOSS#0 MPU Configuration for Read Masters
615	VIDEOSS0_GFX_MPU_WR0_MAIN	0x40AF8000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
616	VIDEOSS0_GFX_MPU_WR1_MAIN	0x40AF8400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
617	VIDEOSS0_GFX_MPU_WR2_MAIN	0x40AF8800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
618	VIDEOSS0_GFX_MPU_WR3_MAIN	0x40AF8C00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
619	VIDEOSS0_GFX_MPU_WR4_MAIN	0x40AF9000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
620	VIDEOSS0_GFX_MPU_WR5_MAIN	0x40AF9400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
621	VIDEOSS0_GFX_MPU_WR6_MAIN	0x40AF9800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
622	VIDEOSS0_GFX_MPU_WR7_MAIN	0x40AF9C00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
623	VIDEOSS0_GFX_MPU_WR8_MAIN	0x40AFA000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
624	VIDEOSS0_GFX_MPU_WR9_MAIN	0x40AFA400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
625	VIDEOSS0_GFX_MPU_WR10_MAIN	0x40AFA800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
626	VIDEOSS0_GFX_MPU_WR11_MAIN	0x40AFAC00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
627	VIDEOSS0_GFX_MPU_WR12_MAIN	0x40AFB000	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters

Table 22-1 PPU fixed structure pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description
628	VIDEOSS0_GFX_MPU_WR13_MAIN	0x40AFB400	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
629	VIDEOSS0_GFX_MPU_WR14_MAIN	0x40AFB800	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
630	VIDEOSS0_GFX_MPU_WR15_MAIN	0x40AFBC00	0x00000004	VIDEOSS#0 MPU Configuration for Write Masters
631	PD_PD	0x40B00000	0x00000100	VIDEOSS#0 Power Domain Control
632	JPEGDEC_JPEGDEC	0x40B10000	0x00002000	VIDEOSS#0 JPEG Decoder

23 Bus masters

The Arbiter (part of flash controller) performs priority-based arbitration based on the master identifier. Each bus master has a dedicated 4-bit master identifier. This master identifier is used for bus arbitration and IPC functionality.

Table 23-1 Bus masters for access and protection control

ID No.	Master ID	Description
0	CPUSS_MS_ID_CM0	Master ID for CM0+
1	CPUSS_MS_ID_CRYPTO	Master ID for Crypto
2	CPUSS_MS_ID_DW0	Master ID for P-DMA0
3	CPUSS_MS_ID_DW1	Master ID for P-DMA1
4	CPUSS_MS_ID_DMAC	Master ID for M-DMA0
9	CPUSS_MS_ID_FAST0	Master ID for External **AXI** Master 0 (Ethernet#0)
10	CPUSS_MS_ID_FAST1	Master ID for External **AXI** Master 1 (JPEG Decoder)
11	CPUSS_MS_ID_FAST2	Master ID for M-DMA1 (AXI DMA)
12	CPUSS_MS_ID_FAST3	Master ID for VIDEO Subsystem
13	CPUSS_MS_ID_CM7_1	Master ID for CM7_1
14	CPUSS_MS_ID_CM7_0	Master ID for CM7_0
15	CPUSS_MS_ID_TC	Master ID for DAP Tap Controller

24 Miscellaneous configuration

Table 24-1 Miscellaneous configuration for CYT4DN devices

Sl. No.	Configuration	Number/ Instances	Description
0	SRSS_NUM_CLKPATH	11	Number of clock paths. One for each of FLL, PLL, Direct and CSV
1	SRSS_NUM_HFROOT	14	Number of CLK_HFs present
2	PERI_PC_NR	8	Number of protection contexts
3	PERI_PERI_PCLK_PCLK_GROUP_NR	2	Number of asynchronous PCLK groups
4	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_8_VECT	9	Group 0, Number of divide-by-8 clock dividers
5	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_16_VECT	16	Group 0, Number of divide-by-16 clock dividers
6	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_16_5_VECT	7	Group 0, Number of divide-by-16.5 clock dividers
7	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_24_5_VECT	3	Group 0, Number of divide-by-24.5 clock dividers
8	PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_CLOCK_VECT	84	Group 0, Number of programmable clocks [1, 256]
9	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_8_VECT	3	Group 1, Number of divide-by-8 clock dividers
10	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_16_VECT	4	Group 1, Number of divide-by-16 clock dividers
11	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_24_5_VECT	7	Group 1, Number of divide-by-24.5 clock dividers
12	PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_CLOCK_VECT	21	Group 1, Number of programmable clocks [1, 256]
13	CPUSS_CM0P_MPU_NR	8	Number of MPU regions in CM0+
14	CPUSS_CM7_0_FPU_LVL	2	CM7_0 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU
15	CPUSS_CM7_0_MPU_NR	16	Number of MPU regions in CM7_0
16	CPUSS_CM7_0_ICACHE_SIZE	16	CM7_0 Instruction cache (ICACHE) size in KB
17	CPUSS_CM7_0_DCACHE_SIZE	16	CM7_0 Data cache size (DCACHE) in KB
18	CPUSS_CM7_0_ITCM_SIZE	64	CM7_0 Instruction TCM (ITCM) size in KB
19	CPUSS_CM7_0_DTCM_SIZE	64	CM7_0 Data TCM (DTCM) size in KB
20	CPUSS_CM7_1_FPU_LVL	2	CM7_1 Floating point unit configuration. 0 - No FPU 1 - Single precision FPU 2 - Single and Double precision FPU
21	CPUSS_CM7_1_MPU_NR	16	Number of MPU regions in CM7_1
22	CPUSS_CM7_1_ICACHE_SIZE	16	CM7_1 Instruction cache (ICACHE) size in KB
23	CPUSS_CM7_1_DCACHE_SIZE	16	CM7_1 Data cache size (DCACHE) in KB
24	CPUSS_CM7_1_ITCM_SIZE	64	CM7_1 Instruction TCM (ITCM) size in KB
25	CPUSS_CM7_1_DTCM_SIZE	64	CM7_1 Data TCM (DTCM) size in KB
26	CPUSS_DW0_CH_NR	76	Number of P-DMA0 channels
27	CPUSS_DW1_CH_NR	84	Number of P-DMA1 channels
28	CPUSS_DMAC_CH_NR	8	Number of M-DMA0 controller channels
29	CPUSS_CRYPTO_BUFF_SIZE	2048	Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)
30	CPUSS_FAULT_FAULT_NR	4	Number of fault structures
31	CPUSS_IPC_IPC_NR	8	Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM7_0 access 2 - Reserved for CM7_1 access 3 - Reserved for DAP access Remaining for user purposes
32	CPUSS_PROT_SMPU_STRUCT_NR	16	Number of SMPU protection structures
33	SCB0_EZ_DATA_NR	256	Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports EZ mode

Table 24-1 Miscellaneous configuration for CYT4DN devices *(continued)*

Sl. No.	Configuration	Number/ Instances	Description
34	TCPWM_TR_ONE_CNT_NR	1	Number of input triggers per counter, routed to one counter
35	TCPWM_TR_ALL_CNT_NR	60	Number of input triggers routed to all counters, based on the pin package
36	TCPWM_GRP_NR	3	Number of TCPWM0 counter groups
37	TCPWM_GRP_NR0_GRP_GRP_CNT_NR	38	Number of counters per TCPWM0 Group #0
38	TCPWM_GRP_NR0_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #0
39	TCPWM_GRP_NR1_GRP_GRP_CNT_NR	12	Number of counters per TCPWM0 Group #1
40	TCPWM_GRP_NR1_CNT_GRP_CNT_WIDTH	16	Counter width in number of bits per TCPWM0 Group #1
41	TCPWM_GRP_NR2_GRP_GRP_CNT_NR	32	Number of counters per TCPWM0 Group #2
42	TCPWM_GRP_NR2_CNT_GRP_CNT_WIDTH	32	Counter width in number of bits per TCPWM0 Group #2
43	CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE	16	Message RAM size in KB shared by all the channels
44	EVTGEN_COMP_STRUCT_NR	16	Number of Event Generator comparator structures

25 Development support

CYT4DN has a rich set of documentation, programming tools, and online resources to assist during the development process. Visit **www.infineon.com** to find out more.

25.1 Documentation

A suite of documentation supports CYT4DN to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

25.1.1 Software user guide

A step-by-step guide for using the sample driver library along with third-party IDEs such as IAR EWARM and GHS Multi.

25.1.2 Technical reference manual

The Technical Reference Manual (TRM) contains all the technical detail needed to use a CYT4DN device, including a complete description of all registers. The TRM is available in the documentation section at **www.infineon.com**.

25.2 Tools

CYT4DN is supported on third-party development tool ecosystems such as IAR and GHS. The device is also supported by Infineon programming utilities for programming, erasing, or reading using Infineon MiniProg4 or Segger J-link. More details are available in the documentation section at **www.infineon.com**.

26 Electrical specifications

26.1 Absolute maximum ratings

Use of this device under conditions outside the min and max limits listed in **Table 26-1** may cause permanent damage to the device. Exposure to conditions within the limits of **Table 26-1** but beyond those of normal operation for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When operated under conditions within the limits of **Table 26-1** but beyond those of normal operation, the device may not operate to specification.

Power considerations

The average chip-junction temperature, T_J, in °C, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \text{Equation. 1}$$

Where:

T_A is the ambient temperature in °C.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{IO} ($P_D = P_{INT} + P_{IO}$).

P_{INT} is the chip internal power. ($P_{INT} = V_{DDD} \times I_{DD} + V_{CCD} \times I_{CC} + V_{DDA} \times I_{VDDA}$)

P_{IO} represents the power dissipation on input and output pins; user determined.

For most applications, $P_{IO} < P_{INT}$ and may be neglected.

On the other hand, P_{IO} may be significant if the device is configured to continuously drive external modules and/or memories.

WARNING:

- The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are guaranteed when the device is operated under these conditions.
- Operation under any conditions other than these conditions may adversely affect reliability of device and can result in device failure.
- No guarantee is made with respect to any use, operating conditions, or combinations not represented in this datasheet. If you want to operate the device under any condition other than listed herein, contact the sales representatives.

Table 26-1 Absolute maximum ratings

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID10	V_{DDD_ABS}	Power supply voltage (V_{DDD})[45, 46]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-4** for assignment of ports to supply domains
SID10A	$V_{DDIO\_GPIO\_ABS}$	Power supply voltage (V_{DDIO_GPIO})[46]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	Applies to all V_{DDIO_GPIO} sources ($V_{DDIO\_GPIO\_1/2/3}$) See **Table 3-4** for assignment of ports to supply domains
SID10B	$V_{DDIO\_SMC\_ABS}$	Power supply voltage (V_{DDIO_SMC})[46]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-4** for assignment of ports to supply domains
SID10C	$V_{DDIO\_HSIO\_ABS}$	Power supply voltage (V_{DDIO_HSIO})[46]	V_{SS} – 0.3	–	V_{SS} + 6.0	V	See **Table 3-4** for assignment of ports to supply domains
SID10D	$V_{DDIO\_SMIF\_ABS}$	Power supply voltage (V_{DDIO_SMIF})[46]	V_{SS} – 0.3	–	V_{SS} + 2.2	V	See **Table 3-4** for assignment of ports to supply domains
SID10E	$V_{DDIO\_SMIF\_HV\_ABS}$	Power supply voltage ($V_{DDIO\_SMIF\_HV}$)[46] Supply for 1.8 V I/Os	V_{SS} – 0.3	–	V_{SS} + 4.0	V	See **Table 3-4** for assignment of ports to supply domains
SID10F	$V_{DDPLL\_FPD0\_ABS}$	Power supply voltage (V_{DDPLL_FPD0})[46] Supply for FPD-Link PLLs	V_{SSA_FPD0} – 0.3	–	V_{SSA_FPD0} + 1.21	V	
SID10G	$V_{DDHA\_FPD0\_ABS}$	Power supply voltage (V_{DDHA_FPD0})[46] Supply for FPD-Link Drivers	V_{SSA_FPD0} – 0.3	–	V_{SSA_FPD0} + 4.0	V	
SID10H	$V_{DDA\_FPD0\_ABS}$	Power supply voltage (V_{DDA_FPD0})[46] Core-supply for FPD-Link	V_{SSA_FPD0} – 0.3	–	V_{SSA_FPD0} + 1.21	V	
SID10F_1	$V_{DDPLL\_FPD1\_ABS}$	Power supply voltage (V_{DDPLL_FPD1})[46] Supply for FPD-Link PLLs	V_{SSA_FPD1} – 0.3	–	V_{SSA_FPD1} + 1.21	V	
SID10G_1	$V_{DDHA\_FPD1\_ABS}$	Power supply voltage (V_{DDHA_FPD1})[46] Supply for FPD-Link Drivers	V_{SSA_FPD1} – 0.3	–	V_{SSA_FPD1} + 4.0	V	
SID10H_1	$V_{DDA\_FPD1\_ABS}$	Power supply voltage (V_{DDA_FPD1})[46] Core-supply for FPD-Link	V_{SSA_FPD1} – 0.3	–	V_{SSA_FPD1} + 1.21	V	
SID10J	$V_{DDA\_MIPI\_ABS}$	Power supply voltage (V_{DDA_MIPI})[46] Supply for MIPI D-PHY	V_{SSA_MIPI} – 0.3	–	V_{SSA_MIPI} + 1.21	V	
SID45	$V_{DDA\_DAC\_ABS}$	Power supply voltage (V_{DDA_DAC})[46] Supply for Audio DAC	V_{SSA_DAC} – 0.3	–	V_{SSA_DAC} + 4.0	V	
SID11	$V_{DDA\_ADC\_ABS}$	Analog power supply voltage (V_{DDA_ADC})[46] Supply for SAR ADC	V_{SSA_ADC} – 0.3	–	V_{SSA_ADC} + 6.0	V	
SID12	V_{REFH_ABS}	SAR Analog reference voltage, HIGH[46]	V_{SSA_ADC} – 0.3	–	V_{SSA_ADC} + 6.0	V	$V_{REFH} \leq V_{DDA\_ADC}$ + 0.3 V
SID12A	V_{REFL_ABS}	SAR Analog reference voltage, LOW[46]	V_{SSA_ADC} – 0.3	–	V_{SSA_ADC} + 0.3	V	
SID13	V_{CCD_ABS}	Power supply voltage (V_{CCD})	V_{SS} – 0.3	–	V_{SS} + 1.21	V	
SID15A	$V_{I\_GPIO\_ABS}$	Input voltage[46]	V_{SS} – 0.5	–	V_{DDIO_GPIO} + 0.5	V	See **Table 3-4** for assignment of ports to supply domains
SID15B	$V_{I\_SMC\_ABS}$	Input voltage[46]	V_{SS} – 0.5	–	V_{DDIO_SMC} + 0.5	V	See **Table 3-4** for assignment of ports to supply domains
SID15C	$V_{I\_HSIO\_ABS}$	Input voltage[46]	V_{SS} – 0.5	–	V_{DDIO_HSIO} + 0.5	V	See **Table 3-4** for assignment of ports to supply domains
SID15E	$V_{I\_SMIF\_ABS}$	Input voltage[46]	V_{SS} – 0.5	–	V_{DDIO_SMIF} + 0.5	V	See **Table 3-4** for assignment of ports to supply domains

Notes

45.Ensure that $V_{DDD} \geq V_{DDIO\_GPIO\_2} \geq V_{DDIO\_GPIO\_1}$. Ensure that V_{DDD} is turned on before $V_{DDIO\_GPIO\_1}$, and $V_{DDIO\_GPIO\_1}$ is turned on before $V_{DDIO\_GPIO\_2}$, or all at the same time. Also ensure $V_{DDIO\_GPIO\_2} \geq V_{DDA\_ADC}$ and $V_{DDIO\_SMC} \geq V_{DDA\_ADC}$ to avoid increased leakage. Operating the mentioned supplies within the same voltage range (i.e. within 2.7V-3.6 V, respectively within 4.5 V-5.5 V) fulfills being "equal".

46..These parameters are based on the condition that $V_{SS} = V_{SSA\_ADC} = V_{SSA\_DAC} = V_{SSA\_MIPI} = V_{SSA\_FPD}$ = 0.0 V.

Table 26-1 Absolute maximum ratings *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID15F	$V_{I\_MIPI\_ABS}$	Input voltage[46]	V_{SSA_MIPI} – 0.3	–	V_{DDA_MIPI} + 0.3	V	
SID16	$V_{I\_ADC\_ABS}$	Analog input voltage to ADC[46]	V_{SSA_ADC} – 0.3	–	V_{DDA_ADC} + 0.3	V	See **Table 3-4** for assignment of ports to supply domains
SID17A	$V_{O\_GPIO\_ABS}$	Output voltage[46]	V_{SS} – 0.3	–	V_{DDIO_GPIO} + 0.3	V	See **Table 3-4** for assignment of ports to supply domains
SID17B	$V_{O\_SMC\_ABS}$	Output voltage[46]	V_{SS} – 0.3	–	V_{DDIO_SMC} + 0.3	V	See **Table 3-4** for assignment of ports to supply domains
SID17C	$V_{O\_HSIO\_ABS}$	Output voltage[46]	V_{SS} – 0.3	–	V_{DDIO_HSIO} + 0.3	V	See **Table 3-4** for assignment of ports to supply domains
SID17E	$V_{O\_SMIF\_ABS}$	Output voltage[46]	V_{SS} – 0.3	–	V_{DDIO_SMIF} + 0.3	V	See **Table 3-4** for assignment of ports to supply domains
SID17G	$V_{O\_FPD0\_ABS}$	Output voltage[46]	V_{SSA_FPD0} – 0.3	–	V_{DDA_FPD0} + 0.3	V	
SID17G_1	$V_{O\_FPD1\_ABS}$	Output voltage[46]	V_{SSA_FPD1} – 0.3	–	V_{DDA_FPD1} + 0.3	V	
SID17H	$V_{O\_PMIC\_EN\_ABS}$	Output voltage[46]	V_{SS} – 0.3	–	V_{DDD} + 0.3	V	For the pin PMIC_EN
SID18	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[47, 48, 49, 50]	–5	–	5	mA	Applicable to general purpose I/O pins
SID18A	ΣI_{CLAMP_ABS}	Total maximum clamp current	–25	–	25	mA	Applicable to general purpose I/O pins in total for $V_{DDIO\_GPIO\_X}$
SID18B	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[47, 48, 49, 50]	–52	–	52	mA	Applicable to GPIO_SMC I/O pins
SID18C	ΣI_{CLAMP_ABS}	Total Maximum clamp current	–624	–	624	mA	Applicable to GPIO_SMC I/O pins clamping current occurred by sudden switching-off of inductive load (stepper motor coil) in total for V_{DDIO_SMC}
SID18F	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[47, 48, 49, 50]	–5	–	5	mA	Applicable to HSIO_STDLN and HSIO_STD pins
SID18G	ΣI_{CLAMP_ABS}	Total Maximum clamp current	–25	–	25	mA	Applicable to I/O pins in total for V_{DDIO_HSIO}
SID18J	$\lvert I_{CLAMP\_ABS}\rvert$	Maximum clamp current[47, 48, 49, 50]	–5	–	5	mA	Applicable to HSIO_ENH pins
SID18K	ΣI_{CLAMP_ABS}	Total Maximum clamp current	–25	–	25	mA	Applicable to I/O pins in total for V_{DDIO_SMIF}
SID20	$I_{OL1\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[51]	–	–	3.5	mA	Setting is 1 mA
SID21	$I_{OL2\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[51]	–	–	7	mA	Setting is 2 mA
SID22	$I_{OL3\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[51	–	–	10	mA	Setting is 5 mA

Notes

47. A current-limiting resistor must be provided such that the current at the I/O pin does not exceed rated values at any time, including during power transients. Refer to **Figure 26-1** for more information on the recommended circuit.
48. V_{DDD} and V_{DDIO} must be sufficiently loaded or protected to prevent them from being pulled out of the recommended operating range by the clamp current.
49. Clamp current can be applied only when the part is powered, and for ports between each pair of VDDIO/VSS pins (excluding ADC pins, ECO_IN/OUT, LPECO_IN/LPECO_OUT, WCO_IN/OUT and XRES_L).
50. When the conditions of [47], [48], [49], and SID18/A/B/C/F/G/J/K are met, $\lvert I_{CLAMP\_ABS}\rvert$ supersedes V_{IA_ABS} and V_{I_ABS}.
51. The maximum output current is the peak current flowing through any one GPIO I/O.

Table 26-1 Absolute maximum ratings *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID22A	$I_{OL4\_GPIO\_ABS}$	LOW-level maximum output current for GPIO[51]	–	–	10	mA	Setting is 6 mA
SID23A	$I_{OL\_PMIC\_EN\_ABS}$	Sink maximum current	–	–	4	mA	For the pin PMIC_EN. Required to add a current limiting series resistor of 1.25 kΩ - 5 kΩ to the PMIC_EN output.
SID23B	$\Sigma I_{OL\_PMIC\_EN\_ABS}$	Sink average current	–	–	1	mA	For the pin PMIC_EN The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio. The operation current period over the average current spec should be less than 100 ns. Required to add a current limiting series resistor of 1.25 kΩ - 5 kΩ to the PMIC_EN output.
SID26	$\Sigma I_{OL\_GPIO\_ABS}$	LOW-level total output current for GPIO[52]	–	–	50	mA	
SID26A	$I_{OL\_SMC\_ABS}$	LOW-level maximum output current for GPIO_SMC[53]	–	–	52	mA	Setting is 30 mA at –40°C
SID26B	$\Sigma I_{OL\_SMC\_ABS}$	LOW-level total output current for GPIO_SMC[54]	–	–	300	mA	25°C < T_A ≤ 105°C
SID26I	$\Sigma I_{OL\_SMC\_ABS}$	LOW-level total output current for GPIO_SMC[54]	–	–	450	mA	–40°C ≤ T_A ≤ 25°C
SID26C	$I_{OL\_SMIF\_ABS}$	LOW-level maximum output current for SMIF[55]	–	–	15	mA	CFG_OUT2/DS_TRIM<2:0> = 0b110
SID26D	$\Sigma I_{OL\_SMIF\_ABS}$	LOW-level total output current for SMIF[56]	–	–	100	mA	
SID26E	$I_{OL\_FPD\_ABS}$	LOW-level maximum output current for FPD-Link[57]	–	–	24	mA	
SID26F	$\Sigma I_{OL\_FPD\_ABS}$	LOW-level total output current for FPD-Link[58]	–	–	120	mA	
SID26G	$I_{OL\_HSIO\_ABS}$	LOW-level maximum output current for HSIO[59]	–	–	15	mA	
SID26H	$\Sigma I_{OL\_HSIO\_ABS}$	LOW-level total output current for HSIO[60]	–	–	150	mA	
SID27	$I_{OH1\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[51]	–	–	–3.5	mA	Setting is 1 mA
SID28	$I_{OH2\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[51]	–	–	–7	mA	Setting is 2 mA

Notes

52.The total output current is the maximum current flowing through all GPIO I/Os (GPIO_STD, and GPIO_ENH).
53.The maximum output current is the peak current flowing through any one GPIO_SMC I/O.
54.The total output current is the maximum current flowing through all SMC I/Os (GPIO_SMC).
55.The maximum output current is the peak current flowing through any one SMIF I/O output.
56.The total output current is the maximum current flowing through all SMIF I/O outputs.
57.The maximum output current is the peak current flowing through any one FPD-link I/O output.
58.The total output current is the maximum current flowing through all FPD-link I/O outputs.

Table 26-1 Absolute maximum ratings *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID29	$I_{OH3\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[51]	–	–	–10	mA	Setting is 5 mA
SID29A	$I_{OH4\_GPIO\_ABS}$	HIGH-level maximum output current for GPIO[51]	–	–	–10	mA	Setting is 6 mA
SID30A	$I_{OH\_PMIC\_EN\_ABS}$	Source maximum current	–	–	–4	mA	For the pin PMIC_EN. Required to add a current limiting series resistor of 1.25 kΩ-5 kΩ to the PMIC_EN output.
SID30B	$\Sigma I_{OH\_PMIC\_EN\_ABS}$	Source average current	–	–	–1	mA	For the pin PMIC_EN The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio. The operation current period over the average current spec should be less than 100 ns. Required to add a current limiting series resistor of 1.25 kΩ - 5 kΩ to the PMIC_EN output.
SID33	$\Sigma I_{OH1\_GPIO\_ABS}$	HIGH-level total output current for GPIO[52]	–	–	–50	mA	
SID33A	$I_{OH\_SMC\_ABS}$	HIGH-level maximum output current for GPIO_SMC[53]	–	–	–52	mA	Setting is 30 mA at –40°C
SID33B	$\Sigma I_{OH\_SMC\_ABS}$	HIGH-level total output current for GPIO_SMC[54]	–	–	–300	mA	
SID33C	$I_{OH\_SMIF\_ABS}$	HIGH-level maximum output current for SMIF[55]	–	–	–15	mA	CFG_OUT2/DS_TRIM<2:0> = 0b110
SID33D	$\Sigma I_{OH\_SMIF\_ABS}$	HIGH-level total output current for SMIF[56]	–	–	–100	mA	
SID33E	$I_{OH\_FPD\_ABS}$	HIGH-level maximum output current for FPD-Link[57]	–	–	–24	mA	
SID33F	$\Sigma I_{OH\_FPD\_ABS}$	HIGH-level total output current for FPD-Link[58]	–	–	–120	mA	
SID33G	$I_{OH\_HSIO\_ABS}$	HIGH-level maximum output current for HSIO[59]	–	–	–15	mA	
SID33H	$\Sigma I_{OH\_HSIO\_ABS}$	HIGH-level total output current for HSIO[60]	–	–	–150	mA	
SID34	P_D	Power dissipation	–	–	2900	mW	
SID36	T_A	Operating ambient temperature	–40	–	105	°C	For S-grade devices
SID38	T_{STG}	Storage temperature	–55	–	150	°C	
SID39	T_J	Operating junction temperature	–40	–	150	°C	
SID39A	V_{ESD_HBM}	Electrostatic discharge human body model	2000	–	–	V	
SID39B1	V_{ESD_CDM1}	Electrostatic discharge charged device model for corner pins	750	–	–	V	
SID39B2	V_{ESD_CDM2}	Electrostatic discharge charged device model for all other pins	500	–	–	V	
SID39C	I_{LU}	The maximum pin current the device can tolerate before triggering a latch-up	–100	–	100	mA	

Notes

59.The maximum output current is the peak current flowing through any one HSIO I/O.

60.The total output current is the maximum current flowing through all HSIO I/Os (HSIO_STD, HSIO_ENH, and HSIO_ENH_PDIFF).

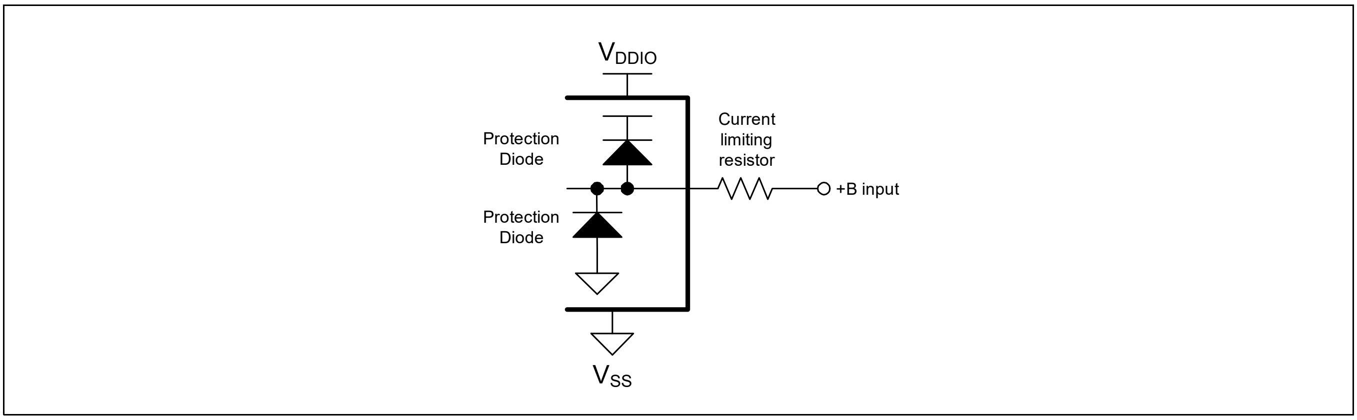


Figure 26-1 **Example of a recommended circuit**[61]

WARNING:
Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current, or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Note
61.+B is the positive battery voltage around 45 V.

26.2 Device-level specifications

Table 26-2 Recommended operating conditions

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended operating conditions							
SID40	V_{DDD}, V_{DDA_ADC}, V_{DDIO_GPIO}, V_{DDIO_SMC},	Power supply voltage[62]	2.7[63]	–	5.5[64]	V	V_{DDIO_GPIO} ($V_{DDIO\_GPIO\_0/1/2}$)
SID40A	V_{DDIO_EFP}	Power supply voltage for eFuse programming[65]	3.0	–	5.5	V	$V_{DDIO\_GPIO\_0}$ for this product, when programming eFuses
SID40B	V_{DDIO_HSIO}	Power supply voltage	3.0	3.3	3.6	V	
SID40D	V_{DDIO_SMIF}	Power supply voltage (V_{DDIO_SMIF}). Supply for 1.8 V I/Os.	1.7	1.8	1.95	V	Disable the IO cell input buffer before shutting off any of the IO supply voltages (V_{DDIO_SMIF} or $V_{DDIO\_SMIF\_HV}$).
SID40DA	$V_{DDIO\_SMIF\_HV}$	Power supply voltage ($V_{DDIO\_SMIF\_HV}$). HV supply for pre-drivers of HSIO_ENH I/Os.	3.0	3.3	3.6	V	
SID40E	V_{DDPLL_FPD0}[68, 69]	Power supply voltage (V_{DDPLL_FPD0}). Supply for FPD-link PLLs.	1.09	1.15	1.21	V	
SID40F	V_{DDHA_FPD0}	Power supply voltage (V_{DDHA_FPD0}). Supply for FPD-link line drivers.	3.0	3.3	3.6	V	
SID40G	V_{DDA_FPD0}[68, 69]	Power supply voltage (V_{DDA_FPD0}). Core-supply for FPD-link.	1.09	1.15	1.21	V	
SID40E_1	V_{DDPLL_FPD1}[68, 69]	Power supply voltage (V_{DDPLL_FPD1}). Supply for FPD-link PLLs.	1.09	1.15	1.21	V	
SID40F_1	V_{DDHA_FPD1}	Power supply voltage (V_{DDHA_FPD1}). Supply for FPD-link line drivers.	3.0	3.3	3.6	V	
SID40G_1	V_{DDA_FPD1}[68, 69]	Power supply voltage (V_{DDA_FPD1}). Core-supply for FPD-link.	1.09	1.15	1.21	V	
SID40H	V_{DDA_MIPI}[68]	Power supply voltage (V_{DDA_MIPI}). Supply for MIPI D-PHY.	1.09	1.15	1.21	V	
SID40J	V_{CCD}[68]	External V_{CCD} power supply	1.09	1.15	1.21	V	External V_{CCD} power supply range when externally supplied at V_{CCD}. V_{CCD} must not be driven by an external supply at startup. See related application note for correct startup sequence.
SID41	C_{S1}	Smoothing capacitor[66, 67]	30.8	94	103.4	µF	
SID43	V_{DDA_DAC}	High voltage supply	3.0	3.3	3.6	V	

Notes

62. Ensure $V_{DDIO\_GPIO\_2} \geq 0.8 \times V_{DDA\_ADC}$ when SARMUX0 is enabled.
63. 3.0 V ±10% is supported with a lower BOD setting option. This setting provides robust protection for internal timing but BOD reset occurs at a voltage below the specified operating conditions. A higher BOD setting option is available (consistent with down to 3.0 V) and guarantees that all operating conditions are met.
64. 5.0 V ±10% is supported with a higher OVD setting option. This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met. Voltage overshoot to a higher OVD setting range for V_{DDD} and V_{DDA_ADC} is permissible, provided the duration is less than 2 hours cumulated. Note that during overshoot voltage condition electrical parameters are not guaranteed.
65. eFuse programming must be executed with the part in a “quiet” state, with minimal activity (preferably only JTAG or a single LIN/CAN channel on V_{DDIO_GPIO} domain).
66. Only one smoothing capacitor, C_{S1} is required per chip (not per VCCD pin). The VCCD pins should be connected together to ensure a low-impedance connection (see the recommendation in **Figure 26-2**).
67. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device, ensure that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature coefficient is normally found within a parts catalog (such as, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to operate to less than datasheet specifications.
68. Analog and digital supply rails to be shorted on the PCB ($V_{DDPLL\_FPD0} = V_{DDPLL\_FPD1} = V_{DDA\_FPD0} = V_{DDA\_FPD1} = V_{DDA\_MIPI} = V_{CCD}$). These supply rails must be connected to the same power supply of V_{CCD}. This supply voltage needs to be filtered in order to eliminate any PLL jitters. It is recommended to use a noise filter to reduce the noise ripple for the FPD-LINK and MIPI-PHY supply.
69. After XRES_L release, internal LDO will be ON, and $V_{CCD} = V_{DDPLL\_FPD} = V_{DDA\_FPD} = 1.15$ V, only then hand over to external PMIC is allowed.

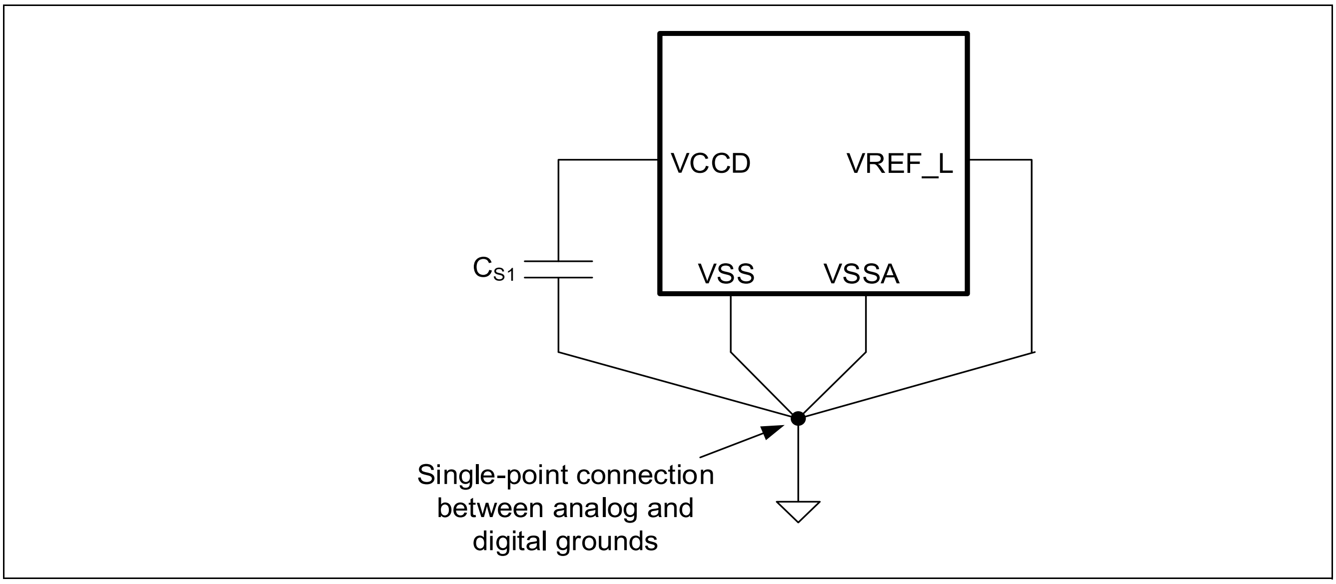


Figure 26-2 Smoothing capacitor

Smoothing capacitor should be placed as close as possible to the VCCD pin.

Table 26-3 DC specifications, CPU current, and transition time specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Execute with Flash							
SID51B	I_{CC1}	V_{CCD} current in external PMIC mode	–	700	1120	mA	Typ: T_A = 25°C, V_{CCD} = 1.15 V, process typ (TT) Max: T_A = 105°C, T_J = 150°C, V_{CCD} = 1.21 V, process worst (FF) (Maximum expected V_{CCD} when T_J = 150°C is reached due to self-heating)
SID52B	I_{DD1}	V_{DDD} current in external PMIC mode, Use case with VIDEOSS (V_{DDD} current for SID51B use case)	–	7	10	mA	Both Cortex®-M7 at 320 MHz generated by PLL with ECO reference, executing Dhrystone from flash with cache enabled. Cortex®-M0+ is sleeping at 100 MHz. Graphics Engine at 250 MHz, operating 2D rendering, drawing, capture, output on 2 displays. All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are enabled. No IO toggling. Typ: T_A = 25°C, V_{DDD} = 5.0 V, V_{CCD} = 1.15 V, process typ (TT) Max: T_A = 105°C, V_{DDD} = 5.5 V, V_{CCD} = 1.21 V, process worst (FF)
SID56	I_{DD1}	V_{DDD} current in internal regulator mode, Execute from flash; Cortex®-M7 CPU in Active mode	–	8	38	mA	Cortex®-M7_0 at 8 MHz generated by IMO reference, executing Dhrystone from flash with cache enabled. Cortex®-M0+ is sleeping at 8 MHz. CM7_1 is powered off. All clocks at 8 MHz generated by IMO. VIDEOSS power switched off All other peripherals, peripheral clocks, interrupts, CSV, DMA, PLL, ECO are disabled. No IO toggling. Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 85°C, V_{DDD} = 5.5 V, process worst (FF)

Table 26-3 DC specifications, CPU current, and transition time specifications *(continued)*

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID50A	I_{DD1}	V_{DDD} current in internal regulator mode. Cortex®-M7/M0+ CPUs in Sleep mode	–	28	70	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS power switched off All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 85°C, V_{DDD} = 5.5 V, process worst (FF)
SID50C	I_{DD1}	V_{DDD} current in internal regulator mode. Cortex®-M7/M0+ CPUs in Sleep mode (room temp)	–	–	40	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS power switched off All peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Max: T_A = 25°C, V_{DDD} = 5.5 V, process worst (FF)
SID50B	I_{CC1}	V_{CCD} current in external PMIC mode Cortex®-M7/M0+ CPUs in Sleep mode VIDEOSS in sleep mode (clocks off)	–	30	500	mA	Clocks running at max frequency, All CPUs in Sleep mode. VIDEOSS in sleep mode All other peripherals, peripheral clocks, interrupts, CSV, DMA, ECO are disabled. No IO toggling. Typ: T_A = 25°C, V_{CCD} = 1.15 V, process typ (TT) Max: T_A = 105°C, V_{CCD} = 1.21 V, process worst (FF)
DeepSleep Mode							
SID59	I_{DD_DS32A}	V_{DDD} current in internal regulator mode. 32 KB SRAM retention, LPECO (4 MHz) operation in DeepSleep mode.	–	150	–	µA	Deep Sleep Mode (RTC and EVTGEN operating, all other peripherals off, CAN MRAM disabled), CM0+ and CM7_0 retain, CM7_1 power switched OFF Typ: T_A = 25°C, V_{DDD} = 5.0 V, V_{CCD} = 1.1 V, process typ (TT) FPD-Link/MIPI Standby currents not included

Table 26-3 DC specifications, CPU current, and transition time specifications *(continued)*

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID59A	I_{DD_DS32A}	V_{DDD} current in internal regulator mode. 32 KB SRAM retention, LPECO (4 MHz) operation in DeepSleep mode. (room temp)	–	–	250	µA	Deep Sleep Mode (RTC at 32 kHz and EVTGEN operating, all other peripherals off, CAN MRAM disabled), CM0+ and CM7_0 retain, CM7_1 power switched OFF Max: V_{DDD} = 5.5 V, T_A = 25°C, process worst (FF) FPD-Link/MIPI Standby currents not included
SID60	I_{DD_DS32B}	V_{DDD} current in internal regulator mode. 32 KB SRAM retention, LPECO (4 MHz) operation in DeepSleep mode.	–	–	2500	µA	DeepSleep Mode (RTC and Event generator operating, all other peripherals off, CAN MRAM disabled), CM0+ and CM7_0 retain, CM7_1 power switched OFF Max: V_{DDD} = 5.5 V, T_A = 85°C, process worst (FF) FPD-Link/MIPI Standby currents not included
SID64	I_{DD_DS32C}	V_{DDD} current in internal regulator mode. 32 KB SRAM retention, ILO operation in DeepSleep mode.	–	50	2500	µA	DeepSleep Mode (RTC and Event generator operating, all other peripherals off, CAN MRAM disabled) CM0+ and CM7_0 retain, CM7_1 power switched OFF Typ: T_A = 25°C, V_{DDD} = 5.0 V, process typ (TT) Max: T_A = 85°C, V_{DDD} = 5.5 V, process worst (FF) FPD-Link/MIPI Standby currents not included
SID64A	I_{DD_DS32D}	32 KB SRAM retention, ILO operation in DeepSleep mode (room temp)	–	–	150	µA	DeepSleep Mode (RTC at 32 kHz and Event generator operating, all other peripherals off, CAN MRAM disabled) CM0+ and CM7_0 retain, CM7_1 power switched OFF Max: T_A = 25°C, V_{DDD} = 5.5 V, process worst (FF) FPD-Link/MIPI Standby currents not included
Hibernate Mode							
SID66	I_{DD_HIB1}	V_{DDD} current, Hibernate Mode + RTC at 32.768 kHz	–	–	20	µA	T_A = 25°C using ILO, V_{DDD} = 5.0 V
SID66A	I_{DD_HIB2}	V_{DDD} current, Hibernate Mode + RTC at 32.768 kHz	–	–	40	µA	T_A = 25°C, using WCO, V_{DDD} = 5.0 V

Table 26-3 DC specifications, CPU current, and transition time specifications *(continued)*

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID66B	I_{DD_HIB3}	V_{DDD} current, Hibernate Mode + RTC at 32.768 kHz	–	–	75	µA	T_A = 85°C, using WCO, V_{DDD} = 5.5 V
SID66C	I_{DD_HIB4}	V_{DDD} current, Hibernate Mode + RTC at 32.768 kHz	–	–	150	µA	T_A = 25°C using LPECO 4 MHz, 20 pF load of LPECO V_{DDD} = 5.0 V
SID66D	I_{DD_HIB5}	V_{DDD} current, Hibernate Mode + RTC at 32.768 kHz	–	–	215	µA	T_A = 85°C, using LPECO 4 MHz, 20 pF load of LPECO V_{DDD} = 5.5 V
Power Mode Transition Times							
SID69_1	t_{ACT_DS}	Power down time from ACTIVE to DEEPSLEEP (using the internal regulator)	–	–	2.8	µs	When IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.
SID69A	t_{ACT_DS}	Power down time from ACTIVE to DeepSleep (using external PMIC)	–	–	6.5	µs	When IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off. The time for the PMIC to deassert its power good signal is not included.
SID67	t_{DS_ACT}	DeepSleep to Active transition time (IMO clock, flash execution)	–	–	26	µs	When using 8 MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T_A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs
SID67A	$t_{DS\_ACT\_FLL}$	DeepSleep to Active transition time (FLL clock, flash execution)	–	–	26	µs	When using FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until Flash execution. T_A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs
SID67B	$t_{DS\_ACT\_PLL}$	DeepSleep to Active transition time (PLL clock)	–	–	60	µs	When using PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until PLL locks. T_A ≥ –5°C Note: At temperatures below –5°C the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 µs

Table 26-3 DC specifications, CPU current, and transition time specifications *(continued)*

All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID68C	t_{HIB_ACT}	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) until CM0+ begins executing ROM boot	–	–	650	µs	Without boot runtime with max. 103.4 µF smoothing capacitor per SID41, no FPD/MIPI filter connected Guaranteed by Design
SID68D	t_{HIB_ACT}	Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) until CM0+ begins executing ROM boot	–	–	1040	µs	Without boot runtime with max. 103.4 µF smoothing capacitor per SID41 + max. 5x11 µF FPD/MIPI filter caps Guaranteed by Design
SID68A	t_{LVR_ACT}	Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot	8	–	10	µs	Without boot runtime. Guaranteed by design
SID68B	t_{LVR_DS}	Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot	–	–	15	µs	Without boot runtime. Guaranteed by design
SID79	$t_{HIBWAKE\text{-}UP\_PW}$	Pulse width for wakeup from Hibernate mode on HIBERANTE_WAKEUP pins	90	–	–	ns	Guaranteed by design
SID80A	t_{RB_N}	ROM boot startup time or wakeup time from hibernate in NORMAL protection state	–	–	1700	µs	FAST_BOOT = 1, CM0+ clocked at 100 MHz
SID80B	t_{RB_S}	ROM boot startup time or wakeup time from hibernate in SECURE protection state	–	–	2300	µs	FAST_BOOT = 1, CM0+ clocked at 100 MHz
SID81A	t_{FB}	Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state	–	–	190	µs	FAST_BOOT = 1, TOC2_FLAGS = 0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms
SID81B	t_{FB_A}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	5000	µs	FAST_BOOT = 1, TOC2_FLAGS = 0x24F, CM0+ clocked at 100 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, APP size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K.
SID81C	t_{FB_B}	Flash boot with app authentication time in NORMAL/SECURE protection state	–	–	8150	µs	FAST_BOOT = 1, TOC2_FLAGS = 0x24F, CM0+ clocked at 100 MHz, Listen window = 0 ms, Public key exponent e = 0x010001, APP size is 64 KB with the last 384 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA3K.
Regulator specifications							
SID600	V_{CCD}	Internal regulator core supply voltage (transient range)	1.05	1.1	1.15	V	

Table 26-3 DC specifications, CPU current, and transition time specifications *(continued)*

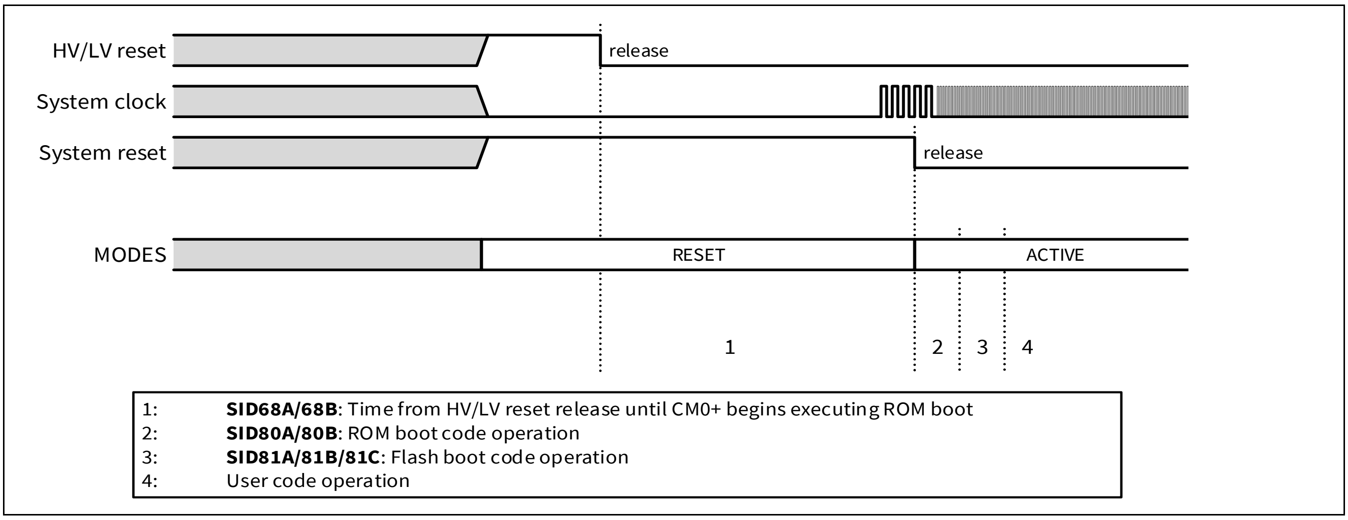
All specifications are valid for –40°C ≤ T_A ≤ 105°C and for 2.7 V to 5.5 V except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID600A	V_{CCD_S}	Internal regulator core supply voltage (static range, no load)	1.075	1.1	1.125	V	Guaranteed by design
SID601	I_{DDD_ACT}	Regulator operating current in Active/Sleep mode	–	900	1500	µA	Guaranteed by design
SID602	I_{DDD_DPSLP}	Regulator operating current in DeepSleep mode	–	1.5	20	µA	Guaranteed by design
SID603	I_{RUSH}	In-rush current	–	–	850	mA	
SID604	I_{ILDOUT}	Internal regulator output current for operation	–	–	300	mA	
SID606	V_{IL}	PMIC digital input LOW voltage (%V_{DDD})	0.3 × V_{DDD}	–	–	V	
SID606A	V_{IH}	PMIC digital input HIGH voltage (%V_{DDD})	–	–	0.7 × V_{DDD}	V	
SID606B	V_{HYST}	PMIC digital input hysteresis (%V_{DDD})	0.05 × V_{DDD}	–	–	V	
SID607	V_{OL}	PMIC digital output LOW voltage	–	–	0.5	V	I_{OL} = 1 mA
SID607A	V_{OH}	PMIC digital output HIGH voltage	V_{DDD} – 0.5	–	–	V	I_{OH} = –1 mA

26.3 Reset specifications

Table 26-4 XRES_L Reset

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
XRES_L DC specifications							
SID73	I_{IDD_XRES}	I_{DD} when XRES_L asserted	–	–	1.7	mA	Typ: T_A = 25 °C, V_{DDD} = 5 V, process typ (TT) Max: T_A = 105 °C, V_{DDD} = 5.5 V, process worst (FF)
SID74	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID75	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID76	R_{PULLUP}	Pull-up resistor	7	–	20	kΩ	
SID77	C_{IN}	Input capacitance	–	–	5	pF	
SID78	$V_{HYSXRES}$	Input voltage hysteresis	0.05 × V_{DDD}	–	–	V	
XRES_L AC specifications							
SID70	t_{XRES_ACT}	XRES_L deasserted to Active transition time	–	–	265	µs	Without boot runtime Guaranteed by design
SID71	t_{XRES_PW}	XRES_L pulse width	5	–	–	µs	
SID72	t_{XRES_FT}	Pulse suppression width	100	–	–	ns	



1: **SID68A/68B**: Time from HV/LV reset release until CM0+ begins executing ROM boot
2: **SID80A/80B**: ROM boot code operation
3: **SID81A/81B/81C**: Flash boot code operation
4: User code operation

Figure 26-3 Reset sequence

26.4 I/O specifications

Table 26-5 I/O specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
GPIO_STD specifications (5-V I/Os, except GPIO_ENH)							
SID650	V_{OL1}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 $V_{DDIO\_GPIO} \geq 4.5$ V
SID651	V_{OL2}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X $V_{DDIO\_GPIO} \geq 4.5$ V
SID651D	V_{OL2}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID652	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $V_{DDIO\_GPIO} \geq 4.5$ V
SID652D	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID653	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $V_{DDIO\_GPIO} \geq 4.5$ V
SID653D	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID654	V_{OH1}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 $V_{DDIO\_GPIO} \geq 4.5$ V
SID654D	V_{OH1}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID655	V_{OH2}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b01 $V_{DDIO\_GPIO} \geq 4.5$ V
SID655D	V_{OH2}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b01 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID656	V_{OH3}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $V_{DDIO\_GPIO} \geq 4.5$ V
SID656D	V_{OH3}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID657	V_{OH4}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $V_{DDIO\_GPIO} \geq 4.5$ V
SID657D	V_{OH4}	Output voltage HIGH level	V_{DDIO_GPIO} – 0.5	–	–	V	I_{OH} = –0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID658	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID659	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID660	V_{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID661	V_{IH_TTL}	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662	V_{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 $4.5\ V \le V_{DDIO\_GPIO} \le 5.5\ V$
SID663	V_{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID664	V_{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665	V_{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 $4.5\ V \le V_{DDIO\_GPIO} \le 5.5\ V$
SID666	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID668	V_{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0> = 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 $4.5\ V \le V_{DDIO\_GPIO} \le 5.5\ V$
SID669	C_{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID670	I_{IL}	Input leakage current	–1	–	1	µA	$V_{DDIO\_GPIO} = V_{DDD} = 5.5\ V$, $V_{SS} < V_I < V_{DDIO\_GPIO\_x}$ $-40\ °C \le T_A \le 105\ °C$ This is valid for the pin which do not have ADC input functionality.
SID671	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	10	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b00, 20-pF load, entire V_{DDIO_GPIO} range
SID672	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b00, 50-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
SID673	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b01, 20-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
SID674	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b10, 10-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
SID675	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	CFG_OUT/DRIVE_SEL<1:0> = 0b11, 6-pF load, entire V_{DDIO_GPIO} range, Guaranteed by design
GPIO_SMC specifications (Stepper Motor Control, 5-V I/Os)							
SID650A	V_{OL2}	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 6\ mA$ CFG_OUT/DRIVE_SEL<1:0> = 0b01 $V_{DDIO\_SMC} \ge 4.5\ V$
SID651A	V_{OL2}	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 5\ mA$ CFG_OUT/DRIVE_SEL<1:0> = 0b01 $V_{DDIO\_SMC} \ge 4.5\ V$
SID651E	V_{OL2}	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 2\ mA$ CFG_OUT/DRIVE_SEL<1:0> = 0b01 $2.7\ V \le V_{DDIO\_SMC} < 4.5\ V$

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID652A	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $V_{DDIO\_SMC} \geq 4.5$ V
SID652E	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $2.7\ V \leq V_{DDIO\_SMC} < 4.5$ V
SID653A	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $V_{DDIO\_SMC} \geq 4.5$ V
SID653E	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $2.7\ V \leq V_{DDIO\_SMC} < 4.5$ V
SID653B	V_{OL5}	Output voltage LOW level	–	–	0.5	V	I_{OL} = 30 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 25 °C < $T_A \leq$ 105 °C $V_{DDIO\_SMC} \geq 4.5$ V
SID653C	V_{OL5}	Output voltage LOW level	–	–	0.5	V	I_{OL} = 40 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 –30 °C < $T_A \leq$ 25 °C $V_{DDIO\_SMC} \geq 4.5$ V
SID653H	V_{OL5}	Output voltage LOW level	–	–	0.5	V	I_{OL} = 52 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 –40 °C ≤ $T_A \leq$ –30 °C $V_{DDIO\_SMC} \geq 4.5$ V
SID654A	V_{OH2}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b01 $V_{DDIO\_SMC} \geq 4.5$ V
SID654E	V_{OH2}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b01 $2.7\ V \leq V_{DDIO\_SMC} < 4.5$ V
SID656A	V_{OH3}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $V_{DDIO\_SMC} \geq 4.5$ V
SID656E	V_{OH3}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $2.7\ V \leq V_{DDIO\_SMC} < 4.5$ V
SID657A	V_{OH4}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $V_{DDIO\_SMC} \geq 4.5$ V
SID657E	V_{OH4}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OH} = –0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $2.7\ V \leq V_{DDIO\_SMC} < 4.5$ V
SID657B	V_{OH5}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OL} = –30 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 25 °C < $T_A \leq$ 105 °C $V_{DDIO\_SMC} \geq 4.5$ V
SID657C	V_{OH5}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OL} = –40 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 –30 °C < $T_A \leq$ 25 °C $V_{DDIO\_SMC} \geq 4.5$ V

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID657I	V_{OH5}	Output voltage HIGH level	V_{DDIO_SMC} – 0.5	–	–	V	I_{OL} = –52 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00 CFG_OUT/SLOW<0:0> = 0b1 –40 °C < T_A ≤ –30 °C V_{DDIO_SMC} ≥ 4.5 V
SID658A	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID659A	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID659B	V_{OUT}	Mid range voltage level	2.45	–	2.55	V	CFG/DRIVE_MODE<2:0> = 0b001
SID660A	V_{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661A	V_{IH_TTL}	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662A	V_{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_SMC} ≤ 5.5 V
SID663A	V_{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDIO_SMC}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID664A	V_{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665A	V_{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDIO_SMC}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_SMC} ≤ 5.5 V
SID666A	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID668A	V_{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V_{DDIO_SMC}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_SMC} ≤ 5.5 V
SID669A	C_{IN}	Input pin capacitance	–	–	7	pF	Test condition: 10/100MHz
SID670A	I_{IL}	Input leakage current	–2	–	2	µA	V_{DDIO_SMC} = V_{DDD} = 5.5 V, V_{SS} < V_I < V_{DDIO_SMC} –40 °C ≤ T_A ≤ 105 °C This is valid for the pin which do not have ADC input functionality.
SID673A	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	1	–	20	ns	5 mA drive strength 20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_OUT/SLOW<0:0> = 0b0, guaranteed by design
SID674A	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	1	–	20	ns	2 mA drive strength 10-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_OUT/SLOW<0:0> = 0b0, guaranteed by design
SID675A	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	1	–	20	ns	1 mA drive strength 6-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b11, CFG_OUT/SLOW<0:0> = 0b0, guaranteed by design

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID676A	$t_{R\_F\_SMC\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	15	–	80	ns	30 mA drive strength No load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676B	$t_{R\_F\_SMC\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	25	–	100	ns	30 mA drive strength 85-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
SID676C	$t_{R\_F\_SMC\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_SMC})	100	–	200	ns	30 mA drive strength 2.7-nF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1
GPIO_ENH Specifications							
SID650C	V_{OL1}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 6 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X $V_{DDIO\_GPIO} \geq 4.5$ V
SID650D	V_{OL1}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X $V_{DDIO\_GPIO} \geq 4.5$ V
SID651C	V_{OL1}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X 2.7 V £ $V_{DDIO\_GPIO} < 4.5$ V
SID652C	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $V_{DDIO\_GPIO} \geq 4.5$ V
SID652F	V_{OL3}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 2.7 V £ $V_{DDIO\_GPIO} < 4.5$ V
SID653F	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $V_{DDIO\_GPIO} \geq 4.5$ V
SID653G	V_{OL4}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID654C	V_{OH1}	Output voltage HIGH level	$V_{DDIO\_GPIO} - 0.5$	–	–	V	I_{OH} = –5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X $V_{DDIO\_GPIO} \geq 4.5$ V
SID654G	V_{OH1}	Output voltage HIGH level	$V_{DDIO\_GPIO} - 0.5$	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b0X $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID655C	V_{OH3}	Output voltage HIGH level	$V_{DDIO\_GPIO} - 0.5$	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $V_{DDIO\_GPIO} \geq 4.5$ V
SID656C	V_{OH3}	Output voltage HIGH level	$V_{DDIO\_GPIO} - 0.5$	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID657G	V_{OH4}	Output voltage HIGH level	$V_{DDIO\_GPIO} - 0.5$	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $V_{DDIO\_GPIO} \geq 4.5$ V
SID657H	V_{OH4}	Output voltage HIGH level	$V_{DDIO\_GPIO} - 0.5$	–	–	V	I_{OH} = –0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11 $2.7\text{ V} \leq V_{DDIO\_GPIO} < 4.5$ V
SID658C	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID659C	R_{PU}	Pull-up resistance	25	50	100	kΩ	

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID660C	V_{IH_CMOS}	Input voltage HIGH threshold in CMOS mode	0.7 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID661C	V_{IH_TTL}	Input voltage HIGH threshold in TTL mode	2.0	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID662C	V_{IH_AUTO}	Input voltage HIGH threshold in AUTO mode	0.8 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID663C	V_{IL_CMOS}	Input voltage LOW threshold in CMOS mode	–	–	0.3 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID664C	V_{IL_TTL}	Input voltage LOW threshold in TTL mode	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665C	V_{IL_AUTO}	Input voltage LOW threshold in AUTO mode	–	–	0.5 × V_{DDIO_GPIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID666C	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID668C	V_{HYST_AUTO}	Hysteresis in AUTO mode	0.05 × V_{DDIO_GPIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b0 4.5 V ≤ V_{DDIO_GPIO} ≤ 5.5 V
SID669C	C_{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID670C	I_{IL}	Input leakage current	–1	–	1	µA	$V_{DDIO\_GPIO} = V_{DDD} = 5.5$ V, $V_{SS} < V_I < V_{DDIO\_GPIO}$ –40 °C ≤ T_A ≤ 105 °C
SID671C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	10	ns	20 pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range
SID672C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	50 pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID673C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID674C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	10-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design
SID675C	$t_{R\_F\_FAST}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	1	–	20	ns	6-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b11, CFG_OUT/SLOW<0:0> = 0b0, entire V_{DDIO_GPIO} range, Guaranteed by design

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID676E	$t_{F\_I2C\_SLOW}$	Fall time (30% to 70% of V_{DDIO_GPIO})	20 × (V_{DDIO_GPIO} / 5.5)	–	250	ns	10-pF to 400-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, minimum external R_{PU} = 400 Ω
SID677C	$t_{R\_F\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	20 × (V_{DDIO_GPIO} / 5.5)	–	160	ns	20-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, output frequency = 1 MHz
SID678C	$t_{R\_F\_SLOW}$	Rise time or fall time (10% to 90% of V_{DDIO_GPIO})	20 × (V_{DDIO_GPIO} / 5.5)	–	250	ns	400-pF load, CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_OUT/SLOW<0:0> = 0b1, output frequency = 400 kHz Guaranteed by design
HSIO_STD specifications (3 V I/Os)							
SID650B	V_{OL0}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 10 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00
SID654F	V_{OL1}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b01
SID655F	V_{OL2}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10
SID656F	V_{OL3}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11
SID657F	V_{OH0}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.5	–	–	V	I_{OH} = –10 mA CFG_OUT/DRIVE_SEL<1:0> = 0b00
SID661D	V_{OH1}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.5	–	–	V	I_{OH} = –2 mA CFG_OUT/DRIVE_SEL<1:0> = 0b01
SID662D	V_{OH2}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.5	–	–	V	I_{OH} = –1 mA CFG_OUT/DRIVE_SEL<1:0> = 0b10
SID663D	V_{OH3}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.5	–	–	V	I_{OH} = –0.5 mA CFG_OUT/DRIVE_SEL<1:0> = 0b11
SID664B	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID665B	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID665E	V_{IH3}	Input Voltage HIGH threshold	1.7	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID665L	V_{IH1}	Input Voltage HIGH threshold	2	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID667D	V_{IH0}	Input Voltage HIGH threshold	0.7 × V_{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID667E	V_{IL3}	Input Voltage LOW threshold	–	–	0.9	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID671J	V_{IL1}	Input Voltage LOW threshold	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID671D	V_{IL0}	Input Voltage LOW threshold	–	–	0.3 × V_{DDIO_HSIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID674B	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID675B	C_{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID676D	I_{IL12}	Input leakage current	–1	–	1	µA	V_{DDIO_HSIO} = 3.6 V, $V_{SS} < V_I < V_{DDIO\_HSIO}$ –40 °C ≤ T_A ≤ 105 °C
HSIO_STDLN specifications (3 V I/Os)							
SID650E	V_{OL0}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 10 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID651F	V_{OL0}	Output LOW voltage level	–	–	0.2	V	I_{OL} = 0.1 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID654I	V_{OL1}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 10 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID655G	V_{OL2}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 2 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID656G	V_{OL3}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 1 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID656H	V_{OL4}	Output LOW voltage level	–	–	0.4	V	I_{OL} = 0.5 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID657J	V_{OH0}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –10 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID658D	V_{OH0}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.2	–	–	V	I_{OH} = –0.1 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000
SID661F	V_{OH1}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –10 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b001 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID662F	V_{OH2}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –2 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID663E	V_{OH3}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –1 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID663F	V_{OH4}	Output HIGH voltage level	V_{DDIO_HSIO} – 0.4	–	–	V	I_{OH} = –0.5 mA CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100 3.0 V ≤ V_{DDIO_HSIO} ≤ 3.6 V
SID664D	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID665F	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID665H	V_{IH3}	Input Voltage HIGH threshold	1.7	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID667G	V_{IH0}	Input Voltage HIGH threshold	0.7 × V_{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0

Table 26-5 **I/O specifications** *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID667I	V_{IH1}	Input Voltage HIGH threshold	2	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID667H	V_{IL3}	Input Voltage LOW threshold	–	–	0.9	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b1 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID671F	V_{IL0}	Input Voltage LOW threshold	–	–	0.3 × V_{DDIO_HSIO}	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID671G	V_{IL1}	Input Voltage LOW threshold	–	–	0.8	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b1
SID674D	V_{HYST_CMOS}	Hysteresis in CMOS mode	0.05 × V_{DDIO_HSIO}	–	–	V	CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0 CFG_IN/VTRIP_SEL<0:0> = 0b0
SID675D	C_{IN}	Input pin capacitance	–	–	5	pF	Test condition: 10/100MHz
SID676H	I_{IL12}	Input leakage current	–1	–	1	µA	$V_{DDIO\_HSIO} = 3.6$ V, $V_{SS} < V_I < V_{DDIO\_HSIO}$ -40 °C ≤ T_A ≤ 105 °C
HSIO_ENH/HSIO_ENH_PDIFF specifications (1.8 V I/Os)							
SID950	V_{OL_XSPI}	Output Voltage LOW level	–	–	0.2	V	$I_{OL} = 0.1$ mA CFG_OUT2/DS_TRIM<2:0> = 0b100
SID950D	V_{OL2}	Output Voltage LOW level	–	–	0.4	V	$I_{OL} = 8$ mA CFG_OUT2/DS_TRIM<2:0> = 0b010, V_{DDIO_SMIF} = 1.7 V ~ 1.95 V
SID950A	V_{OL4}	Output Voltage LOW level	–	–	0.4	V	$I_{OL} = 3$ mA CFG_OUT2/DS_TRIM<2:0> = 0b100, V_{DDIO_SMIF} = 1.7 V ~ 1.95 V
SID950G	V_{OL6}	Output Voltage LOW level	–	–	0.4	V	$I_{OL} = 6$ mA CFG_OUT2/DS_TRIM<2:0> = 0b110, V_{DDIO_SMIF} = 1.7 V ~ 1.95 V
SID954	V_{OH_XSPI}	Output Voltage HIGH level	$V_{DDIO\_SMIF} - 0.2$	–	–	V	$I_{OH} = -0.1$ mA CFG_OUT2/DS_TRIM<2:0> = 0b100
SID954D	V_{OH2}	Output Voltage HIGH level	$V_{DDIO\_SMIF} - 0.4$	–	–	V	$I_{OH} = -8$ mA CFG_OUT2/DS_TRIM<2:0> = 0b010, V_{DDIO_SMIF} = 1.7 V ~ 1.95 V
SID954A	V_{OH4}	Output Voltage HIGH level	$V_{DDIO\_SMIF} - 0.4$	–	–	V	$I_{OH} = -3$ mA CFG_OUT2/DS_TRIM<2:0> = 0b100, V_{DDIO_SMIF} = 1.7 V ~ 1.95 V
SID954G	V_{OH6}	Output Voltage HIGH level	$V_{DDIO\_SMIF} - 0.4$	–	–	V	$I_{OH} = -6$ mA CFG_OUT2/DS_TRIM<2:0> = 0b110, V_{DDIO_SMIF} = 1.7 V ~ 1.95 V
SID958	R_{PD}	Pull-down resistance	25	50	100	kΩ	
SID959	R_{PU}	Pull-up resistance	25	50	100	kΩ	
SID960	V_{IH_CMOS}	Input Voltage HIGH threshold for xSPI and HSSPI in CMOS mode	0.7 × V_{DDIO_SMIF}	–	–	V	
SID961	V_{IL_CMOS}	Input Voltage LOW threshold for xSPI and HSSPI in CMOS mode	–	–	0.3 × V_{DDIO_SMIF}	V	
SID963	C_{IN}	Input pin capacitance	–	–	6	pF	Test condition: 10/100MHz
SID964	I_{IL12}	Input leakage current	–5	–	5	µA	$V_{SS} < V_I < V_{DDIO\_SMIF}$ -40°C ≤ T_A ≤ 105°C

Table 26-5 **I/O specifications** *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID965	V_{OS_US}	Overshoot/Undershoot voltage output	–	–	1	V	Frequency: max 167 MHz Trace length: - 2.1", 50 Ω impedance controlled, followed by a 7.5 pF load CFG_OUT2/DS_TRIM<2:0> = 0b100 - 1.2", 50 Ω impedance controlled, followed by a 15 pF load CFG_OUT2/DS_TRIM<2:0> = 0b110 **Figure 26-4**
SID966	T_{OS_US}	Overshoot/Undershoot duration of output	–	–	5	ns	Frequency: max 167 MHz Trace length: - 2.1", 50 Ω impedance controlled, followed by a 7.5pF load CFG_OUT2/DS_TRIM<2:0> = 0b100 - 1.2", 50 Ω impedance controlled, followed by a 15 pF load CFG_OUT2/DS_TRIM<2:0> = 0b110 **Figure 26-4**
SID965A	$V_{OS\_US\_IN}$	Allowed Overshoot/ Undershoot input voltage on HSIO_ENH	–	–	1	V	Maximum allowed Overshoot/undershoot input on HSIO_ENH IO-cells
SID966B	$T_{OS\_US\_IN}$	Allowed Overshoot/ Undershoot input Duration on HSIO_ENH	–	–	5	ns	Maximum allowed Overshoot/undershoot input on HSIO_ENH IO-cells
SID967	$I_{VDDIO\_SMIF\_HV}$	Current consumption of $V_{DDIO\_SMIF\_HV}$ per SMIF Interface	–	–	15	mA	Max: $T_A = -40°C$, $V_{DDIO\_SMIF\_HV} = 3.6$ V, process worst (FF)
GPIO input specifications							
SID98	t_{FT}	Analog glitch filter (pulse suppression width)	–	–	50[70]	ns	One filter per port group (required for some I^2C speeds)
SID99	t_{INT}	Minimum pulse width for GPIO interrupt	160	–	–	ns	

Note

[70] If more longer pulse suppression width is necessary, use Smart I/O.

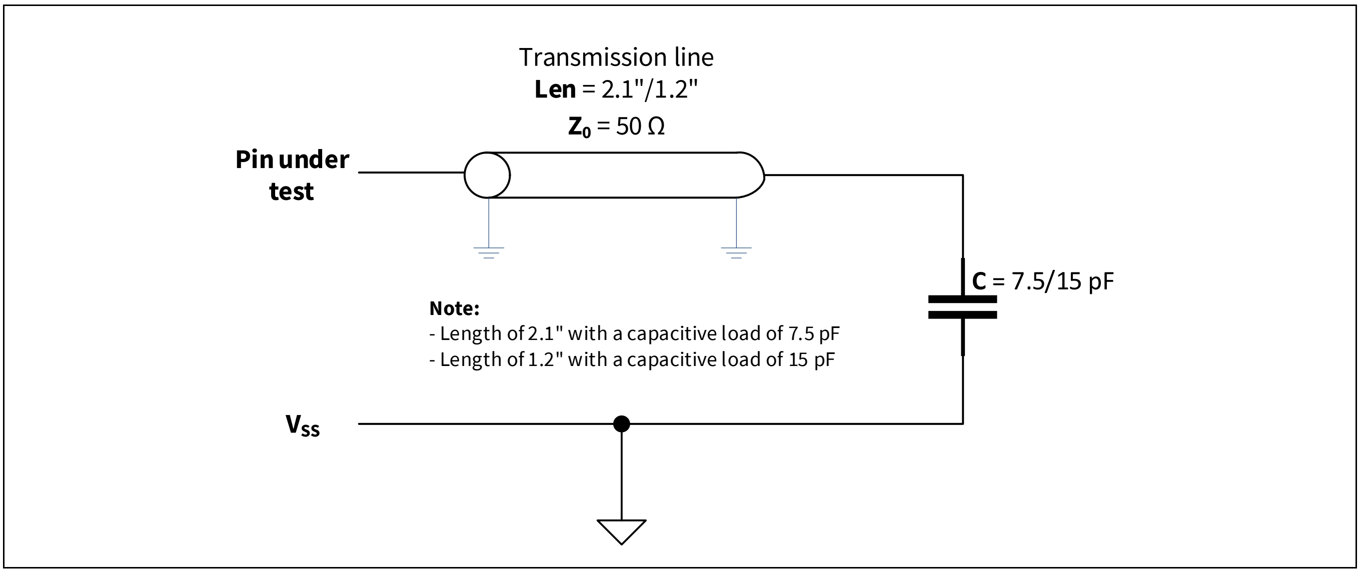
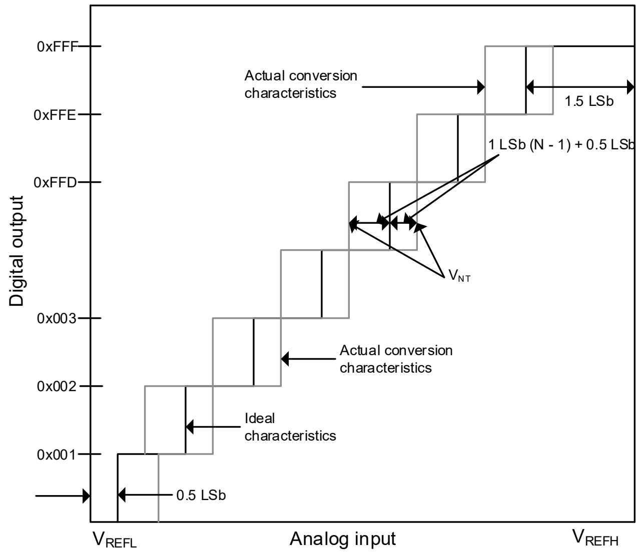


Figure 26-4 Test condition for overshoot, and undershoot

26.5 Analog peripherals

26.5.1 SAR ADC



Total error of digital output N = (V_{NT} {1 LSb × (N – 1) + 0.5 LSb}) / 1 LSb [LSb]

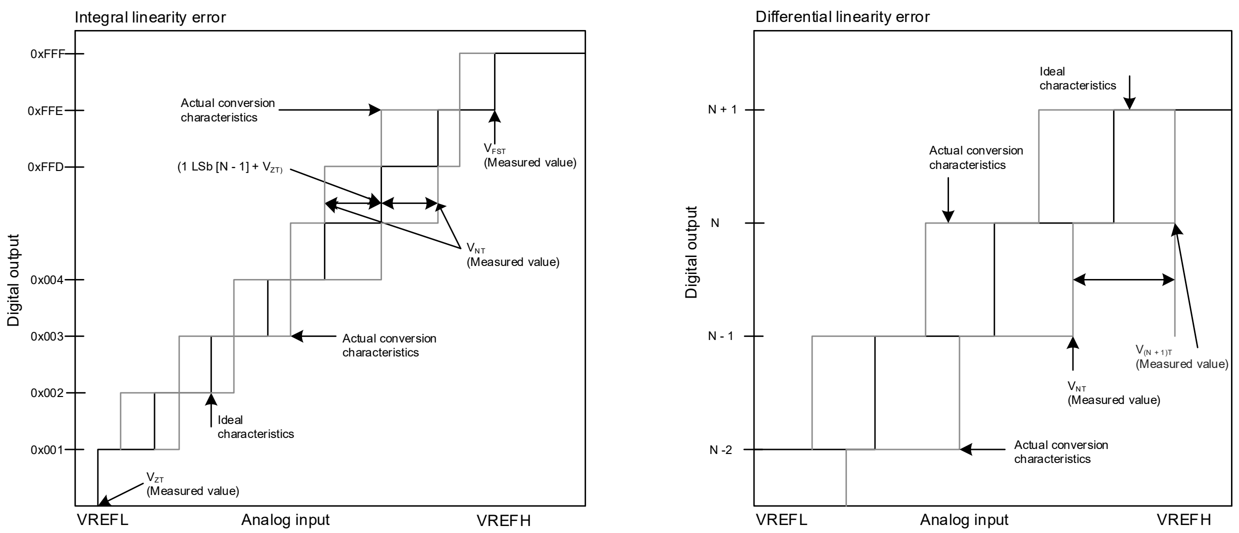
1 LSb (Ideal value) = (V_{REFH} – V_{REFL}) / 4096 [V]

N: A/D converter digital output value
V_{ZT} (Ideal value): V_{REFL} + 0.5 LSb [V]
V_{FST} (Ideal value): V_{REFH} – 1.5 LSb [V]
V_{NT}: Voltage at which the digital output changes from N – 1 to N

Figure 26-4 **ADC characteristics and error descriptions**

Table 26-6 **12-bit SAR ADC DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID100	A_RES	SAR ADC resolution	–	–	12	bits	
SID101	V_{A_INV}	Input voltage range	V_{REFL}	–	V_{REFH}	V	
SID102	V_{REFH}	SAR ADC HIGH reference voltage range	2.7	–	V_{DDA_ADC}	V	ADC performance degrades when high reference is higher than supply
SID103	V_{REFL}	SAR ADC LOW reference voltage range	V_{SSA_ADC}	–	V_{SSA_ADC}	V	ADC performance degrades when low reference is lower than ground
SID103A	V_{BAND_GAP}	Internal band gap reference voltage	0.882	0.9	0.918	V	



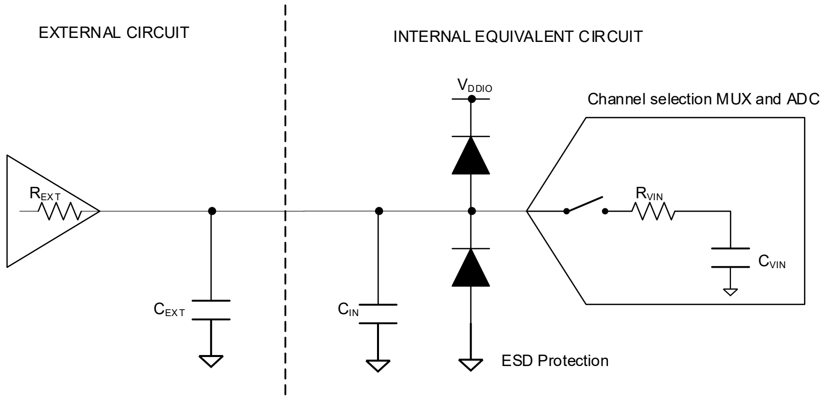
Integral linearity error of digital output N = $(V_{NT} - \{1\ LSb \times (N - 1) + V_{ZT}\}) / 1\ LSb$ [LSb]

Differential linearity error of digital output N = $(V_{(N+1)T} - V_{NT} - 1\ LSb) / 1\ LSb$ [LSb]

$1\ LSb = (V_{FST} - V_{ZT}) / 4094$ [V]

V_{ZT}: Voltage for which digital output changes from 0x000 to 0x001
V_{FST}: Voltage for which digital output changes from 0xFFE to 0xFFF.

Figure 26-5 Integral and differential linearity errors



R_{EXT}: Source impedance
C_{EXT}: On-PCB capacitance
C_{IN}: I/O pad or Input capacitance
R_{VIN}: ADC equivalent input resistance
C_{VIN}: ADC equivalent input capacitance
K: Constant for sampling accuracy, K = ln(abs(4096/LSb_{SAMPLE}))

Sampling Time (t_{SAMPLE}) requirement is shown in the following equation
$t_{SAMPLE} > K \times \{ C_{VIN} \times (R_{VIN} + R_{EXT}) + (C_{IN} + C_{EXT}) \times (R_{EXT}) \}$ [seconds]

K = 9.0" is recommended to get ±0.5 LSB sampling accuracy at 12-bit (LSb_{SAMPLE} = ±0.5)

Figure 26-6 ADC equivalent circuit for analog input

Table 26-7 SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID104	V_{ZT}	Zero transition voltage	–20	–	20	mV	V_{DDA_ADC} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C before offset adjustment
SID105	V_{FST}	Full-scale transition voltage	–20	–	20	mV	V_{DDA_ADC} = 2.7 V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C before offset adjustment
SID114	f_{ADC}	ADC operating frequency	2	–	26.67	MHz	
SID113	t_{S_4P5}	Analog input sample time (4.5 V ≤ V_{DDA_ADC}) for channels of SARMUX0	412	–	–	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113A	t_{S_2P7}	Analog input sample time (2.7 V ≤ V_{DDA_ADC}) for channels of SARMUX0	824	–	–	ns	SARMUX0 inputs are direct into the ADC Guaranteed by design
SID113B	$t_{S\_DR\_4P5}$	Analog input sample time when input is from diagnostic reference (4.5 V ≤ V_{DDA_ADC})	2	–	–	µs	Guaranteed by design
SID113C	$t_{S\_DR\_2P7}$	Analog input sample time when input is from diagnostic reference (2.7 V ≤ V_{DDA_ADC})	2.5	–	–	µs	Guaranteed by design
SID113D	t_{S_TS}	Analog input sample time for temperature sensor	7	–	–	µs	Guaranteed by design
SID106	t_{ST1}	Max throughput (sample per second) for channels of SARMUX0	–	–	1	Msps	4.5 V ≤ V_{DDA_ADC} ≤ 5.5 V, 80 MHz / 3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles
SID106A	t_{ST2}	Max throughput (sample per second) for channels of SARMUX0	–	–	0.5	Msps	2.7 V ≤ V_{DDA_ADC} < 4.5 V, 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID107	C_{VIN}	ADC input sampling capacitance	–	–	4.8	pF	Guaranteed by design
SID108	R_{VIN1}	Input path ON resistance (4.5 V to 5.5 V)	–	–	9.4	kΩ	Guaranteed by design
SID108A	R_{VIN2}	Input path ON resistance (2.7 V to 4.5 V)	–	–	13.9	kΩ	Guaranteed by design
SID108B	R_{DREF1}	Diagnostic path ON resistance (4.5 V to 5.5 V)	–	–	40	kΩ	Guaranteed by design
SID108C	R_{DREF2}	Diagnostic path ON resistance (2.7 V to 4.5 V)	–	–	50	kΩ	Guaranteed by design
SID119	ACC_RLAD	Diagnostic reference resistor ladder accuracy	–4	–	4	%	

Table 26-7 **SAR ADC AC specifications** *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID109	A_TE	Total error	–5	–	5	LSb	$V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, $V_{REFL} = V_{SSA\_ADC}$ –40 °C ≤ T_A ≤ 105 °C Total Error after offset and gain adjustment at 12-bit resolution mode
SID110	A_INL	Integral nonlinearity	–2.5	–	2.5	LSb	$V_{DDA\_ADC} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID111	A_DNL	Differential nonlinearity	–0.99	–	1.9	LSb	$V_{DDA\_ADC} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID112	A_GE	Measure the ADC output with input switching through all input channels of one ADC	–7	–	7	LSb	$V_{DDA\_ADC} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID115	I_{AIC}	Analog input leakage current (GPIO_STD)	–350	–	350	nA	When input pad is selected for conversion, $V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID115B	I_{AIC}	Analog input leakage current (GPIO_ENH)	–700	–	700	nA	When input pad is selected for conversion, $V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID115D	I_{AIC}	Analog input leakage current (GPIO_SMC)	–1075	–	1075	nA	When input pad is selected for conversion, $V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID115A	I_{AIC2}	Analog input leakage current (GPIO_STD)	–	–	165	nA	When input pad is not selected for conversion, $V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID115C	I_{AIC2}	Analog input leakage current (GPIO_ENH)	–	–	515	nA	When input pad is not selected for conversion, $V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID115E	I_{AIC2}	Analog input leakage current (GPIO_SMC)	–	–	1015	nA	When input pad is not selected for conversion, $V_{DDA\_ADC} = V_{REFH} = 2.7$ V to 5.5 V, –40 °C ≤ T_A ≤ 105 °C
SID116	$I_{DIAGREF}$	Diagnostic reference current	–	–	70	µA	
SID117	I_{VDDA}	Analog power supply current while ADC is operating	–	360	550	µA	Per enabled ADC, without diagnosis
SID117A	I_{VDDA_DS}	Analog power supply current while ADC is not operating	–	1	21	µA	Per enabled ADC
SID118	I_{VREF}	Analog reference voltage current while ADC is operating	–	360	550	µA	Per enabled ADC, without diagnosis

Table 26-7 SAR ADC AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID118A	I_{VREF_LEAK}	Analog reference voltage current while ADC is not operating	–	1.8	5	µA	Per enabled ADC
SID118B	$t_{S\_4P5\_1}$	Analog input sample time (4.5 V ≤ V_{DDA_ADC}) for channels of SARMUX1	824	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design
SID118C	$t_{S\_2P7\_1}$	Analog input sample time (2.7 V ≤ V_{DDA_ADC}) for channels of SARMUX1	1648	–	–	ns	Additional delay for SARMUX1 due to additional switches in the path to the ADC Guaranteed by Design
SID119A	t_{ST3}	Max throughput (sample per second) for channels of SARMUX1	–	–	0.5	Msps	4.5 V ≤ V_{DDA_ADC} ≤ 5.5 V, 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles
SID119B	t_{ST4}	Max throughput (sample per second) for channels of SARMUX1	–	–	0.25	Msps	2.7 V ≤ V_{DDA_ADC} < 4.5 V, 80 MHz / 12 = 6.67 MHz, 11 sampling cycles, 15 conversion cycles

Table 26-8 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID201	$T_{SENSACC\_TR}$	Temperature sensor accuracy trimmed	–5	–	5	°C	This spec is valid for the following two conditions: 1. 3.0 V ≤ V_{DDA_ADC}=V_{REFH} ≤ 3.6 V and 3.0 V ≤ V_{DDD} ≤ 3.6 V 2. 4.5 V ≤ V_{DDA_ADC}=V_{REFH} ≤ 5.5 V and 4.5 V ≤ V_{DDD} ≤ 5.5 V (Calibrated accuracy by factory trimming)
SID202	$T_{SENSACC\_STD}$	Temperature sensor accuracy standard	–10	–	10	°C	This spec applies to all valid combinations for V_{DDA_ADC} = V_{REFH} and V_{DDD}, which are not covered by SID201 (Uncalibrated accuracy)

26.6 AC specifications

Unless otherwise noted, the timings are defined with the guidelines mentioned in the **Figure 26-7**.

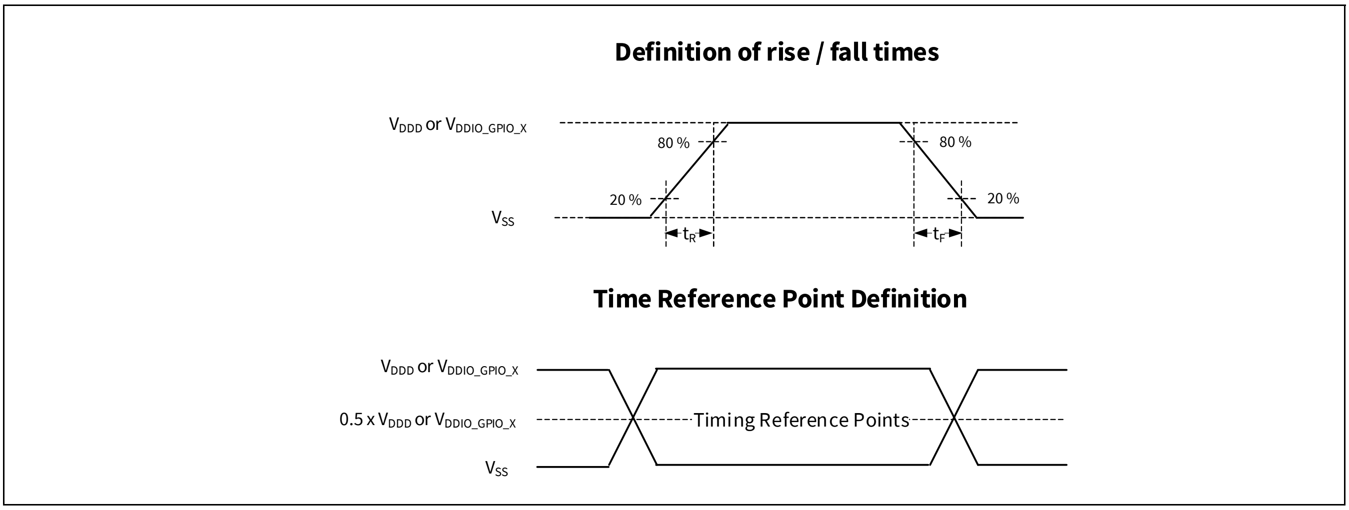


Figure 26-7 AC timings specifications

26.7 Digital peripherals

Table 26-9 Timer/counter/PWM (TCPWM) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID120	f_C	TCPWM operating frequency	–	–	100	MHz	f_C = peripheral clock
SID121	$t_{PWMENEXT}$	Input trigger pulse width for all trigger events	2 / f_C	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID122	t_{PWMEXT}	Output trigger pulse widths	2 / f_C	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID123	t_{CRES}	Resolution of counter	1 / f_C	–	–	ns	Minimum time between successive counts
SID124	t_{PWMRES}	PWM resolution	1 / f_C	–	–	ns	Minimum pulse width of PWM output
SID125	t_{QRES}	Quadrature inputs resolution	2 / f_C	–	–	ns	Minimum pulse width between Quadrature phase inputs.

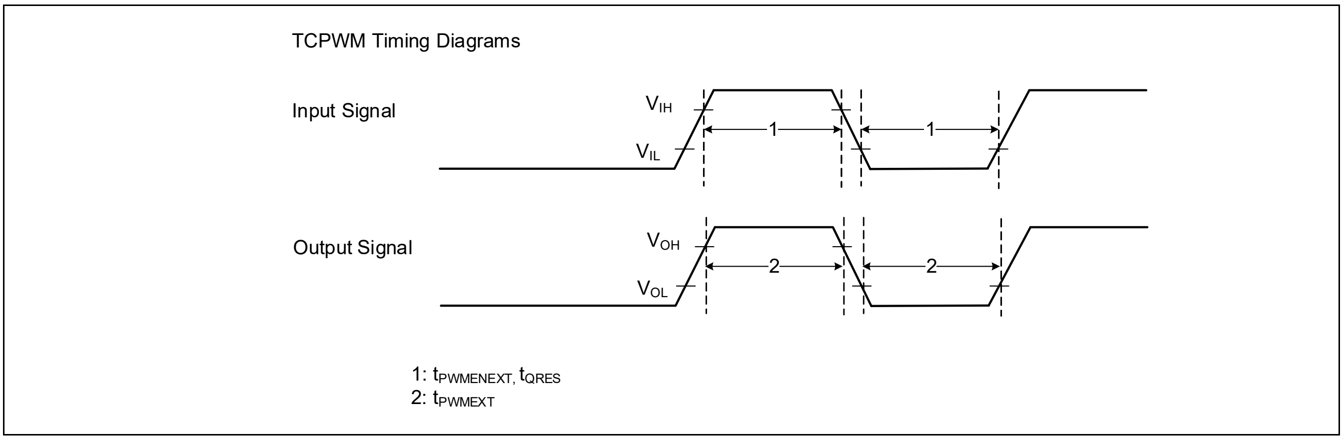


Figure 26-8 TCPWM timing diagrams

Table 26-10 Serial Communication Block (SCB) specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID129	f_{SCB}	SCB operating frequency	–	–	100	MHz	
SID129_2	t_{SPI_TRANS}	SCB transition in SPI mode	–	–	4	ns	
I^2C Interface-Standard-mode							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> =0b100, CFG_SLEW_EXT/SLEW<2:0> =0b000 (**Note**: SID138 is not valid for *HSIO_STDLN*)							
SID130	f_{SCL}	SCL clock frequency	–	–	100	kHz	
SID131	$t_{HD;STA}$	Hold time, START condition	4000	–	–	ns	
SID132	t_{LOW}	Low period of SCL	4700	–	–	ns	
SID133	t_{HIGH}	High period of SCL	4000	–	–	ns	
SID134	$t_{SU;STA}$	Setup time for a repeated START	4700	–	–	ns	
SID135	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	
SID136	$t_{SU;DAT}$	Data setup time	250	–	–	ns	
SID138	t_F	Fall time of SCL and SDA	–	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC, GPIO_STD
SID139	$t_{SU;STO}$	Setup time for STOP	4000	–	–	ns	
SID140	t_{BUF}	Bus-free time between START and STOP	4700	–	–	ns	
SID141	C_B	Capacitive load for each bus line	–	–	400	pF	
SID142	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	3450	ns	
SID143	$t_{VD;ACK}$	Data valid acknowledge time	–	–	3450	ns	

Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
I^{2}C Interface-Fast-mode							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> =0b100, CFG_SLEW_EXT/SLEW<2:0> =0b000 (**Note**: SID158 is not valid for *GPIO_STD, HSIO_STDLN*)							
SID150	f_{SCL}	SCL clock frequency	–	–	400[71]	kHz	
SID151	$t_{HD;STA}$	Hold time, START condition	600	–	–	ns	
SID152	t_{LOW}	Low period of SCL	1300	–	–	ns	
SID153	t_{HIGH}	High period of SCL	600	–	–	ns	
SID154	$t_{SU;STA}$	Setup time for a repeated START	600	–	–	ns	
SID155	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	
SID156	$t_{SU;DAT}$	Data setup time	100	–	–	ns	
SID158	t_F	Fall time of SCL and SDA	20 × (V_{DDIO_GPIO} /5.5)	–	300	ns	Input and output Output: Only valid for GPIO_ENH, GPIO_SMC
SID159	$t_{SU;STO}$	Setup time for STOP	600	–	–	ns	
SID160	t_{BUF}	Bus free time between START and STOP	1300	–	–	ns	
SID161	C_B	Capacitive load for each bus line	–	–	400	pF	
SID162	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	900	ns	
SID163	$t_{VD;ACK}$	Data valid acknowledge time	–	–	900	ns	
SID164	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
I^{2}C Interface-Fast-Plus mode							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b1 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> = 0b100, CFG_OUT/SLOW<0:0> = 0b0 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG/DRIVE_MODE<2:0> =0b100, CFG_SLEW_EXT/SLEW<2:0> =0b000 (**Note**: SID178 is not valid for *GPIO_STD, GPIO_SMC, and HSIO_STDLN*)							
SID170	f_{SCL}	SCL clock frequency	–	–	1[72]	MHz	
SID171	$t_{HD;STA}$	Hold time, START condition	260	–	–	ns	
SID172	t_{LOW}	Low period of SCL	500	–	–	ns	
SID173	t_{HIGH}	High period of SCL	260	–	–	ns	
SID174	$t_{SU;STA}$	Setup time for a repeated START	260	–	–	ns	
SID175	$t_{HD;DAT}$	Data hold time, for receiver	0	–	–	ns	

Notes

71.In order to drive full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL}.

72.In order to drive full bus load at 1 MHz, 20 mA I_{OL} is required at 0.4 V V_{OL}.

Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID176	$t_{SU;DAT}$	Data setup time	50	–	–	ns	
SID178	t_F	Fall time of SCL and SDA	20 × (V_{DDIO_GPIO} /5.5)	–	160	ns	Input and output, 20pF load Output: Only for GPIO_ENH
SID179	$t_{SU;STO}$	Setup time for STOP	260	–	–	ns	
SID180	t_{BUF}	Bus free time between START and STOP	500	–	–	ns	
SID181	C_B	Capacitive load for each bus line	–	–	20	pF	
SID182	$t_{VD;DAT}$	Time for data signal from SCL LOW to SDA output	–	–	450	ns	
SID183	$t_{VD;ACK}$	Data valid acknowledge time	–	–	450	ns	
SID184	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns	
SPI Interface							
Recommended I/O Configuration: (Applicable to all below SPI modes) **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> =0b000 **For SPI speeds ≤ 12.5 MHz** **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0							
SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, GPIO)							
SID190	f_{SPI}	SPI operating frequency	–	–	12.5	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID191	t_{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID192	t_{DSI}	SPI Master: MISO valid before SCLK capturing edge	40	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID193	t_{HMO}	SPI Master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID194	$t_{W\_SCLK\_H\_L}$	SPI SCLK pulse width HIGH or LOW	0.4 × ($1/f_{SPI}$)	0.5 × ($1/f_{SPI}$)	0.6 × ($1/f_{SPI}$)	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID195	t_{VSS}	SPI Master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC

Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID196	t_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 12.5 Mbps for instances on GPIO_STD, GPIO_ENH, GPIO_SMC
SID198	t_{EN_SETUP}	SSEL valid, before the first SCLK capturing edge	0.5 × (1/f_{SPI})	–	–	ns	Min is half clock period
SID199	t_{EN_SHOLD}	SSEL hold, after the last SCLK capturing edge	0.5 × (1/f_{SPI})	–	–	ns	Min is half clock period
SID197	C_{SPIM_MS}	SPI Capacitive Load	–	–	20	pF	
SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1, HSIO)							
SID190A	f_{SPI}	SPI operating frequency	–	–	20	MHz	Do not use half-clock mode: LATE_MISO_SAMPLE = 0 SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) - 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz. for instances on HSIO_STD
SID191A	t_{DMO}	SPI Master: MOSI valid after SCLK driving edge	–	–	9	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STD
SID192A	t_{DSI}	SPI Master: MISO valid before SCLK capturing edge	25	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STD
SID193A	t_{HMO}	SPI Master: Previous MOSI data hold time	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STD
SID194A	$t_{W\_SCLK\_H\_L}$	SPI SCLK pulse width HIGH or LOW	0.4 × (1/f_{SPI})	0.5 × (1/f_{SPI})	0.6 × (1/f_{SPI})	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STD
SID195A	t_{VSS}	SPI Master: MOSI valid after SSEL falling edge (CPHA=0)	–	–	12	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STD
SID196A	t_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns	SPI Master (Full-clock mode: LATE_MISO_SAMPLE = 1) – 20 Mbps For 20 Mbps, SCB operating frequency (f_{SCB}) must be configured to 80 MHz for instances on HSIO_STD
SID197A	C_{SPIM_MS}	SPI Capacitive Load	–	–	20	pF	

Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID198A	t_{EN_SETUP}	SSEL valid, before the first SCLK capturing edge	0.5 × (1/f_{SPI})	–	–	ns	Min is half clock period
SID199A	t_{EN_SHOLD}	SSEL hold, after the last SCLK capturing edge	0.5 × (1/f_{SPI})	–	–	ns	Min is half clock period
SPI Interface Slave (internally clocked, GPIO and HSIO)							
SID205	f_{SPI_INT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, internally clocked
SID206	t_{DMI_INT}	SPI Slave: MOSI Valid before SCLK capturing edge	5	–	–	ns	SPI Slave, internally clocked
SID207	t_{DSO_INT}	SPI Slave: MISO Valid after SCLK driving edge, in the internal-clocked mode	–	–	60	ns	SPI Slave, internally clocked
SID208	t_{HSO_INT}	SPI Slave: Previous MISO data hold time	3	–	–	ns	SPI Slave, internally clocked
SID209	$t_{EN\_SETUP\_INT}$	SPI Slave: SSEL valid to first SCLK valid edge	33	–	–	ns	SPI Slave, internally clocked
SID210	$t_{EN\_HOLD\_INT}$	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI Slave, internally clocked
SID211	$t_{EN\_SETUP\_PRE}$	SPI Slave: from SSEL valid, to SCLK falling edge before the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID212	$t_{EN\_HOLD\_PRE}$	SPI Slave: from SCLK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID213	$t_{EN\_SETUP\_CO}$	SPI Slave: from SSEL valid, to SCLK falling edge in the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID214	$t_{EN\_HOLD\_CO}$	SPI Slave: from SCLK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID215	$t_{W\_DIS\_INT}$	SPI Slave Select inactive time	40	–	–	ns	SPI Slave, internally clocked
SID216	$t_{W\_SCLKH\_INT}$	SPI SCLK pulse width HIGH	32	–	–	ns	SPI Slave, internally clocked
SID217	$t_{W\_SCLKL\_INT}$	SPI SCLK pulse width LOW	32	–	–	ns	SPI Slave, internally clocked
SID218	t_{SIH_INT}	SPI MOSI hold from SCLK	20	–	–	ns	SPI Slave, internally clocked
SID219	C_{SPIS_INT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, internally clocked
SPI Interface Slave (externally clocked, GPIO and HSIO)							
SID220	f_{SPI_EXT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, externally clocked: 12.5 Mbps
SID221	t_{DMI_EXT}	SPI Slave: MOSI Valid before SCLK capturing edge	8	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID222	t_{DSO_EXT}	SPI Slave: MISO Valid after SCLK driving edge, in the external-clocked mode	–	–	30	ns	SPI Slave, externally clocked: 12.5 Mbps
SID223	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID224	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCLK valid edge	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps

Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

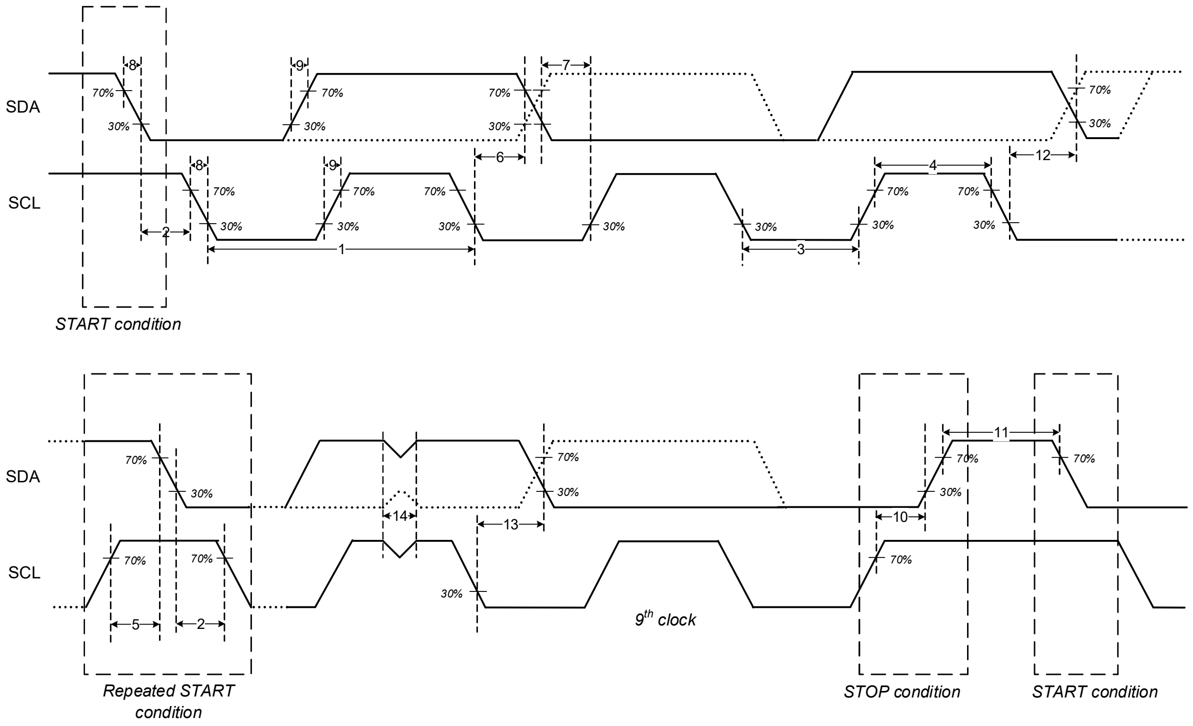
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID225	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID226	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID227	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	32	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID228	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	32	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID229	t_{SIH_EXT}	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID230	C_{SPIS_EXT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 12.5 Mbps
SID231	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns	SPI Slave, externally clocked: 12.5 Mbps
SPI Interface Slave (internally clocked, SMC I/O)							
SID205_2	f_{SPI_INT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, internally clocked
SID206_2	t_{DMI_INT}	SPI Slave: MOSI Valid before SCLK capturing edge	5	–	–	ns	SPI Slave, internally clocked
SID207_2	t_{DSO_INT}	SPI Slave: MISO Valid after SCLK driving edge, in the internal-clocked mode	–	–	64	ns	SPI Slave, internally clocked
SID208_2	t_{HSO_INT}	SPI Slave: Previous MISO data hold time	3	–	–	ns	SPI Slave, internally clocked
SID209_2	$t_{EN\_SETUP\_INT}$	SPI Slave: SSEL valid to first SCLK valid edge	33	–	–	ns	SPI Slave, internally clocked
SID210_2	$t_{EN\_HOLD\_INT}$	SPI Slave Select active (LOW) from last SCLK hold	33	–	–	ns	SPI Slave, internally clocked
SID211_2	$t_{EN\_SETUP\_PRE}$	SPI Slave: from SSEL valid, to SCLK falling edge before the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID212_2	$t_{EN\_HOLD\_PRE}$	SPI Slave: from SCLK falling edge before the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID213_2	$t_{EN\_SETUP\_CO}$	SPI Slave: from SSEL valid, to SCLK falling edge in the first data bit	20	–	–	ns	SPI Slave, internally clocked
SID214_2	$t_{EN\_HOLD\_CO}$	SPI Slave: from SCLK falling edge in the first data bit, to SSEL invalid	20	–	–	ns	SPI Slave, internally clocked
SID215_2	$t_{W\_DIS\_INT}$	SPI Slave Select inactive time	40	–	–	ns	SPI Slave, internally clocked
SID216_2	$t_{W\_SCLKH\_INT}$	SPI SCLK pulse width HIGH	36	–	–	ns	SPI Slave, internally clocked
SID217_2	$t_{W\_SCLKL\_INT}$	SPI SCLK pulse width LOW	36	–	–	ns	SPI Slave, internally clocked
SID218_2	t_{SIH_INT}	SPI MOSI hold from SCLK	20	–	–	ns	SPI Slave, internally clocked
SID219_2	C_{SPIS_INT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, internally clocked
SPI Interface Slave (externally clocked, SMC I/O)							
SID220_2	f_{SPI_EXT}	SPI operating frequency	–	–	12.5	MHz	SPI Slave, externally clocked: 12.5 Mbps

Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID221_2	t_{DMI_EXT}	SPI Slave: MOSI Valid before SCLK capturing edge	8	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID222_2	t_{DSO_EXT}	SPI Slave: MISO Valid after SCLK driving edge, in the external-clocked mode	–	–	34	ns	SPI Slave, externally clocked: 12.5 Mbps
SID223_2	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID224_2	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCLK valid edge	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID225_2	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID226_2	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID227_2	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	36	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID228_2	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	36	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID229_2	t_{SIH_EXT}	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 12.5 Mbps
SID230_2	C_{SPIS_EXT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 12.5 Mbps
SID231_2	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	37	ns	SPI Slave, externally clocked: 12.5 Mbps
SPI Interface Slave (externally clocked, 20 MHz)							
SID220A	f_{SPI_EXT}	SPI operating frequency	–	–	20	MHz	SPI Slave, externally clocked: 20 Mbps
SID221A	t_{DMI_EXT}	SPI Slave: MOSI Valid before SCLK capturing edge	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID222A	t_{DSO_EXT}	SPI Slave: MISO Valid after SCLK driving edge, in the external-clocked mode	–	–	18	ns	SPI Slave, externally clocked: 20 Mbps
SID223A	t_{HSO_EXT}	SPI Slave: Previous MISO data hold time	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID224A	$t_{EN\_SETUP\_EXT}$	SPI Slave: SSEL valid to first SCLK valid edge	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID225A	$t_{EN\_HOLD\_EXT}$	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID226A	$t_{W\_DIS\_EXT}$	SPI Slave Select inactive time	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID227A	$t_{W\_SCLKH\_EXT}$	SPI SCLK pulse width HIGH	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID228A	$t_{W\_SCLKL\_EXT}$	SPI SCLK pulse width LOW	20	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID229A	t_{SIH_EXT}	SPI MOSI hold from SCLK	5	–	–	ns	SPI Slave, externally clocked: 20 Mbps
SID230A	C_{SPIS_EXT}	SPI Capacitive Load	–	–	20	pF	SPI Slave, externally clocked: 20 Mbps
SID231A	t_{VSS_EXT}	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	23	ns	SPI Slave, externally clocked: 20 Mbps

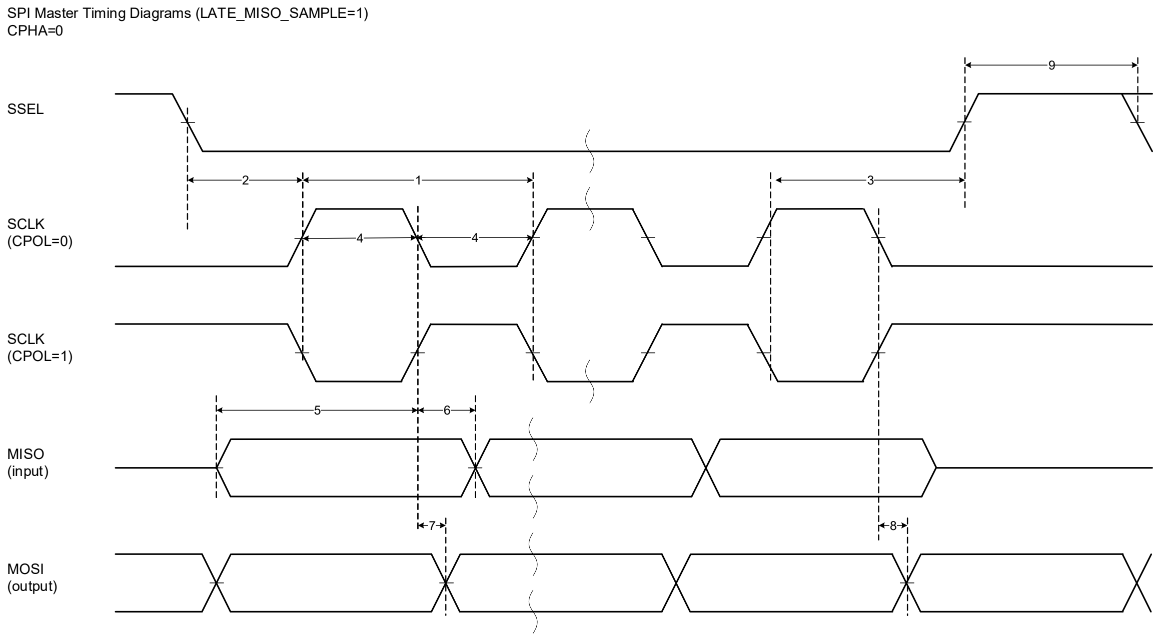
Table 26-10 Serial Communication Block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
UART Interface							
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0 **GPIO_ENH**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_OUT/SLOW<0:0> = 0b0 **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0, CFG_SLEW_EXT/SLEW<2:0> =0b000							
SID240	f_{BPS}	Signaling rate	–	–	10	Mbps	
SID240B	f_{BPS_TX}	Signaling rate for TX on P15.3 for SCB#1 and P18.5 for SCB#4	–	–	25	Mbps	Valid only for TX at 20 pF load
SID241B	f_{ACC}	Frequency accuracy of TX bit time on P15.3 for SCB#1 and P18.5 for SCB#4	–0.5	–	0.5	ns	With PLL, 200 MHz ≤ f_{VCO} ≤ 400 MHz at 20 pF load
SID242B	f_{JIT}	Jitter of TX on P15.3 for SCB#1 and P18.5 for SCB#4	–4.5	–	4.5	ns	at 20 pF load



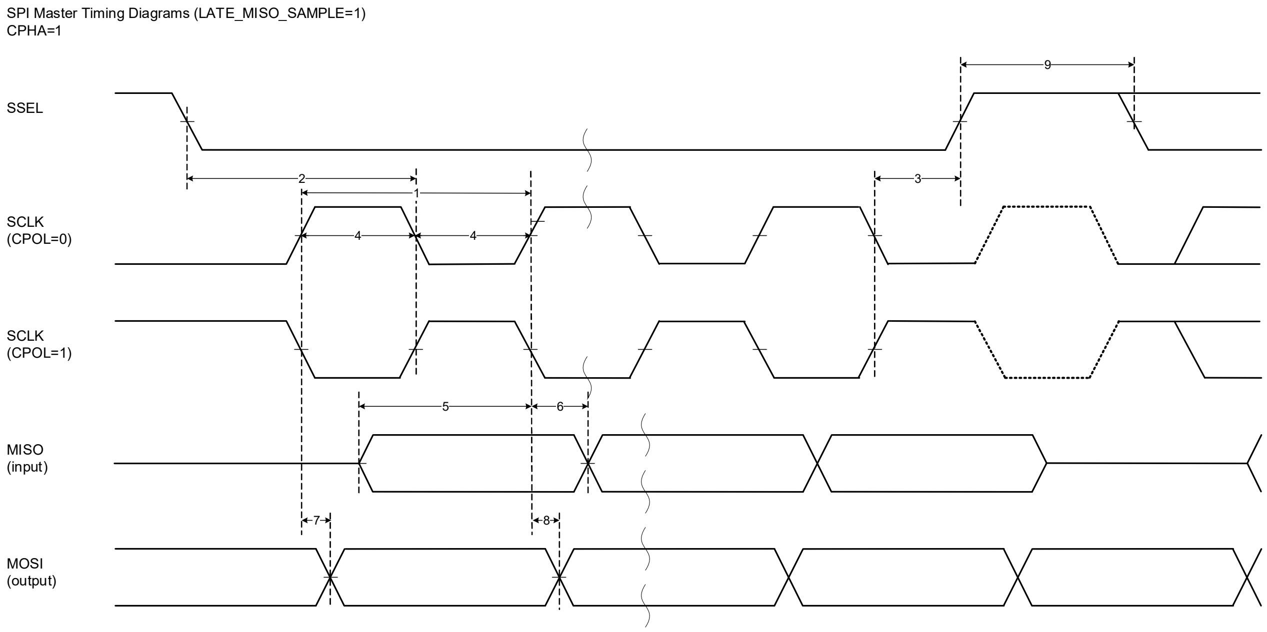
1: SCL clock period = $1/f_{SCL}$
2: Hold time, START condition = $t_{HD;STA}$
3: LOW period of SCL = t_{LOW}
4: HIGH period of SCL = t_{HIGH}
5: Setup time for a repeated START = $t_{SU;STA}$
6: Data hold time, for receiver = $t_{HD;DAT}$
7: Data setup time = $t_{SU;DAT}$
8: Fall time of SCL and SDA = t_F
9: Rise time of SCL and SDA = t_R
10: Setup time for STOP = $t_{SU;STO}$
11: Bus-free time between START and STOP = t_{BUF}
12: Time for data signal from SCL LOW to SDA output = $t_{VD;DAT}$
13: Data valid acknowledge time = $t_{VD;ACK}$
14: Pulse width of spikes that must be suppressed by the input filter = t_{SP}

Figure 26-9 I^2C timing diagrams



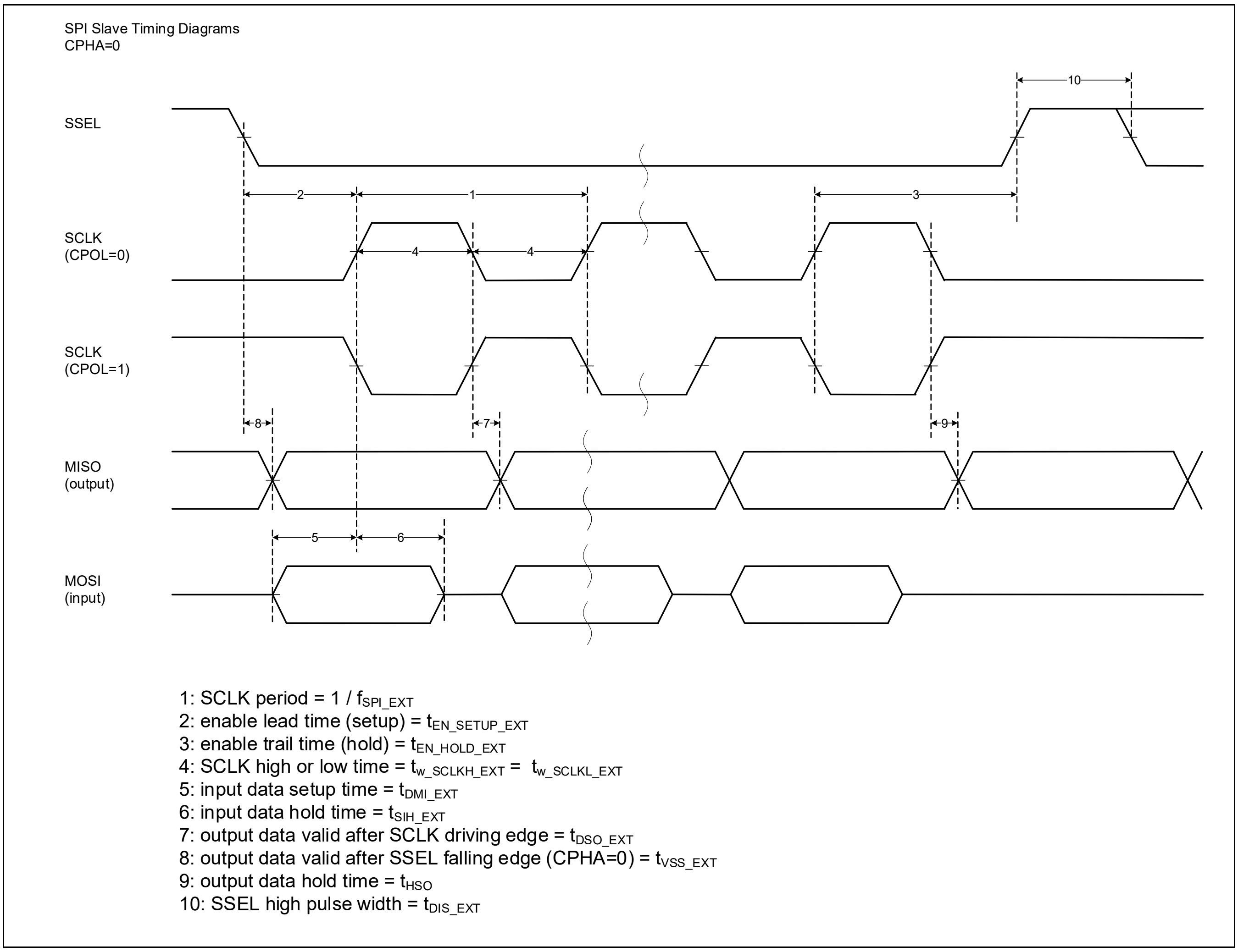
1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{DHI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data hold time = t_{HMO}
9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

Figure 26-10 SPI master timing diagrams with LOW clock phase



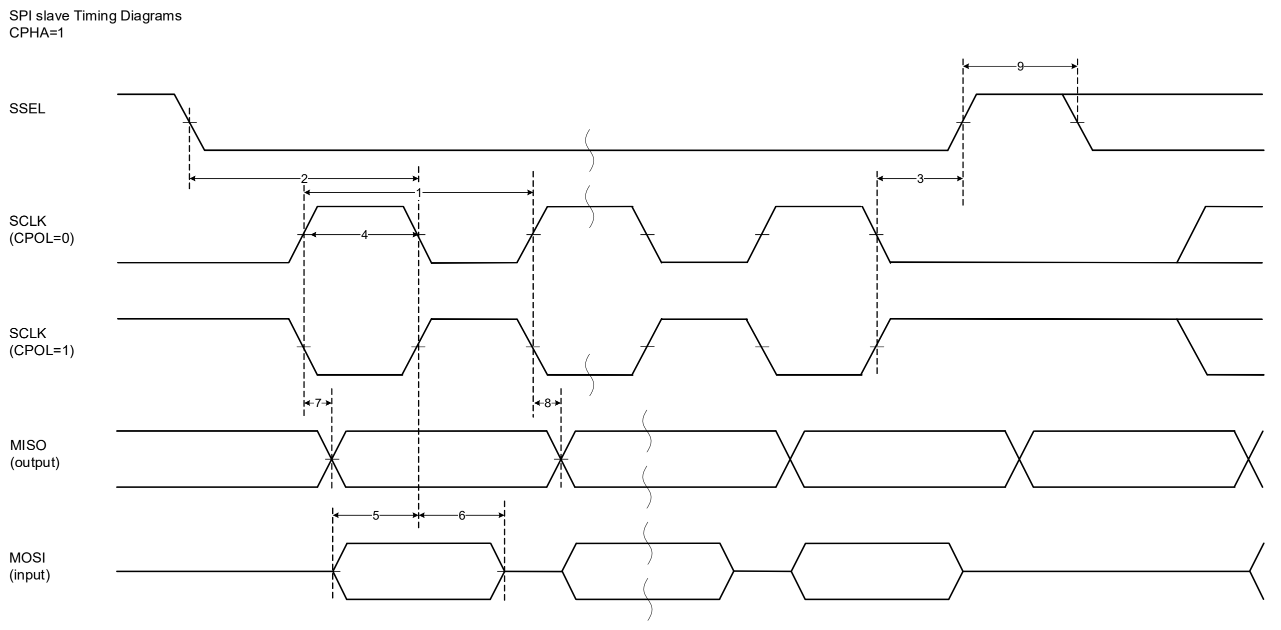
1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL (Refer to the Register TRM)
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL (Refer to the Register TRM)
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{HDI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data hold time = t_{HMO}
9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL (Refer to the Register TRM)

Figure 26-11 SPI master timing diagrams with HIGH clock phase



1: SCLK period = 1 / f_{SPI_EXT}
2: enable lead time (setup) = $t_{EN\_SETUP\_EXT}$
3: enable trail time (hold) = $t_{EN\_HOLD\_EXT}$
4: SCLK high or low time = $t_{w\_SCLKH\_EXT}$ = $t_{w\_SCLKL\_EXT}$
5: input data setup time = t_{DMI_EXT}
6: input data hold time = t_{SIH_EXT}
7: output data valid after SCLK driving edge = t_{DSO_EXT}
8: output data valid after SSEL falling edge (CPHA=0) = t_{VSS_EXT}
9: output data hold time = t_{HSO}
10: SSEL high pulse width = t_{DIS_EXT}

Figure 26-12 SPI slave timing diagrams with LOW clock phase



1: SCLK period = 1 / f_{SPI_EXT}
2: enable lead time (setup) = $t_{EN\_SETUP\_EXT}$
3: enable trail time (hold) = $t_{EN\_HOLD\_EXT}$
4: SCLK high or low time = $t_{w\_SCLKH\_EXT}$ = $t_{w\_SCLKL\_EXT}$
5: input data setup time = t_{DMI_EXT}
6: input data hold time = t_{SIH_EXT}
7: output data valid after SCLK driving edge = t_{DSO_EXT}
8: output data hold time = t_{HSO}
9: SSEL high pulse width = t_{DIS_EXT}

Figure 26-13 SPI slave timing diagrams with HIGH clock phase

Table 26-11 CAN FD specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID630	f_{HCLK}	System clock (HCLK) frequency	–	–	100	MHz	$f_{CCLK} \leq f_{HCLK}$, guaranteed by design
SID631	f_{CCLK}	CAN clock (CCLK) frequency	–	–	100	MHz	$f_{CCLK} \leq f_{HCLK}$, guaranteed by design

Table 26-12 LIN specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID249	f_{LIN}	Internal clock frequency to the LIN block	–	–	100	MHz	
SID250	BR_NOM	Bit rate on the LIN bus	1	–	20	kbps	Guaranteed by design
SID250A	BR_REF	Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode	1	–	115.2	kbps	Guaranteed by design

26.8 Memory

Table 26-13 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257A	V_{PE}	Erase and program voltage	2.7	–	5.5	V	

Table 26-14 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID257	f_{FO}	Maximum operation frequency	–	–	100	MHz	Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 320 MHz
SID254	t_{ERS_SUS}	Maximum time from erase suspend command till erase is indeed suspend	–	–	37.5	µs	
SID255	$t_{ERS\_RES\_SUS}$	Minimum time allowed from erase resume to erase suspend	250	–	–	µs	Guaranteed by design
SID258	t_{BC_WF}	Blank Check time for Work Flash N-byte	–	–	10 + 0.3 × N	µs	At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time
SID258A	$t_{AA\_BC\_ENTRY}$	Time to enter Blank Check mode	–	5	–	µs	
SID258B	$t_{AA\_BC\_EXIT}$	Time to exit Blank Check mode	–	5	–	µs	
SID259	$t_{SECTORERASE1}$	Sector erase time (code-flash: 32 KB)	–	45	90	ms	Includes internal preprogramming time
SID260	$t_{SECTORERASE2}$	Sector erase time (code-flash: 8 KB)	–	15	30	ms	Includes internal preprogramming time
SID261	$t_{SECTORERASE3}$	Sector erase time (work-flash, 2 KB)	–	80	160	ms	Includes internal preprogramming time

Table 26-14 Flash AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID262	$t_{SECTORERASE4}$	Sector erase time (work-flash, 128 B)	–	5	15	ms	Includes internal preprogramming time
SID263	t_{WRITE1}	64-bit write time (code-flash)	–	30	60	µs	Excludes system overhead time
SID264	t_{WRITE2}	256-bit write time (code-flash)	–	40	70	µs	Excludes system overhead time
SID265	t_{WRITE3}	4096-bit write time (code-flash)	–	320	1200	µs	Excludes system overhead time
SID266	t_{WRITE4}	32-bit write time (work-flash)	–	30	60	µs	Excludes system overhead time
SID267	t_{FRET1}	Code-flash retention. 1000 program/erase cycles	20	–	–	years	Temperature at write/erase time. $T_A \leq +85°C$ average
SID182T1	t_{FRET2}	Code-flash retention. 100 program/erase cycles	50	–	–	years	Temperature at write/erase time. $T_A \leq +30°C$ average
SID268	t_{FRET3}	Work-flash retention. 125,000 program/erase cycles	20	–	–	years	Temperature at write/erase time. $T_A \leq +85°C$ average
SID269	t_{FRET4}	Work-flash retention. 250,000 program/erase cycles	10	–	–	years	Temperature at write/erase time. $T_A \leq +85°C$ average
SID182T2	t_{FRET5}	Work-flash retention. 1000 program/erase cycles	50	–	–	years	Temperature at write/erase time. $T_A \leq +30°C$ average
SID612	I_{CC_ACT2}	Program operating current (code or work-flash)	–	15	62	mA	V_{DDD} = 5 V, V_{CCD} = 1.1 V Guaranteed by design
SID613	I_{CC_ACT3}	Erase operating current (code- or work-flash)	–	15	62	mA	V_{DDD} = 5 V, V_{CCD} = 1.1 V Guaranteed by design

26.9 System resources

Table 26-15 System resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
Power-on reset specifications							
SID270	V_{POR_R}	POR rising trip voltage	1.5	–	2.35	V	Guaranteed by design
SID276	V_{POR_F}	POR falling trip voltage	1.45	–	2.1	V	
SID271	V_{POR_H}	Level detection hysteresis	20	–	300	mV	
SID272	t_{DLY_POR}	Delay between V_{DDD} rising through 2.3 V and POR reset output rising through V_{DDD} / 2	–	–	3	µs	Guaranteed by design
SID273	t_{POFF}	Power off time	350	–	–	µs	V_{DDD} < 1.45 V Does not apply to SID274A and SID274B
SID274A	POR_RR1	V_{DDD} power ramp rate with robust BOD - XRES_L asserted (BOD operation is guaranteed)	–	–	100	mV/µs	Applies to ramp up and ramp down
SID274B	POR_RR1	V_{DDD} power ramp rate with robust BOD - XRES_L de-asserted (BOD operation is guaranteed)	1	–	100	mV/µs	Applies to ramp up and ramp down
SID275	POR_RR2	V_{DDD} power ramp rate without robust BOD	100	–	1000	mV/µs	This ramp does not support robust BOD t_{POFF} must be satisfied. Applies to ramp up and ramp down
High-voltage BOD (HV BOD) specifications							
SID500	$V_{TR\_2P7\_R}$	HV BOD 2.7 V trimmed rising trip point for V_{DDD} and V_{DDA_ADC} (default)	2.474	2.55	2.627	V	
SID501	$V_{TR\_2P7\_F}$	HV BOD 2.7 V trimmed falling trip point for V_{DDD} and V_{DDA_ADC} (default)	2.449	2.525	2.601	V	
SID502	$V_{TR\_3P0\_R}$	HV BOD 3.0 V trimmed rising trip point for V_{DDD} and V_{DDA_ADC}	2.765	2.85	2.936	V	
SID503	$V_{TR\_3P0\_F}$	HV BOD 3.0 V trimmed falling trip point for V_{DDD} and V_{DDA_ADC}	2.74	2.825	2.91	V	
SID505	HVBOD_RR_A	Power ramp rate: V_{DDD} and V_{DDA_ADC} (Active)	–	–	100	mV/µs	
SID506	HVBOD_RR_DS	Power ramp rate: V_{DDD} and V_{DDA_ADC} (DeepSleep)	–	–	10	mV/µs	
SID507	$t_{DLY\_ACT\_HVBOD}$	Active mode delay between V_{DDD} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and an internal HV BOD output transitioning through V_{DDD} / 2	–	–	0.5	µs	Guaranteed by design
SID507A	$t_{DLY\_ACT\_HVBOD\_A}$	Active mode delay between V_{DDA_ADC} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and internal HV BOD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID507B	$t_{DLY\_DS\_HVBOD}$	DeepSleep mode delay between V_{DDD}/V_{DDA_ADC} falling/rising through $V_{TR\_2P7\_F/R}$ or $V_{TR\_3P0\_F/R}$ and an internal HV BOD output transitioning through V_{DDD} /2	–	–	4	µs	Guaranteed by design

Table 26-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID508	t_{RES_HVBOD}	Response time of HV BOD, V_{DDD}/V_{DDA_ADC} supply. HV BOD guaranteed to generate pulse for V_{DDD}/V_{DDA_ADC} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below $V_{TR\_2P7\_F}$ or $V_{TR\_3P0\_F}$)	100	–	–	ns	Guaranteed by design
Low-voltage BOD (LV BOD) specifications							
SID510	$V_{TR\_R\_LVBOD}$	LV BOD trimmed rising trip point for V_{CCD}	0.917	0.945	0.973	V	
SID511	$V_{TR\_F\_LVBOD}$	LV BOD trimmed falling trip point for V_{CCD}	0.892	0.92	0.948	V	
SID515	$t_{DLY\_ACT\_LVBOD}$	Active delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID515A	$t_{DLY\_DS\_LVBOD}$	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD output transitioning through V_{DDD} / 2	–	–	12	µs	Guaranteed by design
SID516	t_{RES_LVBOD}	Response time of LV BOD. LV BOD guaranteed to generate pulse for V_{CCD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below $V_{TR\_F\_LVBOD}$)	100	–	–	ns	Guaranteed by design
Low-voltage detector (LVD) DC specifications							
SID520	$V_{TR\_2P8\_F}$	LVD 2.8 V trimmed falling trip point for V_{DDD}	Typ – 4%	2800	Typ + 4%	mV	
SID521	$V_{TR\_2P9\_F}$	LVD 2.9 V trimmed falling trip point for V_{DDD}	Typ – 4%	2900	Typ + 4%	mV	
SID522	$V_{TR\_3P0\_F}$	LVD 3.0 V trimmed falling trip point for V_{DDD}	Typ – 4%	3000	Typ + 4%	mV	
SID523	$V_{TR\_3P1\_F}$	LVD 3.1 V trimmed falling trip point for V_{DDD}	Typ – 4%	3100	Typ + 4%	mV	
SID524	$V_{TR\_3P2\_F}$	LVD 3.2 V trimmed falling trip point for V_{DDD}	Typ – 4%	3200	Typ + 4%	mV	
SID525	$V_{TR\_3P3\_F}$	LVD 3.3 V trimmed falling trip point for V_{DDD}	Typ – 4%	3300	Typ + 4%	mV	
SID526	$V_{TR\_3P4\_F}$	LVD 3.4 V trimmed falling trip point for V_{DDD}	Typ – 4%	3400	Typ + 4%	mV	
SID527	$V_{TR\_3P5\_F}$	LVD 3.5 V trimmed falling trip point for V_{DDD}	Typ – 4%	3500	Typ + 4%	mV	
SID528	$V_{TR\_3P6\_F}$	LVD 3.6 V trimmed falling trip point for V_{DDD}	Typ – 4%	3600	Typ + 4%	mV	
SID529	$V_{TR\_3P7\_F}$	LVD 3.7 V trimmed falling trip point for V_{DDD}	Typ – 4%	3700	Typ + 4%	mV	
SID530	$V_{TR\_3P8\_F}$	LVD 3.8 V trimmed falling trip point for V_{DDD}	Typ – 4%	3800	Typ + 4%	mV	
SID531	$V_{TR\_3P9\_F}$	LVD 3.9 V trimmed falling trip point for V_{DDD}	Typ – 4%	3900	Typ + 4%	mV	
SID532	$V_{TR\_4P0\_F}$	LVD 4.0 V trimmed falling trip point for V_{DDD}	Typ – 4%	4000	Typ + 4%	mV	

Table 26-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID533	$V_{TR\_4P1\_F}$	LVD 4.1 V trimmed falling trip point for V_{DDD}	Typ – 4%	4100	Typ + 4%	mV	
SID534	$V_{TR\_4P2\_F}$	LVD 4.2 V trimmed falling trip point for V_{DDD}	Typ – 4%	4200	Typ + 4%	mV	
SID535	$V_{TR\_4P3\_F}$	LVD 4.3 V trimmed falling trip point for V_{DDD}	Typ – 4%	4300	Typ + 4%	mV	
SID536	$V_{TR\_4P4\_F}$	LVD 4.4 V trimmed falling trip point for V_{DDD}	Typ – 4%	4400	Typ + 4%	mV	
SID537	$V_{TR\_4P5\_F}$	LVD 4.5 V trimmed falling trip point for V_{DDD}	Typ – 4%	4500	Typ + 4%	mV	
SID538	$V_{TR\_4P6\_F}$	LVD 4.6 V trimmed falling trip point for V_{DDD}	Typ – 4%	4600	Typ + 4%	mV	
SID539	$V_{TR\_4P7\_F}$	LVD 4.7 V trimmed falling trip point for V_{DDD}	Typ – 4%	4700	Typ + 4%	mV	
SID540	$V_{TR\_4P8\_F}$	LVD 4.8 V trimmed falling trip point for V_{DDD}	Typ – 4%	4800	Typ + 4%	mV	
SID541	$V_{TR\_4P9\_F}$	LVD 4.9 V trimmed falling trip point for V_{DDD}	Typ – 4%	4900	Typ + 4%	mV	
SID542	$V_{TR\_5P0\_F}$	LVD 5.0 V trimmed falling trip point for V_{DDD}	Typ – 4%	5000	Typ + 4%	mV	
SID543	$V_{TR\_5P1\_F}$	LVD 5.1 V trimmed falling trip point for V_{DDD}	Typ – 4%	5100	Typ + 4%	mV	
SID544	$V_{TR\_5P2\_F}$	LVD 5.2 V trimmed falling trip point for V_{DDD}	Typ – 4%	5200	Typ + 4%	mV	
SID545	$V_{TR\_5P3\_F}$	LVD 5.3 V trimmed falling trip point for V_{DDD}	Typ – 4%	5300	Typ + 4%	mV	
SID546	$V_{TR\_2P8\_R}$	LVD 2.8 V trimmed rising trip point for V_{DDD}	Typ – 4%	2825	Typ + 4%	mV	Same as $V_{TR\_2P8\_F}$ + 25 mV
SID547	$V_{TR\_2P9\_R}$	LVD 2.9 V trimmed rising trip point for V_{DDD}	Typ – 4%	2925	Typ + 4%	mV	Same as $V_{TR\_2P9\_F}$ + 25 mV
SID548	$V_{TR\_3P0\_R}$	LVD 3.0 V trimmed rising trip point for V_{DDD}	Typ – 4%	3025	Typ + 4%	mV	Same as $V_{TR\_3P0\_F}$ + 25 mV
SID549	$V_{TR\_3P1\_R}$	LVD 3.1 V trimmed rising trip point for V_{DDD}	Typ – 4%	3125	Typ + 4%	mV	Same as $V_{TR\_3P1\_F}$ + 25 mV
SID550	$V_{TR\_3P2\_R}$	LVD 3.2 V trimmed rising trip point for V_{DDD}	Typ – 4%	3225	Typ + 4%	mV	Same as $V_{TR\_3P2\_F}$ + 25 mV
SID551	$V_{TR\_3P3\_R}$	LVD 3.3 V trimmed rising trip point for V_{DDD}	Typ – 4%	3325	Typ + 4%	mV	Same as $V_{TR\_3P3\_F}$ + 25 mV
SID552	$V_{TR\_3P4\_R}$	LVD 3.4 V trimmed rising trip point for V_{DDD}	Typ – 4%	3425	Typ + 4%	mV	Same as $V_{TR\_3P4\_F}$ + 25 mV
SID553	$V_{TR\_3P5\_R}$	LVD 3.5 V trimmed rising trip point for V_{DDD}	Typ – 4%	3525	Typ + 4%	mV	Same as $V_{TR\_3P5\_F}$ + 25 mV
SID554	$V_{TR\_3P6\_R}$	LVD 3.6 V trimmed rising trip point for V_{DDD}	Typ – 4%	3625	Typ + 4%	mV	Same as $V_{TR\_3P6\_F}$ + 25 mV
SID555	$V_{TR\_3P7\_R}$	LVD 3.7 V trimmed rising trip point for V_{DDD}	Typ – 4%	3725	Typ + 4%	mV	Same as $V_{TR\_3P7\_F}$ + 25 mV
SID556	$V_{TR\_3P8\_R}$	LVD 3.8 V trimmed rising trip point for V_{DDD}	Typ – 4%	3825	Typ + 4%	mV	Same as $V_{TR\_3P8\_F}$ + 25 mV
SID557	$V_{TR\_3P9\_R}$	LVD 3.9 V trimmed rising trip point for V_{DDD}	Typ – 4%	3925	Typ + 4%	mV	Same as $V_{TR\_3P9\_F}$ + 25 mV
SID558	$V_{TR\_4P0\_R}$	LVD 4.0 V trimmed rising trip point for V_{DDD}	Typ – 4%	4025	Typ + 4%	mV	Same as $V_{TR\_4P0\_F}$ + 25 mV

Table 26-15 **System resources** *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID559	$V_{TR\_4P1\_R}$	LVD 4.1 V trimmed rising trip point for V_{DDD}	Typ – 4%	4125	Typ + 4%	mV	Same as $V_{TR\_4P1\_F}$ + 25 mV
SID560	$V_{TR\_4P2\_R}$	LVD 4.2 V trimmed rising trip point for V_{DDD}	Typ – 4%	4225	Typ + 4%	mV	Same as $V_{TR\_4P2\_F}$ + 25 mV
SID561	$V_{TR\_4P3\_R}$	LVD 4.3 V trimmed rising trip point for V_{DDD}	Typ – 4%	4325	Typ + 4%	mV	Same as $V_{TR\_4P3\_F}$ + 25 mV
SID562	$V_{TR\_4P4\_R}$	LVD 4.4 V trimmed rising trip point for V_{DDD}	Typ – 4%	4425	Typ + 4%	mV	Same as $V_{TR\_4P4\_F}$ + 25 mV
SID563	$V_{TR\_4P5\_R}$	LVD 4.5 V trimmed rising trip point for V_{DDD}	Typ – 4%	4525	Typ + 4%	mV	Same as $V_{TR\_4P5\_F}$ + 25 mV
SID564	$V_{TR\_4P6\_R}$	LVD 4.6 V trimmed rising trip point for V_{DDD}	Typ – 4%	4625	Typ + 4%	mV	Same as $V_{TR\_4P6\_F}$ + 25 mV
SID565	$V_{TR\_4P7\_R}$	LVD 4.7 V trimmed rising trip point for V_{DDD}	Typ – 4%	4725	Typ + 4%	mV	Same as $V_{TR\_4P7\_F}$ + 25 mV
SID566	$V_{TR\_4P8\_R}$	LVD 4.8 V trimmed rising trip point for V_{DDD}	Typ – 4%	4825	Typ + 4%	mV	Same as $V_{TR\_4P8\_F}$ + 25 mV
SID567	$V_{TR\_4P9\_R}$	LVD 4.9 V trimmed rising trip point for V_{DDD}	Typ – 4%	4925	Typ + 4%	mV	Same as $V_{TR\_4P9\_F}$ + 25 mV
SID568	$V_{TR\_5P0\_R}$	LVD 5.0 V trimmed rising trip point for V_{DDD}	Typ – 4%	5025	Typ + 4%	mV	Same as $V_{TR\_5P0\_F}$ + 25 mV
SID569	$V_{TR\_5P1\_R}$	LVD 5.1 V trimmed rising trip point for V_{DDD}	Typ – 4%	5125	Typ + 4%	mV	Same as $V_{TR\_5P1\_F}$ + 25 mV
SID570	$V_{TR\_5P2\_R}$	LVD 5.2 V trimmed rising trip point for V_{DDD}	Typ – 4%	5225	Typ + 4%	mV	Same as $V_{TR\_5P2\_F}$ + 25 mV
SID571	$V_{TR\_5P3\_R}$	LVD 5.3 V trimmed rising trip point for V_{DDD}	Typ – 4%	5325	Typ + 4%	mV	Same as $V_{TR\_5P3\_F}$ + 25 mV
SID573	LVD_RR_A	Power ramp rate: V_{DDD} (Active)	–	–	100	mV/µs	
SID574	LVD_RR_DS	Power ramp rate: V_{DDD} (DeepSleep)	–	–	10	mV/µs	
SID575	$t_{DLY\_ACT\_LVD}$	Active mode delay between V_{DDD} falling/rising through LVD rising/falling point and an internal LVD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID575A	$t_{DLY\_DS\_LVD}$	DeepSleep mode delay between V_{DDD} falling/rising through LVD rising/falling point and an internal LVD output transitioning through V_{DDD} / 2	–	–	4	µs	Guaranteed by design
SID576	t_{RES_LVD}	Response time of LVD, V_{DDD} supply. LVD guaranteed to generate pulse for V_{DDD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below LVD falling trip point.)	100	–	–	ns	Guaranteed by design
High-voltage OVD specifications							
SID580	$V_{TR\_5P0\_R}$	High-voltage OVD 5.0-V trimmed rising trip point for V_{DDD} and V_{DDA_ADC}	5.049	5.205	5.361	V	
SID581	$V_{TR\_5P0\_F}$	High-voltage OVD 5.0-V trimmed falling trip point for V_{DDD} and V_{DDA_ADC}	5.025	5.18	5.335	V	
SID582	$V_{TR\_5P5\_R}$	High-voltage OVD 5.5-V trimmed rising trip point for V_{DDD} and V_{DDA_ADC} (default)	5.548	5.72	5.892	V	

Table 26-15 System resources *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID583	$V_{TR\_5P5\_F}$	High-voltage OVD 5.5-V trimmed falling trip point for V_{DDD} and V_{DDA_ADC} (default)	5.524	5.695	5.866	V	
SID585	HVOVD_RR_A	Power ramp rate: V_{DDD} and V_{DDA_ADC} (Active)	–	–	100	mV/µs	
SID586	HVOVD_RR_DS	Power ramp rate: V_{DDD} and V_{DDA_ADC} (DeepSleep)	–	–	10	mV/µs	
SID587	$t_{DLY\_ACT\_HVOVD}$	Active mode delay between V_{DDD} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID587A	$t_{DLY\_ACT\_HVOVD\_A}$	Active mode delay between V_{DDA_ADC} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD output transitioning through V_{DDD} / 2	–	–	1.5	µs	Guaranteed by design
SID587B	$t_{DLY\_DS\_HVOVD}$	DeepSleep mode delay between V_{DDD}/V_{DDA_ADC} falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD output transitioning through V_{DDD} / 2	–	–	4	µs	Guaranteed by design
SID588	t_{RES_HVOVD}	Response time of HV OVD HV OVD guaranteed to generate pulse for V_{DDD}/V_{DDA_ADC} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above $V_{TR\_5P0\_R}$ or $V_{TR\_5P5\_R}$)	100	–	–	ns	Guaranteed by design
Low-voltage OVD specifications							
SID590	$V_{TR\_R\_LVOVD}$	LV OVD trimmed rising trip point for V_{CCD}	Typ – 3%	1300	Typ + 3%	mV	
SID591	$V_{TR\_F\_LVOVD}$	LV OVD trimmed falling trip point for V_{CCD}	Typ – 3%	1275	Typ + 3%	mV	Same as $V_{TR\_R\_LVOVD}$ – 25 mV
SID595	$t_{DLY\_ACT\_LVOVD}$	Active mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD output transitioning through V_{DDD} / 2	–	–	1	µs	Guaranteed by design
SID595A	$t_{DLY\_DS\_LVOVD}$	DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD output transitioning through V_{DDD} / 2	–	–	12	µs	Guaranteed by design
SID596	t_{RES_LVOVD}	Response time of LV OVD. LV OVD guaranteed to generate pulse for V_{CCD} pulse width greater than this. (For rising-then-falling supply at max ramp rate; pulse width is time above $V_{TR\_R\_LVOVD}$)	100	–	–	ns	Guaranteed by design
Over current detection (OCD) specifications							
SID598	I_{OCD}	Over current detection range for internal Active regulator	312	–	630	mA	Guaranteed by design
SID599	I_{OCD_DPSLP}	Over current detection range for internal DeepSleep regulator	18	–	72	mA	

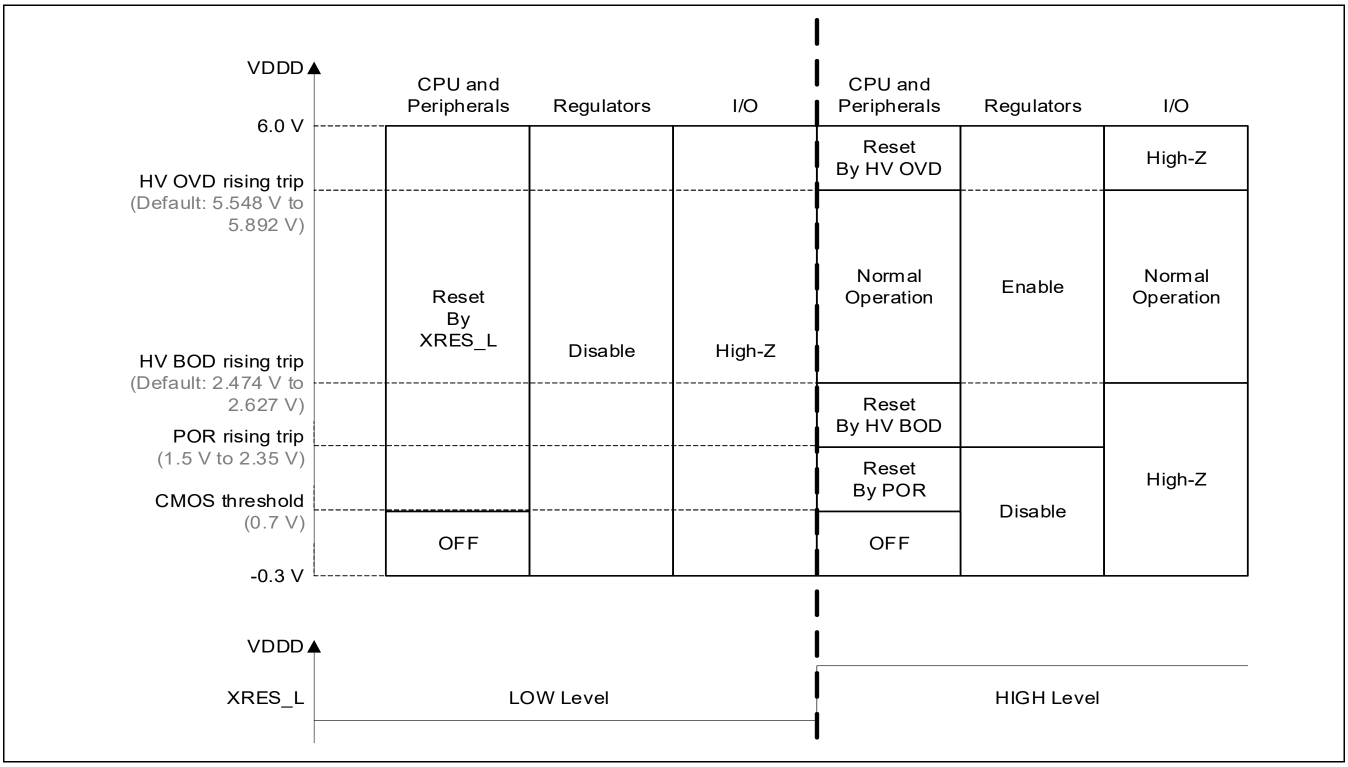


Figure 26-14 Device operations supply range

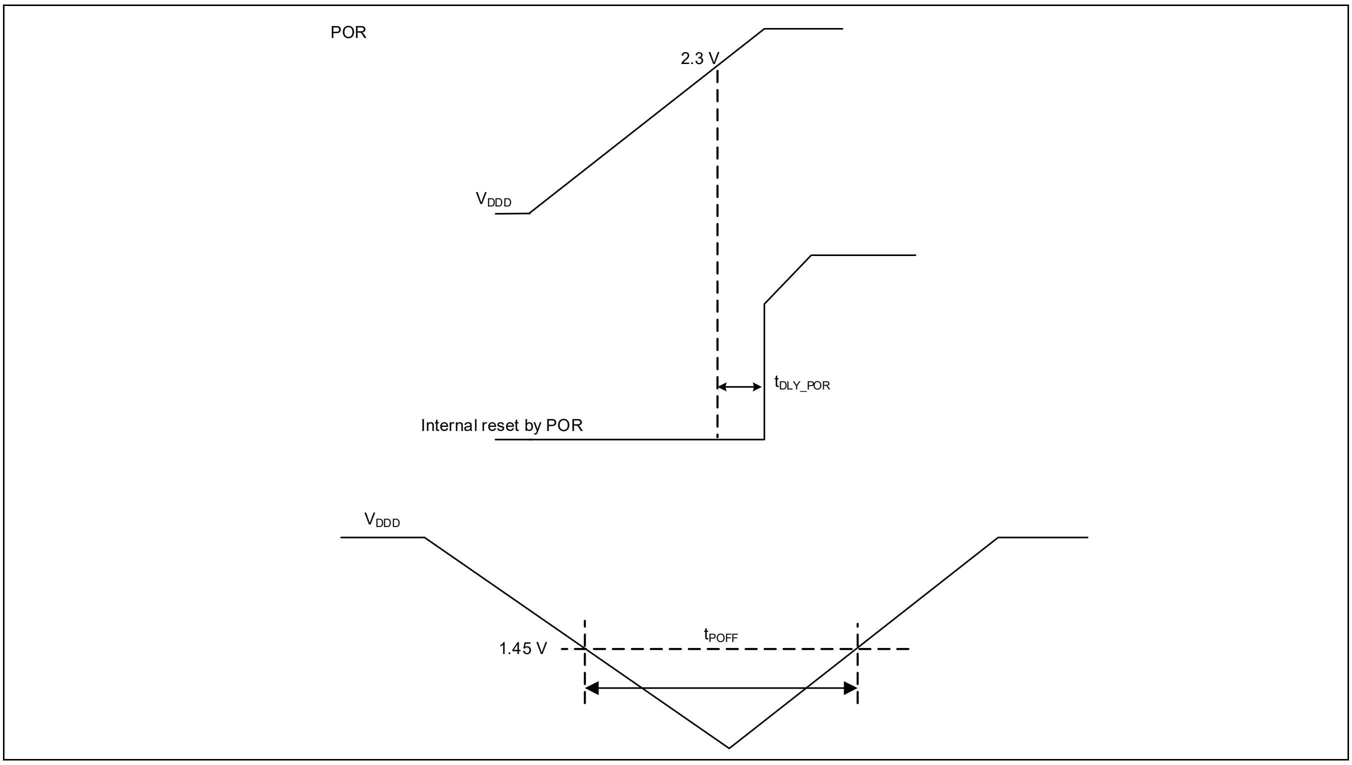


Figure 26-15 POR specifications

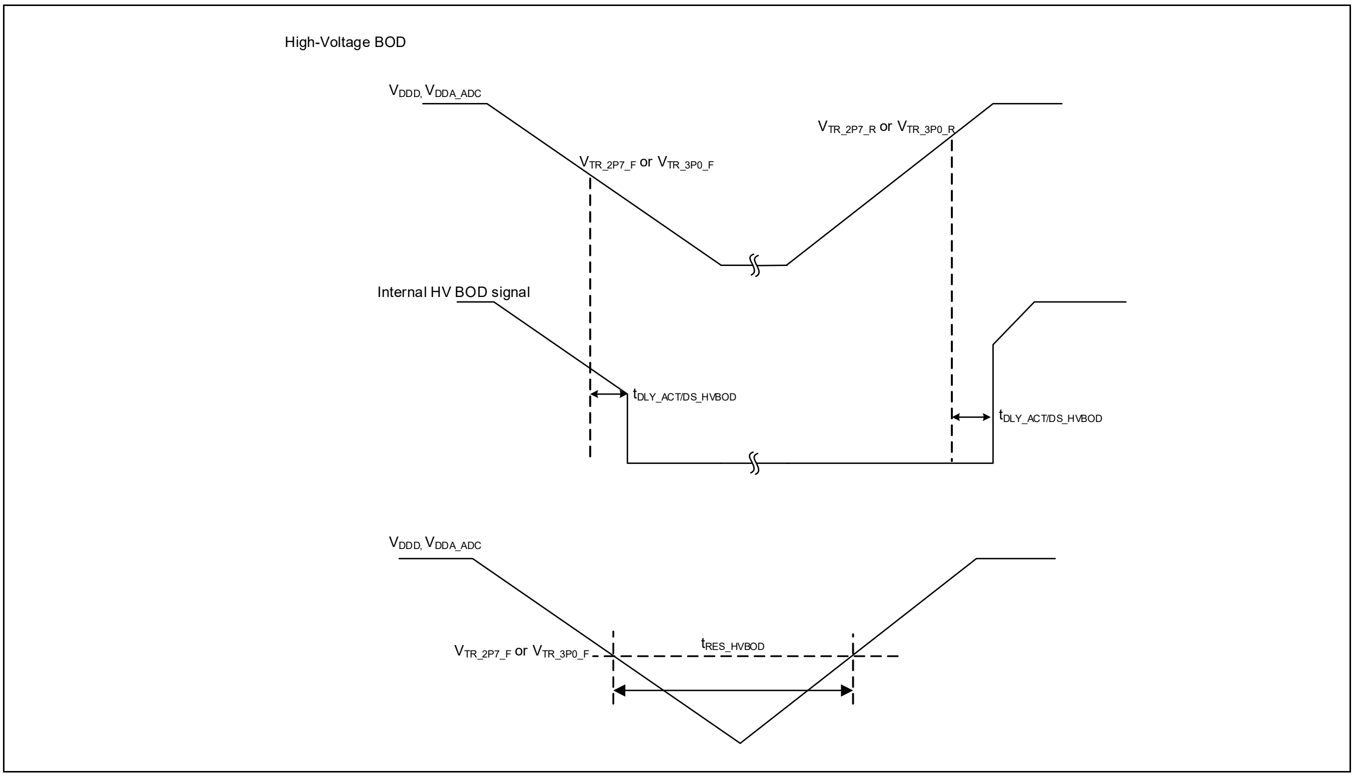


Figure 26-16 High-voltage BOD specifications

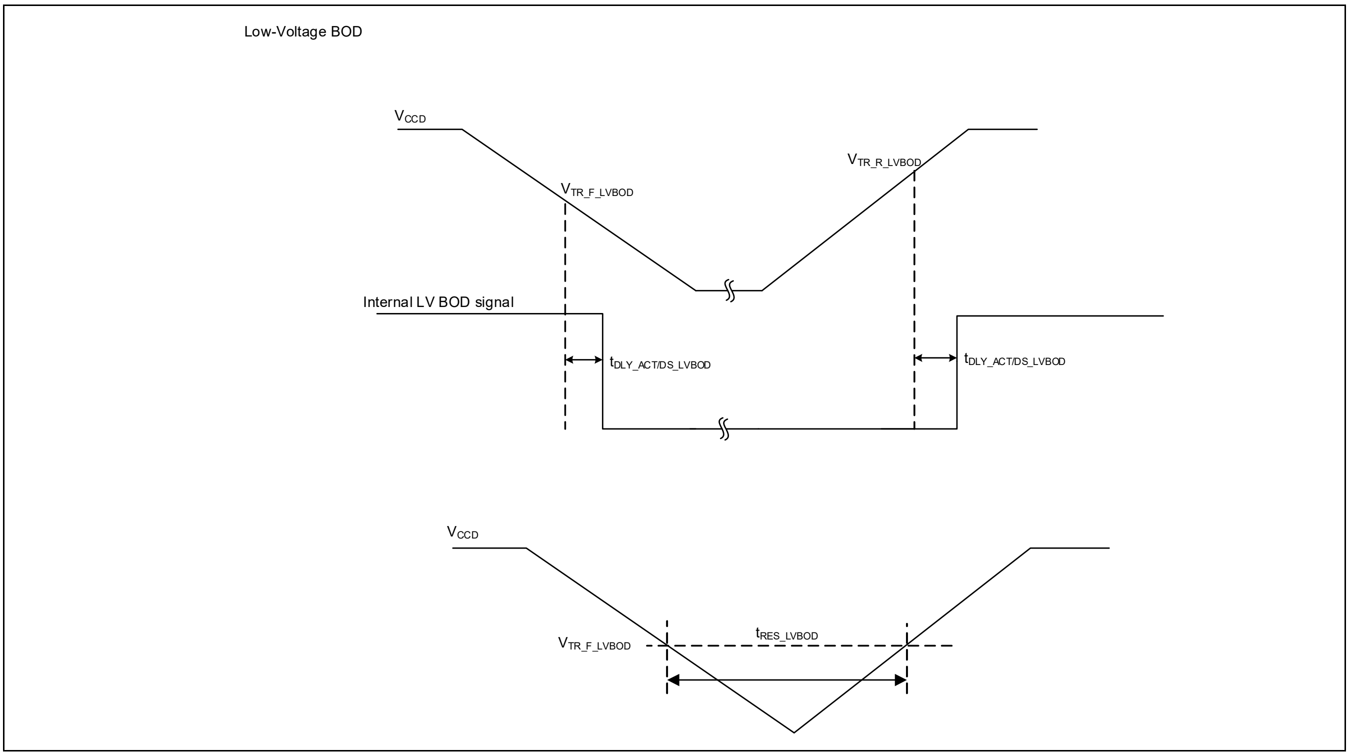


Figure 26-17 Low-voltage BOD specifications

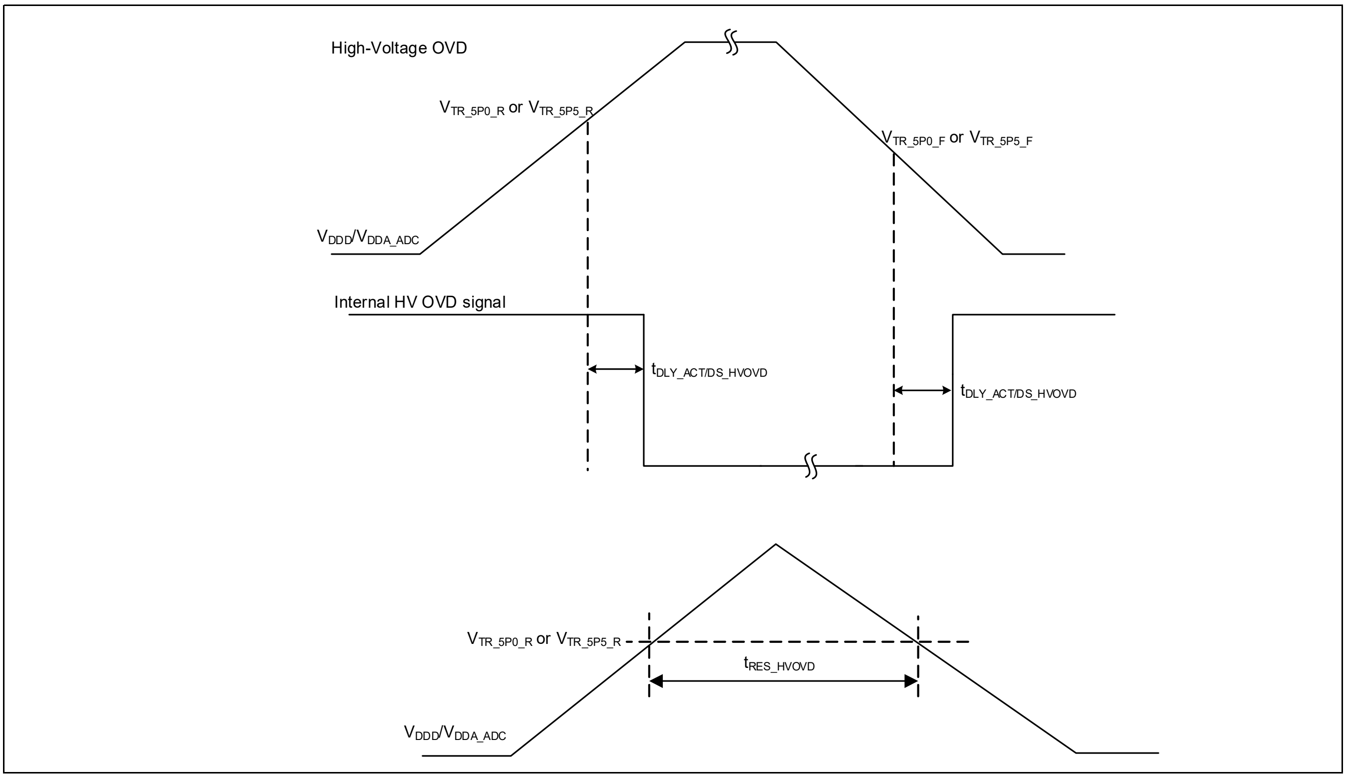


Figure 26-18 **High-voltage OVD specifications**

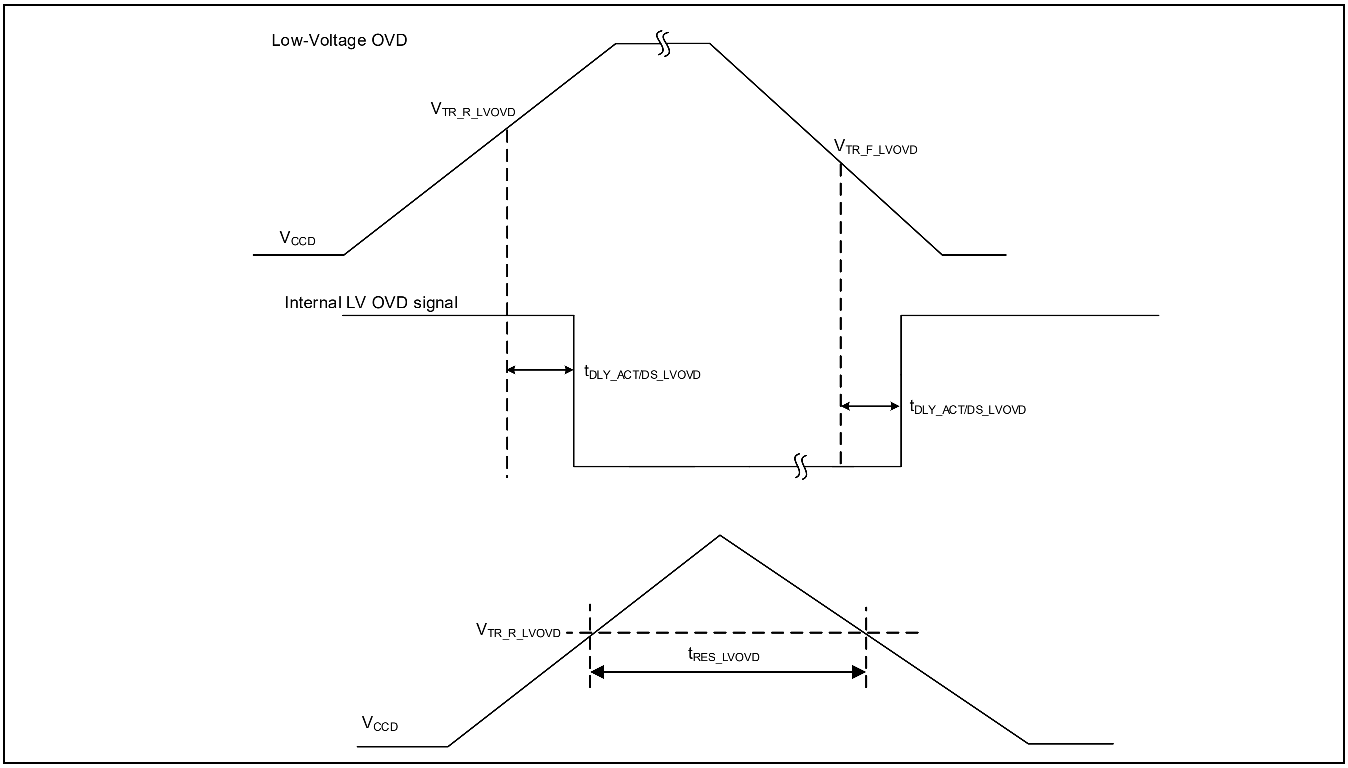


Figure 26-19 **Low-voltage OVD specifications**

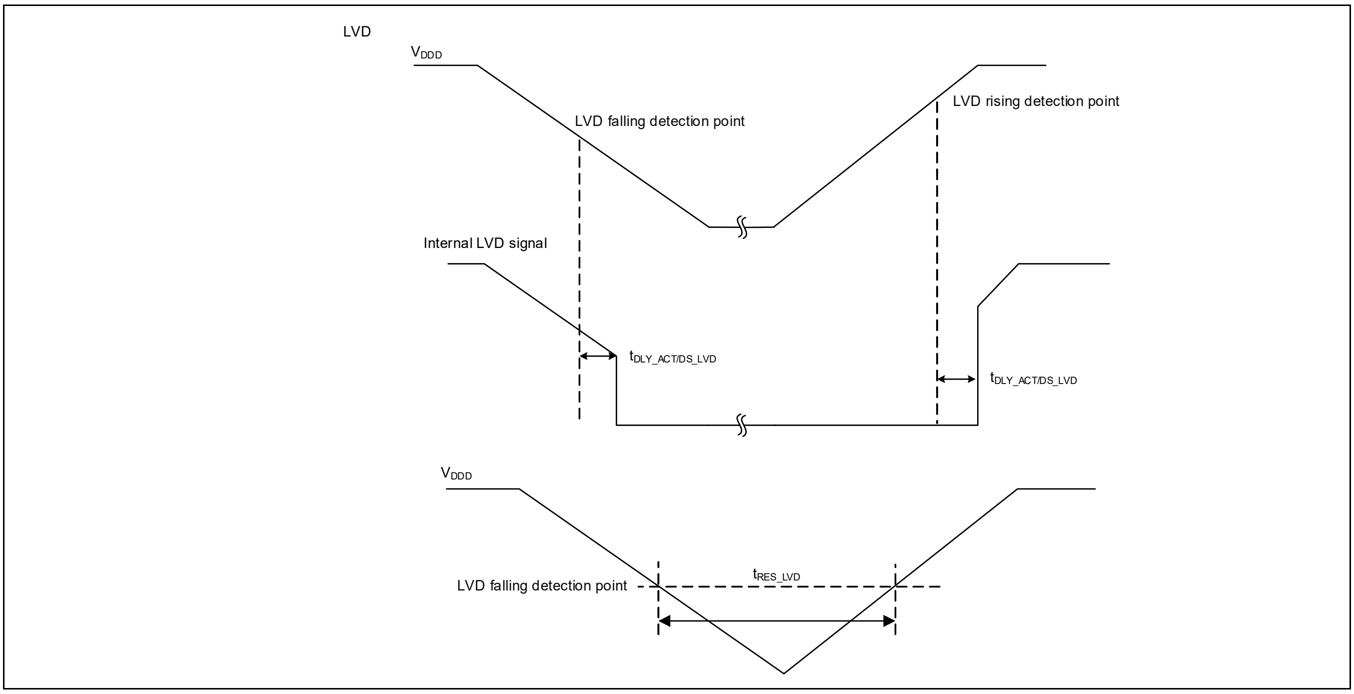


Figure 26-20 LVD specifications

26.9.1 SWD, JTAG, and trace specifications

Table 26-16 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended I/O Configuration: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> =0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID300	f_{SWDCLK}	SWD clock input frequency	–	–	10	MHz	$2.7 V \le V_{DDIO\_GPIO} \le 5.5 V$
SID301	t_{SWDI_SETUP}	SWDI setup time	0.25 × T	–	–	ns	$T = 1 / f_{SWDCLK}$
SID302	t_{SWDI_HOLD}	SWDI hold time	0.25 × T	–	–	ns	$T = 1 / f_{SWDCLK}$
SID303	t_{SWDO_VALID}	SWDO valid time	–	–	0.5 × T	ns	$T = 1 / f_{SWDCLK}$
SID304	t_{SWDO_HOLD}	SWDO hold time	1	–	–	ns	$T = 1 / f_{SWDCLK}$

Table 26-17 JTAG AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended I/O Configuration: **GPIO_STD**: CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID620	t_{JCKH}	TCK HIGH time	25	–	–	ns	30-pF load on TDO
SID621	t_{JCKL}	TCK LOW time	25	–	–	ns	30-pF load on TDO
SID622	t_{JCP}	TCK clock period	62.5	–	–	ns	30-pF load on TDO
SID623	t_{JSU}	TDI/TMS setup time	6.25	–	–	ns	30-pF load on TDO
SID624	t_{JH}	TDI/TMS hold time	6.25	–	–	ns	30-pF load on TDO
SID625	t_{JZX}	TDO High-Z to active	–	–	25	ns	30-pF load on TDO
SID626	t_{JXZ}	TDO active to High-Z	–	–	25	ns	30-pF load on TDO
SID627	t_{JCO}	TDO clock to output	–	–	25	ns	30-pF load on TDO

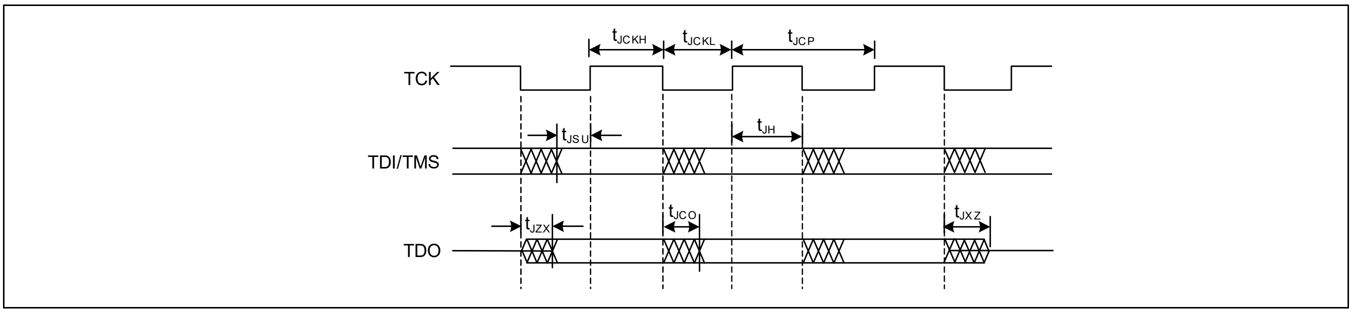


Figure 26-21 JTAG specifications

Table 26-18 Trace specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Recommended I/O Configuration: **HSIO_STDLN**: CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b000, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID1412A	C_{TRACE}	Trace capacitive load	–	–	30	pF	
SID1412	t_{TRACE_CYC}	Trace clock period	20	–	–	ns	Trace clock cycle time for 50 MHz
SID1413	t_{TRACE_CLKL}	Trace clock LOW pulse width	2	–	–	ns	Clock low pulse width
SID1414	t_{TRACE_CLKH}	Trace clock HIGH pulse width	2	–	–	ns	Clock high pulse width
SID1415	t_{TRACE_SETUP}	Trace data setup time	2	–	–	ns	Trace data setup time, CLK_PERI ≥ 75 MHz
SID1416	t_{TRACE_HOLD}	Trace data hold time	1	–	–	ns	Trace data hold time, CLK_PERI ≥ 75 MHz
SID1415A	t_{TRACE_SETUP}	Trace data setup time	3	–	–	ns	Trace data setup time, CLK_PERI < 75 MHz
SID1416A	t_{TRACE_HOLD}	Trace data hold time	2	–	–	ns	Trace data hold time, CLK_PERI < 75 MHz

26.10 Clock specifications

Table 26-19 Root and intermediate clocks[73, 74]

Root Clock	Maximum permitted clock frequency (MHz)[75]	Source	Maximum permitted clock frequency (MHz)[75]						Description
			PLL/FLL Clock source: ECO/LPECO[76]			PLL/FLL Clock source: IMO[77, 78]			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF0	200	PLL200#0	200	NA	NA	191	NA	NA	Root clock for CPUSS, PERI (CLK_MEM)
		FLL	100	NA	NA	100	NA	NA	
	100	PLL200#0	100	NA	NA	95	NA	NA	PERI (CLK_SLOW, CLK_PERI)
		FLL	100	NA	NA	97	NA	NA	
CLK_HF1	320	PLL400#0	320	313	316	306	300	303	CM7 CPU Core#0, CM7 CPU Core#1 clock
		FLL	100	NA	NA	100	NA	NA	
CLK_HF2	100	PLL200#1	100	NA	NA	95	NA	NA	Peripheral clock root other than CLK_PERI
		FLL	100	NA	NA	97	NA	NA	
CLK_HF3	100	PLL200#0	100	NA	NA	95	NA	NA	Event generator (CLK_REF), clock output on EXT_CLK pins (when used as output)
		FLL	100	NA	NA	97	NA	NA	
CLK_HF4	50	PLL200#0	50	NA	NA	47	NA	NA	ETH Channel#0. Internal clock 50 MHz for RMII, External PHY provides 25 MHz for MII
		FLL	50	NA	NA	48	NA	NA	
CLK_HF5	200	PLL400#1 / PLL400#2 / EXT_CLK	200	196	198	191	187	189	Sound Subsystem #0 root clock, ETH0 TSU clock (CLK_IF_SRSS0)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF6	200	PLL400#1 / PLL400#2 / EXT_CLK	200	196	198	191	187	189	Sound Subsystem #1 root clock (CLK_IF_SRSS1)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF7	200	PLL400#1 / PLL400#2 / EXT_CLK	200	196	198	191	187	189	Sound Subsystem #2 root clock (CLK_IF_SRSS2)
		FLL	100	NA	NA	100	NA	NA	
CLK_HF8	333	PLL400#1	333	NA	NA	318	NA	NA	SMIF#0 root clock
		PLL400#2	333	NA	NA	318	NA	NA	
		FLL	NA	NA	NA	NA	NA	NA	

Notes

73. Intermediate clocks that are not listed have the same limitations as that of their parent clock.
74. Table indicates guaranteed mapping between a root clock (CLK_HFx) and the PLL.
75. Maximum clock frequency after the corresponding clock source (PLL/FLL + dividers). All internal tolerances and affects are covered by these frequencies.
76. For ECO, LPECO: up to ±150ppm uncertainty of the external clock source are tolerated by design.
77. The IMO operation frequency tolerance is included.
78. ROM and flash boot execution with IMO/FLL at 100 MHz is guaranteed by design.

Table 26-19 Root and intermediate clocks[73, 74] *(continued)*

Root Clock	Maximum permitted clock frequency (MHz)[75]	Source	Maximum permitted clock frequency (MHz)[75]						Description
			PLL/FLL Clock source: ECO/LPECO[76]			PLL/FLL Clock source: IMO[77, 78]			
			Integer	SSCG	Fractional	Integer	SSCG	Fractional	
CLK_HF9	333	PLL400#1	333	NA	NA	318	NA	NA	SMIF#1 root clock
		PLL400#2	333	NA	NA	318	NA	NA	
		FLL	NA	NA	NA	NA	NA	NA	
CLK_HF10	254	PLL400#3	254	250	252	243	239	241	Video Subsystem root clock
		FLL	100	NA	NA	100	NA	NA	
CLK_HF11	224	PLL400#4	224	220	222	214	210	212	Display#0 root clock (range: 110 MHz to 220 MHz)
		PLL200#2	200	NA	NA	191	NA	NA	
		FLL	100	NA	NA	100	NA	NA	
CLK_HF12	224	PLL400#4	224	220	222	214	210	212	Display#1 root clock (range: 110 MHz to 220 MHz)
		PLL200#2	200	NA	NA	191	NA	NA	
		FLL	100	NA	NA	100	NA	NA	
CLK_HF13	ILO		NA						CSV Dedicated (< 1MHz)
CLK_FAST_0	320	CLK_HF1	320	313	316	306	302	305	CM7 CPU Core#0, intermediate clock
		FLL	100	NA	NA	100	NA	NA	
CLK_FAST_1	320	CLK_HF1	320	313	316	306	302	305	CM7 CPU Core#1, intermediate clock
		FLL	100	NA	NA	100	NA	NA	
CLK_MEM	200	CLK_HF0	200	NA	NA	191	NA	NA	Intermediate clock for SMIF, Flash, Ethernet, VIDEOSS
		FLL	100	NA	NA	100	NA	NA	
CLK_SLOW	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, VIDEOSS
		FLL	100	NA	NA	97	NA	NA	
CLK_PERI	100	CLK_HF0	100	NA	NA	95	NA	NA	Generated by clock gating CLK_HF0, intermediate clock for IOSS, TCPWM0, CPU trace, SMIF, Sound Subsystem, Ethernet
		FLL	100	NA	NA	97	NA	NA	

Table 26-20 PLL400 operation modes

PLL400 operation mode	Spread spectrum clock generation (SSCG)	Fractional
Integer	OFF	OFF
SSCG	ON	OFF
Fractional	OFF	ON

Table 26-21 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID310	f_{IMO}	IMO operating frequency	7.632	8	8.368	MHz	Accuracy after factory trimming
SID311	$t_{STARTIMO}$	IMO startup time	–	–	7.5	µs	Startup time to 90% of final frequency
SID312	I_{IMO_ACT}	IMO current	–	13.5	22	µA	Guaranteed by design

Table 26-22 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID320	$f_{ILOTRIM}$	ILO operating frequency	30.965	32.768	34.57	kHz	5.5% accuracy after factory trimming
SID321	$t_{STARTILO}$	ILO startup time	–	8	12	µs	Startup time to 90% of final frequency
SID323	I_{ILO}	ILO current	–	500	2800	nA	Guaranteed by design

Table 26-23 LPECO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID325	f_{LPECO}	LPECO operating frequency	3.99	–	8.01	MHz	Drive level protection DL ≥ 100 µW, ESR ≤ 200 Ω Crystal load capacitance (C_L) 5 pF to 25 pF
SID329	I_{LPECO_4M}	LPECO current at 4 MHz	–	93	110	µA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID354	I_{LPECO_4M}	LPECO current at 4 MHz	–	97	125	µA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID326	I_{LPECO_4M}	LPECO current at 4 MHz	–	106	145	µA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID355	I_{LPECO_4M}	LPECO current at 4 MHz	–	115	155	µA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID356	I_{LPECO_8M}	LPECO current at 8 MHz	–	140	165	µA	Shared with GPIO, Load: 10 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID357	I_{LPECO_8M}	LPECO current at 8 MHz	–	149	175	µA	Shared with GPIO, Load: 15 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID327	I_{LPECO_8M}	LPECO current at 8 MHz	–	165	190	µA	Shared with GPIO, Load: 20 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0
SID358	I_{LPECO_8M}	LPECO current at 8 MHz	–	183	220	µA	Shared with GPIO, Load: 25 pF BACKUP_LPECO_CTL/LPECO_AMPDET_EN<0:0>=0b0

Note

79.Oscillator startup time is a performance parameter and mainly depending on the chosen external crystal and load capacitance.

Table 26-23 LPECO specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID328	t_{START_LPECO}	LPECO startup time[79]	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (BACKUP_LPECO_CTL.LPECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_LPECO_STATUS.LPECO_READY<0:0>=0b1 and BACKUP_LPECO_STATUS.LPECO_AMPDET_OK<0:0>=0b1).

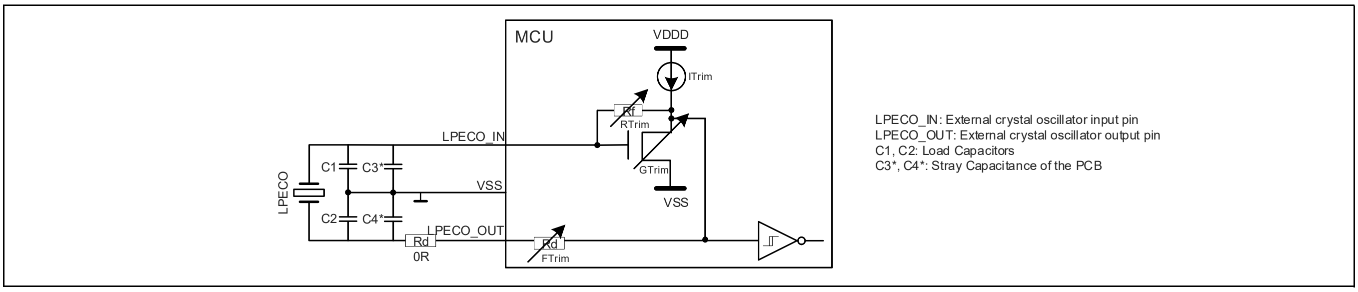


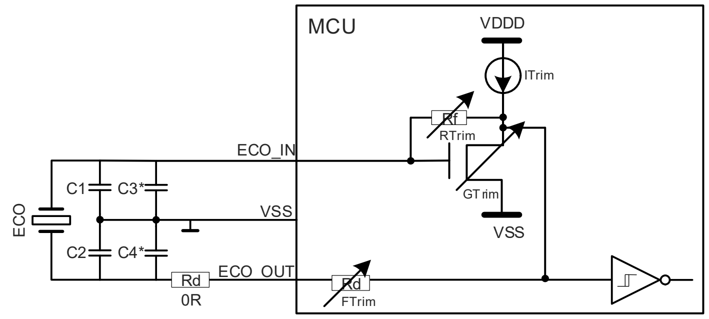
Figure 26-22 LPECO connection scheme[80]

Note

[80] Refer to the family-specific Architecture TRM for more information on crystal requirements (002-25800, TRAVEO™ T2G Automotive Cluster 2D Family Architecture Technical Reference Manual (TRM)).

Table 26-24 ECO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID330	f_{ECO}	Crystal frequency range	7.2	–	33.34	MHz	
SID332	R_{FDBK}	Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100 kΩ step size on RTRIM	100	–	400	kΩ	Guaranteed by design
SID333	I_{ECO3}	ECO current at T_J = 150 °C	–	1200	2000	µA	Maximum operation current at 33 MHz crystal, up to 18 pF load
SID334	t_{START_7M}	7.2-MHz ECO startup time[81]	–	–	10	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_CONFIG.ECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.ECO_OK<0:0>=0b1 and CLK_ECO_STATUS.ECO_READY<0:0>=0b1).
SID335	t_{START_33M}	33-MHz ECO startup time[81]	–	–	1	ms	Startup time to 90% of final frequency. Time from oscillator enable (CLK_ECO_CONFIG.ECO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (CLK_ECO_STATUS.ECO_OK<0:0>=0b1 and CLK_ECO_STATUS.ECO_READY<0:0>=0b1).



ECO_IN: External crystal oscillator input pin
ECO_OUT: External crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB

Figure 26-23 ECO connection scheme[82]

Notes

81. Oscillator startup time is a performance parameter and mainly depending on the chosen external crystal and load capacitance.
82. Refer to the family-specific Architecture TRM for more information on crystal requirements (002-25800, TRAVEO™ T2G Automotive MCU cluster 2D architecture technical reference manual).

Table 26-25 PLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
PLL Specifications for "PLL without SSCG and Fractional Operation" (PLL200)							
SID340	t_{PLL200_LOCK}	Time to achieve PLL lock	–	–	35	µs	Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set
SID341	f_{OUT}	Output frequency from PLL block (PLL_OUT)	10.998	–	200.03	MHz	
SID346	f_{IN}	PLL input frequency (Reference Clock f_{REF})	3.988	–	33.34	MHz	
SID347	I_{PLL_200M}	PLL operating current	–	0.87	1.85	mA	f_{OUT} = 200 MHz
SID348C	f_{PLL_VCO}	VCO frequency, clock output of 'Voltage Control Oscillator (VCO)'	169.9745	–	400.06	MHz	
SID349C	f_{PLL_PFD}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	8.0012	MHz	
SID342	PLL_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID343	PLL_LJIT2	Long term jitter	–0.5	–	0.5	ns	For 500 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID344	PLL_LJIT3	Long term jitter	–0.5	–	0.5	ns	For 1000 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
SID345A1	PLL_LJIT5	Long term jitter	–0.75	–	0.75	ns	For 10000 ns Guaranteed by design f_{PLL_VCO}: 320 MHz or 400 MHz f_{PLL_OUT}: 40 MHz to 200 MHz f_{PLL_PFD}: 8 MHz f_{PLL_IN}: ECO
PLL Specifications for "PLL with SSCG and Fractional Operation" (PLL400)							
SID340A	t_{PLL400_LOCK}	Time to achieve PLL lock	–	–	50	µs	
SID341A	f_{OUT}	Output frequency from PLL block (PLL_OUT)	24.996	–	400.06	MHz	
SID343A	SPREAD_D	Spread spectrum modulation depth	0.5	–	3	%	Downspread only, triangle modulation
SID343B	f_{SPREAD_MR}	Spread spectrum modulation rate	–	–	32	kHz	Selected by modulation divider from f_{PFD}
SID346A	f_{IN}	PLL input frequency (Reference Clock f_{REF})	3.988	–	33.34	MHz	
SID347A	I_{PLL_400M}	PLL operating current	–	1.4	2.2	mA	f_{OUT} = 400 MHz

Table 26-25 PLL specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID348A	f_{PFD_S}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	3.988	–	20.003	MHz	Fractional operation OFF
SID349A	f_{PFD_F}	Phase Detector Frequency, clock output of the Reference Divider (Q) and Feedback Divider (P)	7.9988	–	20.003	MHz	Fractional operation ON
SID345A	f_{VCO}	VCO frequency, Clock output of 'Voltage Control Oscillator (VCO)'	399.94	–	800.12	MHz	
SID342D1	PLL400_LJIT1	Long term jitter	–0.25	–	0.25	ns	For 125 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz
SID343D1	PLL400_LJIT2	Long term jitter	–0.5	–	0.5	ns	For 500 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz
SID344D1	PLL400_LJIT3	Long term jitter	–1	–	1	ns	For 1000 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz
SID345E1	PLL400_LJIT5	Long term jitter	–1.5	–	1.5	ns	For 10000 ns Guaranteed by Design f_{VCO}: 800 MHz (Integer mode) f_{IN}: ECO f_{PFD}: 4 MHz f_{OUT}: 100 MHz to 400 MHz

Table 26-26 FLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID350	t_{FLL_WAKE}	FLL wake up time	–	–	5	µs	Wakeup with < 10 °C temperature change while in DeepSleep. f_{FLL_IN} = 8 MHz, f_{FLL_OUT} = 100 MHz, Time from stable reference clock until FLL frequency is within 5% of final value
SID351	f_{FLL_OUT}	Output frequency from FLL block	24	–	100	MHz	Output range of FLL divided-by-2 output

Table 26-26 FLL specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID352	FLL_CJIT	FLL frequency accuracy	–1	–	1	%	This is added to the error of the source
SID353	f_{FLL_IN}	Input frequency	0.25	–	100	MHz	

Table 26-27 WCO Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID360	f_{WCO}	Watch crystal frequency	–	32.768	–	kHz	Tuning Fork Crystal with following parameters: DL (drive level) ≥ 0.5 µW, ESR ≤ 130 kΩ
SID361	WCO_DC	WCO duty cycle	10	–	90	%	
SID362	t_{START_WCO}	WCO start up time[83]	–	–	1000	ms	Time from oscillator enable (BACKUP_CTL.WCO_EN<0:0>=0b1) to stable oscillation and sufficient amplitude (BACKUP_STATUS.WCO_OK<0:0>=0b1)
SID363	I_{WCO}	WCO current	–	1.4	–	µA	AGC=OFF

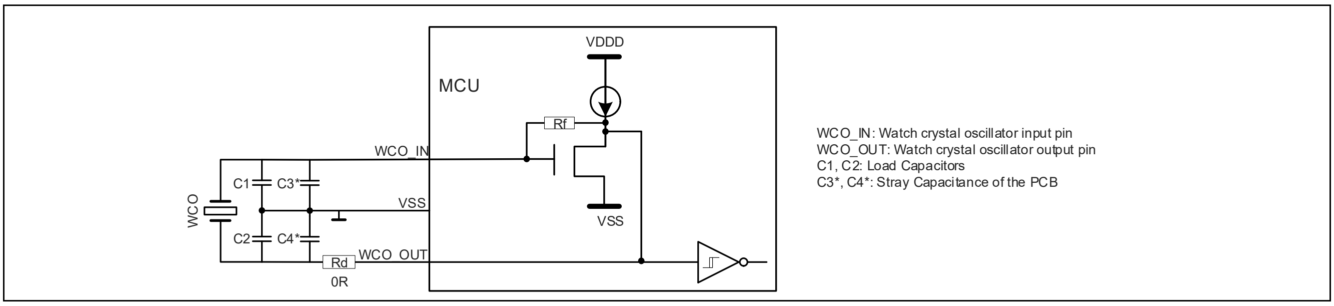


Figure 26-24 WCO connection scheme[84]

Table 26-28 External clock input specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID366	f_{EXT}	External clock input frequency	0.25	–	100	MHz	For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive)
SID367	EXT_DC	Duty cycle	45	–	55	%	

Notes

[83] Oscillator startup time is a performance parameter and mainly depending on the chosen external crystal and load capacitance.

[84] Refer to the family-specific Architecture TRM for more information on crystal requirements (002-25800, TRAVEO™ T2G Automotive MCU cluster 2D architecture technical reference manual).

Table 26-29 MCWDT timeout specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID410	t_{MCWDT1}	Minimum MCWDT timeout	57.85	–	–	µs	When using the ILO (32 kHz + 5.5%) and 16-bit MCWDT counter Guaranteed by design
SID411	t_{MCWDT2}	Maximum MCWDT timeout	–	–	2.12	s	When using the ILO (32.768 kHz – 5.5%) and 16-bit MCWDT counter Guaranteed by design

Table 26-30 WDT timeout specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID412	t_{WDT1}	Minimum WDT timeout	57.85	–	–	µs	When using the ILO (32 kHz + 5.5%) and 32-bit WDT counter. Guaranteed by design
SID413	t_{WDT2}	Maximum WDT timeout	–	–	38.53	h	When using the ILO (32 kHz – 5.5%) and 32-bit WDT counter. Guaranteed by design
SID414	t_{WDT3}	Default WDT timeout	–	1000	–	ms	When using the ILO and 32-bit WDT counter at 0x8000 (default value) Guaranteed by design

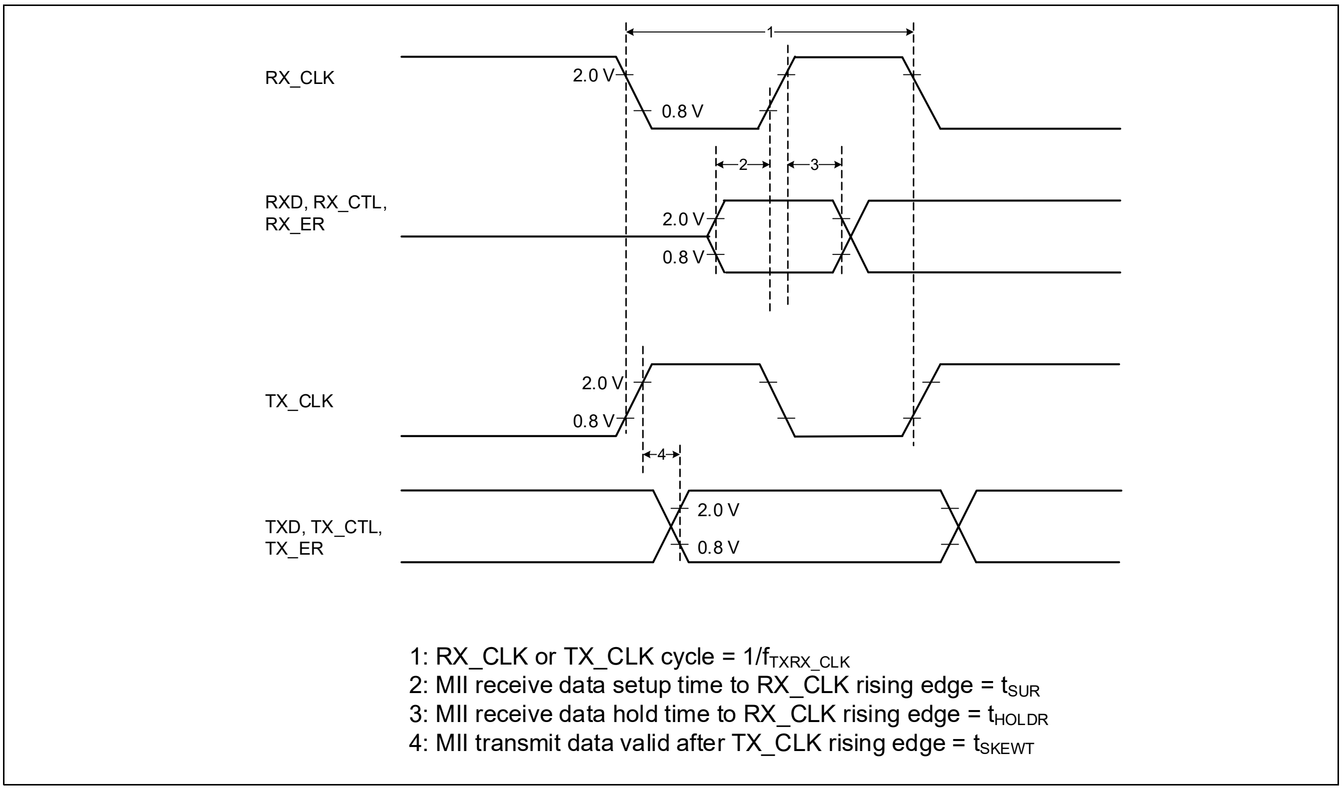
26.11 Ethernet specifications

Table 26-31 Ethernet specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
Ethernet General Specifications							
SID364C	C_L	Load capacitance	–	–	25	pF	for all between MAC and PHY for MII-IF, RMII-IF, MDC/MDIO-IF
SID364A	C_L	Load capacitance	–	–	10	pF	for all between MAC and PHY for RGMII-IF
SID368	f_{SYS}	System clock max frequency	–	–	100	MHz	Guaranteed by design
SID369	f_{AXI}	AXI clock max frequency	–	–	200	MHz	Guaranteed by design
Ethernet MII Specifications							
Recommended I/O configuration: **HSIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b10, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID370	t_{TXCYC}	MII tx_clk cycle	39.5	40	40.5	ns	
SID371	t_{RXCYC}	MII rx_clk cycle	39.5	40	40.5	ns	
SID372B	t_{SKEWT}	MII Transmit data (txd,tx_en,tx_er) valid after tx_clk	0	–	25	ns	
SID373	t_{SUR}	MII Receive data setup to rx_clk rising edge	10	–	–	ns	
SID374	t_{HOLDR}	MII Receive data hold to rx_clk rising edge	10	–	–	ns	
SID375	f_{TXRX_CLK}	MII TX/RX_CLK Clock frequency	–50ppm	25	+50ppm	MHz	
SID376B	DUTY_TXRX_CLK	TX/RX_CLK Duty cycle	35	–	65	%	
SID365A	t_{RF}	Input rise / fall time	–	–	2	ns	20% to 80%
SID365E_1	t_{RFO}	Output rise / fall time	–	–	6.5	ns	20% to 80%
Ethernet RMII Specifications							
Recommended I/O configuration: **HSIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
SID375A	f_{REF_CLK}	RMII reference clock frequency (input)	–50ppm	50	+50ppm	MHz	
SID375B	$f_{REF\_CLK\_OUT}$	RMII reference clock frequency (output)	–2%	50	+2%	MHz	
SID376C	DUTY_REF	Duty cycle of reference clock (output)	35	–	65	%	
SID377	t_{SU}	RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK rising edge.	4	–	–	ns	
SID378	t_{HOLD}	RXD[1:0], CRS_DV, RX_ER, Data hold from REF_CLK rising edge	2	–	–	ns	
SID379	t_{TXOUT}	TXD[1:0], TX_EN Data output delay from REF_CLK rising edge	2	–	14	ns	
SID365C	t_{RF}	Input rise / fall time	–	–	2	ns	20% to 80%

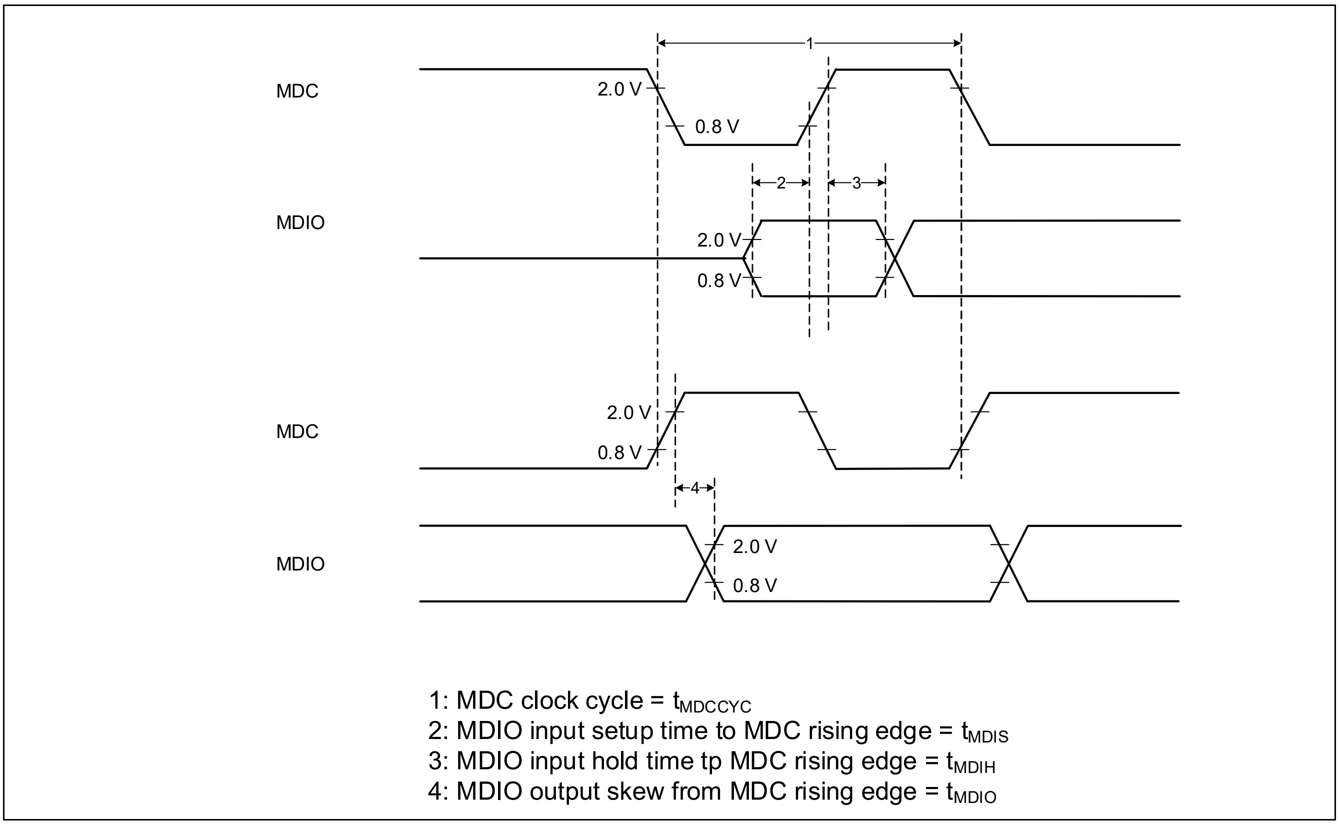
Table 26-31 Ethernet specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID365F_1	t_{RFO}	Output rise / fall time	–	–	6.5	ns	20% to 80%
Ethernet RGMII Specifications							
Recommended I/O configuration **HSIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b00, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0							
SID385	f_{CYC}	REF_CLK, TX_CLK and RX_CLK clock frequency	–50 ppm	125	+50 ppm	MHz	
SID386	DUTY_REF	Duty cycle of reference clock	45	–	55	%	
SID385_1	f_{P_TXCRXC}	TX(TXC)_CLK (External mode) and RX(RXC)_CLK clock frequency	–50 ppm	125	+50 ppm	MHz	
SID385B	t_{P_TXCRXC}	TX(TXC)_CLK (External mode)/RX(RXC)_CLK clock period	7.2	8	8.8	ns	
SID387	t_{SKEWT}	Data to clock output skew	–0.5	–	0.5	ns	
SID388	t_{SKEWR}	Data to clock input skew	1	–	2.6	ns	
SID365	t_{RF}	Rise / fall time	–	–	0.75	ns	20% to 80%, using HSIO_STD
Ethernet MDIO Specifications							
SID395	t_{MDCYC}	MDC clock cycle	400	–	–	ns	
SID395A	t_{HL_MDC}	MDIO Minimum high and low times for MDC	160	–	–	ns	
SID396	t_{MDIS}	MDIO input setup time to MDC rising edge	100	–	–	ns	
SID397	t_{MDIH}	MDIO input hold time to MDC rising edge	0	–	–	ns	
SID398	t_{MDIO}	MDIO output skew from MDC rising edge	10	–	390	ns	
SID365D	t_{RF}	Input rise / fall time	–	–	2	ns	20% to 80%
SID365G_1	t_{RFO}	Output MDIO rise / fall time	–	–	6.5	ns	20% to 80%



1: RX_CLK or TX_CLK cycle = $1/f_{TXRX\_CLK}$
2: MII receive data setup time to RX_CLK rising edge = t_{SUR}
3: MII receive data hold time to RX_CLK rising edge = t_{HOLDR}
4: MII transmit data valid after TX_CLK rising edge = t_{SKEWT}

Figure 26-25 MII timing diagram



1: MDC clock cycle = t_{MDCCYC}
2: MDIO input setup time to MDC rising edge = t_{MDIS}
3: MDIO input hold time tp MDC rising edge = t_{MDIH}
4: MDIO output skew from MDC rising edge = t_{MDIO}

Figure 26-26 MDIO timing diagram

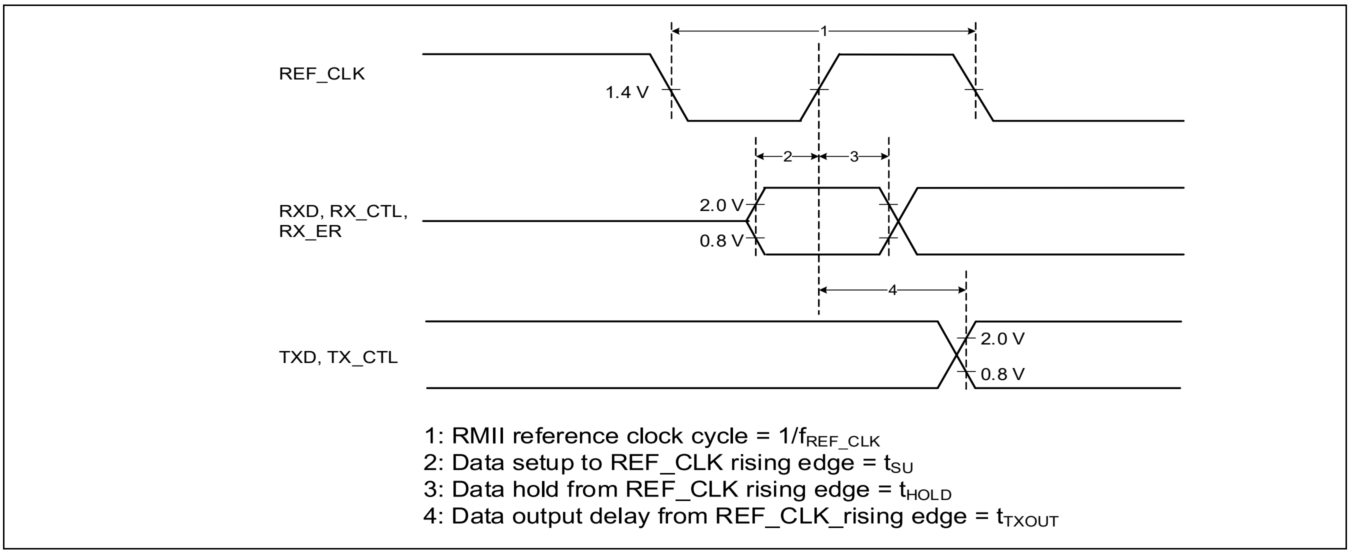


Figure 26-27 RMII timing diagram

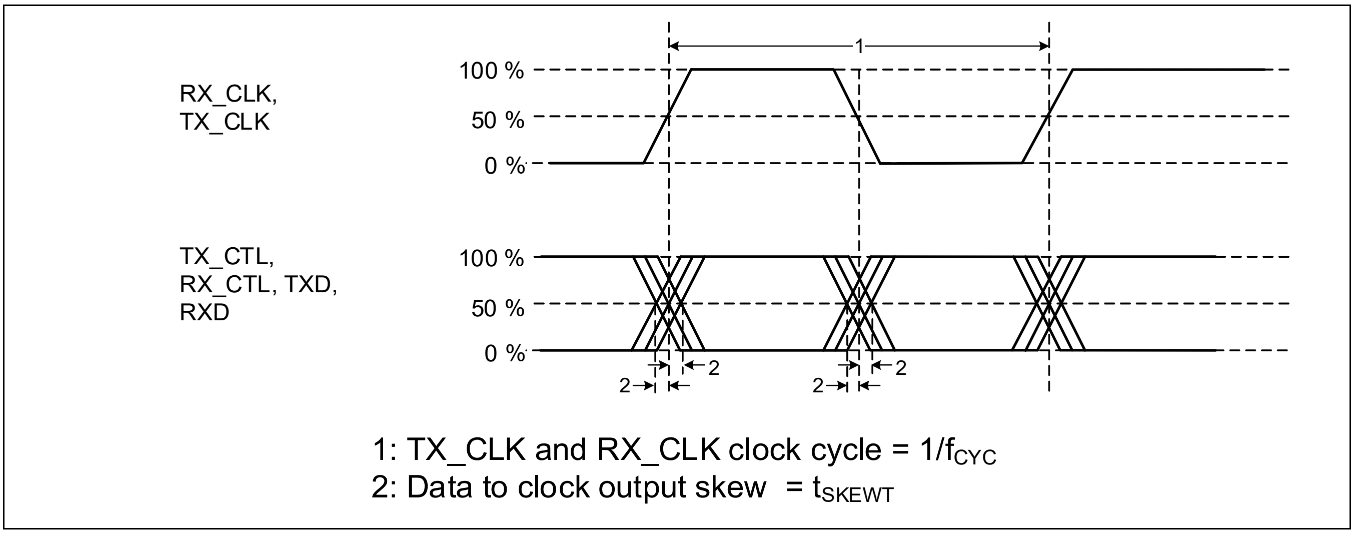


Figure 26-28 RGMII Tx timing diagram

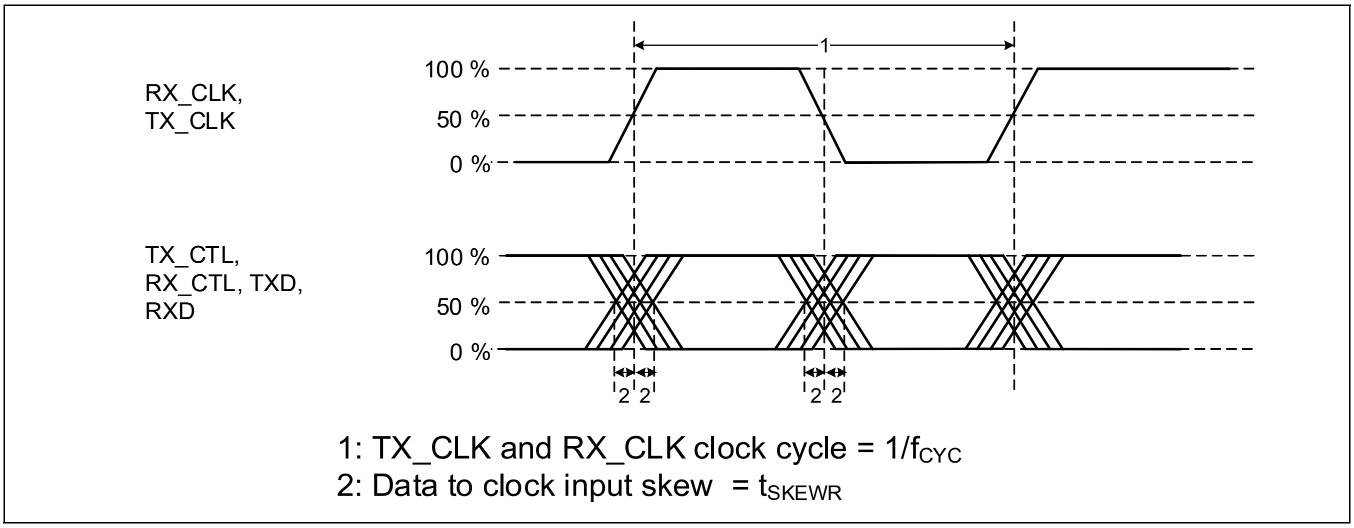


Figure 26-29 RGMII Rx timing diagram

26.11.1 Minimum bus frequency requirements

The following table details the required minimum operating frequencies for all possible Ethernet configurations and MAC speeds. Ethernet module uses **AXI** interface for DMA access.

Table 26-32 Minimum AXI frequency for MAC speeds

DMA bus width	MAC rate	Minimum AXI frequency
64	1 Gbps	65 MHz
64	100 Mbps	10 MHz
64	10 Mbps	10 MHz

26.12 Sound subsystem specifications

Table 26-33 Sound subsystem specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
I^2S I/O settings							
Recommended I/O configuration: **HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> =0b100, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_SLEW_EXT/SLEW<2:0> =0b000 **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> =0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1 **GPIO_ENH:** CFG_OUT/DRIVE_SEL<1:0> =0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_OUT/SLOW<0:0> =0b0 **GPIO_SMC:** CFG_OUT/DRIVE_SEL<1:0> =0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
I^2S Serial Clock Frequency							
SID796	t_{SCLK}	Serial clock period	162	–	–	ns	Guaranteed by design No feature is used for low frequency I^2S operation: DUT RX Master: * RX_IF_CTL.LATE_SAMPLE = 0 * RX_IF_CTL.LATE_CAPTURE = 0b00 DUT TX Slave: No special configuration DUT RX Slave: * RX_IF_CTL.LATE_SAMPLE = 0
SID797	t_{HC}	Serial clock high time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID798	t_{LC}	Serial clock low time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID799	t_{MCLK}	Master clock period	20	–	–	ns	Guaranteed by design
I^2S Transmitter Timing							
SID740	t_{DTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	–	–	0.8 × t_{SCLK}	ns	Guaranteed by design
SID741	t_{HTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID743	$t_{HR\_WS\_POL\_0}$	TX Slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	
I^2S Receiver Timing							
SID751	t_{SR}	Setup on RX_SD/RX_FSYNC (WS) before the rising edge to RX_CLK	0.2 × t_{SCLK}	–	–	ns	Guaranteed by Design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE or SCK_POLARITY setting
SID752A	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the rising edge to RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 0

Table 26-33 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID753	t_{SCLK_TRANS}	SCLK transition timing	1	–	8	ns	20% to 80%
SID754	t_{MCLK_TRANS}	MCLK transition timing	1	–	8	ns	20% to 80%
SID755	t_{DATA_TRANS}	DATA transition timing	1	–	8	ns	20% to 80%
TDM I/O Settings							
Recommended I/O configuration: **For serial clock above 25 MHz** **HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_SLEW_EXT/SLEW<0:0> = 0b0 **For serial clock in between 12.5 MHz, and 25 MHz** **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1 **GPIO_ENH:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_OUT/SLOW<0:0> = 0b0 **For serial clock up to 25 MHz** **HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b100, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_SLEW_EXT/SLEW<0:0> = 0b0 **For serial clock up to 12.5 MHz** **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1 **GPIO_ENH:** CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1, CFG_OUT/SLOW<0:0> = 0b0 **GPIO_SMC**: CFG_OUT/DRIVE_SEL<1:0> = 0b01, CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b1							
TDM Serial Clock							
SID1000B	t_{SCLK}	Serial clock period, TDM[x] (x=0 through 3)	40	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX Slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX Slave: RX_IF_CTL.SCK_POLARITY= 0 For TDM channels on GPIO_STD, GPIO_ENH, HSIO_STDLN, type IO-cells
SID1000D	t_{SCLK}	Serial clock period, TDM[x] (x=0 through 3)	80	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: RX_IF_CTL.LATE_SAMPLE = 1 RX_IF_CTL.LATE_CAPTURE = 0b00 TX Slave: Set TX_IF_CTL.SCK_POLARITY = 1 RX Slave: RX_IF_CTL.SCK_POLARITY = 0
SID1000E	t_{SCLK}	Serial clock period, TDM[x] (x=0 through 1)	20	–	–	ns	Guaranteed by Design TX Master: TX_IF_CTL.SCK_POLARITY = 0 RX Master: not supported at 50MHz TX Slave: not supported at 50MHz RX Slave: not supported at 50MHz For TDM channels on HSIO_STDLN type IO-cells

Table 26-33 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1001	t_{HC}	Serial clock high time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID1002	t_{LC}	Serial clock low time	0.35 × t_{SCLK}	–	–	ns	Guaranteed by design
SID1010	t_{MCLK}	Master clock input period	10	–	–	ns	MCLK must be SCLK*2; The maximum output frequency of the TDM depends on the used I/O type.
SID1002A	t_{MCLK}	Master clock output period	20	–	–	ns	For TDM channels on HSIO_STDLN type I/Os
SID1002B	t_{MCLK}	Master clock output period	40	–	–	ns	For TDM channels on GPIO_STD, GPIO_ENH type I/Os
SID1002C	t_{MCLK}	Master clock output period	80	–	–	ns	For TDM channels on GPIO_SMC type I/Os
SID1002D	t_{MCLK_IH}	Master clock input high time	0.45 × t_{MCLK}	–	–	ns	
SID1002E	t_{MCLK_IL}	Master clock input low time	0.45 × t_{MCLK}	–	–	ns	
SID1002F	t_{MCLK_OH}	Master clock output high time	0.35 × t_{MCLK}	–	–	ns	Only if internal clock source, divided EXT_CLK input, or EXT_CLK input on HSIO_STDLN is used
SID1002G	t_{MCLK_OL}	Master clock output low time	0.35 × t_{MCLK}	–	–	ns	Only if internal clock source, divided EXT_CLK input, or EXT_CLK input on HSIO_STDLN is used
TDM Transmit Timing							
SID1003	t_{DTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	–	–	0.8 × t_{SCLK}	ns	Guaranteed by design
SID1004	t_{HTR}	Delay from rising edge of TX_CLK to transition on TX_SD/TX_FSYNC (WS)	0	–	–	ns	Guaranteed by design
SID1011	$t_{HR\_WS\_POL\_0}$	TX Slave: Hold on TX_FSYNC (WS) after the 1st edge following the driving edge of TX_CLK (SCK_POLARITY = 0, half-cycle hold)	1.8	–	–	ns	
SID1012	$t_{HR\_WS\_POL\_1}$	TX Slave: Hold on TX_FSYNC (WS) after the 2nd edge following the driving edge of TX_CLK (SCK_POLARITY = 1, zero-cycle hold)	1.8	–	–	ns	

Table 26-33 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
TDM Receive Timing							
SID1005	t_{SR}	Setup on RX_SD/RX_FSYNC (WS) before the 1st edge following the driving edge of RX_CLK	0.2 × t_{SCLK}	–	–	ns	Guaranteed by Design Setup time is independent from RX_IF_CTL.LATE_SAMPLE, RX_IF_CTL.LATE_CAPTURE and SCK_POLARITY setting
SID1006C	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the 1st edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 1st edge (0.5 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 0
SID1006D	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the 2nd edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 2nd edge (1 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 1, RX_IF_CTL.LATE_CAPTURE = 0b00 RX-Slave: SCK_POLARITY = 1
SID1006E	t_{HR}	Hold on RX_SD/RX_FSYNC (WS) after the 3rd edge following the driving edge of RX_CLK	1.8	–	–	ns	Guaranteed by Design Sampling edge w.r.t driving edge of RX_SCLK: 3rd edge (1.5 x t_{SCLK}) RX-Master: RX_IF_CTL.LATE_SAMPLE = 0, RX_IF_CTL.LATE_CAPTURE = 0b01 RX Slave: Not Applicable
TDM Transition Timing							
SID1007B	t_{SCLK_TRANS}	SCLK transition timing	1	–	0.15 × t_{SCLK}	ns	Guaranteed by design
SID1008	t_{MCLK_TRANS}	MCLK transition timing	–	–	0.15 × t_{SCLK}	ns	Guaranteed by design
SID1009B	t_{DATA_TRANS}	DATA transition timing	1	–	0.15 × t_{SCLK}	ns	Guaranteed by design
(PCM) PWM							
Recommended I/O configuration: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_ENH:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_SMC:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID1100_1	t_{PW_1}	Pulse width on CH1_P, CH1_N, CH2_P, CH2_N for HSIO	8	–	–	ns	PWM clock ≤ 100 MHz, min pulse width nominal 10 ns – 20% max distortion Guaranteed by design
SID1100_2	t_{PW_2}	Pulse width on CH1_P, CH1_N, CH2_P, CH2_N for GPIO	20	–	–	ns	PWM clock ≤ 40 MHz, min pulse width nominal 25 ns – 20% max distortion Guaranteed by design
SID1101	f_{PWM}	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1110	t_{MCLK}	Master clock input period	10	–	–	ns	Guaranteed by design

Table 26-33 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1111	t_{MCLKI_DUTY}	Master clock input duty cycle	40	–	50	%	Guaranteed by design
Sound Generator							
Recommended I/O configuration: **GPIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **GPIO_SMC:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b011, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID1102	f_{PWM}	PWM sample frequency	15	–	60	kHz	Guaranteed by design
SID1103	t_{MCLK}	Master clock input period	10	–	–	ns	Guaranteed by design
SID1104	t_{MCLKI_DUTY}	Master clock input duty cycle	40	–	50	%	Guaranteed by design
AudioDAC							
SID1300	f_{CLKDA0}	System clock frequency	2.048	–	18.432	MHz	All parameters specified f_S = 44.1 kHz, system clock 256 × f_S and 16-bit data, R_L = 20 kΩ, C_L = 100 pF, unless otherwise noted
SID1301	f_S	Sampling clock	8	–	48	kHz	
SID1302	R_L	Analog output load resistance	20	–	–	kΩ	DAC_L, DAC_R
SID1303	C_L	Analog output load capacitance	–	–	100	pF	DAC_L, DAC_R
SID1304	C_{COM}	Com Capacitance	2.2	–	10	µF	C_L, C_R
SID1305	V_{OUT_MAX}	Analog output single-end output range (±full scale)	0.655 × V_{DDA_DAC}	0.673 × V_{DDA_DAC}	0.690 × V_{DDA_DAC}	V_{P-P}	DAC_L, DAC_R, R_L = 20 kΩ, C_L = 100 pF
SID1306	V_{OUT_ZERO}	Analog output voltage (zero)	0.49 × V_{DDA_DAC}	0.5 × V_{DDA_DAC}	0.51 × V_{DDA_DAC}	V	DAC_L, DAC_R
SID1307	THD + N	THD + N (Signal to Noise + Distortion ratio)	–	–82	–72	dB	These values do not include the noise caused by the analog power supply. Signal frequency: 1 kHz LPF (f_C: 20 kHz)
SID1308	SNR	Signal to Noise ratio	85	89	–	dB	These values do not include the noise caused by the analog power supply. Signal frequency: 1 kHz LPF (f_C: 20 kHz) A-weighting filter
SID1309	DR	Dynamic range	83	86	–	dB	These values do not include the noise caused by the analog power supply. Signal frequency: 1 kHz LPF (f_C: 20 kHz) A-weighting filter
SID1310	GAIN_MM	Gain mismatch between channels	–	–	0.4	dB	Signal frequency: 1 kHz
SID1312	CH_SEP	Channel Separation	–	80	–	dB	
SID1313	Z_{OUT}	Output impedance	150	200	250	Ω	
SID1314	PSRR_50	PSRR @ 50 Hz, digital input = 0	–	–35	–	dB	Digital input: zero noise 50 Hz

Table 26-33 Sound subsystem specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1315	PSRR_1K	PSRR @ 1 kHz, digital input = 0	–	–50	–	dB	Digital input: zero noise 1 kHz
SID1316	PSRR_20K	PSRR @ 20 kHz, digital input = 0	–	–40	–	dB	Digital input: zero noise 20 kHz
SID1318	I_{DD}	Supply current normal operation	–	2.2	3.2	mA	
SID1319	I_{DD_OFF}	Supply current power-down	–	1	100	µA	Typ: T_A = 25 °C, V_{DDA_DAC} = 5.0 V, process typ (TT) Max: T_A = 105 °C, V_{DDA_DAC} = 5.5 V, process worst (FF)
SID1320	t_{START}	Startup Time	–	–	70	ms	C_L and C_R should be 2.2 µF

26.13 CXPI specifications

Table 26-34 CXPI specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1400	f_{CLK_AHB}	CLK_PERI clock frequency	–	–	100	MHz	Guaranteed by design, AHB Interface clock
SID1402	t_{BIT_CONT}	Width of clock disparity against the bit width t_{BIT_REF} of nominal signaling rate	–0.5	–	+0.5	%	Guaranteed by design
SID1403	$t_{RX\_0\_HI\_CONT}$	The time that should be detected the receiving node is HIGH level.	0.02	–	–	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design
SID1404	$t_{TX\_DIF\_CONT}$	Difference of width of LOW-level at the constant threshold that receiving node should discriminate logic ‘1’ and logic ‘0’	0.05	–	–	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, Guaranteed by design $t_{TX\_DIF\_CONT} = t_{TX\_0\_LO} - t_{TX\_1\_LO}$
SID1405	$t_{TX\_0\_PD\_CONT}$[85]	At the time of logical value ‘0’ outputs, time from the LOW level detection of the communication bus unit falling the voltage “TH_dom”.	–	–	0.01	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, CTL0.FILTER_EN bit = '0', Guaranteed by design
SID1406	$t_{TX\_0\_PD\_CONT}$[85]	At the time of logical value ‘0’ outputs, time from the LOW-level detection of the communication bus unit falling the voltage “TH_dom”.	–	–	0.0125	t_{BIT}	$t_{BIT} = 1 / f_{BRC}$, CTL0.FILTER_EN bit = '1', Guaranteed by design
SID1407	$t_{RX\_0\_FF\_CONST}$	Delay from external serial data input pin to a flop. This is a standard to satisfy AC.11.	–	–	20	ns	Guaranteed by design

Note

[85] The AC spec according to CXPI controller specification is maximum 0.01 t_{BIT}. The AC spec, according to the CXPI system specification, including transceiver or driver/receiver is maximum 0.1 t_{BIT}.

Table 26-34 CXPI specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID1408	$t_{TX\_0\_FF\_CONST}$	Delay from a flop to external serial data output pin. This is a standard to satisfy AC.11.	–	–	80	ns	Guaranteed by design
SID1409	BR	Bit rate	–	–	20	kbps	
SID1411	OS	Oversampling factor	–	–	400		

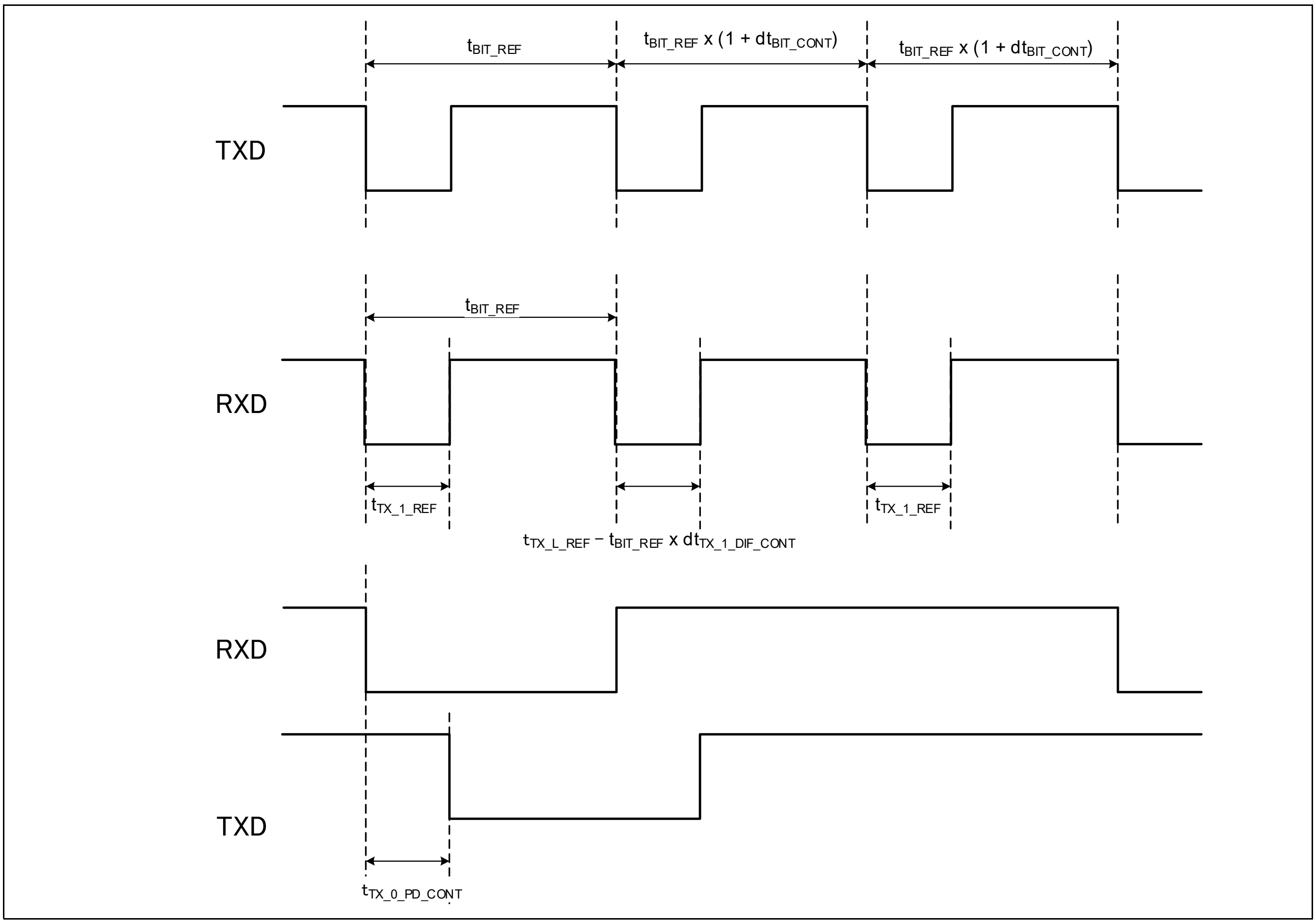


Figure 26-1 CXPI specifications

26.14 Serial memory interface specifications

Table 26-35 xSPI specifications

Spec ID	Parameter	Description	Min	Max	Min	Max	Min	Max	Units
xSPI (JEDEC JESD251)			**xSPI333**		**xSPI266**		**xSPI200**		
Recommended I/O configuration: **xSPI333: HSIO_ENH/1.8 V:** CFG_OUT2/DS_TRIM<2:0> = 0b110, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (dual slave [7.5 pF < load ≤ 15 pF]) **xSPI333: HSIO_ENH/1.8 V:** CFG_OUT2/DS_TRIM<2:0> = 0b100, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single slave [load ≤ 7.5 pF]) **xSPI266: HSIO_ENH/1.8 V:** CFG_OUT2/DS_TRIM<2:0> = 0b110, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (dual slave [7.5 pF < load ≤ 15 pF]) **xSPI266: HSIO_ENH/1.8 V:** CFG_OUT2/DS_TRIM<2:0> = 0b100, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single slave [load ≤ 7.5 pF]) **xSPI200: HSIO_ENH/1.8 V:** CFG_OUT2/DS_TRIM<2:0> = 0b110, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (dual slave [7.5 pF < load ≤ 15 pF]) **xSPI200: HSIO_ENH/1.8 V:** CFG_OUT2/DS_TRIM<2:0> = 0b100, CFG_SLEW_EXT/SLEW<0:0> = 0b0 (single slave [load ≤ 7.5 pF])									
SID1500	t_{CK}	Interface clock period (JEDEC)	6	–	7.5	–	10	–	ns
SID1500DS	t_{CK}	Interface clock period (JEDEC with slave DS)	6.8	–	7.5	–	10	–	ns
SID1500CM	t_{CK}	Interface clock period (CMOS)	6	–	7.5	–	10	–	ns
SID1501	t_{CKDCD}	Allowable clock distortion[86]	–	0.05 × t_{CK}	–	0.05 × t_{CK}	–	0.05 × t_{CK}	ns
SID1502	t_{CKMPW}	Minimum clock pulse width (JEDEC)	2.7	–	3.375	–	4.5	–	ns
SID1502DS	t_{CKMPW}	Minimum clock pulse width (JEDEC with slave DS)	3.06	–	3.375	–	4.5	–	ns
SID1502CM	t_{CKMPW}	Minimum clock pulse width (CMOS)	2.7	–	3.375	–	4.5	–	ns
SID1503	OUT_SR	Output slew rate with respect to V_{OH}/V_{OL}	0.94	–	0.75	–	0.56	–	V/ns
SID1504	t_{OSU}	Output setup time of DS and I/O[7:0] to CK	0.7	–	0.9	–	1.1	–	ns
SID1505	t_{OH}	Output hold time of DS and I/O[7:0] to CK	0.7	–	0.9	–	1.1	–	ns
SID1506	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	0.94	–	0.75	–	0.56	–	V/ns
SID1507	t_{DSMPW}	Input min pulse width of DS (JEDEC)	2.46	–	3.075	–	4.1	–	ns
SID1507CM	t_{DSMPW}	Input min pulse width of DS (CMOS)	2.46	–	3.075	–	4.1	–	ns
SID1508	t_{RQ}	Input DS to I/O[7:0] valid time (JEDEC)	–	0.54	–	0.675	–	0.9	ns
SID1508CM	t_{RQ}	Input DS to I/O[7:0] valid time (CMOS)	–	0.51	–	0.675	–	0.9	ns
SID1509	t_{RQH}	Input I/O[7:0] invalid to DS time (JEDEC)	–	0.54	–	0.675	–	0.9	ns
SID1509CM	t_{RQH}	Input I/O[7:0] invalid to DS time (CMOS)	–	0.51	–	0.675	–	0.9	ns
SID1511	t_{CKLCSL}	CK LOW to CS LOW	4.8	–	6	–	8	–	ns
SID1512	t_{CSLCKH}	CS LOW to CK HIGH	4.8	–	6	–	8	–	ns
SID1513	t_{CKLCSH}	CK LOW to CS HIGH	4.8	–	6	–	8	–	ns
SID1514	t_{CSHCKH}	CS HIGH to CK HIGH	4.8	–	6	–	8	–	ns
SID1515	t_{DSLCSH}	DS LOW to CS HIGH	4.8	–	6	–	8	–	ns
SID1516	t_{CSHDST}	CS HIGH to DS High-Z	–	6	–	7.5	–	10	ns
SID1517	t_{CSLDSL}	CS LOW to DS LOW	0	–	0	–	0	–	ns
SID1518	t_{DSTCSL}	DS High-Z to CS LOW	0	–	0	–	0	–	ns

Note

86. PLL#400 with SSCG = 0, fractional divider = off.

Table 26-36 xSPI (JEDEC JESD251) Tap/DLL setting requirement

Feature	xSPI333		xSPI266		xSPI200	
	Tx (MDL)	Rx (SDL)	Tx (MDL)	Rx (SDL)	Tx (MDL)	Rx (SDL)
Delay Tap Setting for SMIF0 (**Tx (MDL):** *SMIF_CORE_CTL2:MDL_TAP_SEL* **Rx (SDL):** *SMIF_CORE_DEVICE_RX_CAPTURE_CONFIG:NEG_SDL_TAP_SEL / POS_SDL_TAP_SEL*)	6	0	6	1	6	2
Delay Tap Setting for SMIF1 (**Tx (MDL):** *SMIF_CORE_CTL2:MDL_TAP_SEL* **Rx (SDL):** *SMIF_CORE_DEVICE_RX_CAPTURE_CONFIG:NEG_SDL_TAP_SEL / POS_SDL_TAP_SEL*)	6	0	6	1	6	2
DLL Speed Mode (*SMIF_CORE_CTL2:DLL_SPEED_MODE*)	2		1		1	

Table 26-37 Input, output supported voltage reference levels

Signal	Supported modes for voltage reference levels		
	CMOS	JEDEC	JEDEC with slave DS
Clock	$V_T = (50\% \times V_{DDIO\_SMIF})$		
RWDS (output)	$V_T = (50\% \times V_{DDIO\_SMIF})$		$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO\_SMIF}$
DQ[7:0] (output)	$V_T = (50\% \times V_{DDIO\_SMIF})$	$V_{OH}/V_{OL} = 70\% / 30\% \times V_{DDIO\_SMIF}$	
RWDS (input)	$V_T = (50\% \times V_{DDIO\_SMIF})$		
DQ[7:0] (input)	$V_T = (50\% \times V_{DDIO\_SMIF})$	$V_{IH}/V_{IL} = 70\% / 30\% \times V_{DDIO\_SMIF}$	

Notes

- One of the modes (“CMOS”, “JEDEC” or “JEDEC with slave DS”) needs to be selected depending on the requirements of the actual memory.
- Some parameters may be available and listed separately for the individual modes. The corresponding mode will be mentioned in the parameter description.
- Parameters without explicit mode description (e.g. t_{OSU}) are applicable for all modes but the voltage reference level as per the table still applies.
- If a parameter exists for “JEDEC” but not for “JEDEC with slave DS”, the “JEDEC” parameter also applies to “JEDEC with slave DS” (e.g. t_{RQ}).

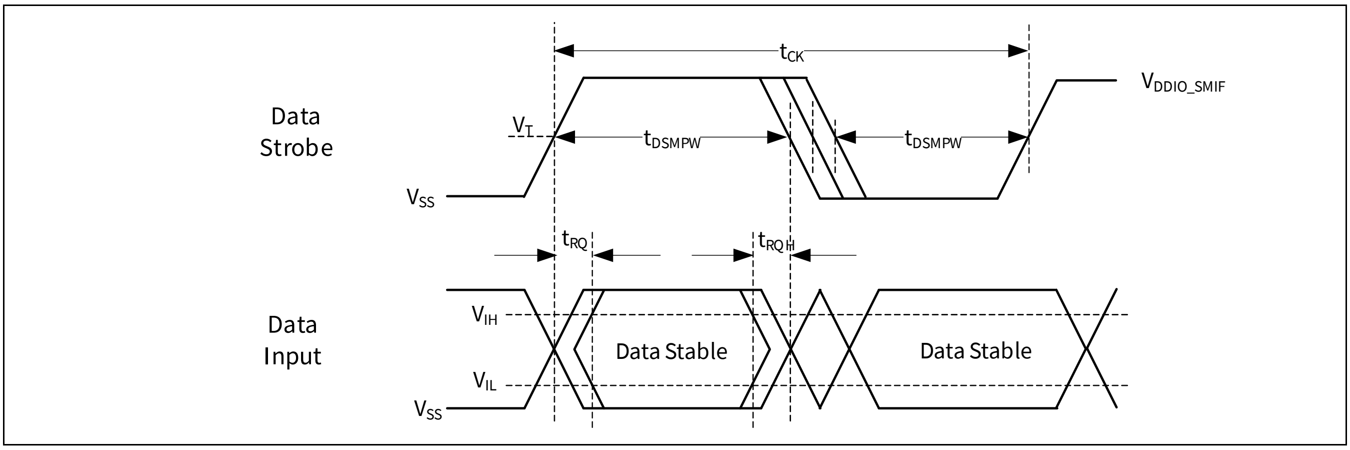


Figure 26-2 xSPI master data input timing reference level (JEDEC)

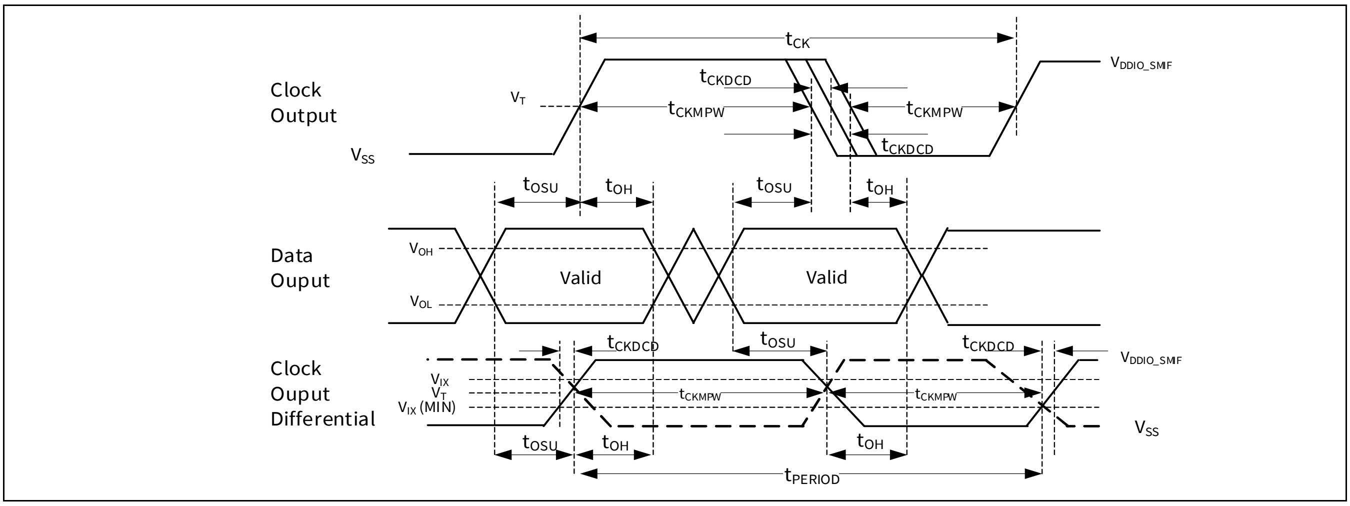


Figure 26-3 xSPI master data output timing reference level (JEDEC)

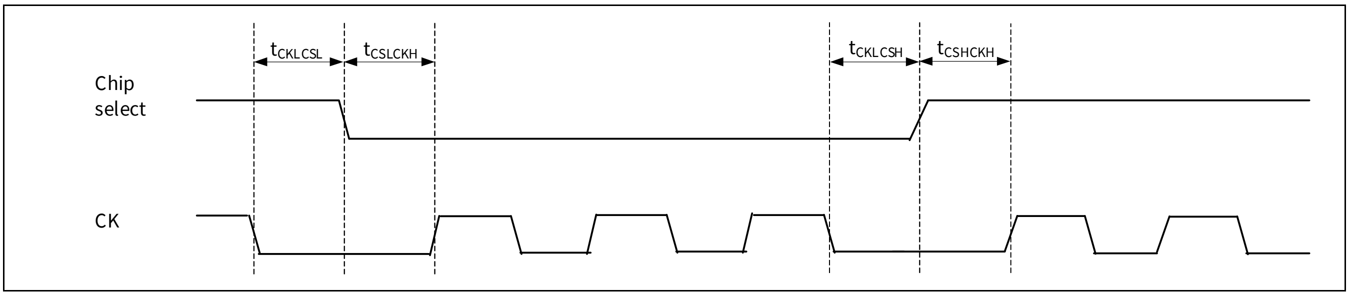


Figure 26-4 xSPI clock to chip select timing diagram

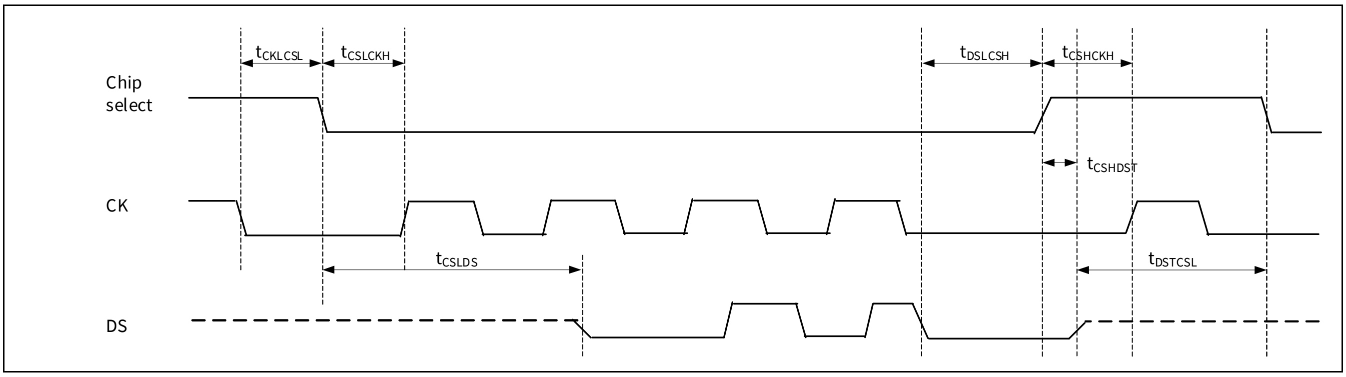


Figure 26-5 xSPI data strobe to chip select timing diagram

Table 26-38 SMIF specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
Standard SPI SDR							
Recommended configuration: **HSIO_ENH/1.8V I/O**: CFG_OUT2/DS_TRIM<2:0 = 0b110, CFG_SLEW_EXT/SLEW<0:0> = 0b0 SMIF_CORE_CTL2:TX_SDR_EXTRA_SETUP = 1 **DLL Tap settings for SMIF0/1:** SMIF_CORE_CTL2:MDL_TAP_SEL = 12 Following DLL Tap settings have to be used if DLP is not used: SMIF_CORE_DEVICE_RX_CAPTURE_CONFIG:NEG_SDL_TAP_SEL / POS_SDL_TAP_SEL = 8 All timings aligned with respect to $V_T = (50\% \times V_{DDIO\_SMIF})$.							
SID1600[87]	t_{CK}	Interface clock period	6	–	100	ns	15-pF output loads, at 1.8 V 160 MHz ≤ f_{DLL} ≤ 333 MHz
SID1601	t_{CKPW}	Clock pulse width	0.45 × t_{CK}	–	0.55 × t_{CK}	ns	15-pF output loads
SID1602_HS	t_{CSS}	CS# active setup to CK (f_{CK} > 50 MHz)	4	–	–	ns	15-pF output loads, f_{CK} > 50 MHz Guaranteed by design
SID1602_LS	t_{CSS}	CS# active setup to CK (f_{CK} ≤ 50 MHz)	5	–	–	ns	15-pF output loads, f_{CK} ≤ 50 MHz Guaranteed by design
SID1603	t_{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1604	t_{CSH3}	CS# active hold to CK (mode 3)	6	–	–	ns	15-pF output loads Guaranteed by design
SID1605[88]	t_{OSU}	Output setup time of DQ[7:0] to CK high (f_{CK} = 166 MHz)	2.1	–	–	ns	15-pF output loads, using 1.8 V
SID1606[89]	t_{OH}	Output hold time of DQ[7:0] to CK high (f_{CK} = 166 MHz)	2.1	–	–	ns	15-pF output loads, using 1.8 V
SID1607	t_{IN_V}	CK low to DQ[7:0] input valid time	1	–	6.7	ns	Only valid in DLP mode
SID1607B	t_{ISU}	DQ[7:0] input setup time	$t_{CK}/4 - 0.25$	–	–	ns	Only valid in non-DLP mode 160 MHz ≤ f_{DLL} ≤ 333 MHz 80 MHz ≤ f_{CK} ≤ 166 MHz SMIF0_COREx-_CTL2.CLKOUT_DIV = 0b00 (divide by 2) Reference CK edge: Fall (pos edge capture mode)

Note

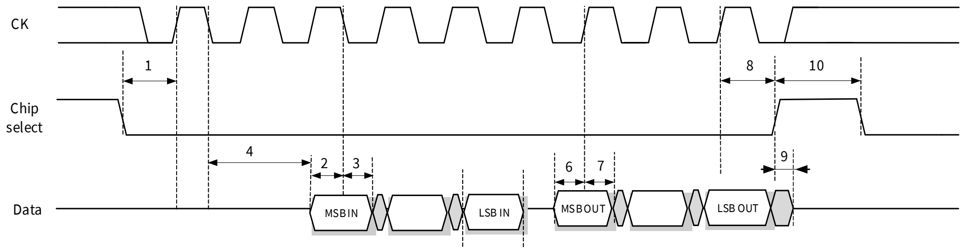
[87] Ensure to explicitly configure PLL#400 in Integer mode with "SSCG = OFF", "Fractional = OFF".

Table 26-38 SMIF specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID1607C	t_{ISU}	DQ[7:0] input setup time	$t_{CK}/2$	–	–	ns	Only valid in non-DLP mode 160 MHz ≤ f_{DLL} ≤ 320 MHz 10 MHz ≤ f_{CK} ≤ 80 MHz SMIF0_COREx-_CTL2.CLKOUT_DIV = [0b01, 0b10, 0b11] (divide by 4, 8, 16) Reference CK edge: Fall (pos edge capture mode)
SID1608	t_{IH}	DQ[7:0] input hold time	1.5	–	–	ns	Only valid in non-DLP mode 200 MHz < f_{DLL} ≤ 333 MHz 100 MHz < f_{CK} ≤ 166 MHz SMIF0_COREx-_CTL2.CLKOUT_DIV = 0b00 (divide by 2) Reference CK edge: Fall (pos edge capture mode)
SID1608A	t_{IH}	DQ[7:0] input hold time	1	–	–	ns	Only valid in non-DLP mode 160 MHz ≤ f_{DLL} ≤ 200 MHz 80 MHz ≤ f_{CK} ≤ 100 MHz SMIF0_COREx-_CTL2.CLKOUT_DIV = 0b00 (divide by 2) Reference CK edge: Fall (pos edge capture mode)
SID1608C	t_{IH}	DQ[7:0] input hold time	0	–	–	ns	Only valid in non-DLP mode 160 MHz ≤ f_{DLL} ≤ 320 MHz 10 MHz ≤ f_{CK} ≤ 80 MHz SMIF0_COREx-_CTL2.CLKOUT_DIV = [0b01, 0b10, 0b11] (divide by 4, 8, 16) Reference CK edge: Fall (pos edge capture mode)
SID1609A	t_{RDV}	Input data valid time of DQ[7:0]	(t_{CK} - t_{INV}), but at least 3.8 ns	–	–	ns	Only valid in DLP mode
SID1610	t_{CS}	CS# HIGH time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1610A	t_{CS}	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1610B	t_{CS}	CS# High time (Program / Erase)	50	–	–	ns	15-pF output loads Guaranteed by design

Table 26-38 **SMIF specifications** *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID1611	t_{DIS}	CS# inactive to output disable	–	–	8	ns	15-pF output loads
SID1612	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	1.125	–	–	V/ns	–
Standard SPI DDR							
Recommended I/O configuration: **HSIO_ENH/1.8V**: CFG_OUT2/DS_TRIM<2:0 = 0b110, CFG_SLEW_EXT/SLEW<0:0> = 0b0 **DLL Tap settings for SMIF0/1:** SMIF_CORE_CTL2:MDL_TAP_SEL = 6, DLP mode has to be used All timings aligned with respect to $V_T = (50\% \times V_{DDIO\_SMIF})$.							
SID1700[87]	t_{CK}	Interface clock period	10	–	12.5	ns	15-pF output loads 160 MHz ≤ f_{DLL} ≤ 200 MHz SMIF0_COREx-_CTL2.CLKOUT_DIV = 0b00 (divide by 2)
SID1701	t_{CKPW}	Clock pulse width	0.45 × t_{CK}	–	0.55 × t_{CK}	ns	15-pF output loads
SID1702_HS	t_{CSS}	CS# active setup to CK (f_{CK} > 50 MHz)	4	–	–	ns	15-pF output loads, f_{CK} > 50 MHz Guaranteed by design
SID1702_LS	t_{CSS}	CS# active setup to CK (f_{CK} ≤ 50 MHz)	5	–	–	ns	15-pF output loads, f_{CK} ≤ 50 MHz Guaranteed by design
SID1703	t_{CSH0}	CS# active hold to CK (mode 0)	4	–	–	ns	15-pF output loads Guaranteed by design
SID1705	t_{OSU}	Output setup time of DQ[7:0] to CK edge	2.1	–	–	ns	15-pF output loads
SID1706[90]	t_{OH}	Output hold time of DQ[7:0] to CK edge (f_{CK} = 100 MHz)	1.3	–	–	ns	15-pF output loads
SID1706B	t_{OH}	Output hold time of DQ[7:0] to CK edge (f_{CK} = 80 MHz)	1.6	–	–	ns	15-pF output loads
SID1707	t_{IN_V}	CK edge to DQ[7:0] input valid time	1	–	6.7	ns	–
SID1709	t_{RDV}	Input data valid time of DQ[7:0]	2.9	–	–	ns	–
SID1710	t_{CS}	CS# High time (Read)	10	–	–	ns	15-pF output loads Guaranteed by design
SID1710A	t_{CS}	CS# High time (Read when Reset feature and Quad mode are both enabled and aborted transaction)	20	–	–	ns	15-pF output loads Guaranteed by design
SID1710B	t_{CS}	CS# High time (Program/Erase)	50	–	–	ns	15-pF output loads Guaranteed by design
SID1711	t_{DIS}	CS# inactive to output disable	–	–	8	ns	15-pF output loads
SID1712	IN_SR	Input slew rate with respect to V_{IH}/V_{IL}	1.125	–	–	V/ns	–



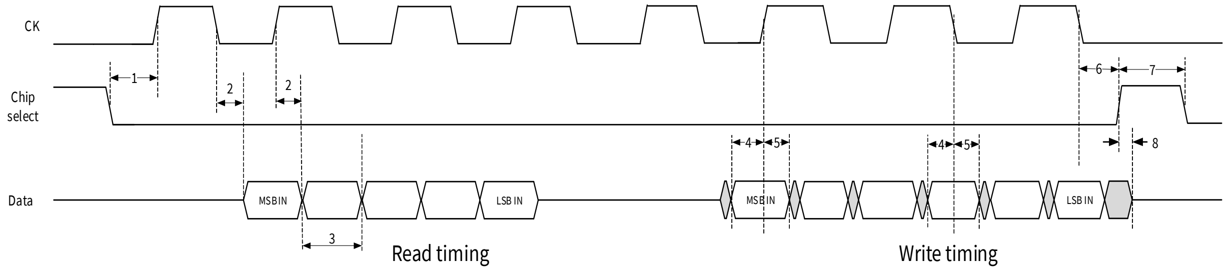
Read timing

Write timing

1: CS# active setup to CK = t_{CSS}
2: Data setup time = t_{ISU^*}
3: Data hold time = t_{IH^*}
4: CK low to DQ[7:0] input valid time = t_{IN_V}
5: Read data valid time of DQ[7:0] = t_{RDV}
6: Output setup of DQ[7:0] to CK rise = t_{OSU}
7: Output hold time of DQ[7:0] from CK rise = t_{OH}
8: CS# active hold to CK = t_{CSH}
9: CS# inactive to output disable = t_{DIS}
10: Chip select HIGH time = t_{CS}

**Note: Reference is CK falling edge for the pos capture mode*

Figure 26-6 SDR write and read timing diagram



Read timing

Write timing

1: CS# active setup to CK = t_{CSS}
2: CK edge to DQ[7:0] input valid time = t_{IN_V}
3: Read data valid time of DQ[7:0] = t_{RDV}
4: Output setup of DQ[7:0] to CK edge = t_{OSU}
5 Output hold time of DQ[7:0] from CK edge = t_{OH}
6: CS# active hold to CK = t_{CSH}
7: Chip select HIGH time = t_{CS}
8: CS# inactive to output disable = t_{DIS}

Figure 26-7 DDR write and read timing diagram

Notes

88. For other frequencies: $t_{OSU} = (13/16 \times t_{DLL}) - 0.3$ ns, t_{DLL} is the clock period of the input clock of the DLL.
89. For other frequencies: $t_{OH} = (13/16 \times t_{DLL}) - 0.3$ ns, t_{DLL} is the clock period of the input clock of the DLL.
90. For t_{OH} timing between 80 MHz and 100 MHz, use following formula: $t_{OH} = 2.8 - 0.015 \times f_{CK}$, where f_{CK} is the memory clock frequency in MHz, and t_{OH} is hold time in ns.

26.15 Graphics subsystem specifications

Table 26-39 Graphics specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Display Output - TTL Mode							
Recommended I/O configuration: **HSIO_STD:** CFG_OUT/DRIVE_SEL<1:0> = 0b01 **HSIO_STDLN:** CFG_DRIVE_EXT<1:0>/DRIVE_SEL_EXT<2:0> = 0b010, CFG_SLEW_EXT/SLEW<0:0> = 0b0							
SID866A	t_{DC1CYC}	Clock Cycle	12.5	–	–	ns	TTL_DSP1_CLOCK, C_L = 15 pF
SID873A	$t_{DC1CKPW}$	Clock pulse width	0.40 × t_{DC1CYC}	–	0.60 × t_{DC1CYC}	ns	TTL_DSP1_CLOCK pulse width, C_L = 15 pF
SID868A	t_{DC1S}	Data/Control output to TTL_DSP1_CLOCK time	4	–	–	ns	TTL_DSP1_DATA_A0[11-0] TTL_DSP1_DATA_A1[11-0] TTL_DSP1_CONTROL[11-0] (TCON for FPD-Link) C_L = 15 pF
SID869A	t_{DC1H}	TTL_DSP1_CLOCK to Data/Control valid time	2.5	–	–	ns	TTL_DSP1_DATA_A0[11-0] TTL_DSP1_DATA_A1[11-0] TTL_DSP1_CONTROL[11-0] (TCON for FPD-Link) C_L = 15 pF
SID890	$t_{DSP0\_CONTROL\_SKEW}$	TTL_DSP0_CONTROL skew	–	–	4	ns	Skew between signals TTL_DSP0_CONTROL[11-3] C_L = 15 pF
Display Capture							
Recommended I/O configuration: CFG_IN_AUTOLVL/VTRIP_SEL<0:0>= 0b0, CFG_IN/VTRIP_SEL<0:0> = 0b0							
SID875	$t_{CAP0CYC}$	Display capture Clock Cycle	12.5	–	–	ns	TTL_CAP0_CLK (HSIO)
SID876	t_{CAP0SU}	Display capture data setup time	1.9	–	–	ns	TTL_CAP0_DATA[35-0] (HSIO)
SID877	t_{CAP0HD}	Display capture data hold time	2.7	–	–	ns	TTL_CAP0_DATA[35-0] (HSIO)
FPD-Link							
FPD-Link should be used with PLL400 in Integer mode. All values are given with PLL400 with SSCG = OFF, Fractional divider = OFF							
SID880	I_{VDDA}	Total analog supply current in TX mode	–	–	30	mA	–
SID881	I_{VDDPLL}	Total PLL supply current in TX mode	–	–	4	mA	–
SID881B	I_{VDDHA}	Total I/O (LVDS driver) supply current in TX mode	–	–	91	mA	–
SID882	I_{VDDA_DPIX}	Total analog supply current in Dual-Pixel mode	–	–	60	mA	–
SID883	I_{VDDPLL_DPIX}	Total PLL supply current in Dual-Pixel mode	–	–	4	mA	–
SID883B	I_{VDDHA_DPIX}	Total I/O (LVDS driver) supply current in Dual-Pixel mode	–	–	182	mA	–
SID884	I_{VDDA_PD}	Total analog supply current in Power-Down mode	–	4	300	µA	Typ: T_A = 25°C, V_{DDA_FPD} = 1.15 V, process typ (TT) Max: T_A = 105°C, V_{DDA_FPD} = 1.21 V, process worst (FF)
SID884_1	$I_{VDDA\_PD\_1}$	Total analog supply current in Power-Down mode (room temp)	–	–	5	µA	Max: T_A = 25°C, V_{DDA_FPD} = 1.15 V (max VREG), process worst (FF)
SID884_2	$I_{VDDA\_PD\_2}$	Total analog supply current in Power-Down mode	–	–	40	µA	Max: T_A = 85°C, V_{DDA_FPD} = 1.15 V (max VREG), process worst (FF)
SID885	I_{VDDPLL_PD}	Total PLL supply current in Power-Down mode	–	3	200	µA	Typ: T_A = 25°C, V_{DDPLL_FPD} = 1.15 V, process typ (TT) Max: T_A = 105°C, V_{DDPLL_FPD} = 1.21 V, process worst (FF)

Table 26-39 Graphics specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID885_1	$I_{VDDPLL\_PD\_1}$	Total PLL supply current in Power-Down mode (room temp)	–	–	4	µA	Max: T_A = 25°C, V_{DDPLL_FPD} = 1.15 V (max VREG), process worst (FF)
SID885_2	$I_{VDDPLL\_PD\_2}$	Total PLL supply current in Power-Down mode	–	–	25	µA	Max: T_A = 85°C, V_{DDPLL_FPD} = 1.15 V (max VREG), process worst (FF)
SID885B	I_{VDDHA_PD}	Total I/O (LVDS driver) supply current in Power-Down mode	–	0.5	50	µA	Typ: T_A = 25°C, V_{DDHA_FPD} = 3.3 V, process typ (TT) Max: T_A = 105°C, V_{DDHA_FPD} = 3.6 V, process worst (FF)
SID885B_1	$I_{VDDHA\_PD\_1}$	Total I/O (LVDS driver) supply current in Power-Down mode (room temp)	–	–	1	µA	Max: T_A = 25°C, V_{DDHA_FPD} = 3.6 V (max VREG), process worst (FF)
SID885B_2	$I_{VDDHA\_PD\_2}$	Total I/O (LVDS driver) supply current in Power-Down mode	–	–	12	µA	Max: T_A = 85°C, V_{DDHA_FPD} = 3.6 V (max VREG), process worst (FF)
SID895	V_{OD}	Steady-state magnitude of the differential output voltage	247	350	454	mV	–
SID896	$V_{\Delta VOD\_M}$	Variation of signal swing voltage between drivers	–	–	25	mV	–
SID897	V_{CM}	Output Common-mode voltage	1.125	1.25	1.375	V	–
SID898	$V_{\Delta VCM\_M}$	Delta in Common-mode voltage between drivers	–	–	25	mV	–
SID899A	I_{SA}	Magnitude of current flowing through output terminal P when the output terminals are short-circuited to ground.	–	–	24	mA	See Figure 6 of “TIA/EIA-644-A” specifications.
SID899B	I_{SB}	Magnitude of current flowing through output terminal M when the output terminals are short-circuited to ground.	–	–	24	mA	See Figure 6 of “TIA/EIA-644-A” specifications.
SID899C	I_{OS}	Magnitude of current flowing through the output terminals when they are short-circuited to each other.	–	–	12	mA	See Figure 7 of “TIA/EIA-644-A” specifications.
SID900	t_{WAKE}	Wakeup time	–	–	1.2	ms	–
SID901	t_{PDD}	Power down delay time	–	–	100	µs	Guaranteed by design
SID902	f_{PX}	Configured pixel clock frequency	7	–	110	MHz	Guaranteed by design
SID903	f_{PX110}	Output clock frequency (110 MHz)	103.7	110	116.3	MHz	When transmitting an alternating 0/1 bit pattern
SID904	f_{PX55}	Output clock frequency (55 MHz)	52.35	55	57.65	MHz	When transmitting an alternating 0/1 bit pattern
SID905	f_{PX28}	Output clock frequency (28 MHz)	26.66	28	29.34	MHz	When transmitting an alternating 0/1 bit pattern
SID906	f_{PX14}	Output clock frequency (14 MHz)	13.28	14	14.72	MHz	When transmitting an alternating 0/1 bit pattern
SID907	f_{PX7}	Output clock frequency (7 MHz)	6.59	7	7.41	MHz	When transmitting an alternating 0/1 bit pattern
SID908	GAIN_JIT_LVDS	Gain region max long-term total jitter	–	–	0.32	UI2 p-p	–
SID909	ATTEN_JIT_LVDS	Attenuation region long-term total jitter	–	–	0.34	UI2 p-p	–
SID910	C2C_JIT	Cycle-to-cycle jitter	–	–	0.11	UI	–
SID911	t_{CSK}	Channel-to-channel skew of driver outputs	–	–	100	ps	–
SID913	TPPos0	Transmit Pulse Position Offset 0	–0.168	0	0.168	ns	–
SID914	TPPos1	Transmit Pulse Position Offset 1	T / 7 – TPPos0	T / 7	T / 7 + TPPos0	ns	–
SID915	TPPos2	Transmit Pulse Position Offset 2	2T / 7 – TPPos0	2T / 7	T / 7 + TPPos0	ns	–

Table 26-39 Graphics specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID916	TPPos3	Transmit Pulse Position Offset 3	3T / 7 – TPPos0	3T / 7	3T / 7 + TPPos0	ns	–
SID917	TPPos4	Transmit Pulse Position Offset 4	4T / 7 – TPPos0	4T / 7	4T / 7 + TPPos0	ns	–
SID918	TPPos5	Transmit Pulse Position Offset 5	5T / 7 – TPPos0	5T / 7	5T / 7 + TPPos0	ns	–
SID919	TPPos6	Transmit Pulse Position Offset 6	6T / 7 – TPPos0	6T / 7	6T / 7 + TPPos0	ns	–
SID920	t_{LLHT}	Differential driver rise time	–	–	390	ps	–
SID921	t_{LHLT}	Differential driver fall time	–	–	390	ps	–
SID922	t_{RF_MATCH}	Lane-to-lane rise/fall delta	–	–	40	ps	–
MIPI/DPHY							
SID1449	f_{PX_BGA}	Pixel clock frequency	–	–	220	MHz	–
SID1417	V_{CMRX}	Common-mode voltage HS receive mode	70	–	330	mV	–
SID1418	V_{IDTH}	Differential input HIGH threshold	70	–	–	mV	–
SID1419	V_{IDTL}	Differential Input LOW threshold	–	–	–70	mV	–
SID1420	V_{IHHS}	Single-ended input HIGH voltage	–	–	460	mV	–
SID1421	V_{ILHS}	Single-ended Input LOW voltage	–40	–	–	mV	–
SID1422	Z_{ID}	Differential Input Impedance	80	–	125	Ω	–
SID1423	V_{IH_LS}	Logic 1 input voltage LS	–	–	880	mV	–
SID1424	V_{IL_LS}	Logic 0 Input voltage LS	550	–	–	mV	–
SID1425	V_{HYST}	Input hysteresis	25	–	–	mV	–
SID1426	I_{LEAK}	Pin leakage current DPx, DNx, CLKP/N in LP mode	–100	–	100	µA	T_A = 85°C
SID1427	I_{VDDA_LP}	Current in LP	–	–	3	mA	–
SID1428	I_{VDDA_PD}	Current when D-PHY powered down	–	8	800	µA	Typ: T_A = 25°C, V_{DDA_MIPI} = 1.15 V, process typ (TT) Max: T_A = 105°C, V_{DDA_MIPI} = 1.21 V, process worst (FF)
SID1428_1	$I_{VDDA\_PD\_1}$	Current when D-PHY powered down (room temp)	–	–	20	µA	Max: T_A = 25°C, V_{DDA_MIPI} = 1.15 V (max VREG), process worst (FF)
SID1428_2	$I_{VDDA\_PD\_2}$	Current when D-PHY powered down	–	–	150	µA	Max: T_A = 85°C, V_{DDA_MIPI} = 1.15 V (max VREG), process worst (FF)
SID1429	I_{VDDA_ULP}	Current in ULP	–	–	2	mA	–
SID1430	I_{VDDA_HS}	current in HS	–	–	35	mA	–
SID1431	$t_{CLK\_TERM\_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	–	–	38	ns	–
SID1432	$t_{D\_TERM\_EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses, VIL,MAX	–	–	38	ns	–
SID1433	t_{CLK_SETTLE}	Time interval during which HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	–	300	ns	–
SID1434	$t_{HS\_SETTTLE}$	Time interval during which the HS receiver shall ignore any DATA Lane HS transitions, starting from the beginning of THSPREPARE. The HS receiver shall ignore any Data Lane transitions before minimum value, and the HS receiver shall respond to any Data Lane transitions after maximum value	85 + 6 × UI	–	145 + 10 × UI	ns	–

Table 26-39 Graphics specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1435	$t_{HS\text{-}SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	–	55 + 4 × UI	ns	–
SID1436	$V_{\Delta VCMRX\_HF}$	Common-mode interference	–	–	100	mV	Beyond 450 MHz
SID1437	$V_{\Delta VCMRX\_LF}$	Common-mode interference	–	–	50	mV	50 to 450 MHz
SID1438	C_{CM}	Common Mode termination	–	–	60	pF	–
SID1439	t_{E_SPIKE}	Input pulse rejection	–	–	300	ps	–
SID1440	t_{MIN_RX}	Minimum pulse width response	–	–	20	ns	–
SID1443	t_{SETUP_BGA}	Data to Clock setup time	0.2	–	–	UI	–
SID1444	t_{HOLD_BGA}	Clock to Data told time	0.2	–	–	UI	–
SID1445	$I_{VDDA\_1P4GBPS\_HS}$	Current in high speed max frequency	–	–	35	mA	–
SID1446	$I_{VDDA\_10M\_LP}$	Current in LP mode max frequency	–	–	2	mA	–

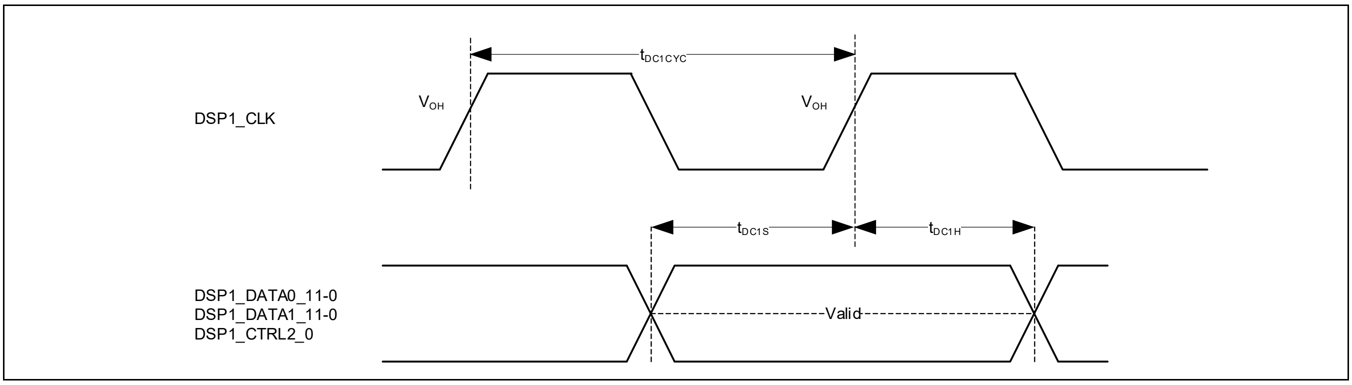


Figure 26-8 TTL display out timing

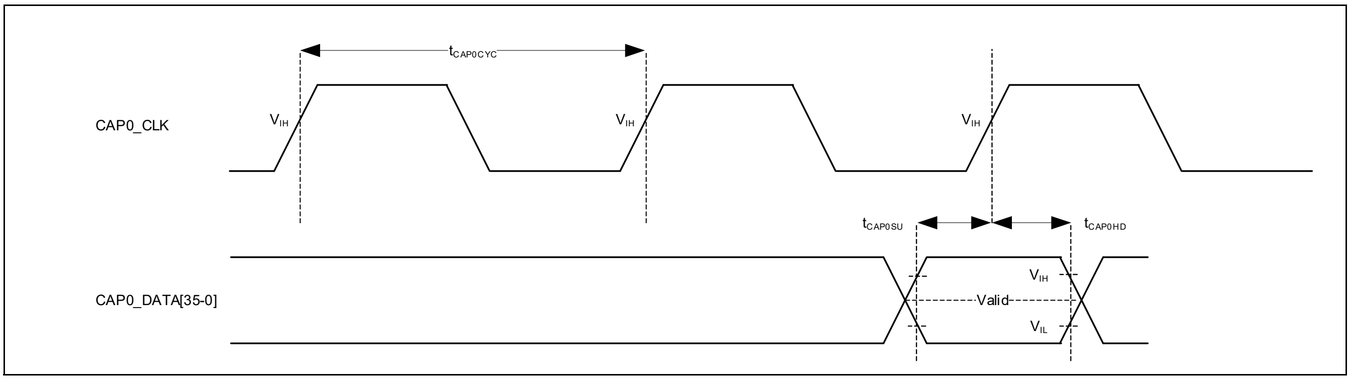


Figure 26-9 Video capture timing

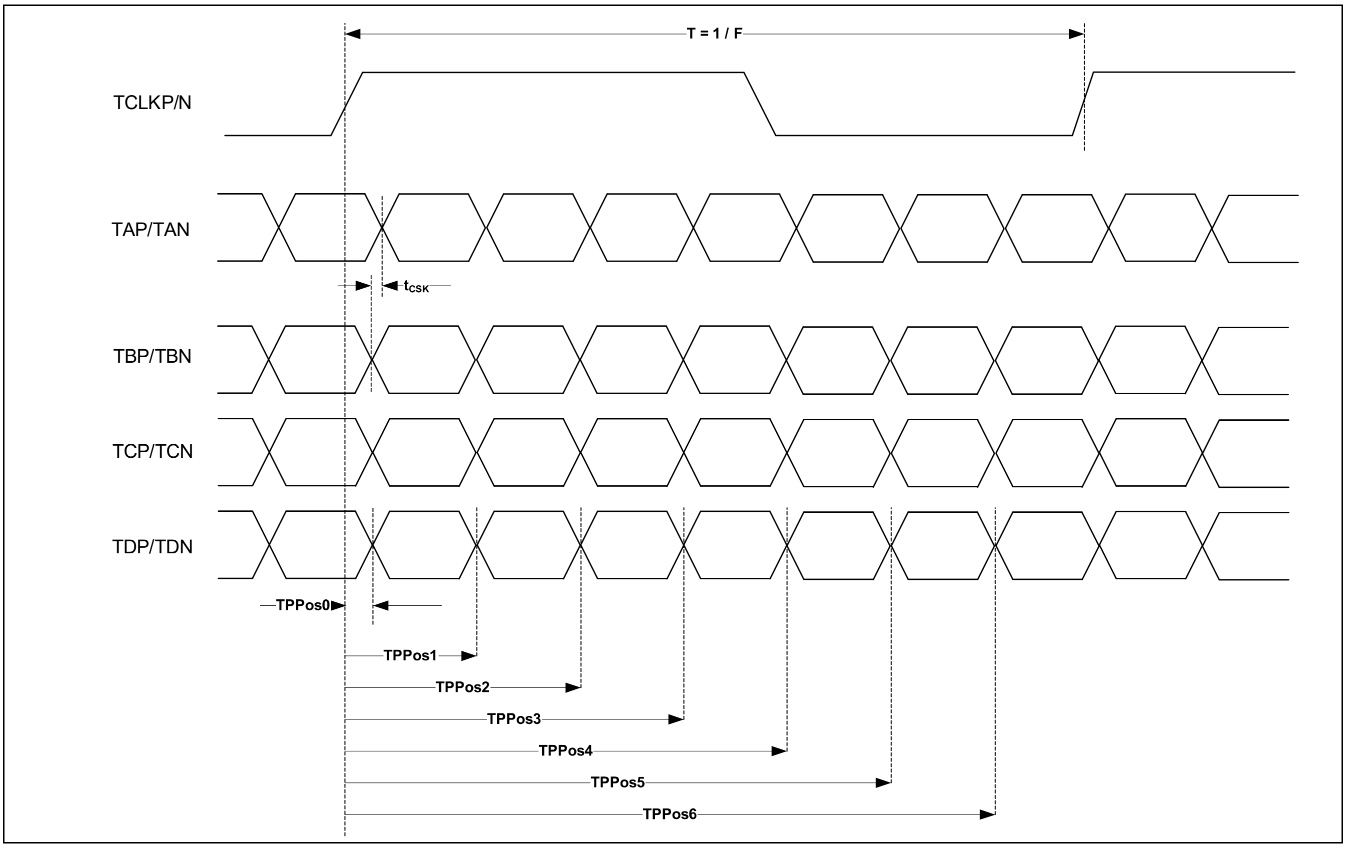


Figure 26-10 FPD-link output pulse position error and channel-to-channel skew

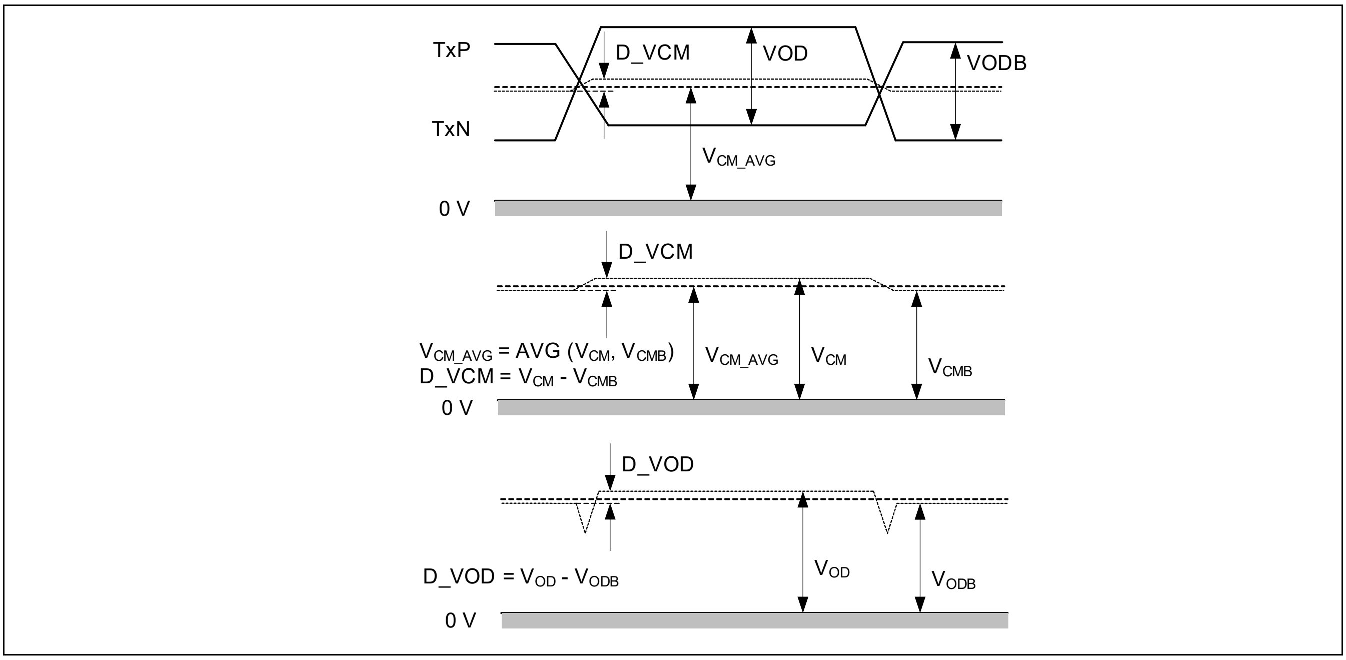


Figure 26-11 Skew between TxP and TxN, and steady-state differential amplitude and common-mode voltages

26.15.1 VIDEOSS capture timing groups

Table 26-40 lists the recommended capture signals segregated as groups, and only signals within a specific group can be used together. The AC timing of signals between different groups is not guaranteed.

Table 26-40 Capture timing groups

PIN	ACT#9	ACT#11
TTL_CAP0_CLK (SID875/80 MHz) - P15.6 (ACT#9) or P20.1 (ACT#11)		
P15.3	TTL_CAP0_DATA[26]	
P15.4		TTL_CAP0_DATA[25]
P15.5	TTL_CAP0_DATA[24]	
P15.7	TTL_CAP0_DATA[0]	TTL_CAP0_DATA[23]
P16.0	TTL_CAP0_DATA[22]	TTL_CAP0_DATA[1]
P16.1	TTL_CAP0_DATA[2]	TTL_CAP0_DATA[21]
P16.2	TTL_CAP0_DATA[20]	TTL_CAP0_DATA[3]
P16.3	TTL_CAP0_DATA[4]	TTL_CAP0_DATA[19]
P16.4	TTL_CAP0_DATA[18]	TTL_CAP0_DATA[5]
P16.5	TTL_CAP0_DATA[6]	TTL_CAP0_DATA[17]
P16.6	TTL_CAP0_DATA[16]	TTL_CAP0_DATA[7]
P16.7	TTL_CAP0_DATA[8]	TTL_CAP0_DATA[15]
P17.0	TTL_CAP0_DATA[14]	TTL_CAP0_DATA[9]
P18.0	TTL_CAP0_DATA[10]	TTL_CAP0_DATA[13]
P18.1	TTL_CAP0_DATA[12]	TTL_CAP0_DATA[11]
P18.2	TTL_CAP0_DATA[12]	TTL_CAP0_DATA[11]
P18.3	TTL_CAP0_DATA[10]	TTL_CAP0_DATA[13]
P18.4	TTL_CAP0_DATA[14]	TTL_CAP0_DATA[9]
P18.5	TTL_CAP0_DATA[8]	TTL_CAP0_DATA[15]
P18.6	TTL_CAP0_DATA[16]	TTL_CAP0_DATA[7]
P18.7	TTL_CAP0_DATA[6]	TTL_CAP0_DATA[17]
P19.0	TTL_CAP0_DATA[18]	TTL_CAP0_DATA[5]
P19.1	TTL_CAP0_DATA[4]	TTL_CAP0_DATA[19]
P19.2	TTL_CAP0_DATA[20]	TTL_CAP0_DATA[3]
P19.3	TTL_CAP0_DATA[2]	TTL_CAP0_DATA[21]
P19.4	TTL_CAP0_DATA[22]	TTL_CAP0_DATA[1]
P19.5	TTL_CAP0_DATA[0]	TTL_CAP0_DATA[23]
P19.6	TTL_CAP0_DATA[24]	
P19.7		TTL_CAP0_DATA[25]
P20.0	TTL_CAP0_DATA[26]	

27 Ordering information

The CYT4DN microcontroller part numbers and features are listed in **Table 27-1**.

Table 27-1 CYT4DN ordering information[91]

Device code	Ordering code	Package	CM7 cores	Code-flash (KB)	Work-flash (KB)	RAM (KB)	ADC channels	SCB	CAN FD	LIN	CXPI	Ethernet channels	SMIF	Audio DAC	MIPI	JPEGDEC	Temperature grade	JTAG ID code
CYT4DNJBAS	CYT4DNJBACQ1BZSGS	327-BGA	2	6336[93]	128[94]	640	48	12	4	2	2	1	1	0	0	No	S[95]	0x2E811069[96]
CYT4DNJBBS	CYT4DNJBBCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	0	0	No	S	0x2E812069
CYT4DNJBCS	CYT4DNJBCCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	0	1	No	S	0x2E813069
CYT4DNJBDS	CYT4DNJBDCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	0	1	No	S	0x2E814069
CYT4DNJBES	CYT4DNJBECQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	1	0	No	S	0x2E815069
CYT4DNJBFS	CYT4DNJBFCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	1	0	No	S	0x2E816069
CYT4DNJBGS	CYT4DNJBGCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	1	1	No	S	0x2E817069
CYT4DNJBHS	CYT4DNJBHCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	1	1	No	S	0x2E818069
CYT4DNJBJS	CYT4DNJBJCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	0	0	Yes	S	0x2E819069
CYT4DNJBKS	CYT4DNJBKCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	0	0	Yes	S	0x2E81A069
CYT4DNJBLS	CYT4DNJBLCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	0	1	Yes	S	0x2E81B069
CYT4DNJBMS	CYT4DNJBMCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	0	1	Yes	S	0x2E81C069
CYT4DNJBNS	CYT4DNJBNCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	1	0	Yes	S	0x2E81D069
CYT4DNJBPS	CYT4DNJBPCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	1	0	Yes	S	0x2E81E069
CYT4DNJBQS	CYT4DNJBQCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	1	1	1	Yes	S	0x2E81F069
CYT4DNJBRS[92]	CYT4DNJBRCQ1BZSGS	327-BGA	2	6336	128	640	48	12	4	2	2	1	2	1	1	Yes	S	0x2E820069

Notes

[91] Supported shipment types are “Tray” (default) and “Tape and Reel”. Add the character ‘T’ at the end to get the ordering code for “Tape and Reel” shipment type.

[92] This part is available as an engineering sample.

[93] Code-flash size 6336 KB = 32 KB × 190 (Large Sectors) + 8 KB × 32 (Small Sectors).

[94] Work-flash size 128 KB = 2 KB × 48 (Large Sectors) + 128 B × 256 (Small Sectors).

[95] S-grade Temperature (–40°C to 105°C).

[96] JTAG ID CODE bits 12 through 27, represents the Silicon ID of the device.

27.1 Part number nomenclature

Table 27-2 Device code nomenclature

Field	Description	Value	Meaning			
CY	Cypress prefix	CY				
T	Category	T	TRAVEO™			
F	Family name	4	TRAVEO™ T2G (Core M7 dual)			
A	Application	D	Cluster with 2D Graphics			
D	Code-flash/Work-flash/SRAM quantity	N	6336 KB / 128 KB / 640 KB			
P	Packages	J	327-BGA			
H	Hardware option	B	Security on (HSM), RSA - 3K			
I	Marketing option		**JPEG**	**Audio DAC**	**MIPI**	**2 x SMIF**
		A	No	No	No	No
		B	No	No	No	Yes
		C	No	No	Yes	No
		D	No	No	Yes	Yes
		E	No	Yes	No	No
		F	No	Yes	No	Yes
		G	No	Yes	Yes	No
		H	No	Yes	Yes	Yes
		J	Yes	No	No	No
		K	Yes	No	No	Yes
		L	Yes	No	Yes	No
		M	Yes	No	Yes	Yes
		N	Yes	Yes	No	No
		P	Yes	Yes	No	Yes
		Q	Yes	Yes	Yes	No
		R	Yes	Yes	Yes	Yes
C	Temperature grade	S	S-grade (–40°C to 105°C)			

Table 27-3 Ordering code nomenclature

Field	Description	Value	Meaning			
CY	Cypress prefix	CY				
T	Category	T	TRAVEO™			
F	Family name	4	TRAVEO™ T2G (Core M7 dual)			
A	Application	D	Cluster with 2D Graphics			
D	Code-flash/Work-flash/SRAM quantity	N	6336 KB / 128 KB / 640 KB			
P	Packages	J	327-BGA			
H	Hardware option	B	Security on (HSM), RSA - 3K			
I	Marketing option		**JPEG**	**Audio DAC**	**MIPI**	**2 x SMIF**
		A	No	No	No	No
		B	No	No	No	Yes
		C	No	No	Yes	No
		D	No	No	Yes	Yes
		E	No	Yes	No	No
		F	No	Yes	No	Yes
		G	No	Yes	Yes	No
		H	No	Yes	Yes	Yes
		J	Yes	No	No	No
		K	Yes	No	No	Yes
		L	Yes	No	Yes	No
		M	Yes	No	Yes	Yes
		N	Yes	Yes	No	No
		P	Yes	Yes	No	Yes
		Q	Yes	Yes	Yes	No
		R	Yes	Yes	Yes	Yes
R	Revision	A	First revision (0x11)			
		B	Second revision (0x21)			
		C	Third revision (0x22)			
F	Fab location	Q	UMC (Fab 12i) Singapore			
X	Reserved	1	Reserved			
K	Package code	BZ	BGA			
C	Temperature grade	A	A-grade (–40 °C to 85 °C)			
		S	S-grade (–40 °C to 105 °C)			
Q	Quality grade	ES	Engineering samples			
		GS	Standard grade of automotive			
S	Shipment type	Blank	Tray shipment			
		T	Tape and Reel shipment			

28 Packaging

CYT4DN microcontroller is offered in the packages listed in the **Table 28-1**.

Table 28-1 Package information

Package	Dimensions[97]	Contact/Lead Pitch	Coefficient of Thermal Expansion	I/O Pins
327-BGA	17 × 17 × 1.70 mm (max)	0.8-mm	a1[98] = 6 ppm/°C, a2[99] = 25 ppm/°C	168

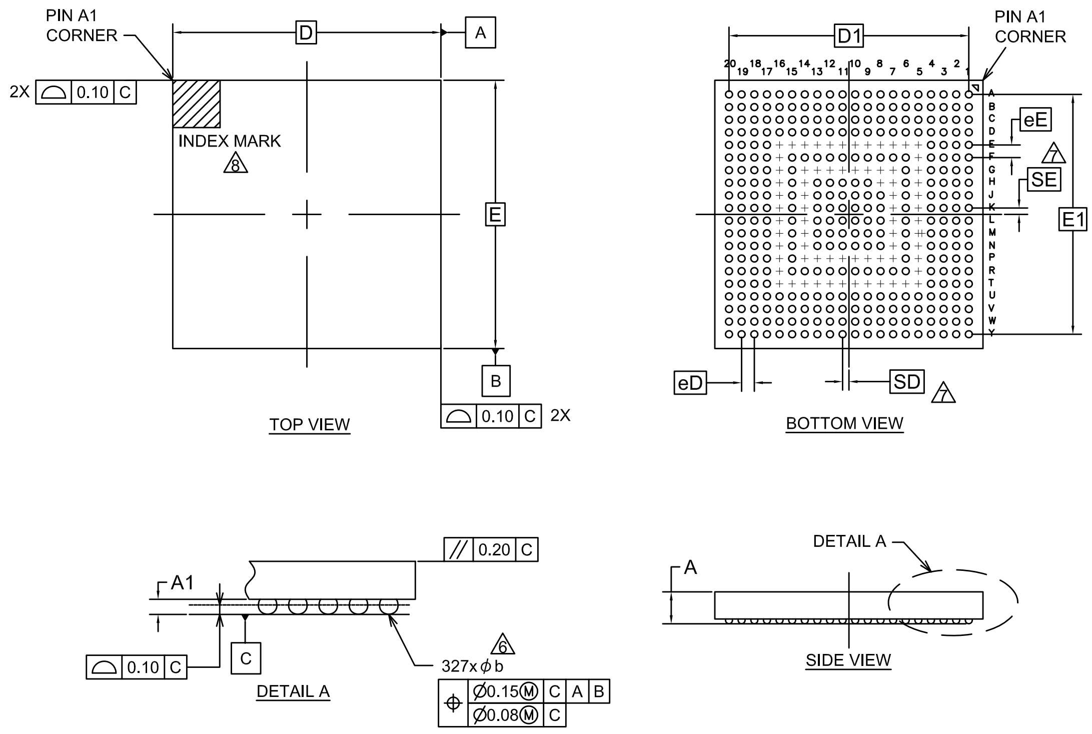
Table 28-2 Package characteristics[100]

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	A-grade	–40	–	85	°C
T_A	Operating ambient temperature	S-grade	–40	–	105	°C
T_J	Operating junction temperature	–	–	–	150	°C
$R_{\theta JA}$	Package thermal resistance, junction to ambient θ_{JA}[101]	327-BGA	–	–	14.8	°C/Watt
$R_{\theta JB}$	Package thermal resistance, junction to board θ_{JB}	327-BGA	–	–	9.9	°C/Watt
$R_{\theta JC}$	Package thermal resistance, junction to case θ_{JC}	327-BGA	–	–	2.1	°C/Watt

Table 28-3 Solder reflow peak temperature, Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	Maximum peak temperature (°C)	Maximum time at peak temperature (seconds)	MSL
327-BGA	260	30	3

Notes
[97] The dimensions (column 2) are valid for room temperature.
[98] a1 = CTE (Coefficient of Thermal Expansion) value below T_g (ppm/°C) (T_g is glass transition temperature which is 131°C).
[99] a2 = CTE value above T_g (ppm/°C).
[100] Board condition complies to JESD51-7(4 Layers).
[101] The T_A and T_J values for the packages will be provided in a later revision of the datasheet.



<table>
<tr><th rowspan="2">SYMBOL</th><th colspan="3">DIMENSIONS</th></tr>
<tr><th>MIN.</th><th>NOM.</th><th>MAX.</th></tr>
<tr><td>A</td><td>-</td><td>-</td><td>1.70</td></tr>
<tr><td>A1</td><td>0.30</td><td>-</td><td>-</td></tr>
<tr><td>D</td><td colspan="3">17.00 BSC</td></tr>
<tr><td>E</td><td colspan="3">17.00 BSC</td></tr>
<tr><td>D1</td><td colspan="3">15.20 BSC</td></tr>
<tr><td>E1</td><td colspan="3">15.20 BSC</td></tr>
<tr><td>MD</td><td colspan="3">20</td></tr>
<tr><td>ME</td><td colspan="3">20</td></tr>
<tr><td>n</td><td colspan="3">327</td></tr>
<tr><td>Φb</td><td>0.40</td><td>0.45</td><td>0.50</td></tr>
<tr><td>eD</td><td colspan="3">0.80 BSC</td></tr>
<tr><td>eE</td><td colspan="3">0.80 BSC</td></tr>
<tr><td>SD / SE</td><td colspan="3">0.40 BSC</td></tr>
</table>

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. JEDEC SPECIFICATION NO. REF. : N/A.

002-28943 **

Figure 28-1 327-ball FBGA package outline (PG-LFBGA-327-800)

29 Appendix

29.1 External IP revisions

Table 29-1 External IP revisions

Module	IP	Revision	Vendor
CANFD	mxttcanfd	M_TTCAN IP revision: Rev.3.2.3	Bosch
Arm® Cortex®-M0+	armcm0p	Cortex-M0+-r0p1	Arm®
Arm® Cortex®-M7	armcm7	Cortex-M7-r1p2	Arm®
Arm® Coresight	armcoresighttk	CoreSight-SoC-TM100-r3p2	Arm®
Ethernet	mxeth	GEM_GXL r1p09	Cadence

29.2 Internal IP revisions

Table 29-2 Internal IP revisions

Module	Revision
SMIF	SMIF version 3.0 (Rev. A), and version 4.0 (Rev. B onwards)

29.3 MIPI formats supported

Table 29-3 MIPI formats supported

MIPI Format	ID	Remarks
YUV422 8-bit	0x1E	Full processing supported
YUV422 10-bit	0x1F	
RGB888	0x24	
RGB666	0x23	
RGB565	0x22	
RGB555	0x21	
RGB444	0x20	
RAW8	0x2A	Data can be written to VRAM as is, no color processing or format conversion supported.
RAW10	0x2B	
RAW12	0x2C	
RAW14	0x2D	
RAW16	0x2E	
RAW20	0x2F	
Generic 8-bit Long Packet Data Types	0x10	Supported
	0x11	Data can be written to VRAM as is, no color processing or format conversion supported.
	0x12	
User Defined Byte-based Data	0x30 - 0x37	Data can be written to VRAM as is, no color processing or format conversion supported.

30 Acronyms

Table 30-1 Acronyms used in the document

Acronym	Description	Acronym	Description
A/D	Analog to Digital	POR	Power-on reset
ABS	Absolute	PPU	Peripheral protection unit
ADC	Analog to Digital converter	PRNG	Pseudo-random number generator
AES	Advanced encryption standard	PSoC™	Programmable system on chip
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus	PWM	Pulse-width modulation
Arm®	Advanced RISC machine, a CPU architecture	MCU	Microcontroller Unit
ASIL	Automotive safety integrity level	MCWDT	Multi-counter watchdog timer
BOD	Brown-out detection	M-DMA	Memory-Direct Memory Access
CAN FD	Controller Area Network with Flexible Data rate	MISO	Master-in slave-out
CMOS	Complementary metal-oxide-semiconductor	MMIO	Memory mapped I/O
CPU	Central Processing Unit	MOSI	Master-out slave-in
CRC	Cyclic redundancy check, an error-checking protocol	MPU	Memory protection unit
CSV	Clock supervisor	NVIC	Nested vectored interrupt controller
DES	Data encryption standard	RAM	Random access memory
DW	Datawire same as P-DMA	RISC	Reduced-instruction-set computing
ECC	Error correcting code	ROM	Read only memory
ECO	External crystal oscillator	RTC	Real-time clock
ETM	Embedded Trace Macrocell	SAR	Successive approximation register
FLL	Frequency Locked Loop	SCB	Serial communication block
FPU	Floating point unit	SCL	I^2C serial clock
GHS	Green hills tool chain with IDE	SDA	I^2C serial data
GPIO	General purpose input/output	SHA	Secure hash algorithm
HSM	Hardware security module	SHE	Secure hardware extension
I/O	Input/output	SMPU	Shared memory protection unit
I^2C	Inter-Integrated Circuit, a communications protocol	SPI	Serial peripheral interface, a communications protocol
ILO	Internal low-speed oscillator	SRAM	Static random access memory
IMO	Internal main oscillator	SWD	Single wire debug
IPC	Inter-processor communication	TCM	Tightly Coupled Memory
IrDA	Infrared interface	TCPWM	Timer/Counter Pulse-width modulator
IRQ	Interrupt request	TTL	Transistor-transistor logic
JTAG	Joint test action group	TRNG	True random number generator
LIN	Local Interconnect Network, a communications protocol	UART	Universal Asynchronous Transmitter Receiver, a communications protocol
LVD	Low voltage detection	WCO	Watch crystal oscillator
OTA	Over-the-air programming	WDT	Watchdog timer reset

Table 30-1 Acronyms used in the document *(continued)*

Acronym	Description	Acronym	Description
OTP	One-time programmable	XIP	eXecute In Place
OVD	Over voltage detection	XTAL	Crystal
P-DMA	Peripheral-Direct Memory Access	PASS	Programmable Analog Subsystem
PLL	Phase Locked Loop		

31 Errata

This section describes the errata for the CYT4DN product family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Infineon Sales Representative if you have questions.

Part numbers affected

Part number
All CYT4DN parts

CYT4DN qualification status

Production samples

CYT4DN errata summary

The following table defines the errata applicability to available CYT4DN family devices.

Items	Errata ID	CYT4DN	Silicon Rev.	Fix status
[1.] **CAN FD RX FIFO top pointer feature does not function as expected**	96	CYT4DNJBACQ1BZSGS CYT4DNJBBCQ1BZSGS CYT4DNJBCCQ1BZSGS CYT4DNJBDCQ1BZSGS CYT4DNJBECQ1BZSGS CYT4DNJBFCQ1BZSGS CYT4DNJBGCQ1BZSGS CYT4DNJBHCQ1BZSGS CYT4DNJBJCQ1BZSGS CYT4DNJBKCQ1BZSGS CYT4DNJBLCQ1BZSGS CYT4DNJBMCQ1BZSGS CYT4DNJBNCQ1BZSGS CYT4DNJBPCQ1BZSGS CYT4DNJBQCQ1BZSGS CYT4DNJBRCQ1BZSGS	C	No silicon fix planned. Use workaround.
[2] **CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set**	97			No silicon fix planned. Use workaround.
[3] **No YUV422 allowed in Direct Capture Mode**	153			No silicon fix planned. Use workaround.
[4] **SWRESET register field of VIDEOSS0_TCONx_SWRESET violates the spec**	172			No silicon fix planned. Use workaround.
[5] **Crypto ECC errors may be set after boot with application authentication**	185			No silicon fix planned. TRM was updated.
[6] **Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode**	198			Fixed to update the Flash settings, from the date code 312xxxxx.
[7] **Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep**	199			No silicon fix planned. TRM was updated.
[8] **A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM**	201			No silicon fix planned. Register TRM was updated.
[9] **Limitation of clock configuration before entering DeepSleep mode**	202			No silicon fix planned. TRM was updated.
[10] **Several data retention information in Register TRM are incorrect**	203			No silicon fix planned. Register TRM was updated.
[11] **SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally**	204			No silicon fix planned. Register TRM was updated.
[12] **Conditions in datasheet for standard SMIF SDR mode extended**	205			No silicon fix planned. Datasheet was updated to add the new recommended configuration (SMIFx_COREy_CTL2.TX_SDR_EXTRA_SETUP = 1).
[13] **Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode**	206			No silicon fix planned. TRM will be updated.
[14] **CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete**	209			No silicon fix planned. Use workaround.

Items	Errata ID	CYT4DN	Silicon Rev.	Fix status
[15] **Update of root and intermediate clocks table in datasheet**	211	CYT4DNJBACQ1BZSGS CYT4DNJBBCQ1BZSGS CYT4DNJBCCQ1BZSGS CYT4DNJBDCQ1BZSGS CYT4DNJBECQ1BZSGS CYT4DNJBFCQ1BZSGS CYT4DNJBGCQ1BZSGS CYT4DNJBHCQ1BZSGS CYT4DNJBJCQ1BZSGS CYT4DNJBKCQ1BZSGS CYT4DNJBLCQ1BZSGS CYT4DNJBMCQ1BZSGS CYT4DNJBNCQ1BZSGS CYT4DNJBPCQ1BZSGS CYT4DNJBQCQ1BZSGS CYT4DNJBRCQ1BZSGS	C	No silicon fix planned. Datasheet was updated.
[16] **Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM**	212			No silicon fix planned. Datasheet was updated. TRM will be updated.

1. CAN FD RX FIFO top pointer feature does not function as expected

Problem definition	RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should be re-start back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not re-start back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA to read messages from the wrong address in Message RAM.
Parameters affected	N/A
Trigger condition(s)	RX FIFO top pointer function is used when RX FIFO n size set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).
Scope of impact	Received message cannot be correctly read by using RX FIFO top pointer function, when RX FIFO n size set to 1 element.
Workaround	Any of the following. 1) Set RX FIFO n size to 2 or more when using RX FIFO top pointer function. 2) Do not use RX FIFO top pointer function when RX FIFO n size set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.
Fix status	No silicon fix planned. Use workaround.

2. CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set

Problem definition	If either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters Bus-off state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.
Parameters affected	N/A
Trigger condition(s)	Either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters Bus-off state.
Scope of impact	The errata is limited to the use case when the Debug on CAN functionality is active. Normal operation of CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the bit CANFD_CH_RXF1S.DMS. In case CANFD_CH_RXF1S.DMS is set to 0b11, DMA request remains active. Bosch classifies this as non-critical error with low severity, there is no fix for the IP. Bosch recommends the workaround listed also here.

Workaround	In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.
Fix status	No silicon fix planned. Use workaround.

3. No YUV422 allowed in Direct Capture Mode	
Problem definition	When VIDEOSS is operating in Direct Capture Mode (video input data goes directly to a display without frame buffer interaction) the YUV 4:2:2 to 4:4:4 up-sampling function is corrupting video in a way that prevents the display engine to properly synchronize.
Parameters affected	N/A
Trigger condition(s)	RASTERMODE = YUV422 in ExtScr4 when destination is ExtDst4 and not Store4 unit.
Scope of impact	YUV422 cannot be used as a color format for video sources in video feed-through applications.
Workaround	Use capture to display with frame buffers or use video source with RGB or YUV444 format.
Fix status	No silicon fix planned. Use workaround.

4. SWRESET register field of VIDEOSS0_TCONx_SWRESET violates the spec	
Problem definition	1. Some devices might have wrong reset values upon reset. 2. The SWRESET field read as zero indicates TCON registers being at reset state. However, according to the spec, a value of one being read on SWRESET field should indicate the reset state. 3. When TCON enters reset, not all registers are reset.
Parameters affected	N/A
Trigger condition(s)	On system reset and while writing to the SWRESET register.
Scope of impact	No impact since the register is not used by the software for debug and not used in customer applications
Workaround	Write only zero to the SWRESET register field to not trigger the reset active state. This register should not be used at all since other register fields of this register are for miniLVDS and this feature is not supported.
Fix status	No silicon fix planned. Use workaround.

5. Crypto ECC errors may be set after boot with application authentication	
Problem definition	Due to the improper initialization of the Crypto memory buffer, Crypto ECC errors may be set after boot with application authentication.
Parameters affected	N/A
Trigger condition(s)	Boot device with application authentication.
Scope of impact	Crypto ECC errors may be set after boot with application authentication.
Workaround	Clear or ignore Crypto ECC errors which generated during boot with application authentication.
Fix status	No silicon fix planned. TRM was updated.

6. Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode	
Problem definition	Code Flash memory can be erased in “Non-Blocking” mode; a Non-Blocking mode supported option allows users to suspend an ongoing erase sector operation. When an ongoing erase operation is interrupted using “Erase Suspend” and “Erase Resume”, Flash cells may not have been erased completely, even after the erase operation complete is indicated by FLASHC_STATUS register. Only Code Flash is impacted by this issue, Work Flash and Supervisory Flash (SFlash) are not impacted.
Parameters affected	N/A
Trigger condition(s)	Using EraseSector System Call in Non-Blocking mode for CM0+ to erase Code Flash and the ongoing erase operation is interrupted using EraseSuspend and EraseResume System calls.
Scope of impact	When Code Flash sectors are erased in Non-Blocking mode and the ongoing erase operation is interrupted by Erase Suspend / Erase Resume, it cannot be guaranteed that the Code Flash cells are fully erased. Any read on the Code Flash area after the erase is complete or read on the programmed data after ProgramRow is complete can trigger ECC errors.
Workaround	Use any of the following: 1) Use Non-Blocking mode for EraseSector, but do not interrupt the erase operation using Erase Suspend / Erase Resume. 2) If a Code Flash sector erase operation is interrupted using Erase Suspend / Erase Resume, then erase the same sector again without Erase Suspend / Erase Resume before reading the sector or programming the sector.
Fix status	Fixed to update the Flash settings from the date code 312xxxxx, via Manufacturing Test Program Update for Code Flash setting; this fix is transferred to TRAVEO™ T2G devices during Infineon Factory Test Flow. Fixed devices will be identified by Device Date Code, which is marked on every TRAVEO™ T2G device.

7. Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep	
Problem definition	The port state is not retained when the port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.
Parameters affected	N/A
Trigger condition(s)	The port selects peripherals (except for LIN or CAN-FD) and MCU wakes up from DeepSleep.
Scope of impact	Unexpected port output change might affect user system.
Workaround	If the port selects peripherals (except for LIN or CAN FD), and the port output value needs to be maintained after wakeup from DeepSleep, set HSIOM_PRTx_PORT_SEL.IOy_SEL = 0 (GPIO) before DeepSleep and set the required output value in GPIO configuration registers. After wakeup, change HSIOM_PRTx-_PORT_SEL.IOy_SEL back to the peripheral module as needed.
Fix status	No silicon fix planned. TRM was updated to add above workaround.

8. A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM	
Problem definition	The following is lacked from the PWR_CTL2.BGREF_LPMODE description in the existing register TRM. “This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.”
Parameters affected	N/A
Trigger condition(s)	Using the PWR_CTL2.BGREF_LPMODE.
Scope of impact	PWR_CTL2.BGREF_LPMODE may not be set or cleared.
Workaround	Use the PWR_CTL2.BGREF_LPMODE according to the following description. “This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.”
Fix status	No silicon fix planned. Register TRM was updated.

9. Limitation of clock configuration before entering DeepSleep mode	
Problem definition	DeepSleep should not be entered while any FLL/PLL is enabled and using ECO/LPECO as its reference clock. Since the unstable ECO/LPECO clock after wakeup is outside the allowed reference clock limits for FLL/PLL, there is possibility of failing the DeepSleep wakeup.
Parameters affected	N/A
Trigger condition(s)	DeepSleep transition while any FLL/PLL is enabled and using ECO/LPECO as its reference clock.
Scope of impact	There is possibility of failing the DeepSleep wakeup.
Workaround	If any FLL/PLL is operating with the ECO/LPECO as its reference clock, change the clock to either ECO/LPECO direct or IMO direct or IMO with FLL/PLL before entering DeepSleep.
Fix status	No silicon fix planned. TRM was updated to add above workaround.

10. Several data retention information in Register TRM are incorrect	
Problem definition	The following registers are described as ‘Retained’ in the Register TRM while it is not guaranteed that the value before entering DeepSleep mode is still readable from the register. - SARADC: PASSx_SARy_CHz_RESULT - SRSS: PWR_LVD_STATUS - SRSS: PWR_LVD_STATUS2 - SRSS: CLK_CAL_CNT1 - SRSS: CLK_CAL_CNT2 - SRSS: CLK_FLL_STATUS - SRSS: WDT_INTR - SRSS: WDT_INTR_MASKED - SRSS: CLK_PLL400Mx_STATUS - MIXER: MIXER_DST_STRUCT_INTR_DST_MASKED
Parameters affected	N/A
Trigger condition(s)	Use of the related function and wakeup from DeepSleep mode.
Scope of impact	The values before entering DeepSleep are not retained.
Workaround	For PASSx_SARy_CHz_RESULT, any of following: 1) Store the conversion values at another memory location before entering DeepSleep mode 2) Restart the conversion after wakeup from DeepSleep mode For the other registers: Rewrite the register value or read the status flags again after wakeup.
Fix status	No silicon fix planned. Register TRM was updated.

11. SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally	
Problem definition	There is possibility of setting the SCBx_INTR_TX.UNDERFLOW bit even if the FIFO is not empty.
Parameters affected	N/A
Trigger condition(s)	Using the TX FIFO for SCB when the AHB-Lite interface clock (CLK_GR6) frequency of the AHB bus is greater than 3x the SCB functionality clock (PCLK_SCBx_CLOCK).
Scope of impact	SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally.
Workaround	Ignore the SCBx_INTR_TX.UNDERFLOW bit if the FIFO is not empty.
Fix status	No silicon fix planned. Register TRM was updated.

12. Conditions in datasheet for standard SMIF SDR mode extended	
Problem definition	The required register setting for SMIF SDR mode (SMIFx_COREy_CTL2.TX_SDR_EXTRA_SETUP = 1) was missing and could lead to incorrect timing.

Parameters affected	Recommended configuration for standard SMIF SDR mode got extended.
Trigger condition(s)	Use of standard SMIF SDR mode.
Scope of impact	Setup time (SID1605) might not be met in standard SMIF SDR mode.
Workaround	Follow the new recommended configuration (SMIFx_COREy_CTL2.TX_SDR_EXTRA_SETUP = 1).
Fix status	No silicon fix planned. Datasheet was updated to add the new recommended configuration (SMIFx_COREy_CTL2.TX_SDR_EXTRA_SETUP = 1).

13. Hardfault may occur when calling the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode

Problem definition	The following SROM APIs read data from bank#0 in SFlash. While doing that the check for active non-blocking erase or program of bank#0 is not performed. Therefore, reading bank#0 while there is an active erase/program operation will trigger a bus error which can result in a hardfault occurrence based on FLASHC_FLASH_CTL register settings. Affected SROM APIs: - ReadSWPU - WriteSWPU - GenerateHash - Checksum* - ComputeBasicHash* - CheckFactoryHash - ProgramWorkFlash** - SwitchOverRegulators - LoadRegulatorsTrims *: Do not call it to calculate on the bank where programming/erasing is in progress. **: Do not use it during non-blocking operation.
Parameters affected	N/A
Trigger condition(s)	Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0.
Scope of impact	The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0.
Workaround	Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0.
Fix status	No silicon fix planned. TRM will be updated.
Impact on Infineon software	Impact: Limitation Related modules: S-LLD, HSM-Perf-Lib Comment: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do anything of following: a) call CySldProt_GetSwpuFlashStructCfg b) call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty.

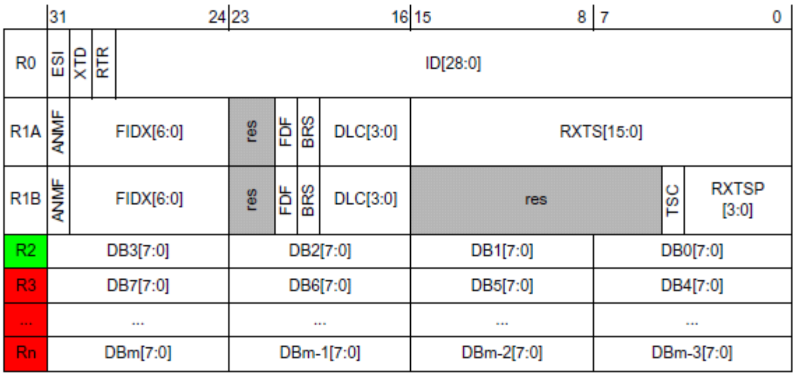
14.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Problem Definition

During frame reception the Rx Handler accesses the external Message RAM for acceptance filtering (read accesses) and for storing of the accepted messages (write accesses).
The time needed for acceptance filtering and for storing of a received message depends on

- The Host clock frequency
- The worst-case latency of the read and write accesses to the external Message RAM
- The number of configured filter elements
- The workload of the transmit message (Tx) handler in parallel to the receive message (Rx) handler

Received data bytes (DB0..DBm) from the CAN Core are buffered in the cache of the Rx Handler before they are written to the Message RAM (in words of 4 byte). Data words inside the Message RAM are numbered from R2 to Rn (n ≤ 17).



	31 … 24	23 … 16	15 … 8	7 … 0
R0	ESI XTD RTR ID[28:0]			
R1A	ANMF FIDX[6:0]	res FDF BRS DLC[3:0]	RXTS[15:0]	
R1B	ANMF FIDX[6:0]	res FDF BRS DLC[3:0]	res	TSC RXTSP [3:0]
R2	DB3[7:0]	DB2[7:0]	DB1[7:0]	DB0[7:0]
R3	DB7[7:0]	DB6[7:0]	DB5[7:0]	DB4[7:0]
...	...	...	...	...
Rn	DBm[7:0]	DBm-1[7:0]	DBm-2[7:0]	DBm-3[7:0]

Figure 1 **Rx Buffer and FIFO Element**

Under the following conditions, a received message has corrupted data while the received message is signaled as valid to the host.
1) The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2) The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5).
3) While condition 1) and 2) apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens.

The data will be corrupted in a way, that in the Message RAM R(i+1) has the same content as Ri.

Despite the corrupted data, the M_TTCAN signals the storage of a valid frame in the Message RAM:
- Rx FIFO: FIFO put index RXFnS.FnPI is updated.
- Dedicated Rx Buffer: New Data flag NDATn.NDxx is set.
- Interrupt flag IR.MRAF is not set.

The issue may occur in the FD Frame Format as well as in the Classic Frame Format.

Figure 2 shows how the available time for acceptance filtering and storage is reduced.

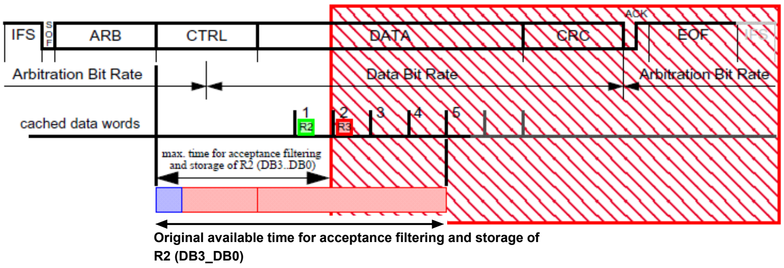


Figure 2 **CAN Frame with DLC>4**

14.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Table 1 **TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5**

Number of configured active filter element 11-bit IDs / 29-bit IDs	Number of active CAN channels in an instance	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
32 / 16	2	3.9 MHz	7.1 MHz	13.1 MHz	22.8 MHz	7.7 MHz	14.1 MHz	26.1 MHz	31.5 MHz
	3	5.4 MHz	9.9 MHz	18.3 MHz	31.8 MHz	10.7 MHz	19.7 MHz	36.5 MHz	44.0 MHz
64 / 32	2	7.4 MHz	13.5 MHz	24.9 MHz	43.4 MHz	14.7 MHz	26.9 MHz	49.8 MHz	60.0 MHz
	3	10.3 MHz	18.8 MHz	34.9 MHz	60.7 MHz	20.5 MHz	37.6 MHz	69.7 MHz	84.0 MHz
96 / 48	2	10. 8 MHz	19.9 MHz	36.8 MHz	64.0 MHz	21.6 MHz	39.7 MHz	73.5 MHz	88.6 MHz
	3	15.1 MHz	27.8 MHz	51.5 MHz	89.6 MHz	30.2 MHz	55.6 MHz	102.9 MHz[3]	124.0 MHz[3]
128 / 64	2	14.3 MHz	26.3 MHz	48.6 MHz	84.7 MHz	28.4 MHz	52.5 MHz	97.2 MHz	117.2 MHz[3]
	3	20.0 MHz	36.8 MHz	68.0 MHz	118.5 MHz[3]	40.0 MHz	73.5 MHz	136.0 MHz[3]	164.0 MHz[3]

1.M_TTCAN always starts at filter element #0 and proceeds through the filter list to find a matching element. Acceptance filtering stops at the first matching element and the following filter elements are not evaluated for this message. Therefore, the sequence of configured filter elements has a significant impact on the performance of the filtering process.
2.Acceptance filtering search for 11-bit IDs and 29-bit IDs filter element runs separately; only one configured filter setting should be considered. Searching for one 29-bit filter element requires approximately double cycles for one 11-bit filter element.
3. Frequency is not reachable since the maximum host clock frequency for M_TTCAN in TRAVEO™ T2G is 100 MHz.

Parameters Affected	N/A
Trigger Condition(s)	Under the following conditions a received message has corrupted data while the received message is signaled as valid to the host: 1) The data length code (DLC) of the received message is greater than 4 (DLC > 4) 2) The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5). 3) While condition 1) and 2) apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens.
Scope of Impact	The erratum is limited to the case when the Host clock frequency used in the actual device is below the limit shown in **Table 1**. Corrupted data is written to the Rx FIFO element from the respective dedicated Rx Buffer. The received frame is nevertheless signaled as valid.

14.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete	
Workaround	Check whether the minimum Host clock frequency (shown in **Table 1**) is below the Host clock frequency used in the actual device. If yes, there is no problem with the selected configuration. If no, use one of the following two workarounds. **1)** Try a different configuration by changing the following parameters until the actual Host clock frequency (CLK_GR5) is above the minimum host frequency shown in **Table 1**: • Increase the CLK_GR5 frequency in the actual device • Reduce the CAN-FD data bit rate • Reduce the number of configured filter elements • Reduce the number of active CAN channels in an instance Also, use DLC ≥ 8 instead of DLCs 5, 6, and 7 in the CAN environment/system, as they place higher demands on the minimum Host clock frequency (the worst case is DLC = 5) or restrict your CAN environment/system to DLC 4. **Note:** While changing the actual host clock frequency, CLK_GR5 must always be equal to or higher than PCLK_-CANFD[x]_CLOCK_CAN[y] for all configurations. **2)** Due to condition 3) listed in **“Trigger Conditions”**, the issue occurs only sporadically. Use an end-to-end (E2E) protection (for example, checksum or CRC covering the data field) and add it to all messages in the CAN system, to detect data corruption in the received frames.
Fix Status	No silicon fix planned. Use workaround.
Impact on Infineon software	Impact: Limitation Related modules: CAN, MCU Comment: Evaluate the impact of the erratum for each CAN instance separately. A CAN instance is the entirety of CanControllers with the same CanControllerInstance value. 1) For the number of active CAN nodes: Use the maximum number of CanController configurations of a CAN instance that can be active (Autosar controller state STARTED or SLEEP) at a time. 2) For the host clock frequency: In McuPeriGroupSettings, locate the setting with McuPeriGroup = MCU_PERI_GROUP5_MMIO5 and take the value from McuPeriGroupClockFrequency. 4) For the number of configured active filter element 11-bit IDs / 29-bit IDs: Use the corresponding values from the "Message RAM (…) linking table" in the generated *Can_PBcfg.h* file. Note that each CanController has its separate table. Take the maximum values. 5) For the arbitration bit rate: Use the maximum CanControllerBaudRate value of all the CanControllers. 6) For the data bit rate: Use the maximum CanControllerFdBaudRate value of all the CanControllers if configured. Otherwise use CanControllerBaudRate.

<table>
<tr><th colspan="2">15.Update of root and intermediate clocks table in datasheet</th></tr>
<tr><td>**Problem Definition**</td><td>The root and intermediate clocks table in the datasheet had typos.</td></tr>
<tr><td>**Parameters Affected**</td><td>
<table>
<tr><th rowspan="3">Root Clock</th><th rowspan="3">Maximum permitted clock frequency (MHz)</th><th rowspan="3">Source</th><th colspan="6">Maximum permitted clock frequency (MHz)</th></tr>
<tr><th colspan="3">PLL/FLL Clock source: ECO/ LPECO</th><th colspan="3">PLL/FLL Clock source: IMO</th></tr>
<tr><th>Integer</th><th>SSCG</th><th>Fractional</th><th>Integer</th><th>SSCG</th><th>Fractional</th></tr>
<tr><td rowspan="2">CLK_HF8/
CLK_HF9</td><td rowspan="2">~~370~~
333</td><td>PLL400 #1</td><td>333</td><td>~~326~~
N/A</td><td>~~329~~
N/A</td><td>318</td><td>~~312~~
N/A</td><td>~~315~~
N/A</td></tr>
<tr><td>PLL400 #2</td><td>333</td><td>~~362~~
N/A</td><td>~~366~~
N/A</td><td>318</td><td>~~312~~
N/A</td><td>~~315~~
N/A</td></tr>
</table>
</td></tr>
<tr><td>**Trigger Condition(s)**</td><td>Using these clocks and clock sources.</td></tr>
<tr><td>**Scope of Impact**</td><td>Reduced frequency under these conditions</td></tr>
<tr><td>**Workaround**</td><td>Follow these maximum permitted clock frequencies.</td></tr>
<tr><td>**Fix Status**</td><td>No silicon fix planned. Datasheet was updated.</td></tr>
<tr><td>**Impact on Infineon Software**</td><td>Impact: Limitation
Related modules: MCU
Comment: Verify that clock settings do not exceed the specified maximum. The value shown in McuClockRootSettings/McuClockRootFrequency must be less than or equal to the maximum permitted root clock. The value shown in McuClockPathSettings/McuClockPathFrequency must be less than or equal to the maximum permitted PLL/FLL clock. MCAL resource property files will be updated so that the validity check of McuClockRootFrequency works correctly.</td></tr>
</table>

<table>
<tr><th colspan="2">16.Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet and architecture TRM</th></tr>
<tr><td>Problem Definition</td><td>The existing datasheet shows 'trig=0' in the description for PASS SARx to TCPWMx direct connect triggers one-to-one, which is the incorrect TCPWM input trigger selection (TR_IN_SEL) value. The correct value is '2'. Therefore, the correct description and Table 25-2 in the architecture TRM (chapter 25) are as follows:
Table 25-2 shows how the multiplexer should be handled for the input trigger event generation. The TRAVEO™ T2G Cluster MCU supports the following input triggers:
- Number of specific one-to-one trigger inputs: 1
- Number of general-purpose trigger inputs: 60

Table 2 Handling input trigger multiplexers
<table>
<tr><th>Input trigger selection</th><th>Input trigger</th><th>Input trigger source</th></tr>
<tr><td>0</td><td>Constant ‘0’</td><td>Constant ‘0’</td></tr>
<tr><td>1</td><td>Constant ‘1’</td><td>Constant ‘1’</td></tr>
<tr><td>2</td><td>HSIOM column ACT#2 or PASS (programmable analog subsystem), through 1:1 trigger mux #2</td><td>Refer to the "Alternate function pin assignments" or "Triggers one-to-one" section in the device datasheet</td></tr>
<tr><td>3</td><td>tr_all_cnt_in[0]</td><td>Refer to the trigger mux block in the device datasheet</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>62</td><td>tr_all_cnt_in[59]</td><td>Refer to the trigger mux block in the device datasheet</td></tr>
</table></td></tr>
<tr><td>Parameters Affected</td><td>N/A</td></tr>
<tr><td>Trigger Condition(s)</td><td>Using the triggers one-to-one for PASS SARx to TCPWMx direct connect</td></tr>
<tr><td>Scope of Impact</td><td>The triggers one-to-one for PASS SARx to TCPWMx direct connect cannot work if TCPWM's input trigger selection is not correct</td></tr>
<tr><td>Workaround</td><td>Use '2' as TCPWM's input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect</td></tr>
<tr><td>Fix Status</td><td>No silicon fix planned. Datasheet was updated. Architecture TRM will be updated.</td></tr>
<tr><td>Impact on Infineon Software</td><td>Impact: No
Related modules: PWM
Comment: The MCAL PWM module does not support one-to-one triggers.</td></tr>
</table>

Revision history

Document revision	Date	Description of changes
**	2018-09-10	New datasheet for NPP
*A	2019-04-08	Modified the title Updated Features and Features list Updated Functional Description Updated Device Address Map Modified the Peripheral I/O Map Added Clock Diagram Added 500-BGA Ball Map Added Package Pin List and Alternate Functions Added Power Pin Assignments Added Alternate Function Pin Assignments Added Interrupts and Wake-up Assignments Added Trigger Multiplexer Added Peripheral Clocks Added Faults, Bus Masters, and other miscellaneous configurations Added PPU Fixed Structure Pairs Updated Electrical Specifications Added Ordering Information, Part Number Nomenclature Updated Packaging.
*B	2019-05-24	Updated **Features list**, **Pin assignment**. Updated **Electrical specifications**. Added **PPU fixed structure pairs**. **Added Table 26-19 for Root and Intermediate Clocks**. Updated **CYT4DN peripheral I/O map**, **Triggers 1:1**, **Bus masters for access and protection control**. Added 500-Ball FBGA Package Outline..
*C	2020-03-30	Updated **Pin assignment** with 327-BGA. Updated Faults Description. Updated **Electrical specifications**. Added 327-BGA Package Diagram.
*D	2020-09-14	Updated **Features** and **Features list**. Updated **DMA controllers**. Modified **Figure 3-1** Updated **Timer/counter/PWM block (TCPWM)**. Updated **Serial memory interface (SMIF)**. Updated **Sound subsystem**. Updated **Graphics**. Updated **Peripheral I/O map**. Updated **Pin assignment**. Updated **Package pin list and alternate functions**, **Power pin assignments**, and **Alternate function pin assignments**. Updated **Interrupts and wake-up assignments** and **Core interrupt types**. Updated **Trigger multiplexer**, **Triggers group inputs**, and **Triggers one-to-one**. Updated **Faults**. Updated **Peripheral protection unit fixed structure pairs**. Updated **Electrical specifications**. Updated **VIDEOSS capture timing groups**. Added **Appendix**.

Document revision	**Date**	**Description of changes**
*E	2020-12-22	Updated **Features**. Corrected DMA Channels in **Functional description**. Updated min ECO frequency. Updated **Peripheral I/O map**. Updated **Pin assignment**. Corrected footnotes for **Table 11-1**. Updated **Faults**. Updated **Electrical specifications**. Added diagrams for **Graphics specifications**. Updated **Packaging**.
*F	2021-05-12	Updated **Features**. Updated **Features list**. Updated **Clock system**, **Power modes**, and **I/Os**. Updated **Pin assignment**. Updated **Package pin list and alternate functions**. Updated **Power pin assignments**. Updated **Alternate function pin assignments**. Updated **Interrupts and wake-up assignments**. Updated **Faults**. Updated **Peripheral protection unit fixed structure pairs**. Updated **Bus masters**. Updated **Electrical specifications**. Updated **Packaging**. Updated **Appendix**.
*G	2021-09-20	Renamed Traveo II to TRAVEO™ T2G. Updated **Features list**. Updated **Alternate function pin assignments**. Updated **Electrical specifications**. Updated **Clock specifications** Added **xSPI (JEDEC JESD251) Tap/DLL setting requirement** Added **Capture timing groups** Updated **Ordering information**
*H	2022-07-01	Updated **Features**, and **Features list** Updated **Blocks and functionality**, **System resources** and **Peripherals** Updated **Peripheral I/O map** Updated **Faults** Updated **Electrical specifications** Updated **Packaging** Updated **MIPI formats supported** Added **Errata** Migrated to IFX template.
*I	2023-02-14	Updated **Features list**. Updated **Peripherals** and **I/Os**. Updated **Peripheral I/O map**. Updated **Package pin list and alternate functions**. Updated **Trigger multiplexer**. Updated **Bus masters**. Updated **Electrical specifications**. Updated **Packaging**
*J	2023-07-18	Added SID1612 and SID1712 in **Table 26-38**. Added content under FDP-LINK in **Table 26-39**. Updated IMO connections in **Figure 7-1**. Updated content for HSIO_STDLN under SPI Interface and UART Interface in **Table 26-10**. Removed SID68 in **Figure 26-3**.

Document revision	Date	Description of changes
*K	2024-03-05	Updated Graphics subsystem features. Updated **Ethernet MAC**. Changed CLK_HF8 clock frequency to 333 in **Table 26-19**. Renamed SID1609 to SID1609A and changed the min value to > (tCK - tINV), but at least 3.8 ns. Changed the description of SID902 to "Configured Pixel Clock Frequency". Updated Details/Conditions for SID963A. Updated **Errata**.

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Email:
erratum@infineon.com

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