

16-Mbit (1M x 16) Pseudo Static RAM

Features

- **Wide voltage range: 2.2V–3.6V**
- **Access Time: 70 ns**
- **Ultra-low active power**
 - Typical active current: 3 mA @ $f = 1 \text{ MHz}$
 - Typical active current: 18 mA @ $f = f_{\text{max}}$
- **Ultra low standby power**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in a 48-ball BGA Package**
- **Operating Temperature: -40°C to $+85^{\circ}\text{C}$**

Functional Description^[1]

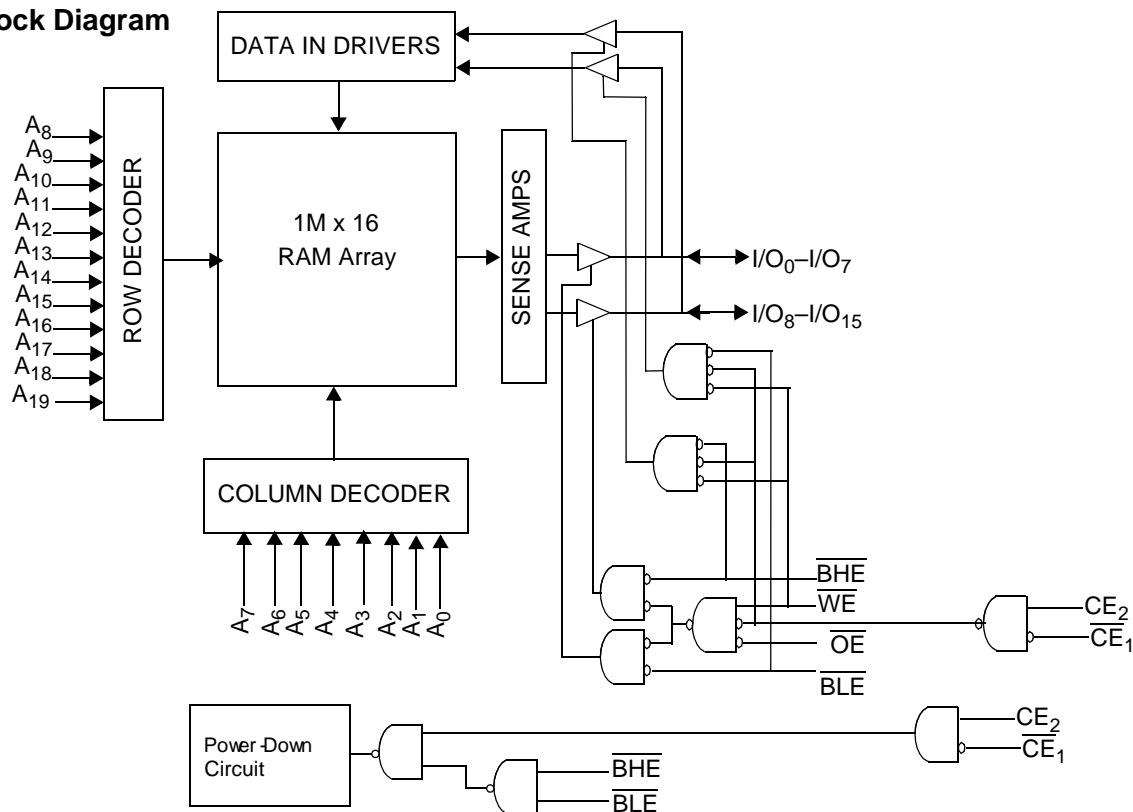
The CYU01M16SCE is a high-performance CMOS Pseudo Static RAM organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{\text{CE}}_1$ HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}_1$ HIGH or CE_2 LOW), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation (CE_1 LOW and CE_2 HIGH and WE LOW).

To write to the device, take Chip Enable ($\overline{\text{CE}}_1$ LOW and CE_2 HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{\text{CE}}_1$ LOW and CE_2 HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . Refer to the truth table for a complete description of read and write modes.

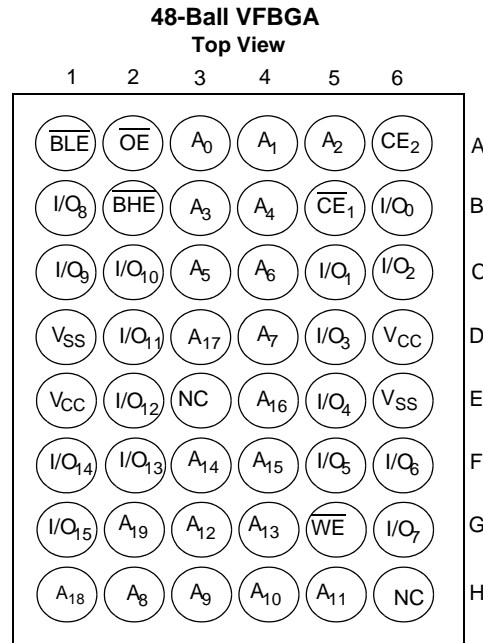
Logic Block Diagram



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2, 3]

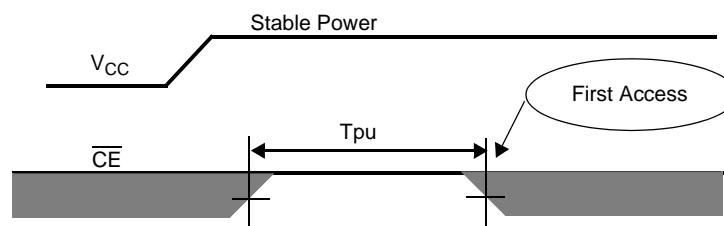


Product Portfolio^[4]

| Product | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|-------------|---------------------------|---------------------|------|------------|--------------------------------|------|----------------------|------|-------------------------------|------|
| | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | | | | | f = 1MHz | | f = f _{max} | | | |
| CYU01M16SCE | Min. | Typ. ^[4] | Max. | 70 | Typ. ^[4] | Max. | Typ. ^[4] | Max. | Typ. ^[4] | Max. |
| | 2.2 | 3.0 | 3.6 | | 3 | 5 | 18 | 25 | 55 | 70 |

Power-up Characteristics

The initialization sequence is shown in the figure below. Chip Select should be \overline{CE}_1 HIGH or CE_2 LOW for at least 200 μs after V_{CC} has reached a stable value. No access must be attempted during this period of 200 μs.



| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------------|--|------|------|------|------|
| T _{pu} | Chip Enable Low After Stable V _{CC} | 200 | | | μs |

Notes:

- Ball H6 and E3 can be used to upgrade to a 32-Mbit and a 64-Mbit density, respectively.
- NC "no connect" - not connected internally to the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (typ) and T_A = 25°C. Tested initially and after design changes that may affect the parameters.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage to

Ground Potential..... -0.3V to $V_{CCMAX} + 0.3V$

DC Voltage Applied to Outputs

in High Z State^[5, 6, 7]..... -0.3V to $V_{CCMAX} + 0.3V$

DC Input Voltage^[5, 6, 7]..... -0.3V to $V_{CCMAX} + 0.3V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... > 200 mA

| Device | Range | Operating Temperature (T _A) | V _{CC} |
|-------------|------------|---|-----------------|
| CYU01M16SCE | Industrial | -40°C to +85°C | 2.2V to 3.6V |

DC Electrical Characteristics (Over the Operating Range)^[5, 6, 7]

| Parameter | Description | Test Conditions | CYU01M16SCE-70 ns | | | Unit |
|------------------|---|--|-----------------------|---------------------|------------------------|------|
| | | | Min. | Typ. ^[4] | Max. | |
| V _{CC} | Supply Voltage | | 2.2 | 3.0 | 3.6 | V |
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.1 mA V _{CC} = 2.2V to 3.6V | V _{CC} - 0.2 | | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 0.1 mA V _{CC} = 2.2V to 3.6V | | | 0.2 | V |
| V _{IH} | Input HIGH Voltage | V _{CC} = 2.2V to 3.6V | 0.8 * V _{CC} | | V _{CC} + 0.3V | V |
| V _{IL} | Input LOW Voltage | V _{CC} = 2.2V to 3.6V | -0.3 | | 0.2 * V _{CC} | V |
| I _{IX} | Input Leakage Current | GND ≤ V _{IN} ≤ V _{CC} | -1 | | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CC} | -1 | | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | f = f _{MAX} = 1/t _{RC} V _{CC} = V _{CCmax} I _{OUT} = 0 mA CMOS levels | | 18 | 25 | mA |
| | | f = 1MHz | | 3 | 5 | mA |
| I _{SB1} | Automatic CE Power-Down Current—CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2V$, CE ₂ ≤ 0.2V, V _{IN} > V _{CC} - 0.2V, V _{IN} < 0.2V, f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V _{CC} = 3.60V | | 55 | 70 | μA |
| I _{SB2} | Automatic CE Power-Down Current—CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2V$, CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = V _{CCMAX} | | 55 | 70 | μA |

Capacitance^[8]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, | 8 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = V _{CC(typ)} | 8 | pF |

Thermal Resistance^[8]

| Parameter | Description | Test Conditions | VFBGA | Unit |
|-----------------|--|---|-------|------|
| Θ _{JA} | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 56 | °C/W |
| Θ _{JC} | Thermal Resistance (Junction to Case) | | 11 | °C/W |

Notes:

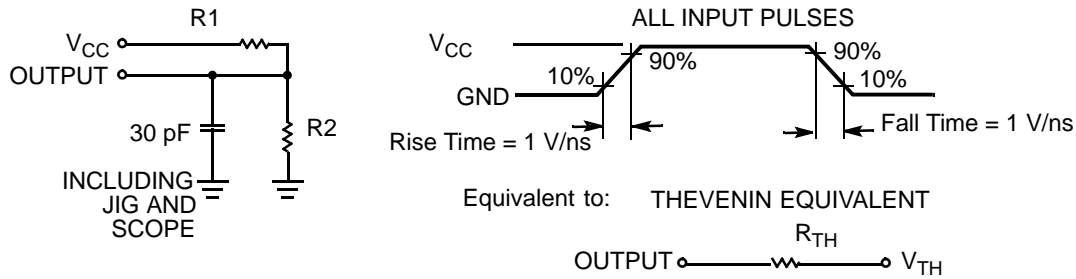
5. V_{IL(MIN)} = -0.5V for pulse durations less than 20 ns.

6. V_{IH(MAX)} = V_{CC} + 0.5V for pulse durations less than 20 ns.

7. Overshoot and undershoot specifications are characterized and are not 100% tested.

8. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



| Parameters | 3.0V (V _{CC}) | Unit |
|-----------------|-------------------------|------|
| R1 | 26000 | Ω |
| R2 | 26000 | Ω |
| R _{TH} | 13000 | Ω |
| V _{TH} | 1.50 | V |

Switching Characteristics Over the Operating Range^[9, 10, 11, 14, 15]

| Parameter | Description | 70 ns | | Unit |
|---------------------------------|--|-------|-------|------|
| | | Min. | Max. | |
| Read Cycle | | | | |
| t _{RC} ^[13] | Read Cycle Time | 70 | 40000 | ns |
| t _{CD} | Chip Deselect Time \overline{CE}_1 = HIGH or CE ₂ =LOW, BLE/BHE High Pulse Time | 15 | | ns |
| t _{AA} | Address to Data Valid | | 70 | ns |
| t _{OHA} | Data Hold from Address Change | 5 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 70 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 35 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[10, 11, 12] | 5 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[10, 11, 12] | | 25 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[10, 11, 12] | 10 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[10, 11, 12] | | 25 | ns |
| t _{DBE} | BLE/BHE LOW to Data Valid | | 70 | ns |
| t _{LZBE} | BLE/BHE LOW to Low Z ^[10, 11, 12] | 5 | | ns |
| t _{HZBE} | BLE/BHE HIGH to High Z ^[10, 11, 12] | | 25 | ns |

Notes:

- Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of V_{CC(typ.)}/2, input pulse levels of 0V to V_{CC}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
- At any given temperature and voltage conditions t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device. All low-Z parameters will be measured with a load capacitance of 30 pF (3V).
- t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- If invalid address signals shorter than min.t_{RC} are continuously repeated for 40 μs, the device needs a normal read timing (t_{RC}) or needs to enter standby state at least once in every 40 μs.
- In order to achieve 70-ns performance, the read access must be Chip Enable (\overline{CE}_1 or CE₂) controlled. That is, the addresses must be stable prior to Chip Enable going active.

Switching Characteristics Over the Operating Range^[9, 10, 11, 14, 15] (continued)

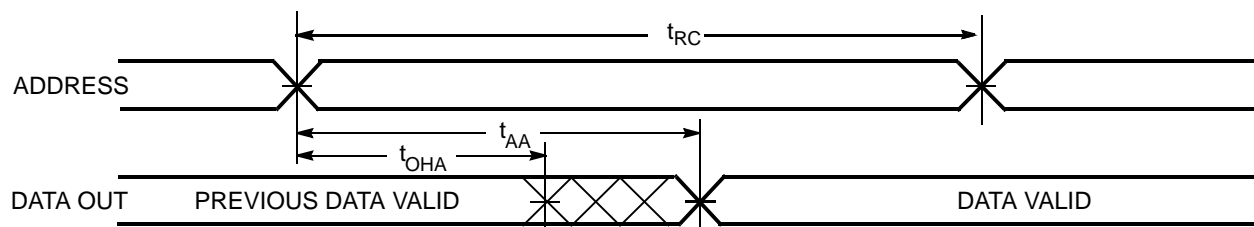
| Parameter | Description | 70 ns | | Unit |
|-----------------------------|---|-------|-------|------|
| | | Min. | Max. | |
| Write Cycle ^[15] | | | | |
| t _{WC} | Write Cycle Time | 70 | 40000 | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 60 | | ns |
| t _{AW} | Address Set-Up to Write End | 60 | | ns |
| t _{CD} | Chip Deselect Time \overline{CE}_1 = HIGH or CE_2 =LOW, BLE/BHE High Pulse Time | 15 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 50 | | ns |
| t _{BW} | $\overline{BLE/BHE}$ LOW to Write End | 60 | | ns |
| t _{SD} | Data Set-Up to Write End | 25 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | ns |
| t _{HZWE} | \overline{WE} LOW to High-Z ^[10, 11, 12] | | 25 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low-Z ^[10, 11, 12] | 10 | | ns |

Note:

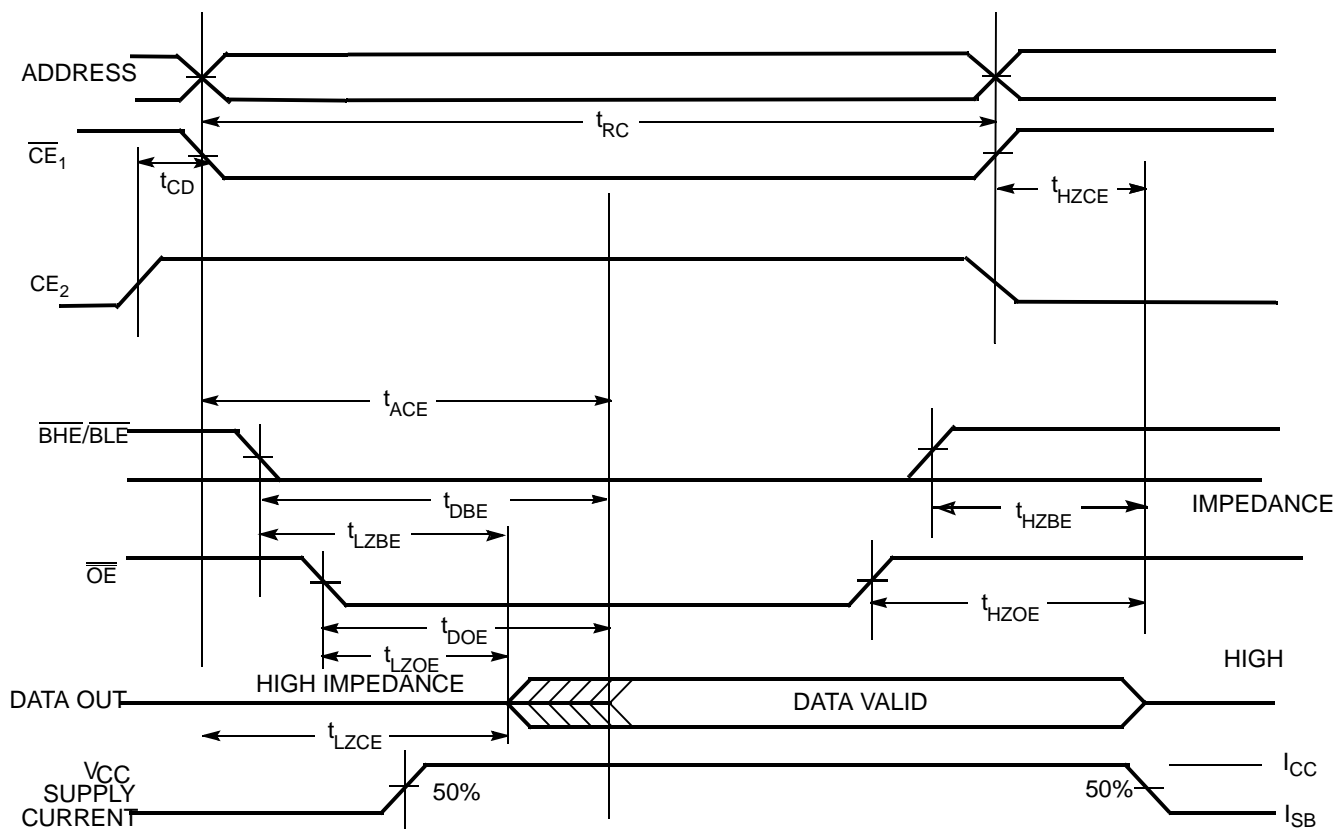
15. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$ or $CE_2 = V_{IH}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)^[17, 18]



Read Cycle 2 (\overline{OE} Controlled)^[16, 18, 19]



Notes:

16. Whenever $\overline{CE}_1 = \text{HIGH}$ or $CE_2 = \text{LOW}$, $\overline{BHE}/\overline{BL0}$ are taken inactive, they must remain inactive for a minimum of 5 ns.

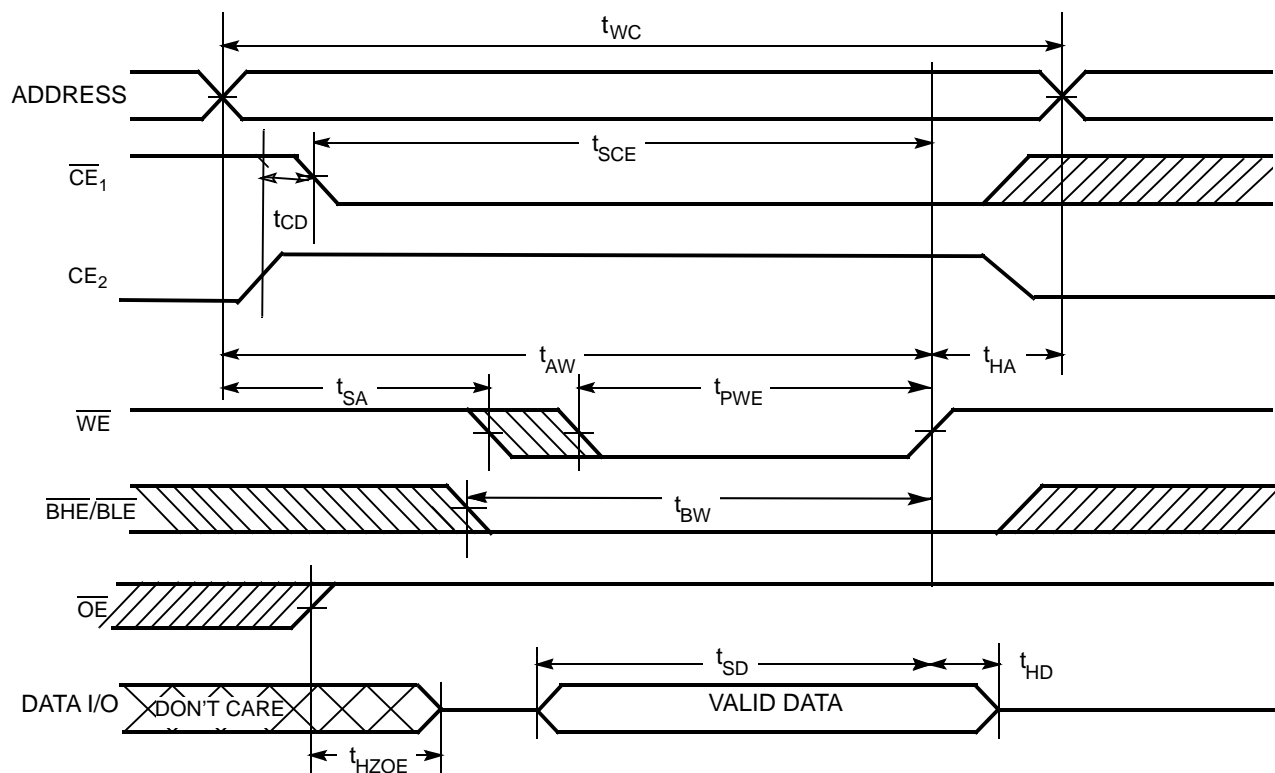
17. Device is continuously selected. $\overline{OE} = \overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$.

18. \overline{WE} is HIGH for Read Cycle.

19. \overline{CE} is the Logical AND of \overline{CE}_1 and CE_2 .

Switching Waveforms (continued)

Write Cycle 1 ($\overline{\text{WE}}$ Controlled)^[15, 12, 16, 19, 20, 21]



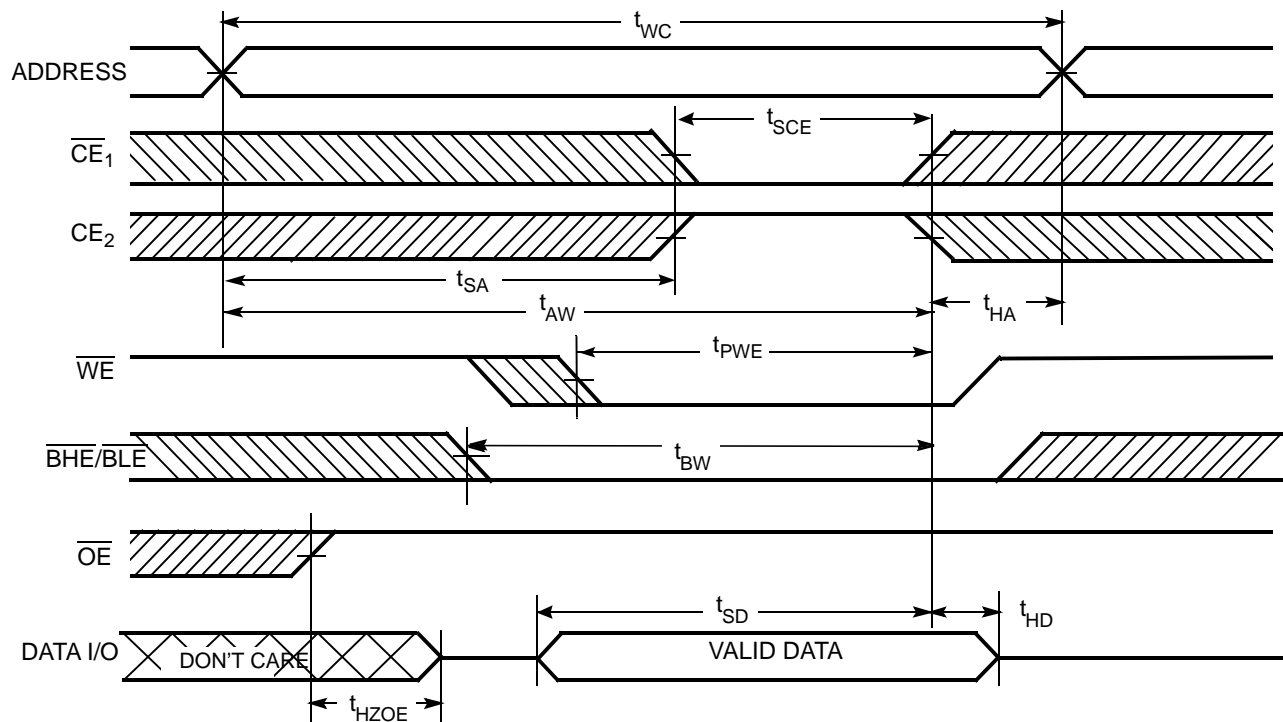
Notes:

20. Data I/O is high-impedance if $\overline{\text{OE}} \geq V_{\text{IH}}$.

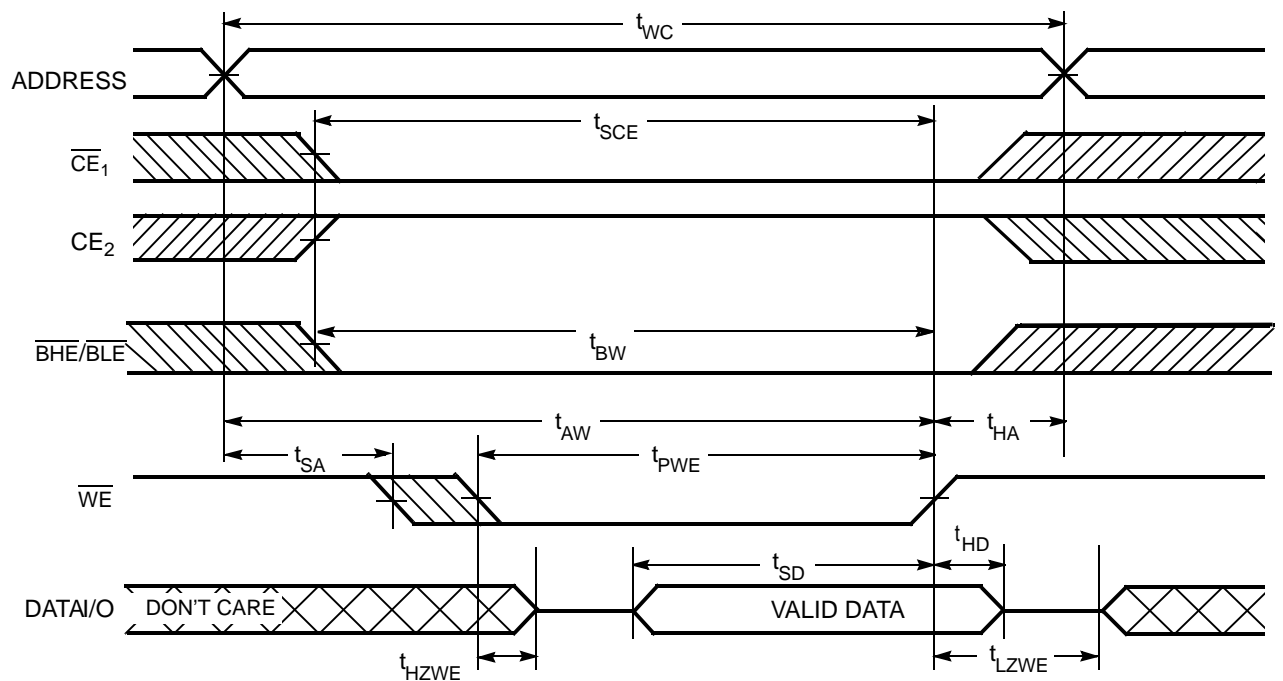
21. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 2 (\overline{CE}_1 or \overline{CE}_2 Controlled)^[15, 12, 16, 20, 21]

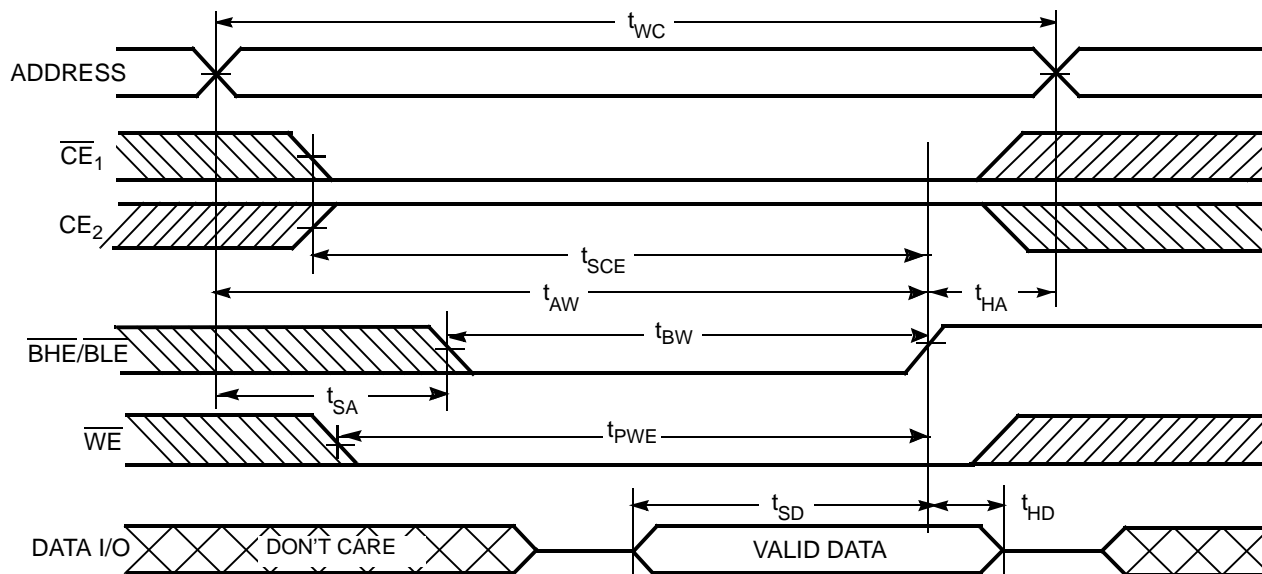


Write Cycle 3 (\overline{WE} Controlled, \overline{OE} LOW)^[16, 21]



Switching Waveforms (continued)

Write Cycle 4 (BHE/BL $\overline{\text{E}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15, 16, 20, 21]



Truth Table^[22]

| $\overline{\text{CE}}_1$ | CE_2 | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | $\overline{\text{BHE}}$ | $\overline{\text{BLE}}$ | Inputs/Outputs | Mode | Power |
|--------------------------|---------------|------------------------|------------------------|-------------------------|-------------------------|---|-----------------------------------|-----------------------------|
| H | X | X | X | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| X | L | X | X | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| X | X | X | X | H | H | High Z | Deselect/Power-down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data Out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z | Read | Active (I_{CC}) |
| L | H | H | L | L | H | Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z | Read | Active (I_{CC}) |
| L | H | H | H | L | L | High Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | H | L | High Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | L | H | High Z | Output Disabled | Active (I_{CC}) |
| L | H | L | X | L | L | Data In (I/O_0 – I/O_{15}) | Write (Upper Byte and Lower Byte) | Active (I_{CC}) |
| L | H | L | X | H | L | Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z | Write (Lower Byte Only) | Active (I_{CC}) |
| L | H | L | X | L | H | Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z | Write (Upper Byte Only) | Active (I_{CC}) |

Note:

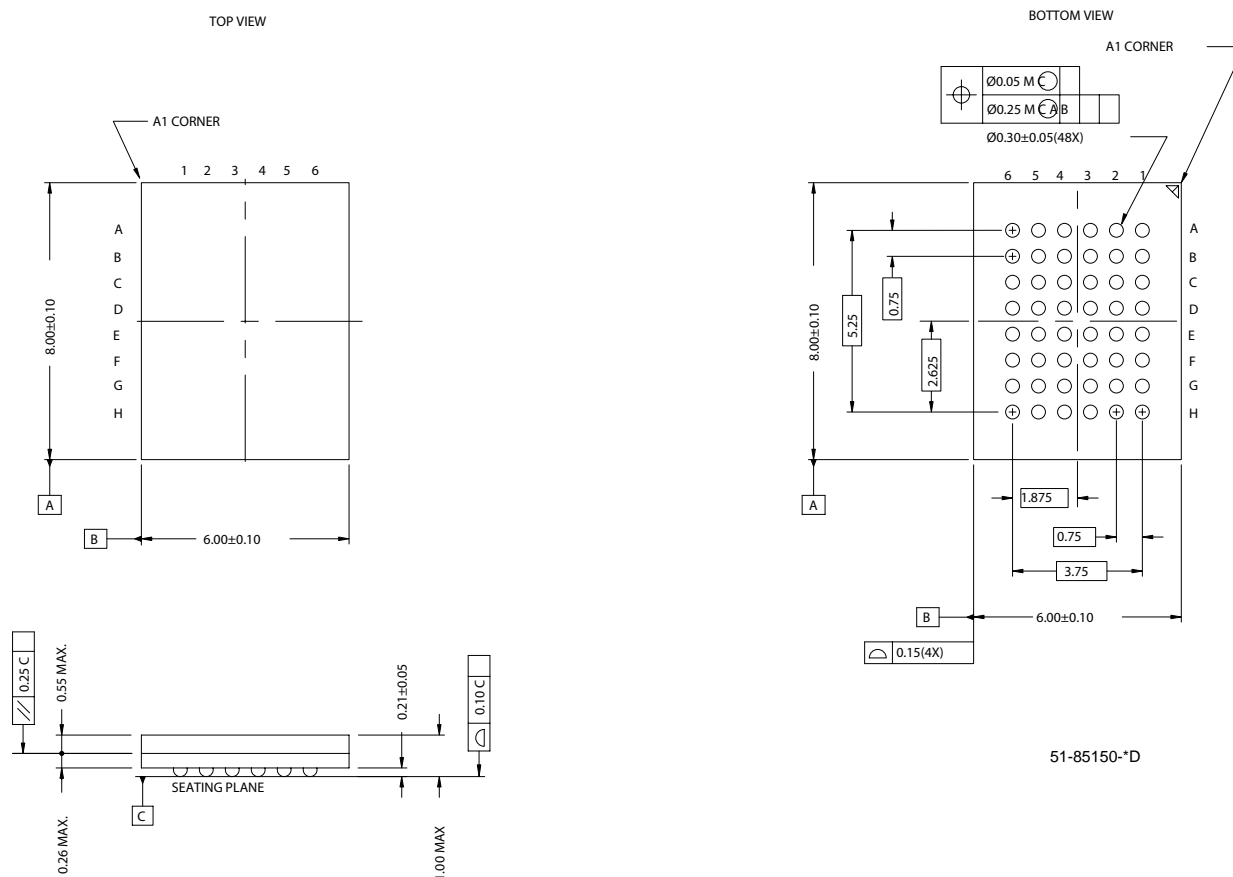
22. H = Logic HIGH, L = Logic LOW, X = Don't Care.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------------|-----------------|--|-----------------|
| 70 | CYU01M16SCEU-70BVXI | 51-85150 | 48-ball Fine Pitch VBGA (6 mm x 8 mm x 1 mm) (Pb-Free) | Industrial |

Package Diagram

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



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Document History Page

| Document Title: CYU01M16SCE MoBL3™ 16-Mbit (1M x 16) Pseudo Static RAM Document Number: 38-05601 | | | | |
|---|---------|------------|-----------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 342199 | See ECN | PCI | New Data sheet |
| *A | 386551 | See ECN | PCI | Changed from Advance to Preliminary Replaced TBDs with appropriate values Changed t_{PC} and t_{PA} from 20 to 25 ns Corrected footnote # 16 as $OE = \overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$ Added separate waveforms for \overline{CE}_1 and CE_2 in Read # 2, Page Read and Write # 1 Timing diagram |
| *B | 422623 | See ECN | HRT | Removed the 55-ns Speed Bin Changed Isb2 Max value from 60 μA to 70 μA Added Isb1 to DC Parameters Added Chip Enable Access Foot Note to AC Parameters Changed the t_{CD} Min value from 5 ns to 15 ns Changed the Page Mode Values (t_{PC} and t_{PAA}) from 25 ns to 35 ns |
| *C | 462289 | See ECN | NXR | Revised MPN from CYU01M16SCCU to CYU01M16SCE Renamed Package Name column with Package Diagram |
| *D | 492939 | See ECN | NXR | Removed Page Mode feature |