



# Bluetooth SoC for Embedded Wireless Devices

## General Description

The Cypress CYW20706 is a single-chip Bluetooth 4.2-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 40 nm CMOS low-power process, the CYW20706 employs the highest level of integration to eliminate all critical external components, thereby minimizing the device's footprint and the costs associated with implementing Bluetooth solutions.

The CYW20706 is the optimal solution for embedded and IoT applications. Built-in firmware adheres to the Bluetooth Low Energy (BLE) profile.

## Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Cypress to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

**Table 1. Mapping Table for Part Number between Broadcom and Cypress**

Broadcom Part Number	Cypress Part Number
BCM20706	CYW20706
BCM20706UA2KFFB4G	CYW20706UA2KFFB4G

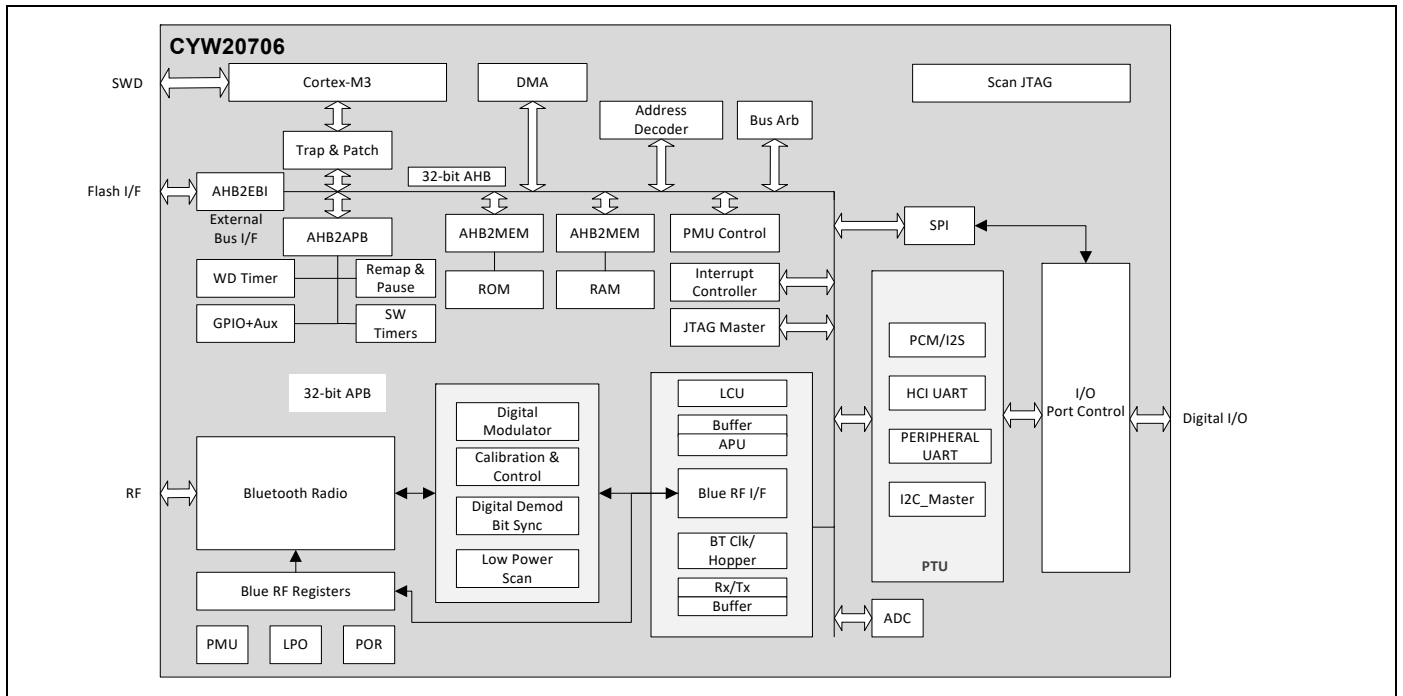
## Features

- Complies with Bluetooth Core Specification version 4.2 including BR/EDR/BLE
- Broadcom proprietary LE data rate up to 2 Mbps
- BLE HID profile version 1.00 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- Excellent receiver sensitivity
- Programmable output power control
- Integrated ARM Cortex-M3 microprocessor core
- On-chip power-on reset (POR)
- Support for EEPROM and serial flash interfaces
- Integrated low dropout regulators (LDO)
- On-chip software controlled PMU
- PCM/I<sup>2</sup>S Interface
- Infrared modulator
- On-chip support for SPI (master/slave modes)
- I2C interface (compatible with NXP I<sup>2</sup>C slaves)
- Package types:
  - 49-pin FBGA package (4.5 mm x 4.0 mm) Bluetooth 4.2-compliant
  - RoHS compliant

## Applications

- Home automation
- Point-of-sale input devices
- Blood pressure monitors
- "Find me" devices
- Heart rate monitors
- Proximity sensors
- Thermometers
- Wearables

**Figure 1. Functional Block Diagram**



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# 1. Functional Description

## 1.1 Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types. The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewatering in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

**Table 2. Bluetooth Features**

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	EDR 2 Mbps and 3 Mbp
SCO	Adaptive Frequency Hopping	–
Paging and Inquiry	eSCO	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	Bluetooth 3.0	Bluetooth 4.0
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	eSCO	–
Bluetooth 4.1	Bluetooth 4.2	
Low Duty Cycle Advertising	Data Packet Length Extension	
Dual Mode	LE Secure Connection	
LE Link Layer Topology	Link Layer Privacy	

### 1.1.1 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state in the Bluetooth Link Controller.

■ States:

- Standby
- Connection
- Page
- Page Scan
- Inquiry
- Inquiry Scan
- Sniff
- Advertising
- Scanning

### 1.1.2 Test Mode Support

The CYW20706 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW20706 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

■ Fixed frequency carrier wave (unmodulated) transmission

- Simplifies some type-approval measurements (Japan)
- Aids in transmitter performance analysis

■ Fixed frequency constant receiver mode

- Receiver output directed to I/O pin
- Allows for direct BER measurements using standard RF test equipment
- Facilitates spurious emissions testing for receive mode

■ Fixed frequency constant transmission

- 8-bit fixed pattern or PRBS-9
- Enables modulated signal measurements with standard RF test equipment

### 1.1.3 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

## 1.2 Microprocessor Unit

The CYW20706 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and SWD interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

### 1.2.1 NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD\_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYW20706 can use SPI Flash or I<sup>2</sup>C EEPROM/serial flash for NVRAM storage.

### 1.2.2 One-Time Programmable Memory

The CYW20706 includes 2 Kbytes of one-time programmable (OTP) memory allow manufacturing customization and to avoid the need for an on-board NVRAM. If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, to save power it is disabled when the boot process is complete. The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded to RAM after the CYW20706 boots and is ready for host transport communication.

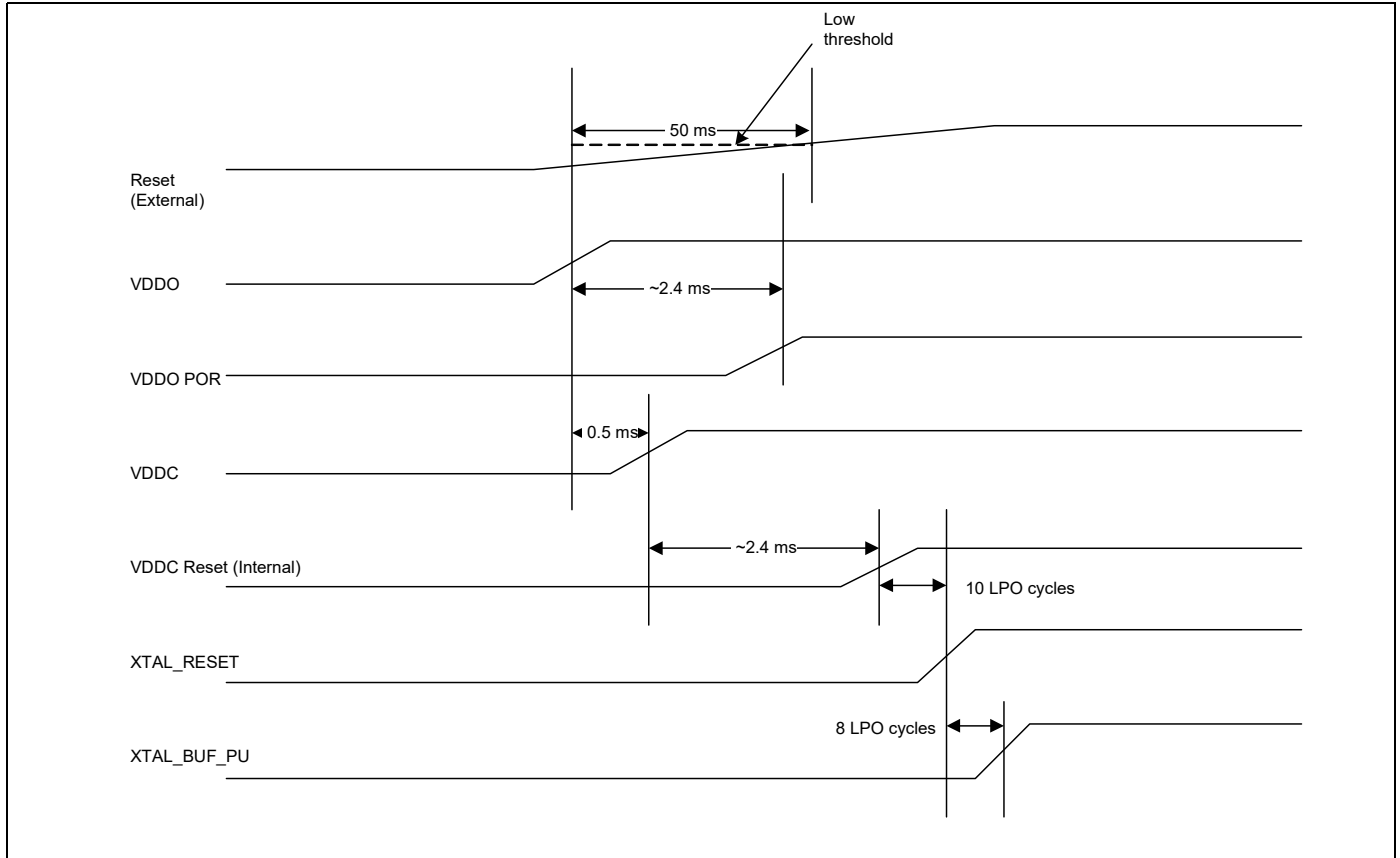
The OTP contents are limited to:

- Parameters required prior to downloading the user configuration to RAM.
- Parameters unique to each part and each customer (for example, the Bluetooth device address).

### 1.2.3 External Reset

An external active-low reset signal, RESET\_N, can be used to put the CYW20706 in the reset state. An external voltage detector reset IC with 50 ms delay is needed on the RESET\_N. The RESET\_N should be released only after the VDDO supply voltage level has been stabilized for 50 ms.

Figure 2. Reset Timing



**Note:** The Reset signal should remain below this threshold 50 ms after VDDO is stable. Note that the representation of this signaling diagram is extended and not drawn to scale.

### 1.3 Integrated Radio Transceiver

The CYW20706 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20706 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

#### 1.3.1 Transmitter

The CYW20706 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates  $\pi/4$ -DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the BLE specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

#### Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK,  $\pi/4$ -DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

#### Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

#### Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

#### 1.3.2 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYW20706 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

#### Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

#### Receiver Signal Strength Indicator

The radio portion of the CYW20706 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

#### 1.3.3 Local Oscillator Generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW20706 uses an internal RF and IF loop filter.



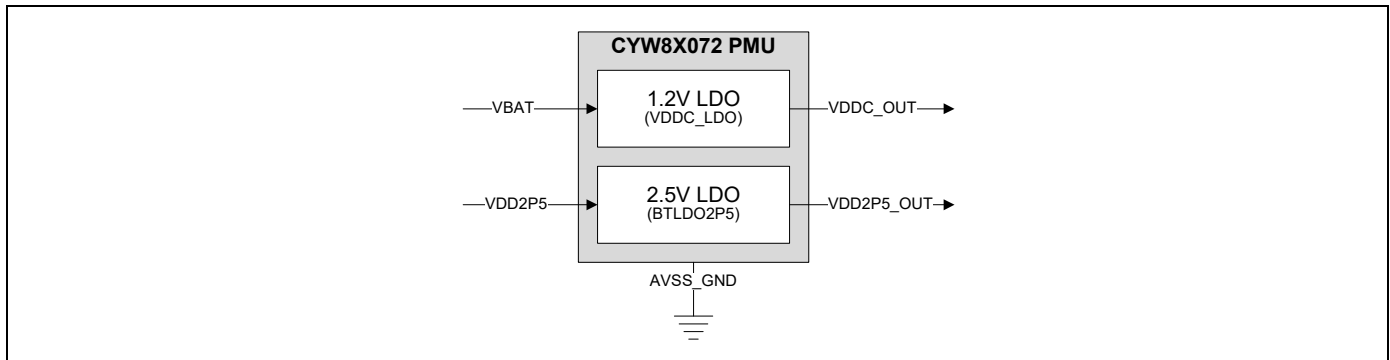
### 1.3.4 Calibration

The CYW20706 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

### 1.3.5 Internal LDO

The CYW20706 uses two LDOs - one for 1.2V and the other for 2.5V. The 1.2V LDO provides power to the baseband and radio and the 2.5V LDO powers the PA.

**Figure 3. LDO Functional Block Diagram**



## 1.4 Collaborative Coexistence

The CYW20706 provides extensions and collaborative coexistence with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously within close proximity of each other. The device supports industry-standard coexistence signaling, including 802.15.2, and supports coexistence with CY WLAN and non-CY third-party WLAN solutions.

## 1.5 Global Coexistence Interface

The CYW20706 supports the proprietary coexistence interface Global Coexistence Interface (GCI) for coexistence between BT and WLAN devices. GCI is a bi-directional bus between Cypress BT and Cypress WLAN.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over 2-wire interface. Between two wire one is GCI\_SECI\_IN and another is GCI\_SECI\_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI\_SECI\_IN and GCI\_SECI\_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

### 1.5.1 SECI I/O

The CYW20706 devices have dedicated GCI\_SECI\_IN and GCI\_SECI\_OUT pins. The two pin functions can be mapped to any of the Cypress Global Coexistence Interface (GCI) GPIO. Pin function mapping is controlled by the configuration file that is stored in on-chip RAM from the host.

## 1.6 Peripheral Transport Unit

### 1.6.1 I<sup>2</sup>C Communications Interface

The CYW20706 provides a 2-pin master I<sup>2</sup>C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as trackball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I<sup>2</sup>C slave devices. I<sup>2</sup>C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by I<sup>2</sup>C:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I<sup>2</sup>C-compatible speed.)
- 1 MHz (Compatibility with high-speed I<sup>2</sup>C-compatible devices is not guaranteed.)

The following transfer types are supported by I<sup>2</sup>C:

- Read (Up to 127 bytes can be read.)
- Write (Up to 127 bytes can be written.)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written.)
- Write-then-Read (Up to 127 bytes can be written and up to 127 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20706 are required on both the SCL and SDA pins for proper operation.

### 1.6.2 HCI UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 4 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYW20706 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 4 Mbps. The baud rate of the CYW20706 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

[Table 3](#) contains example values to generate common baud rates.

**Table 3. Common Baud Rate Examples**

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
4M	0xFF	0xF4	High rate	0.00
3M	0xFF	0xF8	High rate	0.00
2M	0xFF	0xF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW20706 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$ .

**Peripheral UART Interface**

The CYW20706 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin as shown in [Table 4](#).

**Table 4. CYW20706 Peripheral UART**

Pin Name	pUART_TX	pUART_RX	pUART_CTS_N	pUART_RTS_N
Configured pin name	P0	P2	P3	P6
	P31	P33	P3	P30

## 1.7 PCM Interface

The CYW20706 includes a PCM interface that shares pins with the I<sup>2</sup>S interface. The PCM Interface on the CYW20706 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW20706 generates the PCM\_CLK and PCM\_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW20706.

### 1.7.1 Slot Mapping

The CYW20706 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

### 1.7.2 Frame Synchronization

The CYW20706 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three-bit periods and the pulse starts coincident with the first bit of the first slot.

### 1.7.3 Data Formatting

The CYW20706 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW20706 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

### 1.8 Clock Frequencies

The CYW20706 49-pin FBGA package supports 20, 24, and 40 MHz crystals (XTAL) by selecting the correct crystal strapping options. Other frequencies also supported by firmware configuration. [Table 5](#) lists the strapping options.

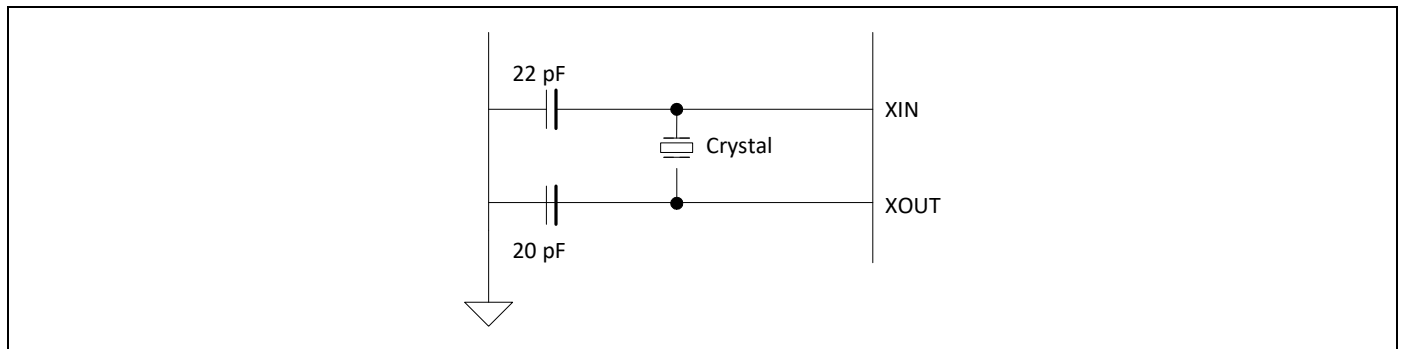
**Table 5. Crystal Strapping Options for the 49-Pin FBGA Package**

Strapping Option Pin		XTAL Frequency
BT_XTAL_STRAP_1	BT_XTAL_STRAP_0	
Pull Low	Pull Low	40 MHz
Pull Low	Pull High	24 MHz
Pull High	Pull Low	20 MHz
Pull High	Pull High	Read from serial flash or EEPROM (Supported XTAL Frequency is 26 MHz).

#### 1.8.1 Crystal Oscillator

The XTAL must have an accuracy of  $\pm 20$  ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see [Figure 4](#)).

**Figure 4. Recommended Oscillator Configuration—12 pF Load Crystal**



[Table 6](#) shows the recommended crystal specifications.

**Table 6. Reference Crystal Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	20	24	40	MHz
Oscillation mode	–	Fundamental			–
Frequency tolerance	@25°C	–	$\pm 10$	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	$\pm 10$	–	ppm
Equivalent series resistance	–	–	–	60	$\Omega$
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	$\mu$ W
Aging	–	–	–	$\pm 10$	ppm/year
Shunt capacitance	–	–	–	2	pF

## HID Peripheral Block

The peripheral blocks of the CYW20706 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

## 1.9 GPIO Ports

### 1.9.1 49-Pin FBGA Package

The CYW20706 49-pin FBGA package has 24 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V. The following GPIOs are available:

- BT\_GPIO\_0/P36/P38 (triple bonded; only one of three is available)
- BT\_GPIO\_1/P25/P32 (triple bonded; only one of three is available)
- BT\_GPIO\_3/P27/P33 (triple bonded; only one of three is available)
- BT\_CLK\_REQ/P4/P24 (triple bonded; only one of three is available)
- BT\_GPIO\_5/P15 (dual bonded; only one of two is available)
- BT\_GPIO\_6/P11/P26 (triple bonded; only one of three is available)
- BT\_GPIO\_7/P30 (Dual bonded; only one of two is available)
- BT\_CLK\_REQ/P4/P24 (triple bonded; only one of three is available)
- I<sup>2</sup>S\_PCM\_IN/P12 (dual bonded; only one of two is available)
- I<sup>2</sup>S\_PCM\_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- I<sup>2</sup>S\_PCM\_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- I<sup>2</sup>S\_WS\_PCM\_SYNC/P0/P34 (triple bonded; only one of three is available)

All of these pins can be programmed as ADC inputs.

## Port 26–Port 29

P[26:29] consist of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have PWM functionality, which can be used for LED dimming.

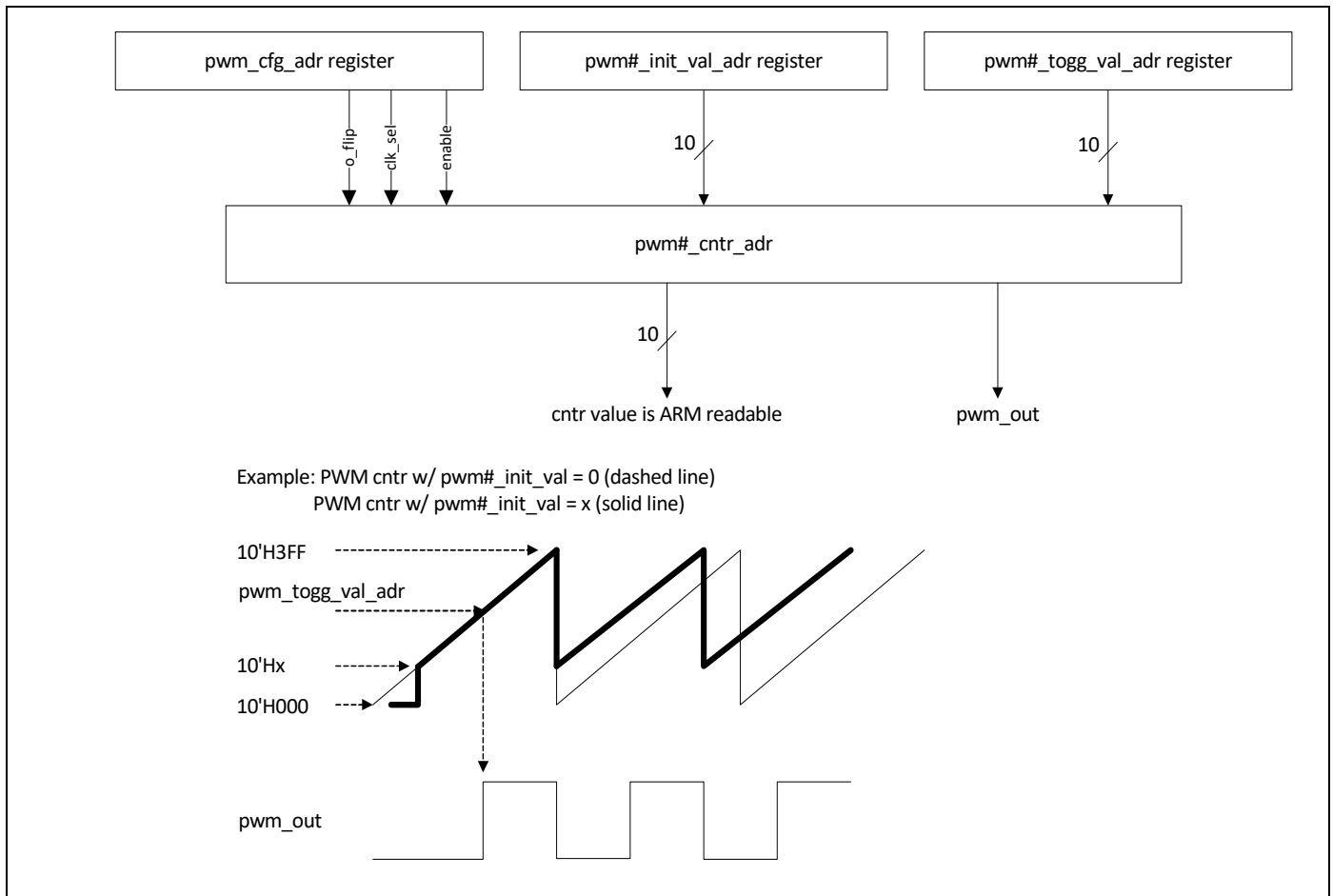
### 1.10 PWM

The CYW20706 has four internal PWMs. The PWM module consists of the following:

- PWM1–4
- Each of the four PWM channels, PWM1–4, contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1–4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 5 shows the structure of one PWM.

Figure 5. PWM Block Diagram



### 1.11 Triac Control

The CYW20706 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYW20706 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYW20706 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

**Note:** Subject to support in WICED Studio.

### 1.12 Serial Peripheral Interface

The CYW20706 has two independent SPI interfaces. One is a master-only interface (SPI\_2) and the other (SPI\_1) can be either a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20706 has optional I/O ports that can be configured individually and separately for each functional pin. The CYW20706 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The CYW20706 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.

**Note:** SPI voltage depends on VDDO; therefore, it defines the type of devices that can be supported.

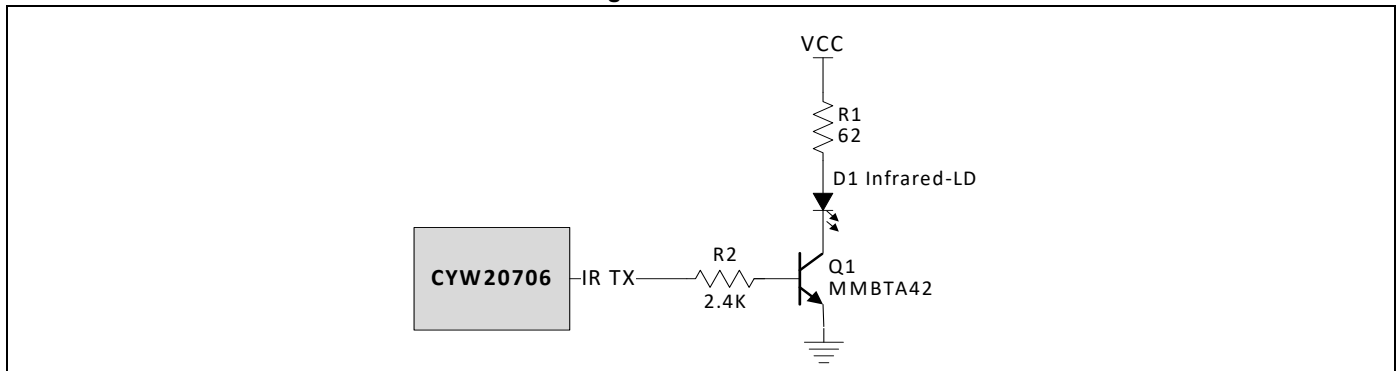
### 1.13 Infrared Modulator

The CYW20706 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767  $\mu$ sec. The CYW20706 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to underrun (see [Figure 6](#)).

**Note:** Subjected to driver support in WICED.

Figure 6. Infrared TX





## 1.14 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

### 1.14.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

### 1.14.2 Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDEOFF (deep sleep) mode.

### 1.14.3 BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYW20706 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYW20706 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDEOFF (deep sleep) mode

The CYW20706 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the CYW20706 immediately enters Active mode.

In HIDEOFF mode, the CYW20706 baseband and core are powered off by disabling power to VDDC\_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

## 2. Pin Assignments

### 2.1 Pin Descriptions

#### 2.1.1 49-Pin FBGA List

Table 7. CYW20706 49-Pin FBGA List

Pin	Signal	I/O	Power Domain	Description
<b>Radio</b>				
A2	RFOP	I/O	VDD_RF	RF I/O antenna port
A4	XO_IN	I	VDD_RF	Crystal or reference input
A5	XO_OUT	O	VDD_RF	Crystal oscillator output
<b>Voltage Regulators</b>				
D1	VBAT	I	N/A	VBAT input pin. This must be less than or equal to VDDO.
E1	VDD2P5_IN	I	N/A	2.5V LDO input
E2	VDD2P5_OUT	O	N/A	2.5V LDO output
F1	VDDC_OUT	O	N/A	1.2V LDO output
<b>Straps</b>				
G3	BT_XTAL_STRAP_0	I	VDDO	A strap for choosing the XTAL frequencies.
F2	BT_XTAL_STRAP_1	I	VDDO	A strap for choosing the XTAL frequencies.
A6	RST_N	I	VDDO	Active-low reset input
G7	BT_TM1	I	VDDO	Reserved: connect to ground.
<b>Digital I/O</b>				
F8	BT_GPIO_0	I	VDDO	BT_GPIO_0/BT_DEV_WAKE A signal from the host to the CYW20706 that the host requires attention.
	P36	I/O	VDDO	GPIO: P36 A/D converter input 3 Quadrature: QDZ0 SPI_1: SPI_CLK (master and slave) Auxiliary Clock Output: ACLK0 External T/R switch control: ~tx_pd
	P38	I/O	VDDO	GPIO: P38 A/D converter input 1 SPI_1: MOSI (master and slave) IR_TX
F7	BT_GPIO_1	O	VDDO	BT_GPIO_1/BT_HOST_WAKE A signal from the CYW20706 device to the host indicating that the Bluetooth device requires attention.
	P25	I/O	VDDO	GPIO: P25 SPI_1: MISO (master and slave) Peripheral UART: puart_rx
	P32	I/O	VDDO	GPIO: P32 A/D converter input 7 Quadrature: QDX0 SPI_1: SPI_CS (slave only) Auxiliary clock output: ACLK0 Peripheral UART: puart_tx
E4	BT_GPIO_2	I	VDDO	When high, this signal extends the XTAL warm-up time for external CLK requests. Otherwise, it is typically connected to ground.

Table 7. CYW20706 49-Pin FBGA List (Cont.)

Pin	Signal	I/O	Power Domain	Description
C5	BT_GPIO_3	I/O	VDDO	General-purpose I/O
	P27 PWM1	I/O	VDDO	GPIO: P27 SPI_1: MOSI (master and slave) Optical control output: QOC1 Triac control 2 Current: 16 mA sink
	P33	I/O	VDDO	GPIO: P33 A/D converter input 6 Quadrature: QDX1 SPI_1: MOSI (slave only) Auxiliary clock output: ACLK1 Peripheral UART: puart_rx
D6	BT_GPIO_4	I/O	VDDO	General-purpose I/O: can also be configured as a GCI pin.
	P6	I/O	VDDO	GPIO: P6 Quadrature: QDZ0 Peripheral UART: puart_rts SPI_1: SPI_CS (slave only) 60Hz_main
	LPO_IN	I	N/A	External LPO input
	P31	I/O	VDDO	GPIO: P31 A/D converter input 8 Peripheral UART: puart_tx
B5	BT_GPIO_5	I/O	VDDO	General-purpose I/O: can also be configured as a GCI pin. Debug UART
	P15	I/O	VDDO	GPIO: P15 A/D converter input 20 IR_RX 60Hz_main
B6	BT_GPIO_6	I/O	VDDO	General-purpose I/O: can also be configured as a GCI pin.
	P11	I/O	VDDO	GPIO: P11 Keyboard scan output (column): KSO3 A/D converter input 24
	P26 PWM0	I/O	VDDO	GPIO: P26 SPI_1: SPI_CS (slave only) Optical control output: QOC0 Triac control 1 Current: 16 mA sink
C6	BT_GPIO_7	I/O	VDDO	General-purpose I/O: can also be configured as a GCI pin.
	P30	I/O	VDDO	GPIO: P30 A/D converter input 9 Peripheral UART: puart_rts
F5	BT_UART_RXD	I	VDDO	UART receive data
F4	BT_UART_TXD	O	VDDO	UART transmit data
F3	BT_UART_RTS_N	O	VDDO	UART request to send output
G4	BT_UART_CTS_N	I	VDDO	UART clear to send input

**Table 7. CYW20706 49-Pin FBGA List (Cont.)**

Pin	Signal	I/O	Power Domain	Description
G8	BT_CLK_REQ	O	VDDO	Used for shared-clock application.
	P4	I/O	VDDO	GPIO: P4 Quadrature: QDY0 Peripheral UART: puart_rx SPI_1: MOSI (master and slave) IR_TX
	P24	I/O	VDDO	GPIO: P24 SPI_1: SPI_CLK (master and slave) Peripheral UART: puart_tx
D8	SPI2_MISO_I2C_SCL	I/O	VDDO	BSC CLOCK
E8	SPI2_MOSI_I2C_SDA	I/O	VDDO	BSC DATA
E7	SPI2_CLK	O	VDDO	Serial flash SPI clock
D7	SPI2_CSN	O	VDDO	Serial flash active-low chip select
C7	I2S_DI/PCM_IN	I/O	VDDO	PCM/I2S data input. I2C_SDA
	P12	I/O	VDDO	GPIO: P12 A/D converter input 23
A8	I2S_DO/PCM_OUT	I/O	VDDO	PCM/I2S data output. I2C_SCL
	P3	I/O	VDDO	GPIO: P3 Quadrature: QDX1 Peripheral UART: puart_cts SPI_1: SPI_CLK (master and slave)
	P29 PWM3	I/O	VDDO	GPIO: P29 Optical control output: QOC3 A/D converter input 10, LED2 Current: 16 mA sink
	P35	I/O	VDDO	GPIO: P35 A/D converter input 4 Quadrature: QDY1 Peripheral UART: puart_cts BSC: SDA
B7	I2S_CLK/PCM_CLK	I/O	VDDO	PCM/I2S clock Fp1
	P2	I/O	VDDO	GPIO: P2 Quadrature: QDX0 Peripheral UART: puart_rx SPI_1: SPI_CS (slave only) SPI_1: MOSI (master only)
	P28 PWM2	I/O	VDDO	GPIO: P28 Optical control output: QOC2 A/D converter input 11, LED1 Current: 16 mA sink
	P37	I/O	VDDO	GPIO: P37 A/D converter input 2 Quadrature: QDZ1 SPI_1: MISO (slave only) Auxiliary clock output: ACLK1 BSC: SCL

Table 7. CYW20706 49-Pin FBGA List (Cont.)

Pin	Signal	I/O	Power Domain	Description
C8	I <sup>2</sup> S_WS/ PCM_SYNC	I/O	VDDO	PCM sync/I2S word select
	P0	I/O	VDDO	GPIO: P0 A/D converter input 29 Peripheral UART: puart_tx SPI_1: MOSI (master and slave) IR_RX, 60Hz_main <b>Note:</b> Not available during TM1 = 1.
	P34	I/O	VDDO	GPIO: P34 A/D converter input 5 Quadrature: QDY0 Peripheral UART: puart_rx External T/R switch control: tx_pd
G2	BT_OTP_3P3V_ON	I	VDDO	<ul style="list-style-type: none"> <li>If OTP is used, pull this pin high.</li> <li>If OTP is not used, pull this pin low.</li> </ul>
<b>JTAG</b>				
D5	JTAG_SEL	I/O	VDDO	ARM JTAG debug mode control. Connect to GND for all applications.
<b>Supplies</b>				
G1	BT_OTP_VDD3P3V	I	N/A	3.3V OTP supply voltage
B4	BT_IFVDD1P2	I	N/A	Radio IF PLL supply
A1	BT_PAVDD2P5	I	N/A	Radio PA supply
B1	BT_LNAVDD1P2	I	N/A	Radio LNA supply
C1	BT_VCOVDD1P2	I	N/A	Radio VCO supply
A3	BT_PLLVDD1P2	I	N/A	Radio RF PLL supply
B8, G6	VDDC	I	N/A	Core logic supply
G5	VDDO	I	N/A	Digital I/O supply voltage
A7, B2, B3, C2, D2, F6	VSS	–	N/A	Ground

2.2 Ball Map

2.2.1 49-Pin FBGA Ball Map

Figure 7. CYW20706 49-Pin FBGA Ball Map

	1	2	3	4	5	6	7	8	
A	BT_PAVDD2P5	RFOP	BT_PLLVDD1P2	XO_IN	XO_OUT	RST_N	VSS	I <sup>2</sup> S_DO/PCM_OUT/P3/ P29/P35	A
B	BT_LNAVDD1P2	VSS	VSS	BT_IFVDD1P2	BT_GPIO_5/P15	BT_GPIO_6/ P11/P26	I <sup>2</sup> S_CLK/ PCM_CLK/ P2/P28/P37	VDDC	B
C	BT_VCOVDD1P2	VSS	NC	NC	BT_GPIO_3/P27/ P33	BT_GPIO_7/ P30	I <sup>2</sup> S_DI/PCM_IN/ P12	I <sup>2</sup> S_WS/PCM_SYNC/P0/ P34	C
D	VBAT	VSS	NC	NC	JTAG_SEL	BT_GPIO_4/ P6/LPO_IN/ P31	SPI2_CSN	SPI2_MISO_I <sup>2</sup> C_SCL	D
E	VDD2P5_IN	VDD2P5_OUT	NC	BT_GPIO_2	NC	NC	SPI2_CLK	SPI2_MOSI_I <sup>2</sup> C_SDA	E
F	VDDC_OUT	BT_XTAL_STRAP_1	BT_UART_RTS_N	BT_UART_TXD	BT_UART_RXD	VSS	BT_GPIO_1/P25/ P32	BT_GPIO_0/P36/P38	F
G	BT_OTP_VDD3P3V	BT_OTP_3P3V_ON	BT_XTAL_STRAP_0	BT_UART_CTS_N	VDDO	VDDC	BT_TM1	BT_CLK_REQ/P4/P24	G
	1	2	3	4	5	6	7	8	

### 3. Specifications

#### 3.1 Electrical Characteristics

Table 8 shows the maximum electrical rating for voltages referenced to VDD pin.

**Table 8. Absolute Maximum Ratings**

Parameter	Specification			Units
	Minimum	Nominal	Maximum	
Ambient temperature of operation	-30	25	85	°C
Storage temperature	-40	-	150	°C
ESD tolerance HBM	-2000	-	2000	V
ESD tolerance MM	-100	-	100	V
ESD tolerance CDM	-500	-	500	V
Latch-up	-200	-	200	mA
VDDC	-0.5	-	1.38	V
VDDO	-0.5	-	3.795	V
VDD_RF (excluding PA)	-0.5	-	1.38	V
VDDPA	-0.5	-	3.565	V
VBAT	-0.5	-	3.795	V
BT_OTP_VDD3P3V	-0.5	-	3.795	V
VDD2P5_IN	-0.5	-	3.795	V

Table 9 shows the power supply characteristics for the range  $T_J = 0^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Table 9. Power Supply Specifications**

Parameter	Conditions	Min.	Typ.	Max.	Units
VDD Core	-	1.14	1.2	1.26	V
VDDO <sup>1</sup>	-	1.62	3.3	3.6	V
VDDRF	Excluding class 1 PA	1.14	1.2	1.26	V
VDDPA	Class 1 operation	2.25	2.5 to 2.8	2.94	V
VBAT <sup>1</sup>	-	1.62	3.3	3.6	V
BT_OTP_VDD3P3V	-	3.0	3.3	3.6	V
VDD2P5_IN	-	3.0	3.3	3.6	V

1. VDDO must be  $\geq$  VBAT.

**Table 10. VDDC LDO Electrical Specifications**

Parameter	Conditions	Min.	Typical	Max.	Unit	
Input Voltage	–	1.62	3.3	3.6	V	
Nominal Output Voltage	–	–	1.2	–	V	
DC Accuracy	Accuracy at any step, including bandgap reference.	–5	–	5	%	
Output Voltage Programmability	Range	0.89	–	1.34	V	
	Step Size	–	30	–	mV	
Load Current	–	–	–	40	mA	
Dropout Voltage	$I_{load} = 40\text{ mA}$	–	–	200	mV	
Line Regulation	$V_{in}$ from 1.62V to 3.6V, $I_{load} = 40\text{ mA}$	–	–	0.2	%Vo/V	
Load Regulation	$I_{load} = 1\text{ mA to }40\text{ mA}$ , $V_{out} = 1.2\text{V}$ , Package + PCB $R = 0.3\Omega$	–	0.02	0.05	%Vo/mA	
Quiescent Current	No load @ $V_{in} = 3.3\text{V}$	–	18	23	$\mu\text{A}$	
Power down Current	$V_{in} = 3.3\text{V @}25\text{C}$	–	0.2	–	$\mu\text{A}$	
	$V_{in} = 3.6\text{ @}80\text{C}$	–	TBD	–	–	
Output Noise	$I_{load} = 15\text{ mA}$ , 100 kHz	–	–	40	nV/sqrtHz	
	$I_{load} = 15\text{ mA}$ , 2 MHz	–	–	14	nV/sqrtHz	
PSRR	$V_{in} = 3.3$ , $V_{out} = 1.2\text{V}$ , $I_{load} = 40\text{ mA}$	1 kHz	65	–	–	dB
		10 kHz	60	–	–	dB
		100 kHz	55	–	–	dB
Over Current Limit	–	100	–	–	mA	
Turn-on Time	$V_{BAT} = 3.3\text{V}$ , BG already on, LDO OFF to ON, $C_o = 1\text{ }\mu\text{F}$ , 90% of $V_{out}$	–	–	100	$\mu\text{s}$	
In-rush current during turn-on	During start-up, $C_o = 1\text{ }\mu\text{F}$	–	–	60	mA	
Transient Performance	$I_{load} = 1\text{ mA to }15\text{ mA}$ and $15\text{ mA to }1\text{ mA}$ in $1\text{ }\mu\text{s}$	–	–	40	mV	
	$I_{load} = 15\text{ mA to }40\text{ mA}$ and $40\text{ mA to }15\text{ mA}$ in $1\text{ }\mu\text{s}$	–	–	25	–	
External Output Capacitor	Ceramic cap with $\text{ESR} \leq 0.5\Omega$	0.8	1	4.7	$\mu\text{F}$	
External Input Capacitor	Ceramic, X5R, 0402, $\pm 20\%$ , 10V.	–	1	–	$\mu\text{F}$	



Table 11. BTLDO\_2P5 Electrical Specifications

Parameters	Conditions	Min	Typ	Max	Units
Input supply voltage, $V_{in}$	Min = $V_o + 0.2V = 2.7V$ (for $V_o = 2.5V$ ) Dropout voltage requirement must be met under maximum load for performance specs.	3.0	3.3	3.6	V
Nominal output voltage, $V_o$	Default = 2.5V	–	2.5	–	V
Output voltage programmability	Range Accuracy at any step (including line/load regulation), load >0.1 mA	2.2 –5	–	2.8 5	V %
Dropout voltage	At max load	–	–	200	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load; $V_{in} = V_o + 0.2V$ , $V_{in} = V_o + 0.2V$	–	8 660	16 700	$\mu A$
Leakage current	Power-down mode. At junction temperature 85°C.	–	1.5	5	$\mu A$
Line regulation	$V_{in}$ from ( $V_o + 0.2V$ ) to 3.6V, max load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, $V_{in} = 3.6V$	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o + 0.2V$ , $V_o = 2.5V$ , $C_o = 2.2 \mu F$ , max load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	150	$\mu s$
External output capacitor, $C_o$	Ceramic, X5R, 0402, (ESR: 5m-240 m $\Omega$ ), $\pm 20\%$ , 6.3V	0.7	2.2	2.64	$\mu F$
External input capacitor	Ceramic, X5R, 0402, $\pm 20\%$ , 10V	–	1	–	$\mu F$

3.1.1 Digital I/O Characteristics

Table 12. Digital I/O Characteristics

Characteristics	Value	Symbol	Minimum	Typical	Maximum	Unit
<b>Input Voltage</b>						
■ Low	VDDO = 1.8V	$V_{IL}$	–	–	0.6	V
	VDDO = 3.3	$V_{IL}$	–	–	0.8	V
■ High	VDDO = 1.8V	$V_{IH}$	1.1	–	–	V
	VDDO = 3.3V	$V_{IH}$	2.0	–	–	V
<b>Output Voltage</b>						
■ Low	–	$V_{OL}$	–	–	0.4	V
■ High	VDDO – 0.4V	$V_{OH}$	–	–	–	V
<b>Input Current</b>						
■ Low	–	$I_{IL}$	–	–	1.0	$\mu$ A
■ High	–	$I_{IH}$	–	–	1.0	$\mu$ A
<b>Output Current</b>						
■ Low	VDDO = 3.3V, $V_{OL}$ = 0.4V	$I_{OL}$	–	–	2.0	mA
■ High	VDDO = 3.3V, $V_{OH}$ = 2.9V	$I_{OH}$	–	–	4.0	mA
	VDDO = 1.8V, $V_{OH}$ = 1.4	$I_{OH}$	–	–	TBD	mA
<b>Input capacitance</b>	–	$C_{IN}$	–	–	0.4	pF

**Note:** In Table 13, current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDO and VDD2P5\_IN.

## 3.1.2 Current Consumption

**Table 13. Bluetooth, BLE, BR and EDR Current Consumption, Class 1**

Mode	Remarks	Typ.	Unit
<b>3DH5/3DH5</b>	–	37.10	mA
<b>BLE</b>			
■ BLE	Connected 600 ms interval	211	μA
■ BLE ADV	1.00 sec ADV interval	176	μA
■ BLE Scan	No devices present. A 1.28-sec interval with 11.25 ms scan window.	355	μA
<b>DMx/DHx</b>			
■ DM1/DH1	–	32.15	mA
■ DM3/DH3	–	38.14	mA
■ DM5/DH5	–	38.46	mA
<b>HIDOFF</b>	Deep sleep	2.69	μA
<b>Page scan</b>	Periodic scan rate is 1.28 sec	0.486	mA
<b>Receive</b>			
■ 1 Mbps	Peak current level during reception of a basic-rate packet.	26.373	mA
■ EDR	Peak current level during the reception of a 2 or 3 Mbps rate packet.	26.373	mA
<b>Sniff Slave</b>			
■ 11.25 ms	–	4.95	mA
■ 22.5 ms	–	2.6	mA
■ 495.00 ms	Based on one attempt and no timeout.	254	μA
<b>Transmit</b>			
■ 1 Mbps	Peak current level during the transmission of a basic-rate packet: GFSK output power = 10 dBm.	60.289	mA
■ EDR	Peak current level during the transmission of a 2 or 3 Mbps rate packet. EDR output power = 8 dBm.	52.485	mA

**Note:** In Table 14, current consumption measurements are taken at input of VDD2P5\_IN, VDDO, and VBAT combined (VDD2P5\_IN = VDDO = VBAT = 3.0V).

**Table 14. Bluetooth and BLE Current Consumption, Class 2 (0 dBm)**

Mode	Remarks	Typ.	Unit
<b>3DH5/3DH5</b>	–	31.57	mA
<b>BLE</b>			
■ BLE ADV	1.00 sec ADV interval	174	μA
■ BLE Scan	No devices present. A 1.28-sec interval with 11.25 ms scan window.	368	μA
<b>DMx/DHx</b>			
■ DM1/DH1	–	27.5	mA
■ DM3/DH3	–	31.34	mA
■ DM5/DH5	–	32.36	mA

### 3.2 RF Specifications

**Note:**

- All specifications in Table 15 are for industrial temperatures.
- All specifications in Table 15 are single-ended. Unused inputs are left open.

**Table 15. Receiver RF Specifications**

Parameter	Conditions	Minimum	Typical <sup>1</sup>	Maximum	Unit
<b>General</b>					
Frequency range	–	2402	–	2480	MHz
RX sensitivity <sup>2</sup>	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	LE GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
	$\pi/4$ -DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	$\pi/4$ -DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
<b>Interference Performance</b>					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I $\geq$ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
C/I cochannel	$\pi/4$ -DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I $\geq$ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–40	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I $\geq$ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB
<b>Out-of-Band Blocking Performance (CW)<sup>3</sup></b>					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Table 15. Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical <sup>1</sup>	Maximum	Unit
<b>Out-of-Band Blocking Performance, Modulated Interferer</b>					
776–764 MHz	CDMA	–	–10 <sup>4</sup>	–	dBm
824–849 MHz	CDMA	–	–10 <sup>4</sup>	–	dBm
1850–1910 MHz	CDMA	–	–23 <sup>4</sup>	–	dBm
824–849 MHz	EDGE/GSM	–	–10 <sup>4</sup>	–	dBm
880–915 MHz	EDGE/GSM	–	–10 <sup>4</sup>	–	dBm
1710–1785 MHz	EDGE/GSM	–	–23 <sup>4</sup>	–	dBm
1850–1910 MHz	EDGE/GSM	–	–23 <sup>4</sup>	–	dBm
1850–1910 MHz	WCDMA	–	–23 <sup>4</sup>	–	dBm
1920–1980 MHz	WCDMA	–	–23 <sup>4</sup>	–	dBm
<b>Intermodulation Performance<sup>5</sup></b>					
BT, Df = 5 MHz	–	–39.0	–	–	dBm
<b>Spurious Emissions<sup>6</sup></b>					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM Rx	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz
<b>GLONASS Band Spurious Emissions<sup>7</sup></b>					
Spurious Emissions	-	-	-118	-	dBm/Hz
<b>Out-of-Band Noise Floor</b>					
1570-1580MHz	GPS	-	-147	-	dBm/Hz
1592-1610MHz	GLONASS	-	-147	-	dBm/Hz

1. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
2. The receiver sensitivity is measured at BER of 0.1% on the device interface.
3. Meets this specification using a front-end bandpass filter.
4. Numbers are referred to the pin output with an external BPF filter.
5. f<sub>0</sub> = –64 dBm Bluetooth-modulated signal, f<sub>1</sub> = –39 dBm sine wave, f<sub>2</sub> = –39 dBm Bluetooth-modulated signal, f<sub>0</sub> = 2f<sub>1</sub> – f<sub>2</sub>, and |f<sub>2</sub> – f<sub>1</sub>| = n\*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
6. Includes baseband radiated emissions.
7. Max TX power (12dBm at chip out), Modulation is PRBS9, Modulation type is GFSK.

**Note:**

- All specifications in Table 16 are for industrial temperatures.
- All specifications in Table 16 are single-ended. Unused inputs are left open.

Table 16. Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
<b>General</b>					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK Tx power <sup>1</sup>	–	–	12	–	dBm
Class1: EDR Tx power <sup>2</sup>	–	–	9	–	dBm
Class 2: GFSK Tx power	–	–	2	–	dBm
Power control step	–	2	4	8	dB
<b>Modulation Accuracy</b>					
$\pi/4$ -DQPSK Frequency Stability	–	–10	–	10	kHz
$\pi/4$ -DQPSK RMS DEVM	–	–	–	20	%
$\pi/4$ -QPSK Peak DEVM	–	–	–	35	%
$\pi/4$ -DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
<b>In-Band Spurious Emissions</b>					
1.0 MHz <  M – N  < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz <  M – N  < 2.5 MHz	–	–	–	–20	dBm
M – N  $\geq$ 2.5 MHz	–	–	–	–40	dBm
<b>Out-of-Band Spurious Emissions</b>					
30 MHz to 1 GHz	–	–	–	–36.0 <sup>3</sup>	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 <sup>3, 4</sup>	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

1. 12 dBm output for GFSK measured with PAVDD = 2.5V.
2. 9 dBm output for EDR measured with PAVDD = 2.5V.
3. Maximum value is the value required for Bluetooth qualification.
4. Meets this spec using a front-end band pass filter.

**Table 17. BLE RF Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	N/A	2402	–	2480	MHz
Rx sense <sup>1</sup>	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
Tx power <sup>2</sup>	N/A	–	9	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max <sup>3</sup>	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

1. Dirty Tx is Off.
2. The BLE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc. The output is capped at 12 dBm out. The BLE Tx power at the antenna port cannot exceed the 10 dBm EIRP specification limit.
3. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

### 3.3 Timing and AC Characteristics

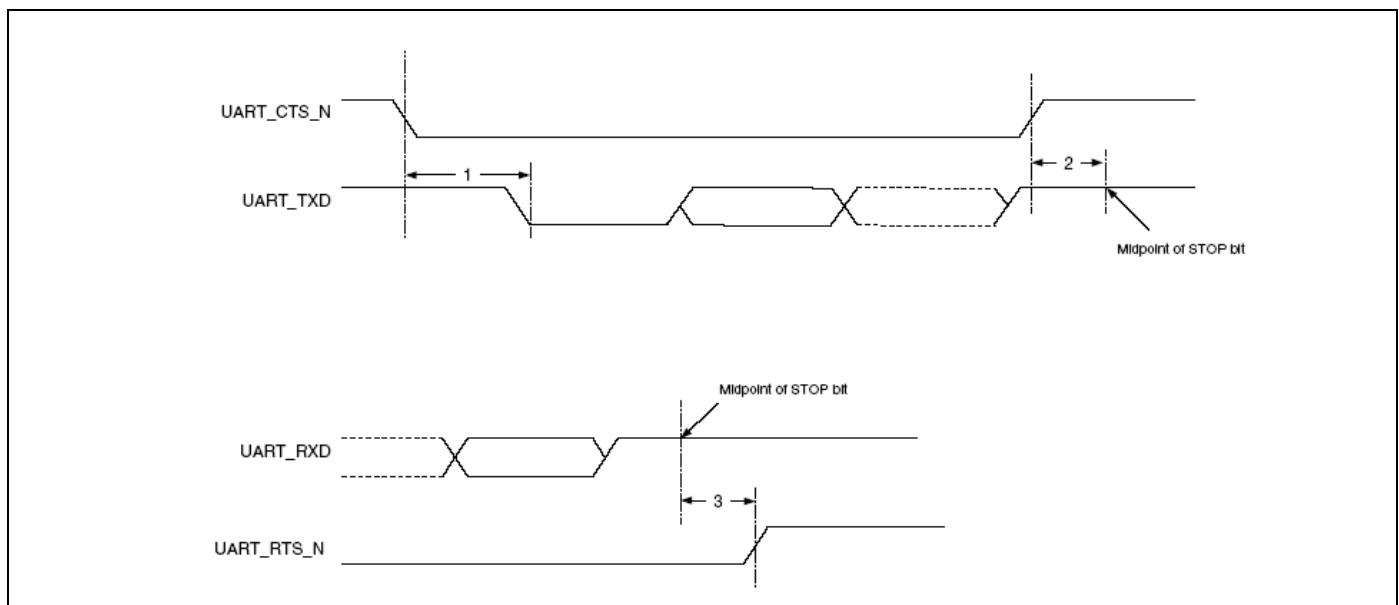
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

#### 3.3.1 UART Timing

**Table 18. UART Timing Specifications**

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

**Figure 8. UART Timing**



3.3.2 SPI Timing

The SPI interface can be clocked up to 12 MHz.

Table 19 and Figure 9 show the timing requirements when operating in SPI Mode 0 and 2.

Table 19. SPI Mode 0 and 2

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	$\infty$	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	$\infty$	ns
3	Time from master assert SPI_CSN to first clock edge	20	$\infty$	ns
4	Setup time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
5	Hold time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	$\infty$	ns
8	Idle time between subsequent SPI transactions	1 SCK	$\infty$	ns

Figure 9. SPI Timing, Mode 0 and 2

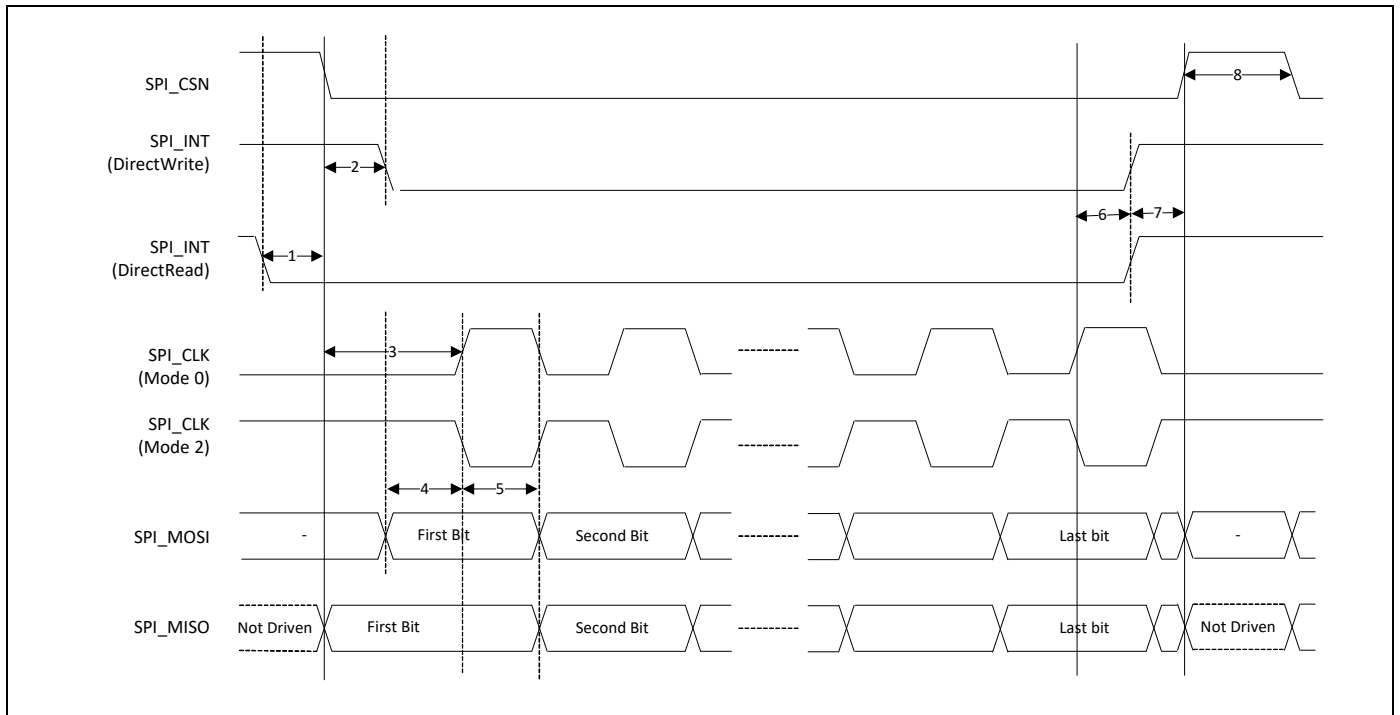


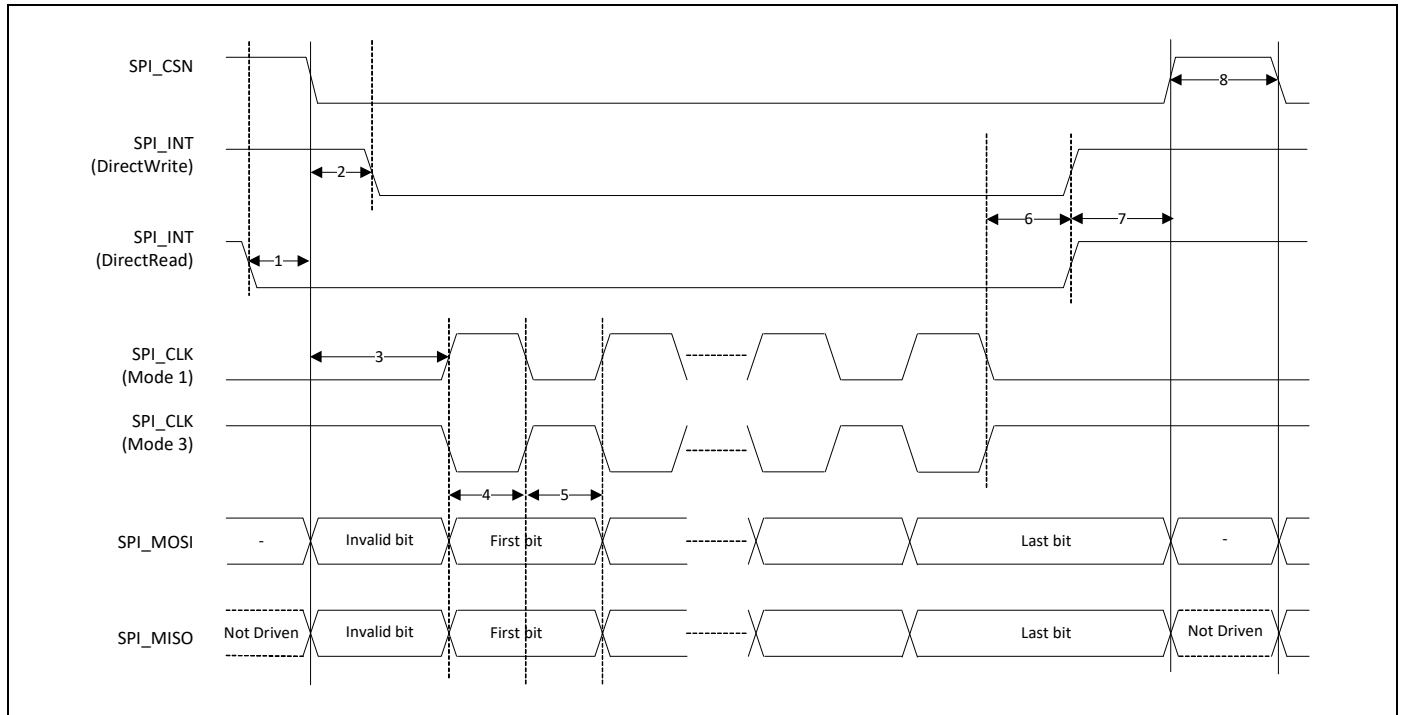
Table 20 and Figure 10 show the timing requirements when operating in SPI Mode 0 and 2.



Table 20. SPI Mode 1 and 3

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	$\infty$	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	$\infty$	ns
3	Time from master assert SPI_CSN to first clock edge	20	$\infty$	ns
4	Setup time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
5	Hold time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	$\infty$	ns
8	Idle time between subsequent SPI transactions	1 SCK	$\infty$	ns

Figure 10. SPI Timing, Mode 1 and 3



3.3.3 BSC Interface Timing

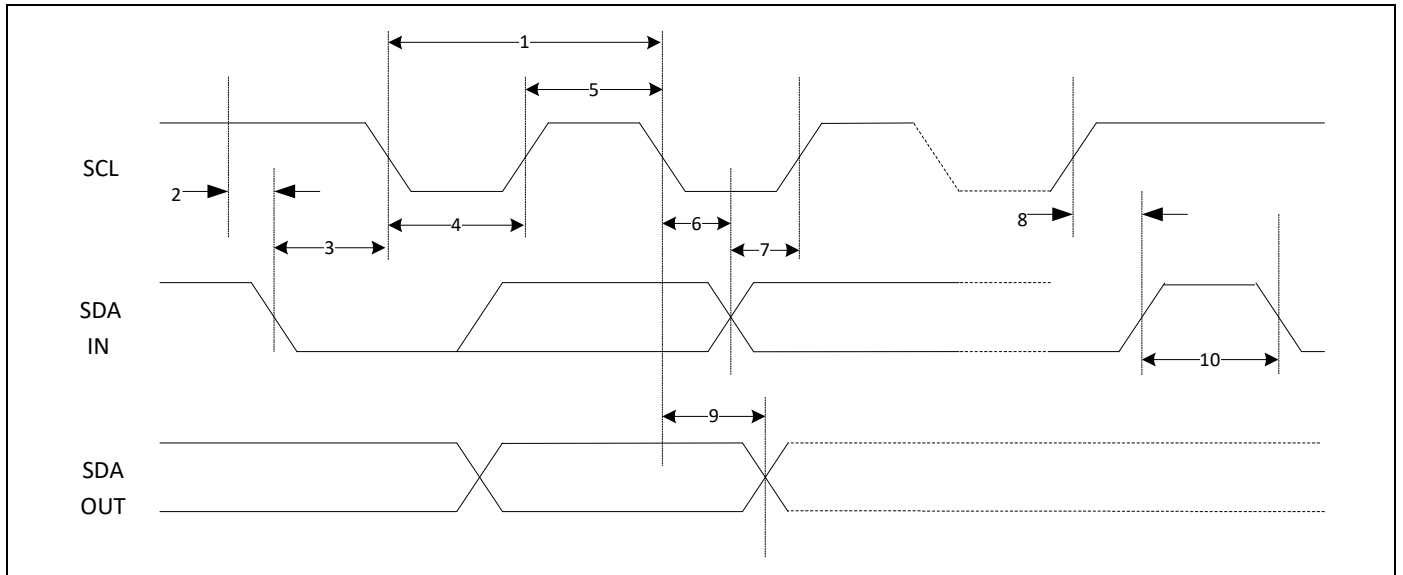
The specifications in Table 21 references Figure 11.

Table 21. BSC Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	-	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	-	ns
3	START condition hold time	280	-	ns
4	Clock low time	650	-	ns
5	Clock high time	280	-	ns
6	Data input hold time <sup>1</sup>	0	-	ns
7	Data input setup time	100	-	ns
8	STOP condition setup time	280	-	ns
9	Output valid from clock	-	400	ns
10	Bus free time <sup>2</sup>	650	-	ns

1. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
2. Time that the CBUS must be free before a new transaction can start.

Figure 11. BSC Interface Timing Diagram



3.3.4 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 12. PCM Timing Diagram (Short Frame Sync, Master Mode)

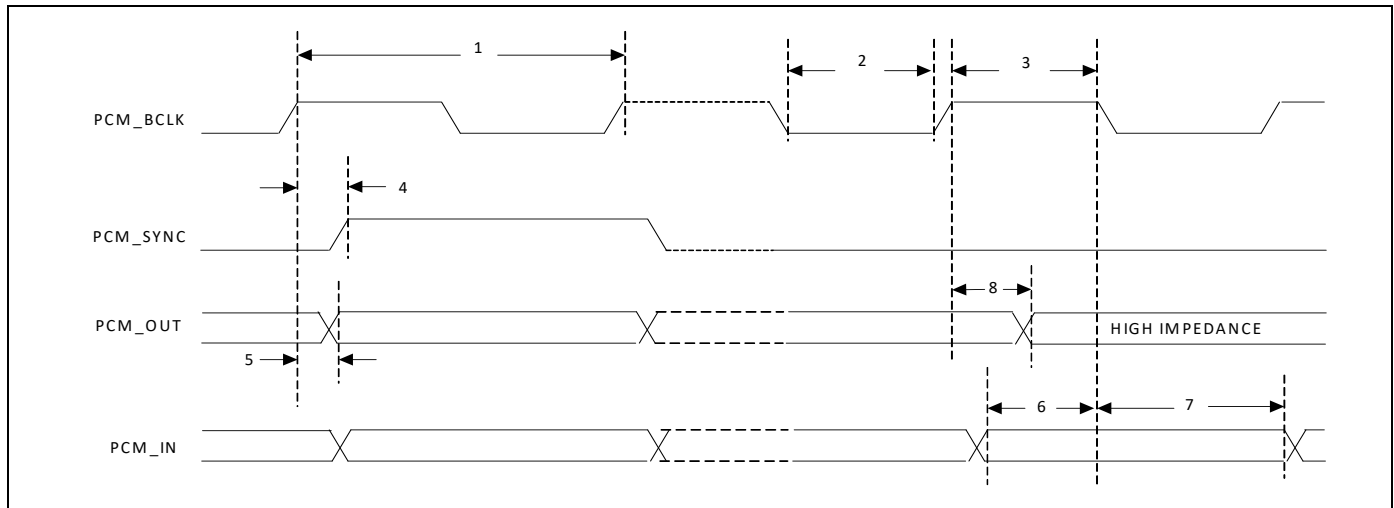


Table 22. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC delay	0	–	25.0	ns
5	PCM_OUT delay	0	–	25.0	ns
6	PCM_IN setup	8.0	–	–	ns
7	PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

Short Frame Sync, Slave Mode

Figure 13. PCM Timing Diagram (Short Frame Sync, Slave Mode)

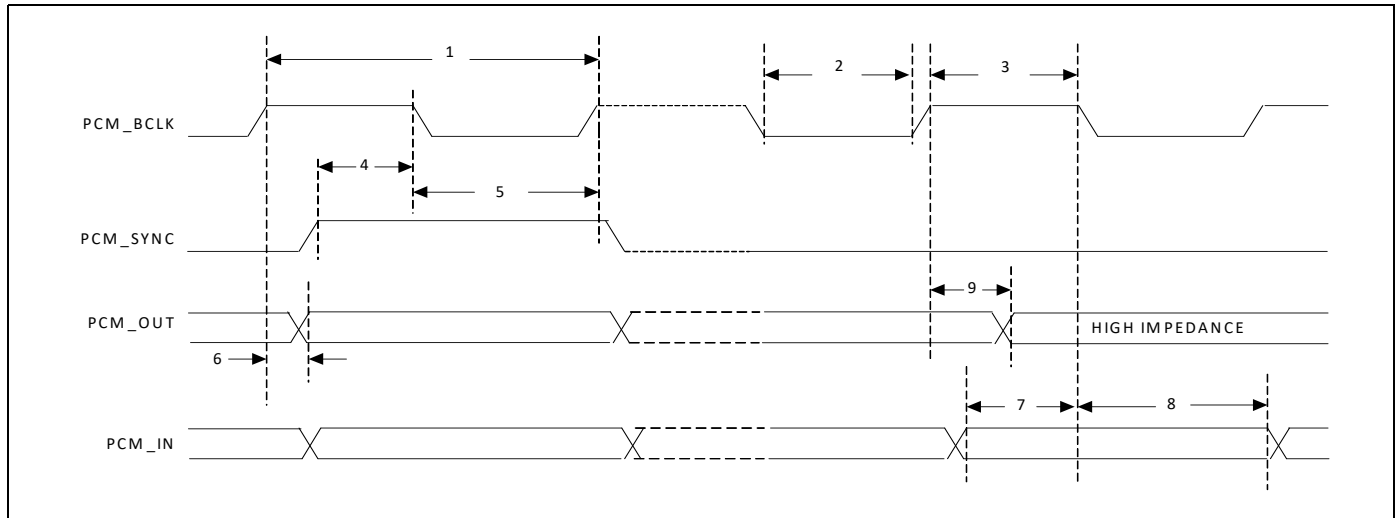


Table 23. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC setup	8.0	–	–	ns
5	PCM_SYNC hold	8.0	–	–	ns
6	PCM_OUT delay	0	–	25.0	ns
7	PCM_IN setup	8.0	–	–	ns
8	PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

Long Frame Sync, Master Mode

Figure 14. PCM Timing Diagram (Long Frame Sync, Master Mode)

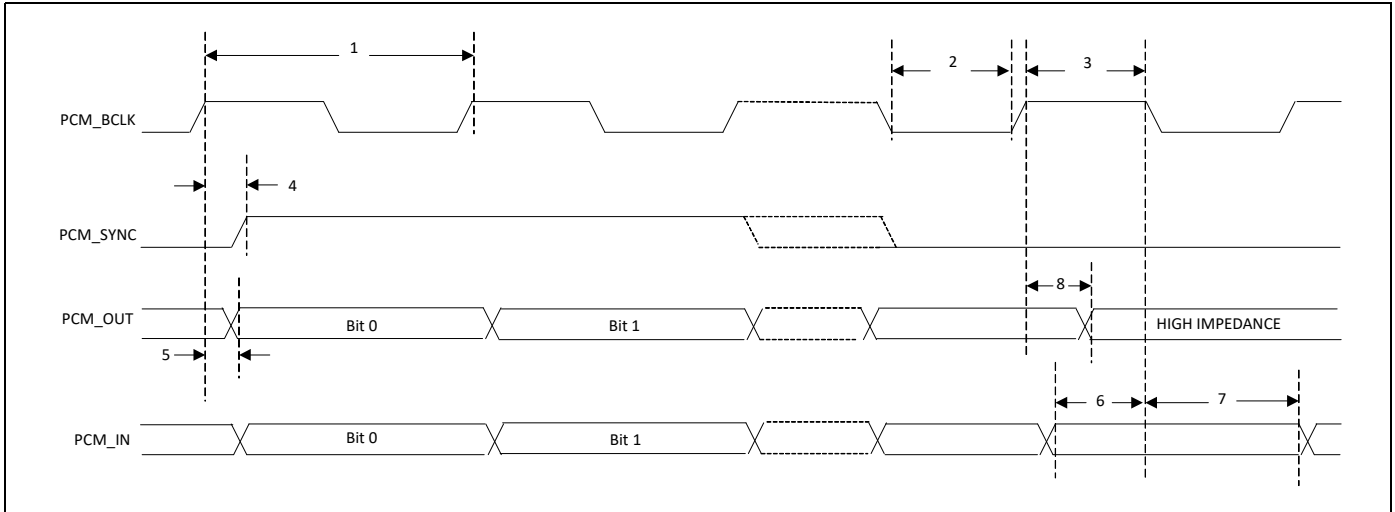


Table 24. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC delay	0	–	25.0	ns
5	PCM_OUT delay	0	–	25.0	ns
6	PCM_IN setup	8.0	–	–	ns
7	PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

Long Frame Sync, Slave Mode

Figure 15. PCM Timing Diagram (Long Frame Sync, Slave Mode)

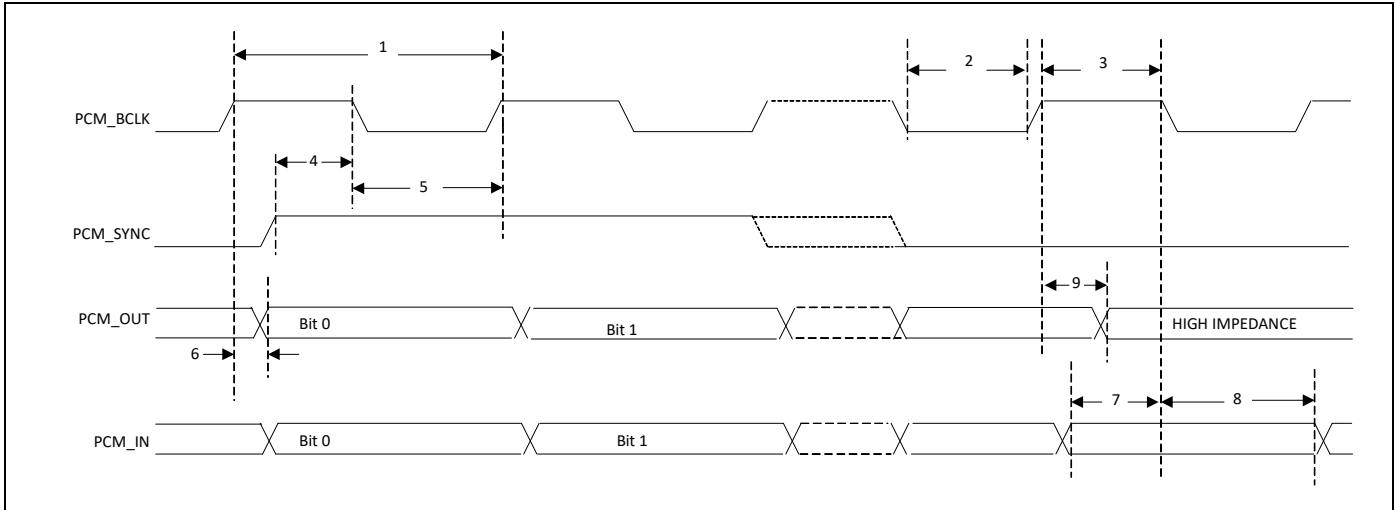


Table 25. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC setup	8.0	–	–	ns
5	PCM_SYNC hold	8.0	–	–	ns
6	PCM_OUT delay	0	–	25.0	ns
7	PCM_IN setup	8.0	–	–	ns
8	PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

3.3.5 I<sup>2</sup>S Timing

The CYW20706 supports two independent I<sup>2</sup>S digital audio ports. The I<sup>2</sup>S interface supports both master and slave modes. The I<sup>2</sup>S signals are:

- I<sup>2</sup>S clock: I<sup>2</sup>S SCK
- I<sup>2</sup>S Word Select: I<sup>2</sup>S WS
- I<sup>2</sup>S Data Out: I<sup>2</sup>S SDO
- I<sup>2</sup>S Data In: I<sup>2</sup>S SDI

I<sup>2</sup>S SCK and I<sup>2</sup>S WS become outputs in master mode and inputs in slave mode, while I<sup>2</sup>S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I<sup>2</sup>S bus, per the I<sup>2</sup>S specification. The MSB of each data word is transmitted one bit clock cycle after the I<sup>2</sup>S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I<sup>2</sup>S WS is low, and right-channel data is transmitted when I<sup>2</sup>S WS is high. Data bits sent by the CYW20706 are synchronized with the falling edge of I<sup>2</sup>S\_SCK and should be sampled by the receiver on the rising edge of I<sup>2</sup>S\_SCK.

The clock rate in master mode is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

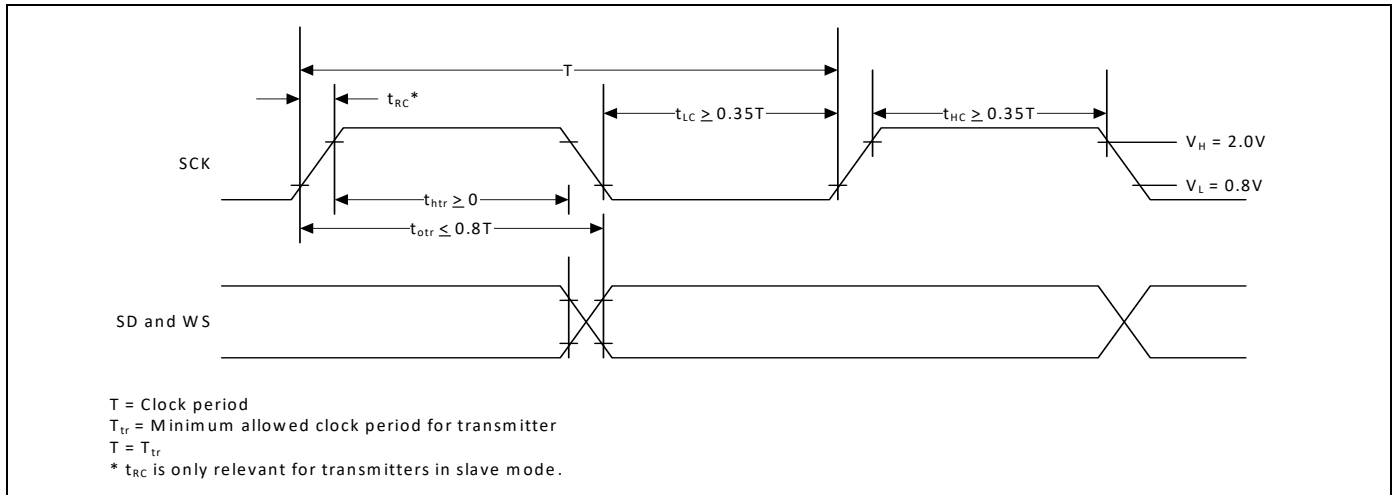
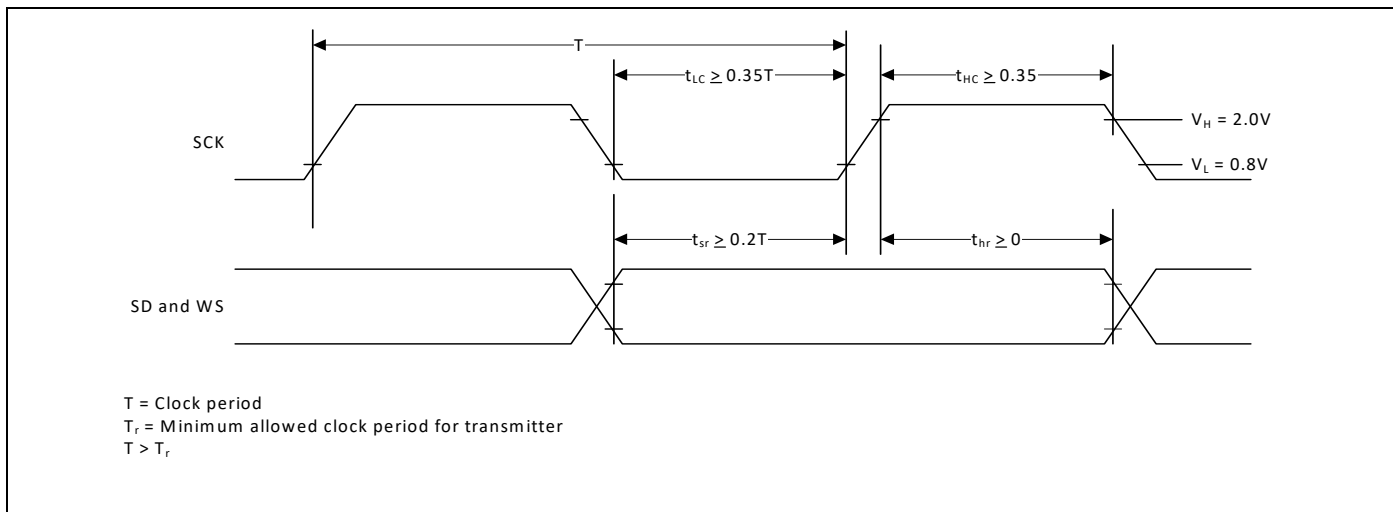
**Note:** Timing values specified in Table 26 are relative to high and low threshold levels.

**Table 26. Timing for I<sup>2</sup>S Transmitters and Receivers**

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	$T_{tr}$	–	–	–	$T_r$	–	–	–	1
<b>Master Mode: Clock generated by transmitter or receiver</b>									
HIGH $t_{HC}$	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
LOW $t_{LC}$	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
<b>Slave Mode: Clock accepted by transmitter or receiver</b>									
HIGH $t_{HC}$	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
LOW $t_{LC}$	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time $t_{RC}$	–	–	$0.15T_{tr}$	–	–	–	–	–	4
<b>Transmitter</b>									
Delay $t_{dtr}$	–	–	–	$0.8T$	–	–	–	–	5
Hold time $t_{htr}$	0	–	–	–	–	–	–	–	4
<b>Receiver</b>									
Setup time $t_{sr}$	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time $t_{hr}$	–	–	–	–	–	0	–	–	6

1. The system clock period T must be greater than  $T_{tr}$  and  $T_r$  because both the transmitter and receiver have to be able to handle the data transfer rate.
2. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason,  $t_{HC}$  and  $t_{LC}$  are specified with respect to T.
3. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than  $0.35T_r$ , any clock that meets the requirements can be used.
4. Because the delay ( $t_{dtr}$ ) and the maximum transmitter speed (defined by  $T_{tr}$ ) are related, a fast transmitter driven by a slow clock edge can result in  $t_{dtr}$  not exceeding  $t_{RC}$  which means  $t_{htr}$  becomes zero or negative. Therefore, the transmitter has to guarantee that  $t_{htr}$  is greater than or equal to zero, so long as the clock rise time  $t_{RC}$  is not more than  $t_{RCmax}$ , where  $t_{RCmax}$  is not less than  $0.15T_{tr}$ .
5. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
6. The data setup and hold time must not be less than the specified receiver setup and hold time.

**Note:** The time periods specified in Figure 16 and Figure 17 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

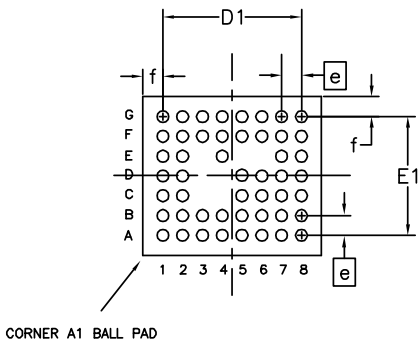
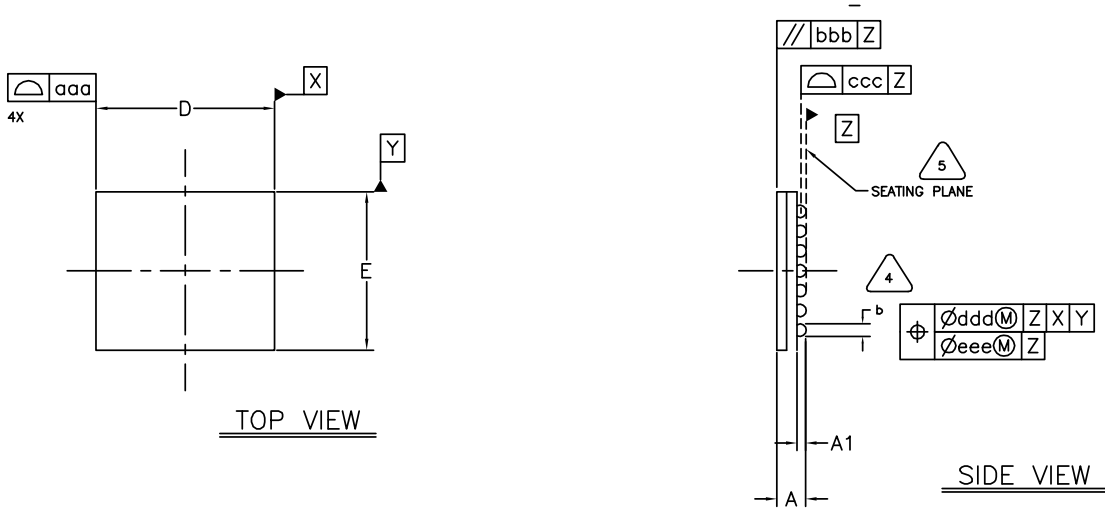
**Figure 16. I<sup>2</sup>S Transmitter Timing**

**Figure 17. I<sup>2</sup>S Receiver Timing**




### 4. Mechanical Information

#### 4.1 Package Diagrams

Figure 18. CYW20706 49-pin FBGA Package (4.5 mm x 4.0 mm)



**BOTTOM VIEW**  
(49 SOLDER BALLS)

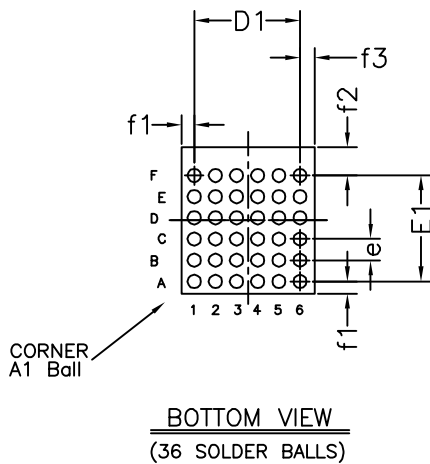
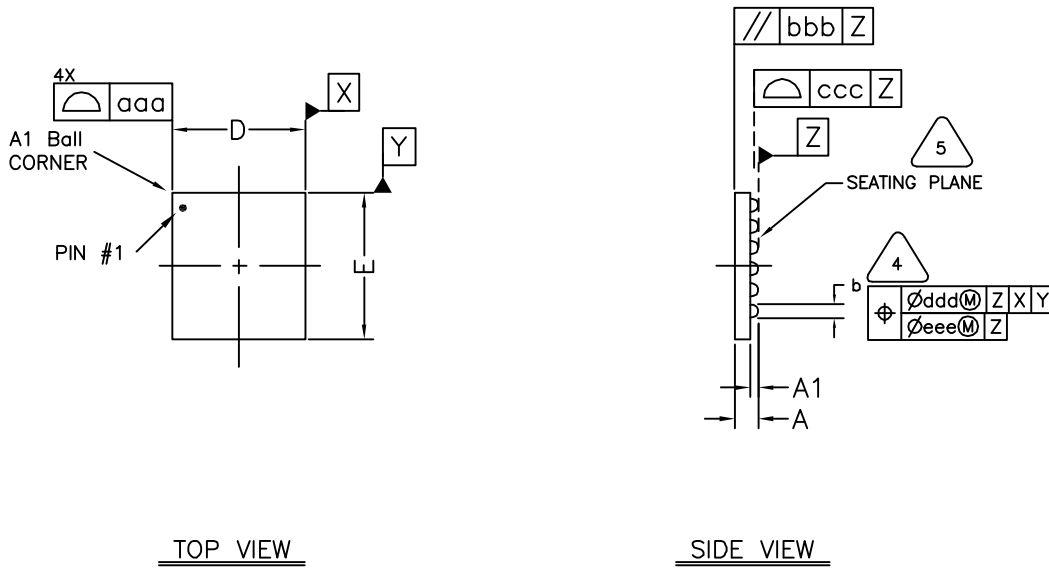
DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	-	-	1.05
A1	0.13	0.16	0.19
D	4.40	4.50	4.60
D1		3.50 BSC	
E	3.90	4.00	4.10
E1		3.00 BSC	
b	0.20	0.25	0.30
e		0.50 BSC	
f	-	0.5	-
aaa	-	-	0.10
bbb	-	-	0.10
ccc	-	-	0.08
ddd	-	-	0.15
eee	-	-	0.05

Filename: MOD-000-0000-000

- 5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
- 3. THE BASIC SOLDER BALL GRID PITCH IS 0.50mm
- 2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-207.
- 1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 19. CYW20706 36-pin WLBGA Package (2.8 mm x 2.5 mm)



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.18	0.19	0.22
D	2.47	2.51	2.55
D1	2.0 REF.		
E	2.73	2.77	2.81
E1	2.0 REF.		
b	0.20	0.25	0.30
e	0.40 BSC		
f1	0.23 BSC		
f2	0.54 BSC		
f3	0.28 BSC		
aaa	-	-	0.10
bbb	-	-	0.10
ccc	-	-	0.05
ddd	-	-	0.10
eee	-	-	0.05

AGILE: MOD01978

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.  
NOTES: UNLESS OTHERWISE SPECIFIED
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.
3. THE BASIC SOLDER BUMP PITCH IS 0.40mm
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

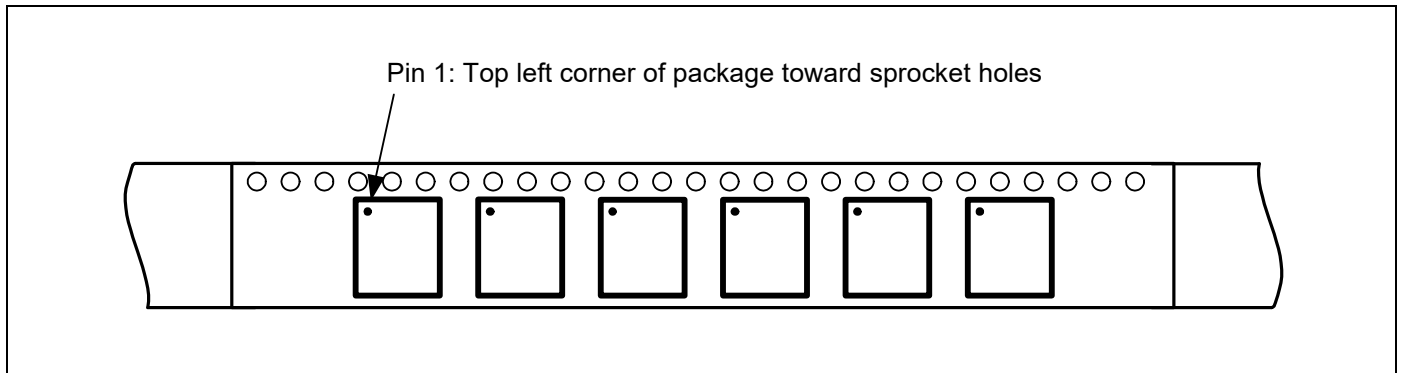
## 4.2 Tape Reel and Packaging Specifications

**Table 27. CYW20706 Tape Reel Specifications**

Parameter	Value
Quantity per reel	2500
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Tape pitch	12 mm

The top-left corner of the CYW20706 package is situated near the sprocket holes, as shown in [Figure 20](#).

**Figure 20. Pin 1 Orientation**



## 5. Ordering Information

**Table 28. Ordering Information**

Part Number	Package
CYW20706UA2KFFB4G	49-pin FBGA

## 6. Additional information

### 6.1 Acronyms and Abbreviations

The following list of acronyms and abbreviations may appear in this document.

Term	Description
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
AHB	advanced high-performance bus
APB	advanced peripheral bus
APU	audio processing unit
ARM7TDMI-S™	Acorn RISC Machine 7 Thumb instruction, Debugger, Multiplier, Ice, Synthesizable
BR	Basic Rate
BTC	Bluetooth controller
COEX	coexistence
DFU	device firmware update
DH	Data high rate
DM	Data medium rate
DMA	direct memory access
EBI	external bus interface
EDR	Enhanced Data Rate
GFSK	Gaussian Frequency Shift Keying
HCI	Host Control Interface
HV	high voltage
IDC	initial digital calibration
IF	intermediate frequency
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low dropout
LHL	lean high land
LPO	low power oscillator
LV	LogicVision™
MIA	multiple interface agent
PCM	pulse code modulation
PLL	phase locked loop
PMU	power management unit
POR	power-on reset
PWM	pulse width modulation

Term	Description
QD	quadrature decoder
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read-only memory
RX/TX	receive, transmit
SPI	serial peripheral interface
SW	software
UART	universal asynchronous receiver/transmitter
UPI	μ-processor interface
WD	watchdog

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: <http://www.cypress.com/glossary>.

## 6.2 IoT Resources

Cypress provides a wealth of data at <http://www.cypress.com/internet-things-iot> to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (<https://community.cypress.com/>).

## Document History Page

Document Title: CYW20706 Bluetooth SoC for Embedded Wireless Devices				
Document Number: 002-19479				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5852544	SGUP	08/31/2017	New Datasheet
*A	6084990	CHSI	03/01/2018	<p>Changed Broadcom Serial Communications (BSC) to I2C throughout the document.</p> <p>Updated <a href="#">Figure 1. Functional Block Diagram</a>.</p> <p>Added <a href="#">Table 2. Bluetooth Features</a>.</p> <p>Updated <a href="#">1.4. Collaborative Coexistence</a> and <a href="#">1.5. Global Coexistence Interface</a>.</p> <p><a href="#">Table 2</a>: Removed 6M Baud rate.</p> <p>Removed Common Baud rate Examples Table.</p> <p>Added a Note: "Subject to support in WICED Studio" in <a href="#">1.11. Triac Control</a> section.</p> <p>Added a Note: "Subjected to driver support in WICED" in <a href="#">1.13. Infrared Modulator</a> section.</p> <p>Updated <a href="#">Acronyms and Abbreviations</a> section.</p> <p>Updated <a href="#">Table 5. Crystal Strapping Options for the 49-Pin FBGA Package</a>.</p> <p>Removed "Preliminary" status from datasheet.</p>
*B	6105228	MILI	03/21/2018	Updated Minimum, Typical and Maximum values of <a href="#">Table 22</a> , <a href="#">Table 23</a> , <a href="#">Table 24</a> and <a href="#">Table 25</a> .

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