AIROC™ Bluetooth® & Bluetooth® LE system on chip

For wireless devices

General description

Infineon AIROC™ CYW20706 is a single-chip Bluetooth® 5.4-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 40 nm CMOS low-power process, the CYW20706 employs the highest level of integration to eliminate all critical external components, thereby minimizing the device's footprint and the costs associated with implementing Bluetooth® solutions.

The CYW20706 is the optimal solution for embedded and IoT applications. Built-in firmware adheres to the Bluetooth® Low Energy profile.

Infineon part numbering scheme

Infineon is converting the acquired IoT part numbers from Infineon to the Infineon part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Infineon part number marking. The table provides Infineon ordering part number that matches an existing IoT part number.

Table 1 Mapping table for part number between Broadcom and Infineon

Broadcom part number	Infineon part number
BCM20706	CYW20706
BCM20706UA2KFFB4G	CYW20706UA2KFFB4G

Features

- Complies with Bluetooth® Core Specification version 5.4 including BR/EDR/Bluetooth® LE
- Bluetooth® Device ID profile version 1.3 compliant
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- Excellent receiver sensitivity
- Programmable output power control
- Integrated Arm® Cortex®-M3 microprocessor core
- On-chip power-on reset (POR)
- Support for EEPROM and serial flash interfaces
- Integrated low dropout regulators (LDO)
- On-chip software controlled PMU
- PCM/I^2S Interface
- Infrared modulator
- On-chip support for SPI (master/slave modes)
- I2C interface (compatible with NXP I^2C slaves)
- Package types:
  - 49-ball FCBGA package (4.5 mm × 4.0 mm × 1.0 mm) Bluetooth® 5.4-compliant
  - RoHS compliant

Applications

- Home automation
- Point-of-sale input devices
- Blood pressure monitors
- “Find me” devices
- Heart rate monitors
- Proximity sensors
- Thermometers
- Wearables

Functional block diagram

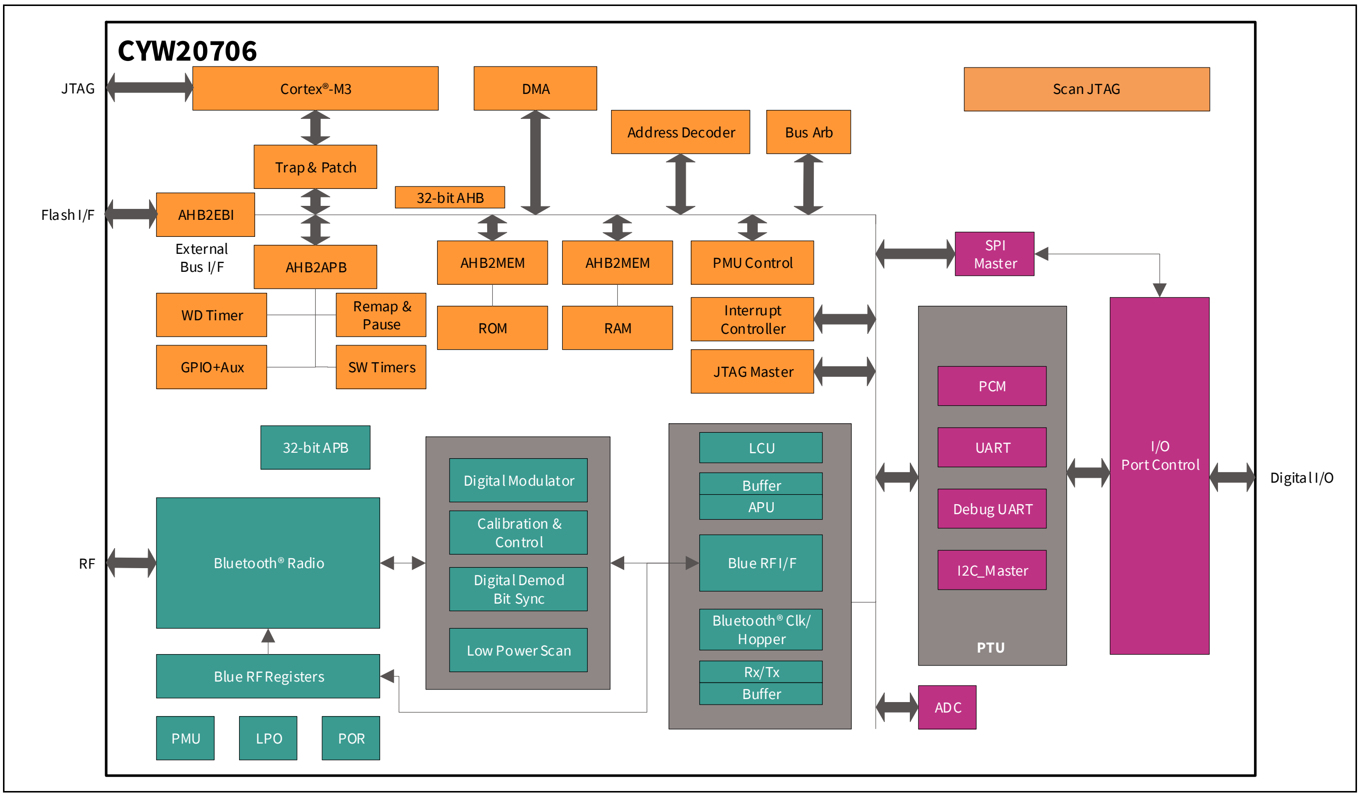

Figure 1 **Functional block diagram**

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1 Functional description

1.1 Bluetooth® Baseband Core (BBC)

The BBC implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth® slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Table 2 Bluetooth® features

Bluetooth® features		
Bluetooth® 1.0	**Bluetooth® 1.2**	**Bluetooth® 2.0**
Basic Rate	Interlaced scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive Frequency Hopping	–
Paging and inquiry	eSCO	–
Page and inquiry scan	–	–
Sniff	–	–
Bluetooth® 2.1	**Bluetooth® 3.0**	**Bluetooth® 4.0**
Secure Simple Pairing	Unicast connectionless data	Bluetooth® Low Energy
Enhanced inquiry response	Enhanced power control	–
Sniff subrating	eSCO	–
Bluetooth® 4.1	**Bluetooth® 4.2**	**Bluetooth® 5.0**
Low duty cycle advertising	Data packet length extension	Slot availability mask
Dual mode	LE Secure Connection	High duty cycle advertising
LE link layer topology	Link layer privacy	–
Bluetooth® 5.2		
Enhanced attribute protocol		
LE Power Control		
LE Isochronous Channels		

1.1.1 Link control layer

The link control layer is part of the Bluetooth® link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state in the Bluetooth® Link Controller.

- States:
  - Standby
  - Connection
  - Page
  - Page Scan
  - Inquiry
  - Inquiry scan
  - Sniff
  - Advertising
  - Scanning

1.1.2 Test mode support

The CYW20706 fully supports Bluetooth® Test Mode as described in Part I:1 of the Specification of the Bluetooth® System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth® Test Mode, the CYW20706 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct bit error rate (BER) measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

1.1.3 Frequency hopping generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth® clock, and device address.

1.2 Microprocessor unit

The CYW20706 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and SWD interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

1.2.1 NVRAM configuration data and storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYW20706 can use SPI Flash or I^2C EEPROM/serial flash for NVRAM storage.

1.2.2 One-time programmable memory

The CYW20706 includes 2 Kb of one-time programmable (OTP) memory allow manufacturing customization and to avoid the need for an on-board NVRAM. If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, to save power it is disabled when the boot process is complete. The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded to RAM after the CYW20706 boots and is ready for host transport communication.

The OTP contents are limited to:

- Parameters required prior to downloading the user configuration to RAM
- Parameters unique to each part and each customer (for example, the Bluetooth® device address)

1.2.3 External reset

An external active LOW reset signal, RESET_N, can be used to put the CYW20706 in the reset state. An external voltage detector reset IC with 50 ms delay is needed on the RESET_N. The RESET_N should be released only after the VDDO supply voltage level has been stabilized for 50 ms.

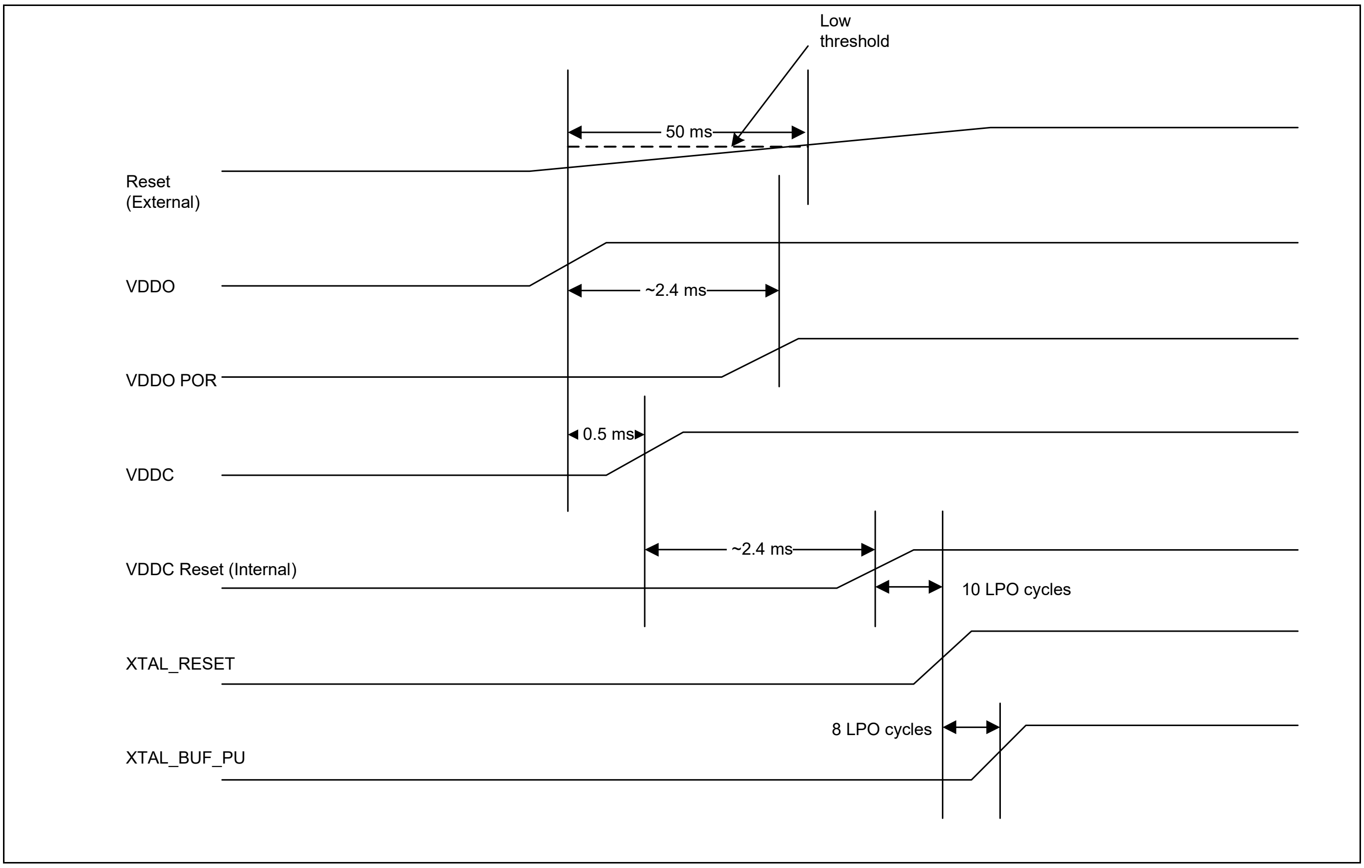


Figure 2 Reset timing [1]

Note

1. The reset signal should remain below this threshold 50 ms after VDDO is stable. Note that the representation of this signaling diagram is extended and not drawn to scale.

1.3 Integrated radio transceiver

The CYW20706 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth® wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20706 is fully compliant with the Bluetooth® Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

1.3.1 Transmitter

The CYW20706 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the Bluetooth® LE specification. The transmitter PA bias can also be adjusted to provide Bluetooth® Class 1 or Class 2 operation.

1.3.1.1 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

1.3.1.2 Power amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth® and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth® is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

1.3.2 Receiver

The receiver path uses a low-IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYW20706 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth® function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

1.3.2.1 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

1.3.2.2 Receiver signal strength indicator

The radio portion of the CYW20706 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

1.3.3 Local oscillator generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW20706 uses an internal RF and IF loop filter.

1.3.4 Calibration

The CYW20706 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within two percent of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

1.3.5 Internal LDO

The CYW20706 uses two LDOs – one for 1.2 V and the other for 2.5 V. The 1.2 V LDO provides power to the baseband and radio and the 2.5 V LDO powers the PA.

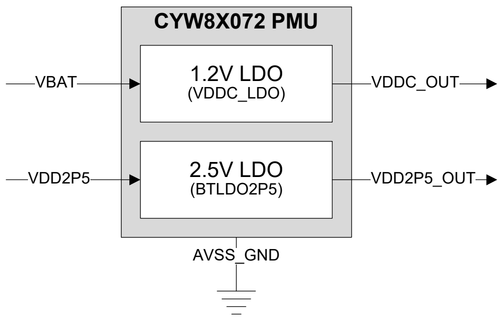


Figure 3 LDO functional block diagram

1.4 Collaborative coexistence

The CYW20706 provides extensions and collaborative coexistence with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth® to operate simultaneously within close proximity of each other. The device supports industry-standard coexistence signaling, including 802.15.2, and supports coexistence with CY WLAN and non-CY third-party WLAN solutions.

1.5 Global coexistence interface

The CYW20706 supports the proprietary coexistence interface Global Coexistence Interface (GCI) for coexistence between Bluetooth® and WLAN devices. GCI is a bi-directional bus between Infineon Bluetooth® and Infineon WLAN.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over two-wire interface. Between the two wires, one is GCI_SECI_IN and another is GCI_SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI_SECI_IN and GCI_SECI_OUT function
- It supports generic UART communication between WLAN and Bluetooth® devices
- To conserve power, it is disabled when inactive
- It supports automatic resynchronization upon waking from sleep mode
- It supports a baud rate of up to 4 Mbps

1.5.1 SECI I/O

The CYW20706 devices have dedicated GCI_SECI_IN and GCI_SECI_OUT pins. The two pin functions can be mapped to any of the Infineon Global Coexistence Interface (GCI) GPIO. Pin function mapping is controlled by the configuration file that is stored in on-chip RAM from the host.

1.6 Peripheral transport unit

1.6.1 I2C communications interface

The CYW20706 provides a two-pin master I2C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as trackball or touch-pad modules, and motion tracking ICs used in mouse devices. I2C does not support multi-master capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by I2C:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I^2C-compatible speed)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed)

The following transfer types are supported by I2C:

- Read (Up to 127 bytes can be read)
- Write (Up to 127 bytes can be written)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written.)
- Write-then-Read (Up to 127 bytes can be written and up to 127 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20706 are required on both the SCL and SDA pins for proper operation.

1.6.2 HCI UART interface

The UART physical interface is a standard, four-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 4 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYW20706 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 4 Mbps. The baud rate of the CYW20706 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Note: HCI-UART and SPI cannot be used simultaneously since they share a hardware FIFO.

Table 3 contains example values to generate common baud rates.

Table 3 Common baud rate examples

Baud rate (bps)	Baud rate adjustment		Mode	Error (%)
	High nibble	Low nibble		
4M	0xFF	0xF4	High rate	0.00
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW20706 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

1.6.2.1 Peripheral UART interface

The CYW20706 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin as shown in **Table 4**.

Table 4 CYW20706 peripheral UART

Pin name	pUART_TX	pUART_RX	pUART_CTS_N	pUART_RTS_N
Configured pin name	P0	P2	P3	P6
	P31	P33	P3	P30

1.7 PCM interface

The CYW20706 includes a PCM interface that shares pins with the I^2S interface. The PCM Interface on the CYW20706 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW20706 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW20706.

1.7.1 Slot mapping

The CYW20706 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

1.7.2 Frame synchronization

The CYW20706 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three-bit periods and the pulse starts coincident with the first bit of the first slot.

1.7.3 Data formatting

The CYW20706 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW20706 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked MSB first.

1.8 Clock frequencies

The CYW20706 49-ball FCBGA package supports 20, 24, and 40 MHz crystals (XTAL) by selecting the correct crystal strapping options. Other frequencies also supported by firmware configuration. **Table 5** lists the strapping options.

Table 5 Crystal strapping options for the 49-ball FCBGA package

Strapping option pin		XTAL frequency
BT_XTAL_STRAP_1	BT_XTAL_STRAP_0	
Pull Low	Pull Low	40 MHz
Pull Low	Pull High	24 MHz
Pull High	Pull Low	20 MHz
Pull High	Pull High	Read from serial flash or EEPROM (Supported XTAL frequency is 26 MHz)

1.8.1 Crystal oscillator

The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth® specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see **Figure 4**).

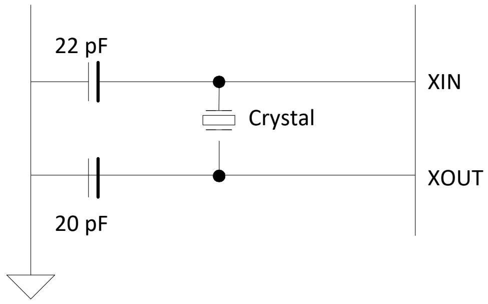


Figure 4 Recommended oscillator configuration—12 pF load crystal

Table 6 shows the recommended crystal specifications.

Table 6 Reference crystal electrical specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	20	24	40	MHz
Oscillation mode	–	Fundamental			–
Frequency tolerance	at 25°C	–	±10	–	ppm
Tolerance stability over temp	at 0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	60	W
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	µW
Aging	–	–	–	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

1.8.1.1 HID peripheral block

The peripheral blocks of the CYW20706 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

1.9 GPIO ports

1.9.1 49-ball FCBGA package

The CYW20706 49-ball FCBGA package has 24 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3 V or 4 mA at 1.8 V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3 V or 8 mA at 1.8 V. The following GPIOs are available:

- BT_GPIO_0/P36/P38 (triple bonded; only one of three is available)
- BT_GPIO_1/P25/P32 (triple bonded; only one of three is available)
- BT_GPIO_3/P27/P33 (triple bonded; only one of three is available)
- BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- BT_GPIO_5/P15 (dual bonded; only one of two is available)
- BT_GPIO_6/P11/P26 (triple bonded; only one of three is available)
- BT_GPIO_7/P30 (Dual bonded; only one of two is available)
- BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)
- I^2S_PCM_IN/P12 (dual bonded; only one of two is available)
- I^2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)
- I^2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)
- I^2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of three is available)

All of these pins can be programmed as ADC inputs.

Port 26–Port 29

P[26:29] consist of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have PWM functionality, which can be used for LED dimming.

1.10 PWM

The CYW20706 has four internal PWMs. The PWM module consists of the following:

- PWM1–4
- Each of the four PWM channels, PWM1–4, contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1–4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 5 shows the structure of one PWM.

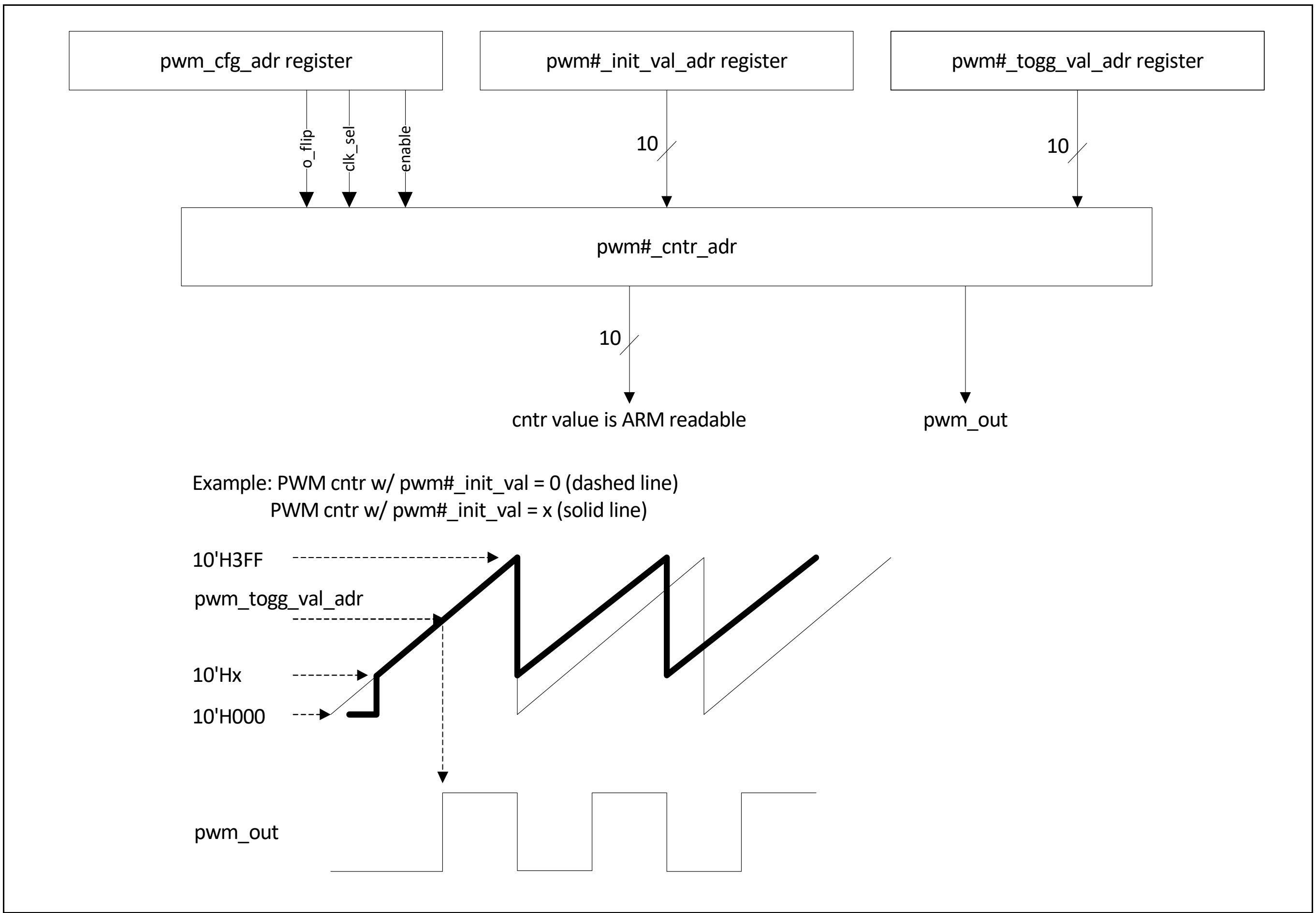


Figure 5 PWM block diagram

1.11 Serial peripheral interface

The CYW20706 has two independent SPI interfaces. One is a master-only interface (SPI_2) and the other (SPI_1) can be either a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20706 has optional I/O ports that can be configured individually and separately for each functional pin. The CYW20706 acts as an SPI master device that supports 1.8 V or 3.3 V SPI slaves. The CYW20706 can also act as an SPI slave device that supports a 1.8 V or 3.3 V SPI master.

Note: SPI voltage depends on VDDO; therefore, it defines the type of devices that can be supported.

1.12 Power management unit

The power management unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

1.12.1 RF power management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

1.12.2 Host controller power management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDOFF (Deep Sleep) mode.

1.12.3 BBC power management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth®-specified low-power connection mode. While in these low-power connection modes, the CYW20706 runs on the low-power oscillator and wakes up after a predefined time period.

The CYW20706 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode

The CYW20706 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the CYW20706 immediately enters active mode.

In HIDOFF mode, the CYW20706 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

2 Pin assignments

2.1 Pin descriptions

2.1.1 49-ball FCBGA list

Table 7 CYW20706 49-ball FCBGA list

Pin	Signal	I/O	Power domain	Description
Radio				
A2	RFOP	I/O	VDD_RF	RF I/O antenna port
A4	XO_IN	I	VDD_RF	Crystal or reference input
A5	XO_OUT	O	VDD_RF	Crystal oscillator output
Voltage regulators				
D1	VBAT	I	N/A	VBAT input pin; this must be less than or equal to VDDO
E1	VDD2P5_IN	I	N/A	2.5 V LDO input
E2	VDD2P5_OUT	O	N/A	2.5 V LDO output
F1	VDDC_OUT	O	N/A	1.2 V LDO output
Straps				
G3	BT_XTAL_STRAP_0	I	VDDO	A strap for choosing the XTAL frequencies
F2	BT_XTAL_STRAP_1	I	VDDO	A strap for choosing the XTAL frequencies
A6	RST_N	I	VDDO	Active LOW reset input
G7	BT_TM1	I	VDDO	Reserved: Connect to ground
Digital I/O				
F8	BT_GPIO_0	I	VDDO	BT_GPIO_0/BT_DEV_WAKE A signal from the host to the CYW20706 that the host requires attention.
	P36	I/O	VDDO	GPIO: P36 A/D converter input 3 Quadrature: QDZ0 SPI_1: SPI_CLK (master and slave) Auxiliary clock output: ACLK0 External T/R switch control: ~tx_pd
	P38	I/O	VDDO	GPIO: P38 A/D converter input 1 SPI_1: MOSI (master and slave) IR_TX
F7	BT_GPIO_1	O	VDDO	BT_GPIO_1/BT_HOST_WAKE A signal from the CYW20706 device to the host indicating that the Bluetooth® device requires attention.
	P25	I/O	VDDO	GPIO: P25 SPI_1: MISO (master and slave) Peripheral UART: puart_rx
	P32	I/O	VDDO	GPIO: P32 A/D converter input 7 Quadrature: QDX0 SPI_1: SPI_CS (slave only) Auxiliary clock output: ACLK0 Peripheral UART: puart_tx

Table 7 CYW20706 49-ball FCBGA list (Cont.)

Pin	Signal	I/O	Power domain	Description
E4	BT_GPIO_2	I	VDDO	When high, this signal extends the XTAL warm-up time for external CLK requests. Otherwise, it is typically connected to ground.
C5	BT_GPIO_3	I/O	VDDO	General-purpose I/O
	P27 PWM1	I/O	VDDO	GPIO: P27 SPI_1: MOSI (master and slave) Optical control output: QOC1 Triac control 2 Current: 16 mA sink
	P33	I/O	VDDO	GPIO: P33 A/D converter input 6 Quadrature: QDX1 SPI_1: MOSI (slave only) Auxiliary clock output: ACLK1 Peripheral UART: puart_rx
D6	BT_GPIO_4	I/O	VDDO	General-purpose I/O; can also be configured as a GCI pin
	P6	I/O	VDDO	GPIO: P6 Quadrature: QDZ0 Peripheral UART: puart_rts SPI_1: SPI_CS (slave only) 60Hz_main
	LPO_IN	I	N/A	External LPO input
	P31	I/O	VDDO	GPIO: P31 A/D converter input 8 Peripheral UART: puart_tx
B5	BT_GPIO_5	I/O	VDDO	General-purpose I/O; can also be configured as a GCI pin Debug UART
	P15	I/O	VDDO	GPIO: P15 A/D converter input 20 IR_RX 60Hz_main
B6	BT_GPIO_6	I/O	VDDO	General-purpose I/O; can also be configured as a GCI pin
	P11	I/O	VDDO	GPIO: P11 Keyboard scan output (column): KSO3 A/D converter input 24
	P26 PWM0	I/O	VDDO	GPIO: P26 SPI_1: SPI_CS (slave only) Optical control output: QOC0 Triac control 1 Current: 16 mA sink
C6	BT_GPIO_7	I/O	VDDO	General-purpose I/O: can also be configured as a GCI pin.
	P30	I/O	VDDO	GPIO: P30 A/D converter input 9 Peripheral UART: puart_rts
F5	BT_UART_RXD	I	VDDO	UART receive data
F4	BT_UART_TXD	O	VDDO	UART transmit data
F3	BT_UART_RTS_N	O	VDDO	UART request to send output

Table 7 CYW20706 49-ball FCBGA list (Cont.)

Pin	Signal	I/O	Power domain	Description
G4	BT_UART_CTS_N	I	VDDO	UART clear to send input
G8	BT_CLK_REQ	O	VDDO	Used for shared-clock application
	P4	I/O	VDDO	GPIO: P4 Quadrature: QDY0 Peripheral UART: puart_rx SPI_1: MOSI (master and slave) IR_TX
	P24	I/O	VDDO	GPIO: P24 SPI_1: SPI_CLK (master and slave) Peripheral UART: puart_tx
D8	SPI2_MISO_I^{2}C_SCL	I/O	VDDO	I2C CLOCK
E8	SPI2_MOSI_I^{2}C_SDA	I/O	VDDO	I2C DATA
E7	SPI2_CLK	O	VDDO	Serial flash SPI clock
D7	SPI2_CSN	O	VDDO	Serial flash active-low chip select
C7	I^{2}S_DI/PCM_IN	I/O	VDDO	PCM/I2S data input I^{2}C_SDA
	P12	I/O	VDDO	GPIO: P12 A/D converter input 23
A8	I^{2}S_DO/PCM_OUT	I/O	VDDO	PCM/I2S data output I2C_SCL
	P3	I/O	VDDO	GPIO: P3 Quadrature: QDX1 Peripheral UART: puart_cts SPI_1: SPI_CLK (master and slave)
	P29 PWM3	I/O	VDDO	GPIO: P29 Optical control output: QOC3 A/D converter input 10, LED2 Current: 16 mA sink
	P35	I/O	VDDO	GPIO: P35 A/D converter input 4 Quadrature: QDY1 Peripheral UART: puart_cts I2C: SDA
B7	I^{2}S_CLK/PCM_CLK	I/O	VDDO	PCM/I2S clock Fp1
	P2	I/O	VDDO	GPIO: P2 Quadrature: QDX0 Peripheral UART: puart_rx SPI_1: SPI_CS (slave only) SPI_1: MOSI (master only)
	P28 PWM2	I/O	VDDO	GPIO: P28 Optical control output: QOC2 A/D converter input 11, LED1 Current: 16 mA sink
	P37	I/O	VDDO	GPIO: P37 A/D converter input 2 Quadrature: QDZ1 SPI_1: MISO (slave only) Auxiliary clock output: ACLK1 I2C: SCL

Table 7 CYW20706 49-ball FCBGA list (Cont.)

Pin	Signal	I/O	Power domain	Description
C8	I^2S_WS/PCM_SYNC	I/O	VDDO	PCM sync/I2S word select
	P0	I/O	VDDO	GPIO: P0 A/D converter input 29 Peripheral UART: puart_tx SPI_1: MOSI (master and slave) IR_RX, 60Hz_main **Note:** Not available during TM1 = 1.
	P34	I/O	VDDO	GPIO: P34 A/D converter input 5 Quadrature: QDY0 Peripheral UART: puart_rx External T/R switch control: tx_pd
G2	BT_OTP_3P3V_ON	I	VDDO	If OTP is used, pull this pin to HIGH. If OTP is not used, pull this pin to LOW.
JTAG				
D5	JTAG_SEL	I/O	VDDO	Arm® JTAG debug mode control. Connect to GND for all applications.
Supplies				
G1	BT_OTP_VDD3P3V	I	N/A	3.3 V OTP supply voltage
B4	BT_IFVDD1P2	I	N/A	Radio IF PLL supply
A1	BT_PAVDD2P5	I	N/A	Radio PA supply
B1	BT_LNAVDD1P2	I	N/A	Radio LNA supply
C1	BT_VCOVDD1P2	I	N/A	Radio VCO supply
A3	BT_PLLVDD1P2	I	N/A	Radio RF PLL supply
B8, G6	VDDC	I	N/A	Core logic supply
G5	VDDO	I	N/A	Digital I/O supply voltage
A7, B2, B3, C2, D2, F6	VSS	–	N/A	Ground

2.2 Ball map

2.2.1 49-ball FCBGA ball map

Table 8 CYW20706 49-ball FCBGA ball map

	1	2	3	4	5	6	7	8	
A	BT_PAVDD2P5	RFOP	BT_ PLLVDD1P2	XO_IN	XO_OUT	RST_N	VSS	I^{2}S_DO/ PCM_OUT/P3/ P29/P35	**A**
B	BT_ LNAVDD1P2	VSS	VSS	BT_IFVDD1P2	BT_GPIO_5/ P15	BT_GPIO_6/ P11/P26	I^{2}S_CLK/ PCM_CLK/ P2/P28/P37	VDDC	**B**
C	BT_ VCOVDD1P2	VSS	NC	NC	BT_GPIO_3/ P27/P33	BT_GPIO_7/ P30	I2S_DI/ PCM_IN/P12	I^{2}S_WS/ PCM_SYNC/ P0/P34	**C**
D	VBAT	VSS	NC	NC	JTAG_SEL	BT_GPIO_4/ P6/LPO_IN/ P31	SPI2_CSN	SPI2_MISO_ I^{2}C_SCL	**D**
E	VDD2P5_IN	VDD2P5_OUT	NC	BT_GPIO_2	NC	NC	SPI2_CLK	SPI2_MOSI_ I^{2}C_SDA	**E**
F	VDDC_OUT	BT_XTAL_ STRAP_1	BT_UART_ RTS_N	BT_UART_TXD	BT_UART_RXD	VSS	BT_GPIO_1/ P25/P32	BT_GPIO_0/ P36/P38	**F**
G	BT_OTP_ VDD3P3V	BT_OTP_ 3P3V_ON	BT_XTAL_ STRAP_0	BT_UART_ CTS_N	VDDO	VDDC	BT_TM1	BT_CLK_REQ/ P4/P24	**G**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	

3 Specifications

3.1 Electrical characteristics

Table 9 shows the maximum electrical rating for voltages referenced to VDD pin.

Table 9 Absolute maximum ratings

Parameter	Specification			Units
	Minimum	Nominal	Maximum	
Ambient temperature of operation	−30	25	85	°C
Storage temperature	−40	–	150	°C
ESD tolerance HBM	−2000	–	2000	V
ESD tolerance MM	−100	–	100	V
ESD tolerance CDM	−500	–	500	V
Latch-up	−200	–	200	mA
VDDC	−0.5	–	1.38	V
VDDO	−0.5	–	3.795	V
VDD_RF (excluding PA)	−0.5	–	1.38	V
VDDPA	−0.5	–	3.565	V
VBAT	−0.5	–	3.795	V
BT_OTP_VDD3P3V	−0.5	–	3.795	V
VDD2P5_IN	−0.5	–	3.795	V

Table 10 shows the power supply characteristics for the range T_J = 0°C to 125°C.

Table 10 Power supply specifications

Parameter	Conditions	Min	Typ	Max	Units
VDD Core	–	1.14	1.2	1.26	V
VDDO[2]	–	1.62	3.3	3.6	V
VDDRF	Excluding class 1 PA	1.14	1.2	1.26	V
VDDPA	Class 1 operation	2.25	2.5 to 2.8	2.94	V
VBAT[2]	–	1.62	3.3	3.6	V
BT_OTP_VDD3P3V	–	3.0	3.3	3.6	V
VDD2P5_IN	–	3.0	3.3	3.6	V

Note

2. VDDO must be ≥ VBAT.

Table 11 VDDC LDO electrical specifications

Parameter	Conditions		Min	Typ	Max	Unit
Input voltage	–		1.62	3.3	3.6	V
Nominal output voltage	–		–	1.2	–	V
DC Accuracy	Accuracy at any step, including bandgap reference.		–5	–	5	%
Output voltage programmability	Range		0.89	–	1.34	V
	Step size		–	30	–	mV
Load current	–		–	–	40	mA
Dropout voltage	I_{load} = 40 mA		–	–	200	mV
Line regulation	Vin from 1.62 V to 3.6 V, I_{load} = 40 mA		–	–	0.2	%Vo/V
Load regulation	I_{load} = 1 mA to 40 mA, Vout = 1.2 V, Package + PCB R = 0.3 Ω		–	0.02	0.05	%Vo/mA
Quiescent current	No load at Vin = 3.3 V		–	18	23	µA
Power down current	Vin = 3.3 V at 25°C		–	0.2	–	µA
Output noise	I_{load} = 15 mA, 100 kHz		–		40	nV/sqrtHz
	I_{load} = 15 mA, 2 MHz		–		14	nV/sqrtHz
PSRR	Vin = 3.3 V, Vout = 1.2 V, I_{load} = 40 mA	1 kHz	65	–	–	dB
		10 kHz	60	–	–	dB
		100 kHz	55	–	–	dB
Overcurrent limit	–		100	–	–	mA
Turn-on time	VBAT = 3.3 V, BG already on, LDO OFF to ON, Co = 1 µF, 90% of Vout		–	–	100	µs
In-rush current during turn-on	During start-up, Co = 1 µF		–	–	60	mA
Transient performance	I_{load} = 1 mA to 15 mA and 15 mA to 1 mA in 1 µs		–	–	40	mV
	I_{load} = 15 mA to 40 mA and 40 mA to 15 mA in 1 µs		–	–	25	–
External output capacitor	Ceramic cap with ESR ≤ 0.5 Ω		0.8	1	4.7	µF
External input capacitor	Ceramic, X5R, 0402, ±20%, 10 V		–	1	–	µF

Table 12 BTLDO_2P5 electrical specifications

Parameters	Conditions	Min	Typ	Max	Units
Input supply voltage, Vin	Min = Vo + 0.2 V = 2.7 V (for Vo = 2.5 V) Dropout voltage requirement must be met under maximum load for performance specs.	3.0	3.3	3.6	V
Nominal output voltage, Vo	Default = 2.5 V	–	2.5	–	V
Output voltage programmability	Range Accuracy at any step (including line/load regulation), load > 0.1 mA	2.2 –5	–	2.8 5	V %
Dropout voltage	At max load	–	–	200	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load; Vin = Vo + 0.2 V, Vin = Vo + 0.2 V	–	8 660	16 700	µA
Leakage current	Power-down mode. At junction temperature 85°C.	–	1.5	5	µA
Line regulation	Vin from (Vo + 0.2 V) to 3.6 V, max load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, Vin = 3.6 V	–	–	0.3	mV/mA
PSRR	Vin ≥ Vo + 0.2 V, Vo = 2.5 V, Co = 2.2 µF, max load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	150	µs
External output capacitor, Co	Ceramic, X5R, 0402, (ESR: 5m–240 mΩ), ±20%, 6.3 V	0.7	2.2	2.64	µF
External input capacitor	Ceramic, X5R, 0402, ±20%, 10 V	–	1	–	µF

3.1.1 Digital I/O characteristics

Table 13 Digital I/O characteristics

Characteristics	Value	Symbol	Minimum	Typical	Maximum	Unit
Input voltage						
Low	VDDO = 1.8 V	V_{IL}	–	–	0.6	V
	VDDO = 3.3 V	V_{IL}	–	–	0.8	V
High	VDDO = 1.8 V	V_{IH}	1.1	–	–	V
	VDDO = 3.3 V	V_{IH}	2.0	–	–	V
Output voltage						
Low	–	V_{OL}	–	–	0.4	V
High	VDDO – 0.4 V	V_{OH}	–	–	–	V
Input current						
Low	–	I_{IL}	–	–	1.0	µA
High	–	I_{IH}	–	–	1.0	µA
Output current						
Low	VDDO = 3.3 V, V_{OL} = 0.4 V	I_{OL}	–	–	8.0	mA
	VDDO = 1.8 V, V_{OL} = 0.4 V	I_{OL}	–	–	4.0	mA
High	VDDO = 3.3 V, V_{OH} = 2.9 V	I_{OH}	–	–	8.0	mA
	VDDO = 1.8 V, V_{OH} = 1.4 V	I_{OH}	–	–	4.0	mA
Input capacitance	–	C_{IN}	–	–	0.4	pF

3.1.2 Current consumption

Table 14 Bluetooth®, Bluetooth® LE, BR, and EDR current consumption, Class 1 [3]

Mode	Remarks	Typ	Unit
3DH5/3DH5	–	37.10	mA
Bluetooth® LE			
Bluetooth® LE	Connected 600 ms interval	211	µA
Bluetooth® LE ADV	1.00 s ADV interval	176	µA
Bluetooth® LE Scan	No devices present; A 1.28-s interval with 11.25 ms scan window.	355	µA
DMx/DHx			
DM1/DH1	–	32.15	mA
DM3/DH3	–	38.14	mA
DM5/DH5	–	38.46	mA
HIDOFF	Deep Sleep	2.69	µA
Page scan	Periodic scan rate is 1.28 s	0.486	mA
Receive			
1 Mbps	Peak current level during reception of a basic-rate packet	26.373	mA
EDR	Peak current level during the reception of a 2 or 3 Mbps rate packet	26.373	mA
Sniff slave			
11.25 ms	–	4.95	mA
22.5 ms	–	2.6	mA
495.00 ms	Based on one attempt and no timeout	254	µA
Transmit			
1 Mbps	Peak current level during the transmission of a basic-rate packet GFSK output power = 10 dBm	60.289	mA
EDR	Peak current level during the transmission of a 2 or 3 Mbps rate packet EDR output power = 8 dBm	52.485	mA

Table 15 Bluetooth® and Bluetooth® LE current consumption, Class 2 (0 dBm) [4]

Mode	Remarks	Typ	Unit
3DH5/3DH5	–	31.57	mA
Bluetooth® LE			
Bluetooth® LE ADV	1.00 s ADV interval	174	µA
Bluetooth® LE Scan	No devices present. A 1.28-s interval with 11.25 ms scan window	368	µA
DMx/DHx			
DM1/DH1	–	27.5	mA
DM3/DH3	–	31.34	mA
DM5/DH5	–	32.36	mA

Notes

3. In **Table 14**, current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDO and VDD2P5_IN.
4. In **Table 15**, current consumption measurements are taken at input of VDD2P5_IN, VDDO, and VBAT combined (VDD2P5_IN = VDDO = VBAT = 3.0 V).

3.2 RF specifications

Table 16 Receiver RF specifications [5, 6]

Parameter	Conditions	Minimum	Typical [7]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[8]	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	LE GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference performance					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–40	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB

Notes

5. All specifications in **Table 16** are for industrial temperatures.
6. All specifications in **Table 16** are single-ended. Unused inputs are left open.
7. Typical operating conditions are 1.22 V operating voltage and 25°C ambient temperature.
8. The receiver sensitivity is measured at BER of 0.1% on the device interface.

Table 16 Receiver RF specifications [5, 6] (Cont.)

Parameter	Conditions	Minimum	Typical [7}	Maximum	Unit
C/I image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB
Out-of-band blocking performance (CW)[9}					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000 MHz–2399 MHz	0.1% BER	–	–27	–	dBm
2498 MHz–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-band blocking performance, modulated interferer					
776 MHz–764 MHz	CDMA	–	–10[10}	–	dBm
824 MHz–849 MHz	CDMA	–	–10[10}	–	dBm
1850 MHz–1910 MHz	CDMA	–	–23[10}	–	dBm
824 MHz–849 MHz	EDGE/GSM	–	–10[10}	–	dBm
880 MHz–915 MHz	EDGE/GSM	–	–10[10}	–	dBm
1710 MHz–1785 MHz	EDGE/GSM	–	–23[10}	–	dBm
1850 MHz–1910 MHz	EDGE/GSM	–	–23[10}	–	dBm
1850 MHz–1910 MHz	WCDMA	–	–23[10}	–	dBm
1920 MHz–1980 MHz	WCDMA	–	–23[10}	–	dBm
Intermodulation performance[11}					
Bluetooth®, Df = 5 MHz	–	–39.0	–	–	dBm
Spurious emissions[12}					
30 MHz–1 GHz	–	–	–	–62	dBm
1 GHz–12.75 GHz	–	–	–	–47	dBm
65 MHz–108 MHz	FM Rx	–	–147	–	dBm/Hz
746 MHz–764 MHz	CDMA	–	–147	–	dBm/Hz
851 MHz–894 MHz	CDMA	–	–147	–	dBm/Hz
925 MHz–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805 MHz–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930 MHz–1990 MHz	PCS	–	–147	–	dBm/Hz
2110 MHz–2170 MHz	WCDMA	–	–147	–	dBm/Hz
GLONASS band spurious emissions[13}					
Spurious Emissions	–	–	–118	–	dBm/Hz
Out-of-band noise floor					
1570 MHz–1580 MHz	GPS	–	–147	–	dBm/Hz
1592 MHz–1610 MHz	GLONASS	–	–147	–	dBm/Hz

Notes
9. Meets this specification using a front-end bandpass filter.
10. Numbers are referred to the pin output with an external BPF filter.
11. f0 = –64 dBm Bluetooth®-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth®-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n × 1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
12. Includes baseband radiated emissions.
13. Max TX power (12 dBm at chip out), modulation is PRBS9, modulation type is GFSK.

Table 17 Transmitter RF specifications [14, 15]

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK Tx power[16}	–	–	12	–	dBm
Class1: EDR Tx power[17}	–	–	9	–	dBm
Class 2: GFSK Tx power	–	–	2	–	dBm
Power control step	–	2	4	8	dB
Modulation accuracy					
π/4-DQPSK Frequency Stability	–	–10	–	10	kHz
π/4-DQPSK RMS DEVM	–	–	–	20	%
π/4-QPSK Peak DEVM	–	–	–	35	%
π/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-band spurious emissions					
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-band spurious emissions					
30 MHz to 1 GHz	–	–	–	–36.0[18}	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[18, 19}	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

Notes
14.All specifications in **Table 17** are for industrial temperatures.
15.All specifications in **Table 17** are single-ended. Unused inputs are left open.
16.12 dBm output for GFSK measured with PAVDD = 2.5 V.
17.9 dBm output for EDR measured with PAVDD = 2.5 V.
18.Maximum value is the value required for Bluetooth® qualification.
19.Meets this spec using a front-end band pass filter.

Table 18 Bluetooth® LE RF specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	N/A	2402	–	2480	MHz
Rx sense[20]	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
Tx power[21]	N/A	–	9	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[22]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

Notes

20. Dirty Tx is Off.
21. The Bluetooth® LE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc. The output is capped at 12 dBm out. The Bluetooth® LE Tx power at the antenna port cannot exceed the 10 dBm EIRP specification limit.
22. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

3.3 Timing and AC characteristics

In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

3.3.1 UART timing

Table 19 UART timing specifications

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

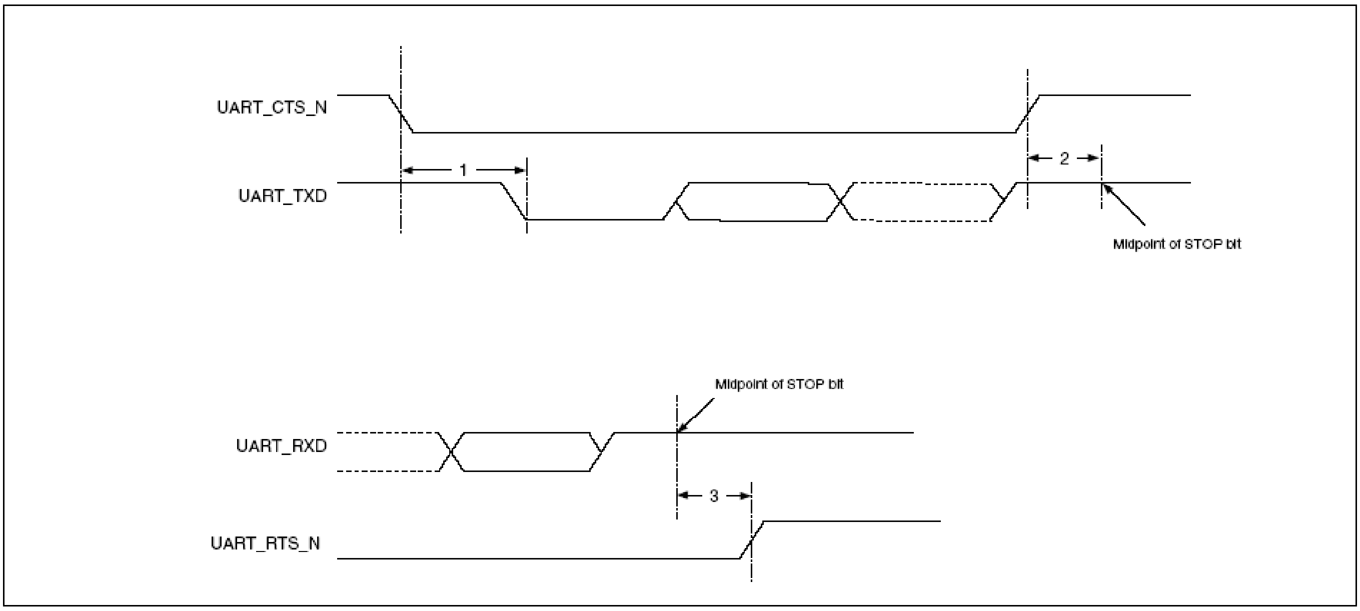


Figure 6 UART timing

3.3.2 SPI timing

The SPI interface can be clocked up to 12 MHz.

Table 20 and **Figure 7** show the timing requirements when operating in SPI Mode 0 and 2.

Table 20 SPI Mode 0 and 2

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	ns
3	Time from master assert SPI_CSN to first clock edge	20	∞	ns
4	Setup time for MOSI data lines	8	$^1/_2$ SCK	ns
5	Hold time for MOSI data lines	8	$^1/_2$ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	ns
8	Idle time between subsequent SPI transactions	1 SCK	∞	ns

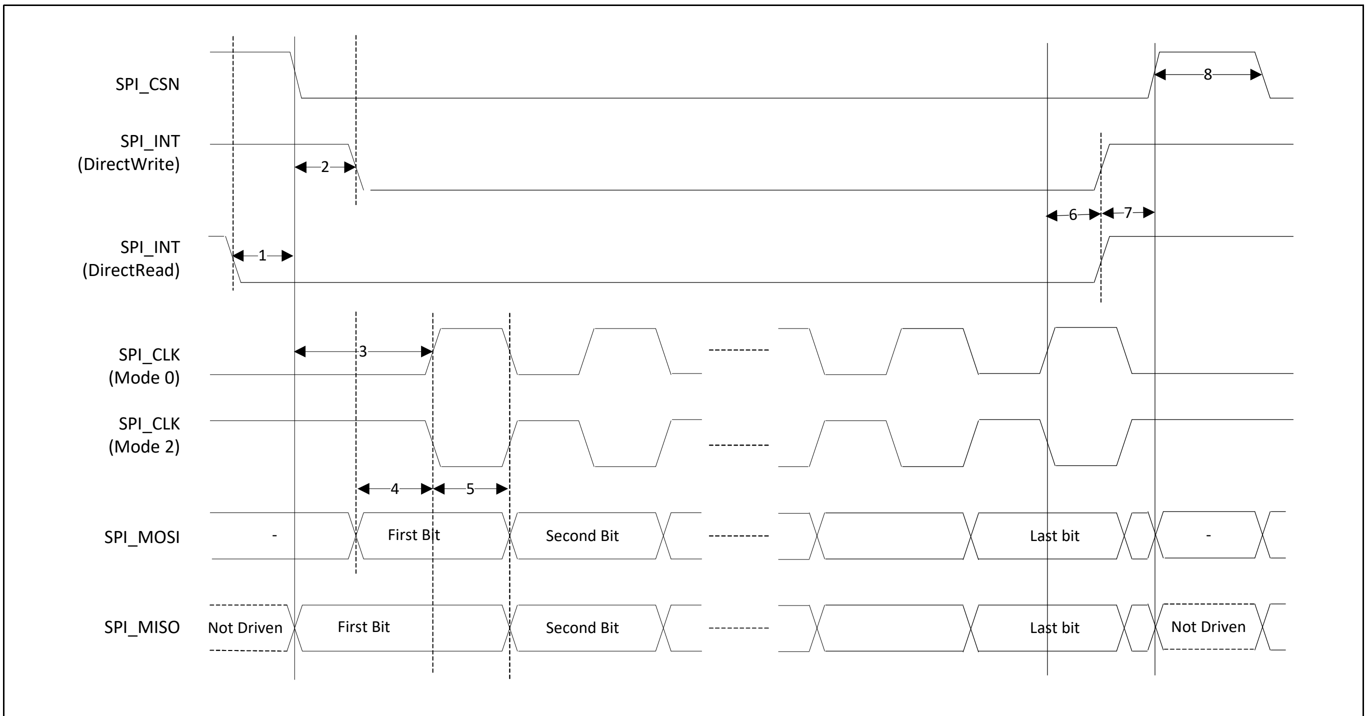


Figure 7 SPI timing, Mode 0 and 2

Table 21 and **Figure 8** show the timing requirements when operating in SPI Mode 0 and 2.

Table 21 SPI Mode 1 and 3

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	ns
3	Time from master assert SPI_CSN to first clock edge	20	∞	ns
4	Setup time for MOSI data lines	8	$^1/_2$ SCK	ns
5	Hold time for MOSI data lines	8	$^1/_2$ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	ns
8	Idle time between subsequent SPI transactions	1 SCK	∞	ns

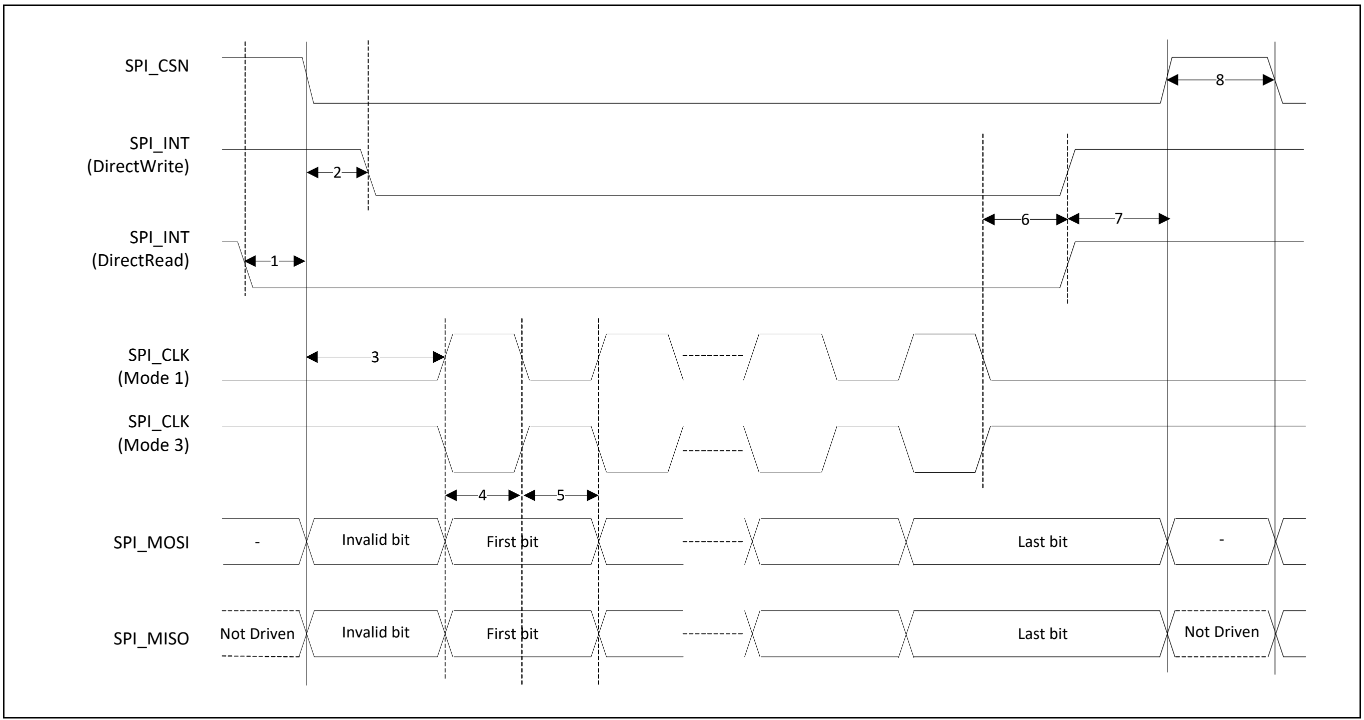


Figure 8 SPI timing, Mode 1 and 3

3.3.3 I2C interface timing

The specifications in Table 22 references Figure 9.

Table 22 I2C interface timing specifications (up to 1 MHz)

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	–	100 400 800 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[23}	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[24}	650	–	ns

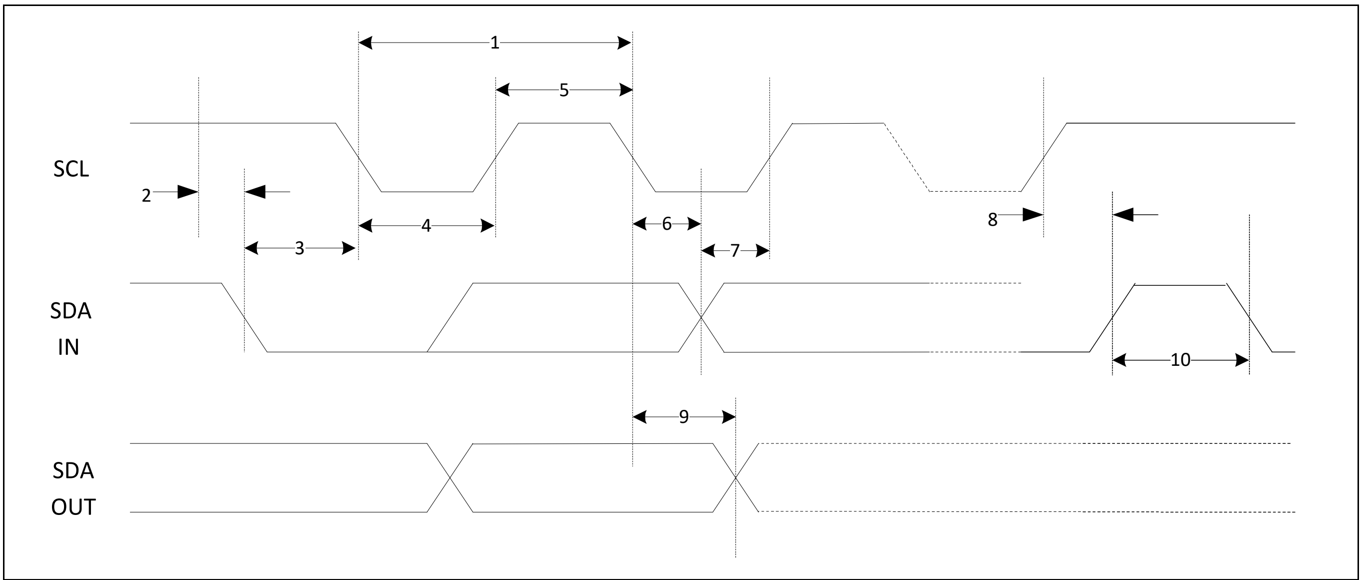


Figure 9 I2C interface timing diagram

Notes

23. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
24. Time that the CBUS must be free before a new transaction can start.

3.3.4 PCM interface timing

3.3.4.1 Short frame sync, master mode

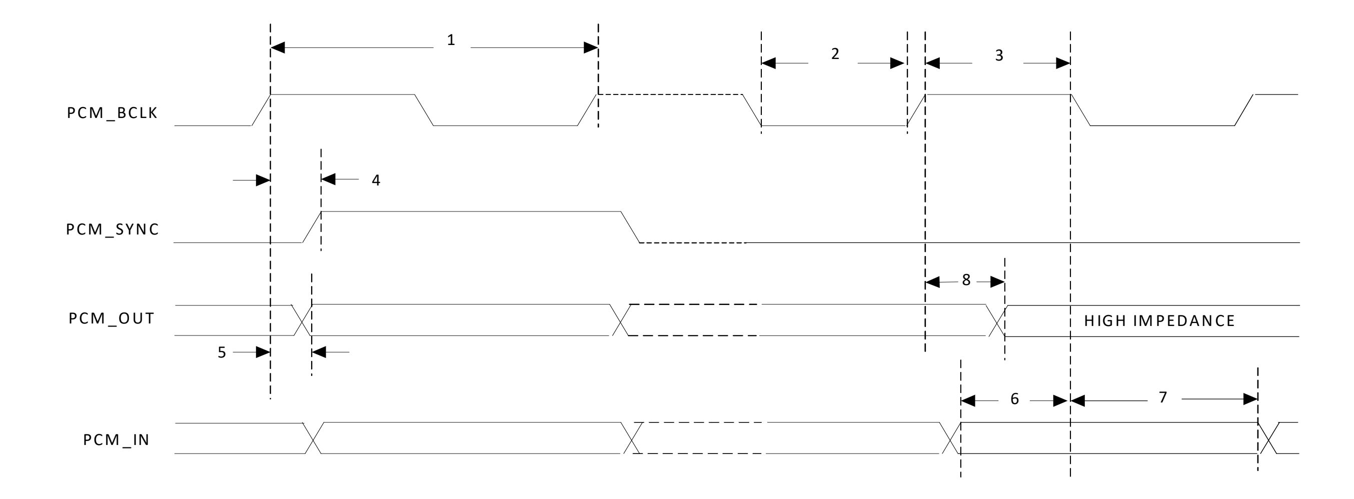


Figure 10 PCM timing diagram (Short frame sync, master mode)

Table 23 PCM interface timing specifications (Short frame sync, master mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC delay	0	–	25.0	ns
5	PCM_OUT delay	0	–	25.0	ns
6	PCM_IN setup	8.0	–	–	ns
7	PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

3.3.4.2 Short frame sync, slave mode

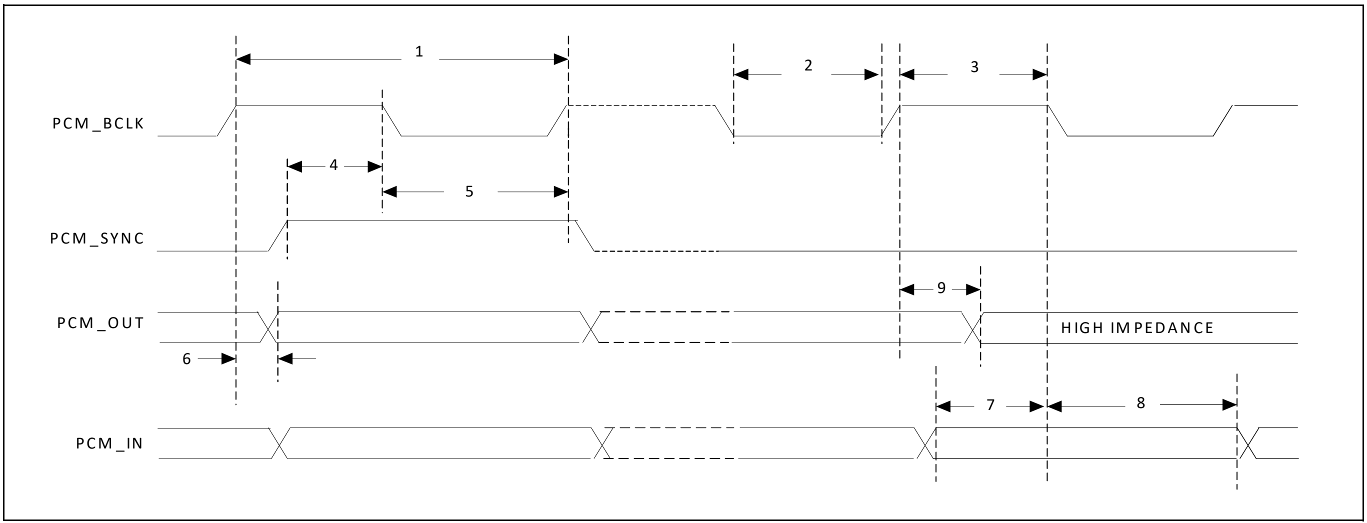


Figure 11 PCM timing diagram (Short frame sync, slave mode)

Table 24 PCM interface timing specifications (Short frame sync, slave mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC setup	8.0	–	–	ns
5	PCM_SYNC hold	8.0	–	–	ns
6	PCM_OUT delay	0	–	25.0	ns
7	PCM_IN setup	8.0	–	–	ns
8	PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

3.3.4.3 Long frame sync, master mode

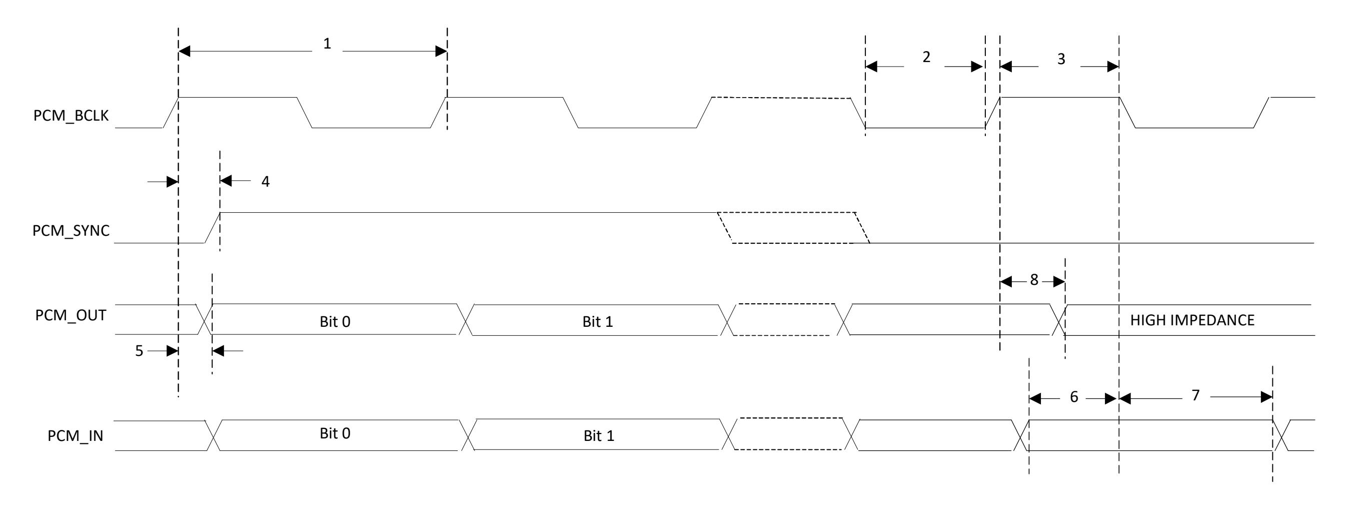


Figure 12 PCM timing diagram (Long frame sync, master mode)

Table 25 PCM interface timing specifications (Long frame sync, master mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC delay	0	–	25.0	ns
5	PCM_OUT delay	0	–	25.0	ns
6	PCM_IN setup	8.0	–	–	ns
7	PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

3.3.4.4 Long frame sync, slave mode

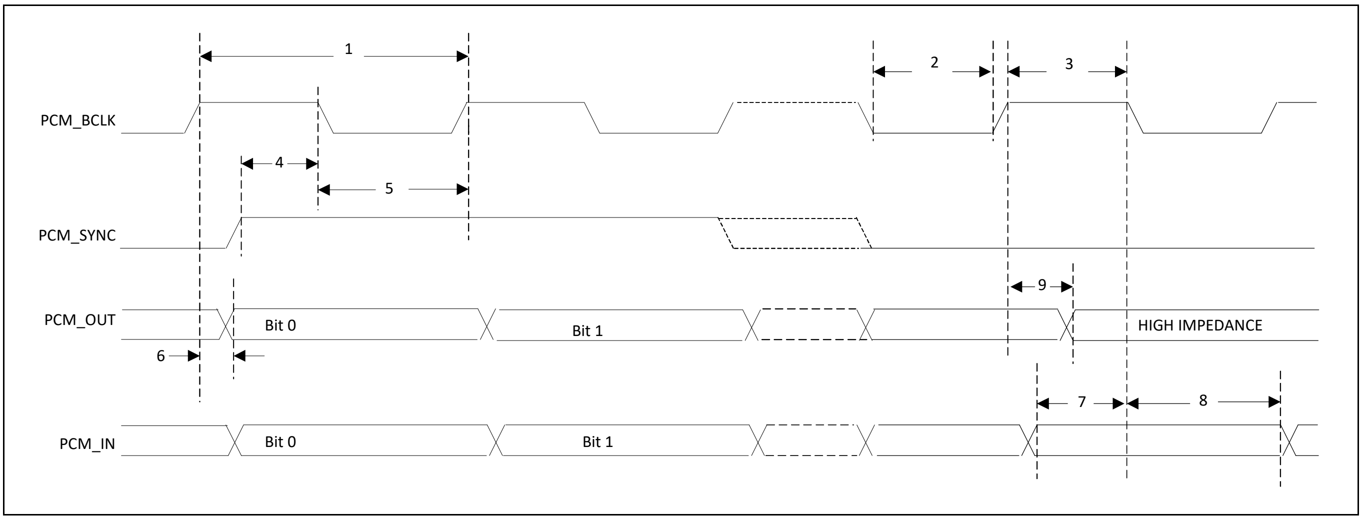


Figure 13 PCM timing diagram (Long frame sync, slave mode)

Table 26 PCM interface timing specifications (Long frame sync, slave mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	PCM_SYNC setup	8.0	–	–	ns
5	PCM_SYNC hold	8.0	–	–	ns
6	PCM_OUT delay	0	–	25.0	ns
7	PCM_IN setup	8.0	–	–	ns
8	PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25.0	ns

3.3.5 I^{2}S timing

The CYW20706 supports two independent I^{2}S digital audio ports. The I^{2}S interface supports both master and slave modes. The I^{2}S signals are:

- I^{2}S Clock: I^{2}S SCK
- I^{2}S Word Select: I^{2}S WS
- I^{2}S Data Out: I^{2}S SDO
- I^{2}S Data In: I^{2}S SDI

I^{2}S SCK and I^{2}S WS become outputs in master mode and inputs in slave mode, while I^{2}S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I^{2}S bus, per the I^{2}S specification. The MSB of each data word is transmitted one bit clock cycle after the I^{2}S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I^{2}S WS is low, and right-channel data is transmitted when I^{2}S WS is high. Data bits sent by the CYW20706 are synchronized with the falling edge of I^{2}S_SCK and should be sampled by the receiver on the rising edge of I^{2}S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

Table 27 Timing for I^2S transmitters and receivers [25]

	Transmitter				Receiver				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	Note 26
Master mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	–	Note 27
LOW t_{LC}	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	–	Note 27
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	Note 28
LOW t_{LC}	–	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	Note 28
Rise time t_{RC}	–	–	$0.15 \times T_{tr}$	–	–	–	–	–	Note 29
Transmitter									
Delay t_{dtr}	–	–	–	$0.8 \times T$	–	–	–	–	Note 30
Hold time t_{htr}	0	–	–	–	–	–	–	–	Note 29
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2 \times T_r$	–	–	Note 31
Hold time t_{hr}	–	–	–	–	–	0	–	–	Note 31

Notes

25. Timing values specified in **Table 27** are relative to high and low threshold levels.
26. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
27. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
28. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35 \times T_r$, any clock that meets the requirements can be used.
29. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15 \times T_{tr}$.
30. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
31. The data setup and hold time must not be less than the specified receiver setup and hold time.

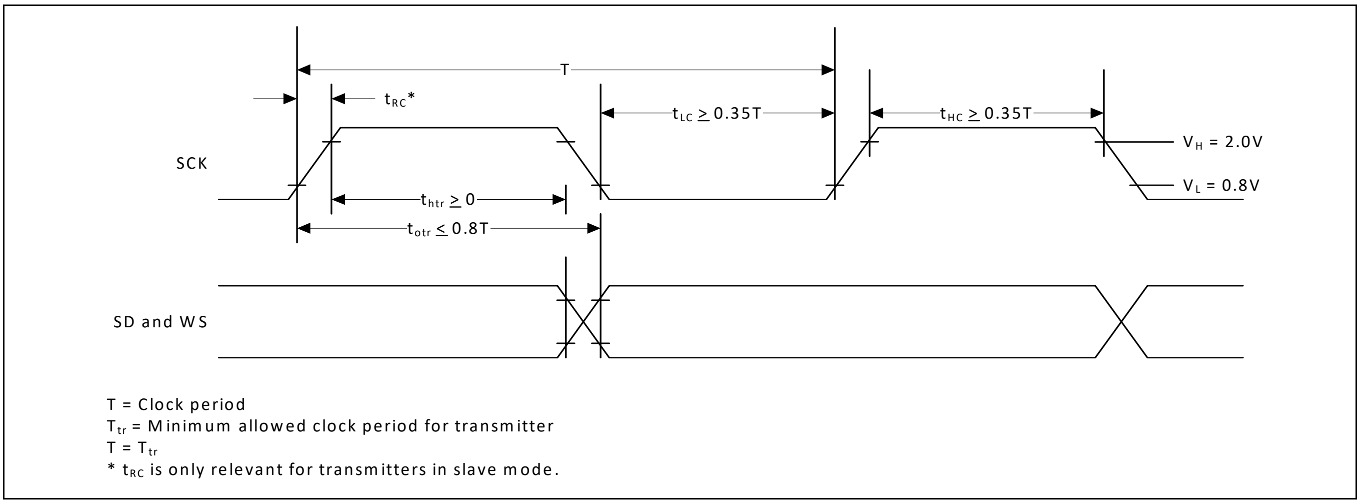


Figure 14 **I²S transmitter timing**

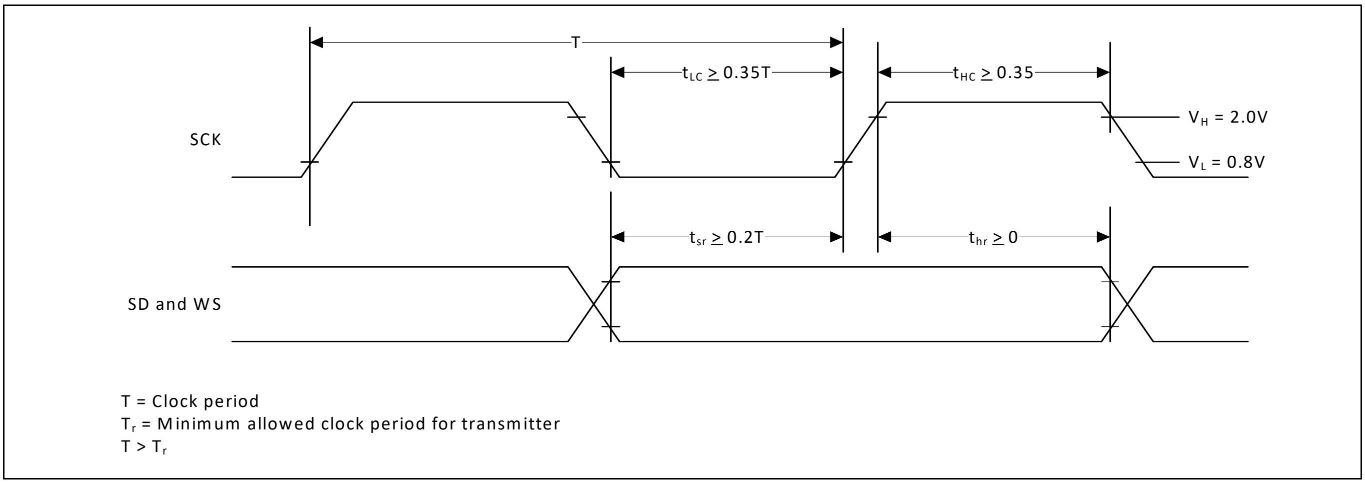


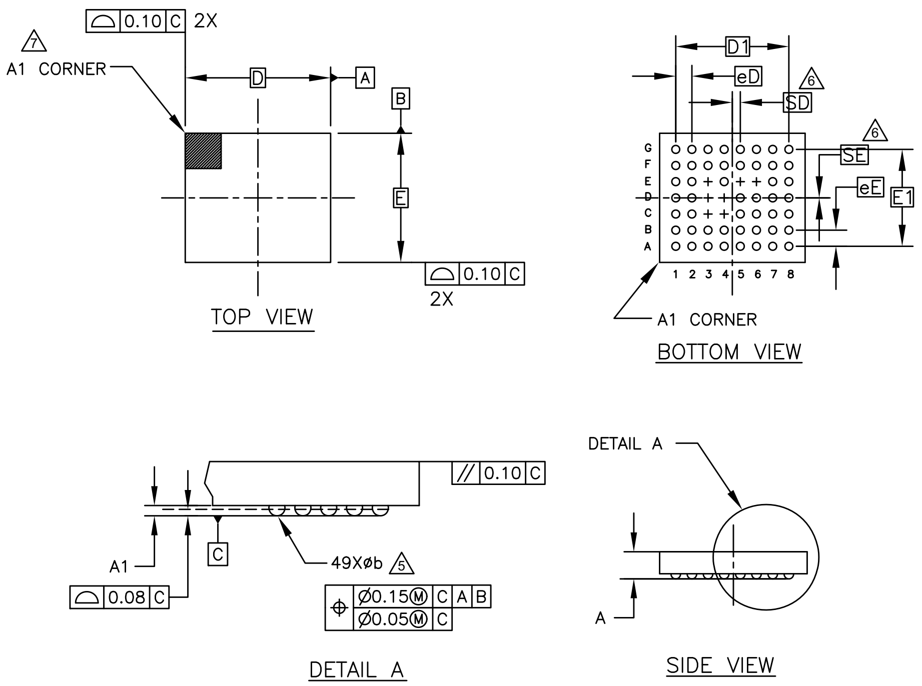
Figure 15 **I²S receiver timing**

Note

32. The time periods specified in **Figure 14** and **Figure 15** are defined by the transmitter speed. The receiver specifications must match transmitter performance.

4 Mechanical information

4.1 Package diagrams



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	-	-	1.00
A1	0.13	-	-
D	4.50 BSC		
E	4.00 BSC		
D1	3.50 BSC		
E1	3.00 BSC		
MD	8		
ME	7		
N	49		
Øb	0.20	0.25	0.30
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-207.

002-13601 Rev. *B

Figure 16 CYW20706 49-ball FCBGA (4.5 mm × 4.0 mm × 1.0 mm) FR49A/VDN049 package outline

4.2 Tape reel and packaging specifications

Table 28 CYW20706 tape reel specifications

Parameter	Value
Quantity per reel	2500
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Tape pitch	12 mm

The top-right corner of the CYW20706 package is situated near the sprocket holes, as shown in **Figure 17**.

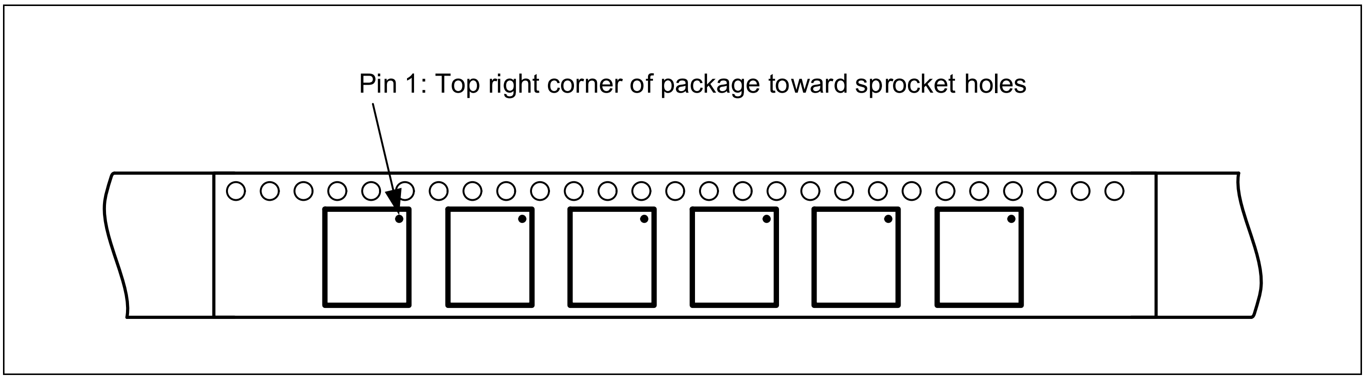


Figure 17 Pin 1 orientation

5 Ordering information

Table 29 Ordering information

Product	Package
CYW20706UA2KFFB4G	49-ball FCBGA

6 IoT resources

Infineon provides a wealth of data at **Security for IoT** to help you select the right IoT device for your design, and quickly and effectively integrate the device into your design. Infineon provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from **Infineon support community**.

7 Acronyms

Table 30 Acronyms used in this document

Term	Description
ADC	analog-to-digital converter
AFH	Adaptive Frequency Hopping
AHB	advanced high-performance bus
APB	advanced peripheral bus
APU	audio processing unit
ARM7TDMI-S™	Acorn RISC Machine 7 Thumb instruction, Debugger, Multiplier, Ice, Synthesizable
BR	Basic Rate
BTC	Bluetooth® controller
COEX	coexistence
DFU	device firmware update
DH	data high rate
DM	data medium rate
DMA	direct memory access
EBI	external bus interface
EDR	Enhanced Data Rate
GFSK	Gaussian frequency shift keying
HCI	host control interface
HV	high voltage
IDC	initial digital calibration
IF	intermediate frequency
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low dropout
LHL	lean high land
LPO	low power oscillator
LV	LogicVision™
MIA	multiple interface agent
PCM	pulse code modulation
PLL	phase locked loop
PMU	power management unit
POR	power-on reset
PWM	pulse width modulation
QD	quadrature decoder
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency

Table 30 Acronyms used in this document (Cont.)

Term	Description
ROM	read-only memory
RX/TX	receive, transmit
SPI	serial peripheral interface
SW	software
UART	universal asynchronous receiver/transmitter
UPI	µ-processor interface
WD	watchdog

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Infineon documents, go to **Glossary**.

8 Document conventions

8.1 Units of measure

Table 31 Units of measure

Symbol	Unit of measure
°C	degree Celsius
dB	decibel
dBi	decibels relative to isotropic
dBm	decibel-milliwatts
GHz	gigahertz
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
kV	kilovolt
mA	milliamperes
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
mm	millimeters
Msps	megasamples per second
mV	millivolt
µA	microampere
µF	microfarad
µm	micrometers
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*D	2024-07-18	Released to web.
*E	2025-03-03	Updated **Tape reel and packaging specifications**. Updated **Figure 17**.

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